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Decoupling effects of material and package on single-pulse limit capability of power MOSFETs*

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Abstract: Pulsed power systems often connect switches in series or parallel to increase voltage and current ratings. However, this approach significantly increases system complexity and parasitic effects. The ultimate capability of a single device under extreme single-pulse conditions remains underexplored. Furthermore, the independent contributions of device materials and packaging to this capability need to be clearly distinguished. To address this, we developed a test platform for extreme pulse voltage, current, and gate drive voltage. We conducted single narrow-pulse stress tests on power MOSFETs with various material and packaging combinations. Specifically, we tested Silicon (Si) and Silicon Carbide (SiC) devices in both low-inductance metal/Kelvin packages and traditional plastic packages. Our results reveal a comparative trend among different material–packaging combinations between material and packaging on pulse capability. First, the overvoltage ratio (OVR) is primarily governed by the material's critical breakdown electric field. Consequently, SiC devices exhibit a higher OVR (1.5–1.6) than Si devices (1.3). Second, the overcurrent ratio (OCR) and current rise rate depend heavily on the package's parasitic inductance. Devices in low-inductance packages show superior dynamic response and a higher OCR (approximately 9×) than those in traditional 3-pin plastic packages (approximately 7×). Additionally, moderately increasing the gate drive voltage (from 25 V to 40 V) induces a transient overdrive effect. Under this condition, the overdrive gain of SiC devices is approximately four times that of Si devices. Furthermore, analyzing the typical waveforms of voltage and transient leakage current provides an effective, non-destructive method to identify soft avalanche breakdown. This study deepens our understanding of how materials and packaging independently affect single-pulse limits. These insights can help reduce the need for series/parallel switch arrays and guide better device selection in pulsed power systems.

Key words: Power MOSFET; Single-pulse limit; Decoupling; Material and package; Soft avalanche breakdown.

1 Introduction

Pulsed power technology is widely used in particle accelerators, environmental protection, and biomedicine [1], [2], [3]. High-voltage pulse generation largely depends on the performance and reliability of semiconductor switches [4], [5], [6]. Power MOSFETs are widely used as switching components in these systems due to their fast-switching speeds and simple gate control. However, the growing demand for higher peak power and faster transient responses exposes these devices to increasingly severe electro-thermal stress [7], [8], [9]. Traditional design methods rely mainly on the Safe Operating Area (SOA) provided in device datasheets. Existing SOA boundaries are typically defined by thermal stability limits under finite pulse widths. In practice, engineers often use conservative derating and

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series/parallel configurations to ensure device safety. While this approach guarantees reliability, it increases system complexity and parasitic effects, ultimately degrading overall performance [10], [11], [12]. In contrast, many pulsed power systems operate under single-pulse or low-repetition-rate conditions. In these cases, the pulse width (typically in the microsecond range) is much shorter than the device's thermal time constant. Heat diffusion is restricted, creating an approximately adiabatic process with minimal thermal accumulation. Consequently, the device limits are primarily governed by transient electrical stress [13]. Therefore, the actual transient withstand capability of power MOSFETs often exceeds the limits defined by traditional SOA curves [14]. However, the ultimate capability of a single device under extreme single-pulse conditions remains underexplored. Furthermore, the independent effects of material and packaging on this capability need to be clearly distinguished.

Recent studies have widely investigated the high breakdown voltage [15], integrated overcurrent protection [16], and gate drive voltage effects [17] of SiC MOSFETs. However, most of these works focus on conventional gate drive voltages ($\leqslant$20 V) and rated current ranges [18], [19]. The combined effects of extreme overvoltage, overcurrent, and gate drive voltage remain underexplored. More importantly, existing literature rarely treats "material" and "packaging" (e.g., plastic, metal, and pin count) as independent variables for systematic comparison. This makes it difficult to clearly distinguish their independent contributions to the ultimate pulse capability [20], [21]. The impact of package parasitic inductance on switching transients is widely recognized. However, it is often treated as a secondary factor. Few studies have systematically decoupled packaging effects from material properties as independent variables.

To address these issues, we designed a multi-dimensional extreme test method. We systematically evaluated power MOSFETs with three typical material-package combinations. By comparing devices with the same package but different materials, and the same material but different packages, we built an experimental framework to decouple these two factors. This framework reveals two key decoupling features. First, the overvoltage ratio (OVR) closely correlates with the upper limit of the material's critical breakdown electric field. Second, the overcurrent ratio (OCR) and current rise rate may be strongly associated with the package parasitic inductance. Furthermore, we propose a quantitative model for transient overdrive gain. This model analyzes how increasing the gate drive voltage from 25 V to 40 V affects the gains in peak current and rise time. Finally, we introduce a non-destructive method to infer soft breakdown based on waveform characteristics. Specifically, a "voltage overshoot → drop → stabilization" pattern, combined with transient leakage current features, helps identify soft avalanche breakdown.

The remainder of this paper is organized as follows. Section 2 introduces the device selection and experimental methodology. Section 3 presents the experimental results for extreme pulse voltage, extreme pulse current, and extreme gate drive voltage. Section 4 discusses the decoupling characteristics and underlying mechanisms. Specifically, it analyzes the material's impact on the overvoltage ratio (OVR) and the potential significant effect of packaging on the overcurrent ratio (OCR). Furthermore, it elaborates on the transient overdrive gain model and the waveform-based inference mechanism for soft avalanche breakdown. Section 5 outlines the limitations of this study and suggests directions for future work. Finally, Section 6 concludes the paper.

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2 Experimental Setup and Methodology

2.1 Device Selection

To investigate the decoupling effects of semiconductor materials and package parasitics on the single-pulse ultimate capability of MOSFETs, we selected three commercial power MOSFETs. Their key parameters are listed in

Table 1.

Table 1 Part Numbers and Key Parameters of the Tested MOSFET

Model	Rated Voltage (V)	Rated Current (A)	On-Resistance (mΩ)	Package Type	Material	Pin Count
HSK60R070FK2	600	47	60–70	Plastic (TO-247-3)	Si	3
MSS150A-1200	1200	68	40	Metal (TO-247-3)	SiC	3
C2M0045170P	1700	72	45	Plastic (TO-247-4L)	SiC	4

These three devices represent three typical material-package combinations: a Si device in a 3-pin plastic package (HSK60R070FK2), a SiC device in a 3-pin metal package (MSS150A-1200), and a SiC device in a 4-pin Kelvin plastic package (C2M0045170P).

In our selection strategy, HSK60R070FK2 and C2M0045170P share the same plastic packaging but use different materials. This comparison allows for a preliminary analysis of the impact of material properties. Conversely, MSS150A-1200 and C2M0045170P share the same SiC material but feature different packaging (metal vs. Kelvin plastic).

This comparison effectively isolates the impact of package parasitics. This comparative strategy provides a solid experimental foundation for the subsequent decoupling analysis.

2.2 Test Circuit

Extreme pulse voltage test: To evaluate how material and packaging affect the transient overvoltage withstand capability, we designed an extreme pulse voltage test platform. The circuit schematic is shown in Fig. 1. It consists of two main loops: a charging loop and a discharging loop. During the charging phase, the primary switch $Q1$ turns on. The pulse transformer then transfers energy to the secondary side to charge the capacitor C. During the discharging phase, $Q1$ turns off first. After a short delay, the device under test (DUT), $Q2$, is triggered to turn on. The energy stored in capacitor C is then rapidly discharged through $Q2$. This process applies a single high-voltage pulse stress to the DUT.

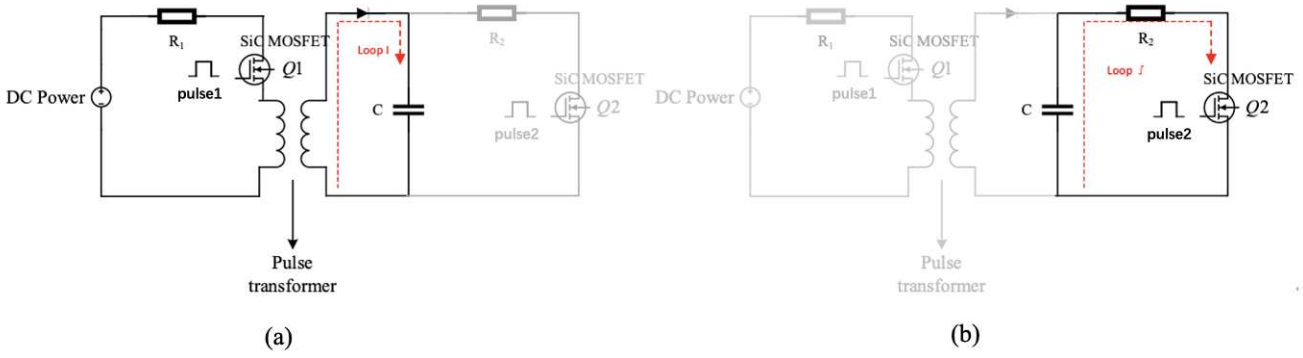


Fig.1 Test circuit for single-pulse voltage limits：(a) charging circuit ; (b) discharging circuit

Extreme pulse current test: To evaluate the current handling margin and the impact of package parasitics on the extreme current, we built a dedicated test platform, as shown in Fig. 2. To achieve the highest possible current rise rate, capacitor C is connected directly in parallel with the device under test. No current-limiting resistors are employed within the discharge loop During the test, capacitor C is first pre-charged to a target voltage. A gate drive signal then turns on the DUT. The stored energy rapidly discharges through the switch, generating a single narrow current pulse. We gradually increase the charging voltage to raise the peak pulse current. This process continues until the device fails or the test equipment reaches its maximum limit.

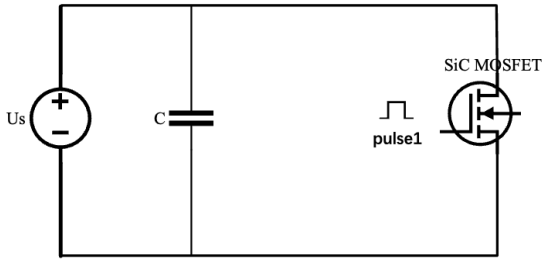


Fig. 2 Test circuit for single-pulse current limit

Extreme gate drive voltage test: To evaluate how the gate drive voltage enhances the ultimate single-pulse current capability, we used the test circuit shown in Fig. 2. During the test, only the gate drive voltage was varied from 25 V to 40 V, while all other conditions remained unchanged. For each voltage level, the peak pulse current and the current rise time were recorded.

2.3 Test Circuit

In the experiments, the drain-source voltage is measured using a high-voltage differential probe. The drain current is measured with a coaxial current loop. The gate-source voltage is measured by a high-impedance passive probe. A high-bandwidth digital oscilloscope records all transient waveforms synchronously.

Note that the test probes and measurement loops inevitably introduce parasitic parameters. These parasitics may affect the rise time and peak values of the high-frequency transient waveforms. However, the core objective of this study is to evaluate the differences in the ultimate capabilities among devices with different materials and packages. The test platform and measurement equipment remain completely identical for all three DUTs.

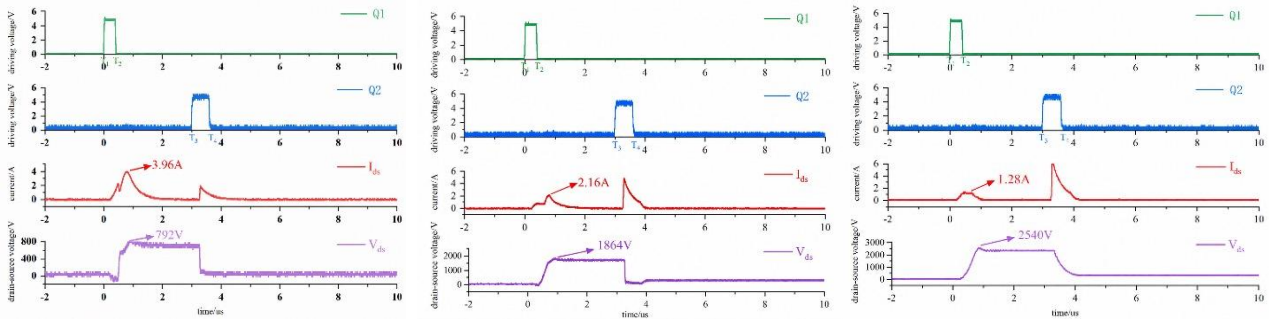
The parasitic effects from the probes and loops act as systematic errors. They do not affect the comparative conclusions regarding the relative ultimate capabilities among the devices. Therefore, the decoupling analysis in this study focuses on the trends resulting from the material and package differences.

3 Experimental Result

3.1 Extreme pulse voltage test

Fig. 3 shows the typical waveforms of the three MOSFETs during the extreme pulse voltage test. These waveforms include the trigger signal, drain-source voltage, and drain current. All three devices exhibit a consistent transient response. Before the DUT is triggered, the drain-source voltage rises rapidly to an overshoot peak. It then drops and stabilizes at a certain voltage level. This process is accompanied by a distinct transient leakage current pulse.

Quantitatively, the rated voltages of HSK60R070FK2, MSS150A-1200, and C2M0045170P are 600 V, 1200 V, and 1700 V, respectively. Their measured peak overshoot voltages reach 792 V, 1864 V, and 2540 V, respectively. The corresponding voltage rise times are 330 ns, 195 ns, and 265 ns.



(a) (b) (c)

Fig.3 Test results of single-pulse voltage limits: (a) HSK60R070FK2；(b) MSS150A-1200；(c) C2M0045170P

Notably, when the devices are subjected to transient overvoltage without a turn-on gate signal, an ampere-level

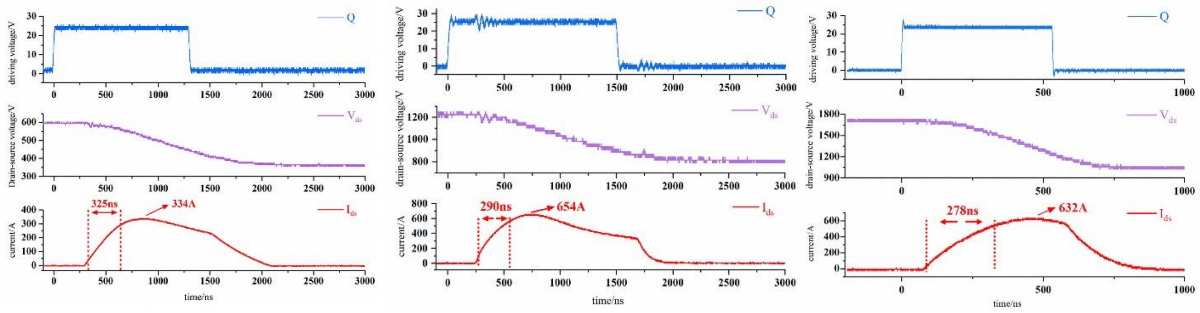
transient leakage current flows between the drain and source. The peak values of this current are 3.96 A, 2.16 A, and 1.28 A, respectively. After the leakage current reaches its peak, the drain-source voltage drops accordingly. Eventually, the leakage current decays to zero as the voltage stabilizes. This transient leakage current phenomenon is highly coupled with the "overshoot-drop-stabilization" characteristic of the voltage. It provides a crucial waveform basis for inferring soft avalanche breakdown in the subsequent analysis.

3.2 Extreme pulse current test

Fig. 4 shows the waveforms from the extreme pulse current test. With a 1.6 μF energy storage capacitor and a 25 V gate drive voltage, all three devices demonstrate a transient current capability far exceeding their rated values.

The rated currents of HSK60R070FK2, MSS150A-1200, and C2M0045170P are 47 A, 68 A, and 72 A. Under the extreme test, their measured peak currents reach 334 A, 654 A, and 632 A, respectively. The corresponding current rise times are 325 ns, 290 ns, and 278 ns.

In terms of the waveform, the pulse currents for all three devices rise rapidly to a peak and then decay exponentially. The pulse widths range from approximately 0.7 to 2 μs.



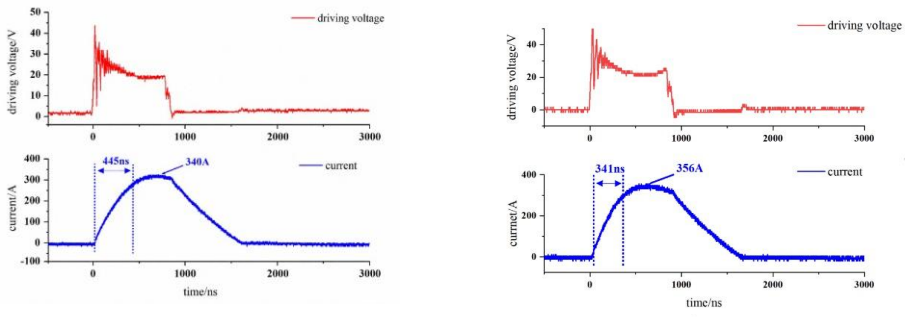
(a) (b) (c)

Fig.4 Test results of single-pulse current limits: (a) HSK60R070FK2；(b) MSS150A-1200；(c) C2M0045170P

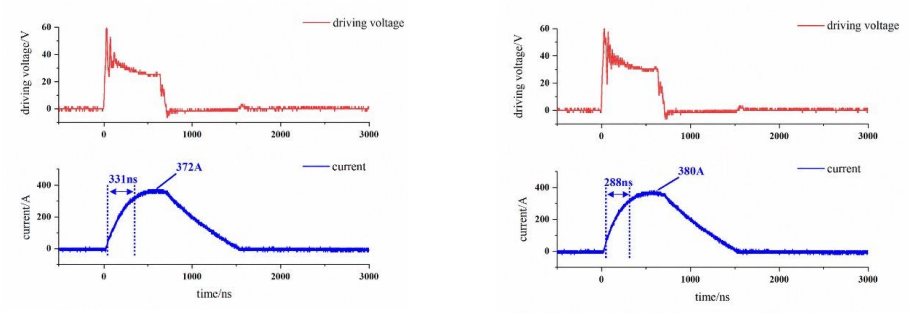
3.3 Extreme gate drive voltage test

Figs. 5–7 show the extreme pulse current waveforms of the three MOSFETs at different gate drive voltages. The tests were conducted at four voltage levels: 25 V, 30 V, 35 V, and 40 V. The results show that as the gate drive voltage increases from 25 V to 40 V, the peak current of all devices steadily increases. Meanwhile, the current rise time consistently decreases.

However, when VGS exceeds 35 V, the growth rate of the peak current slows down significantly and approaches saturation. This indicates that the transient overdrive effect is gradually limited by the carrier injection capability of the channel or the parasitic parameters of the power loop.

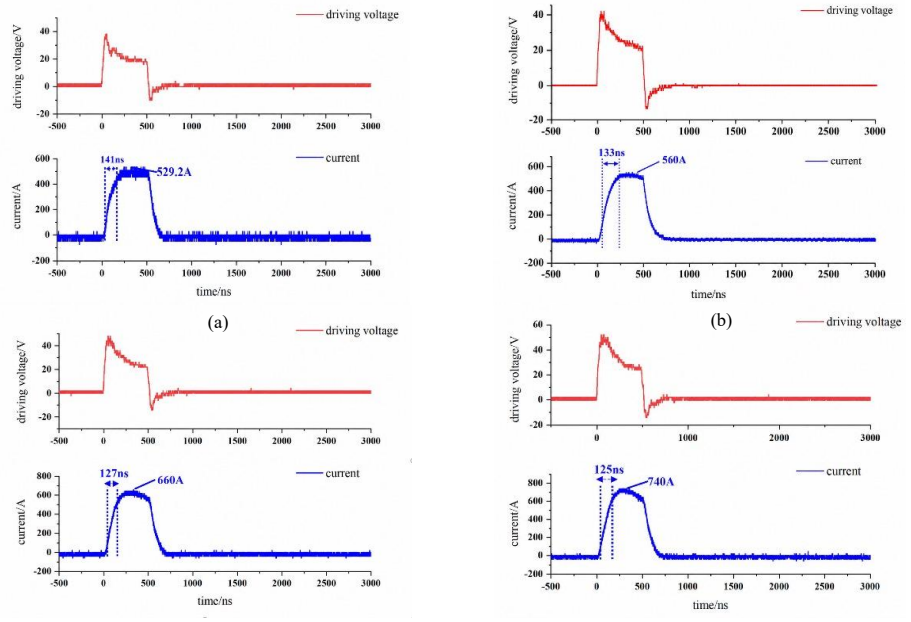


(a) (b)



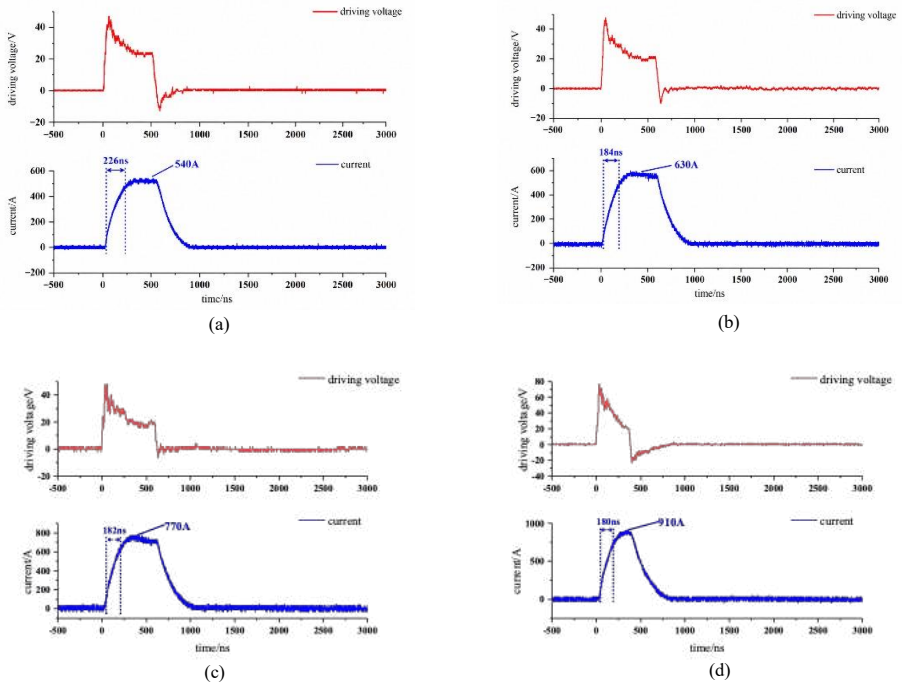
(c) (d)

Fig. 5 Waveforms of HSK60R070FK2 under different gate drive voltages：(a) 25V；(b) 30V；(c) 35V；(d) 40V



(a) (b) (c) (d)

Fig. 6 Waveforms of MSS150A-1200 under different gate drive voltages：(a) 25V；(b) 30V；(c) 35V；(d) 40V



(a) (b) (c) (d)

Fig. 7 Waveforms of C2M0045170P under different gate drive voltages：(a) 25V；(b) 30V；(c) 35V；(d) 40V

4 Discussion and decoupling analysis

4.1 Material-driven overvoltage ratio analysis

The three devices have different rated voltages. Therefore, we introduce the OVR for normalized comparison, as shown in Fig. 8. The OVR is defined as $OVR = V_{\mathrm{DS,peak}}/V_{\mathrm{DSS,rated}}$. Here, $V_{\mathrm{DS,peak}}$ is the transient peak drain-source voltage captured during the single-pulse test and used for OVR calculation. In contrast, the post-overshoot steady-state $V_{\mathrm{DS,peak}}$ is adopted as the criterion to judge whether the device reaches its withstand boundary. The experimental results show that the two SiC devices (MSS150A-1200 and C2M0045170P) achieve $OVRs$ of 1.6 and 1.5, respectively. Both values are higher than the 1.3 measured for the Si device (HSK60R070FK2). Notably, the two SiC devices have significantly different rated voltages. However, their $OVRs$ remain stable between 1.5 and 1.6. They do not show a monotonic increase as the voltage rating increases.

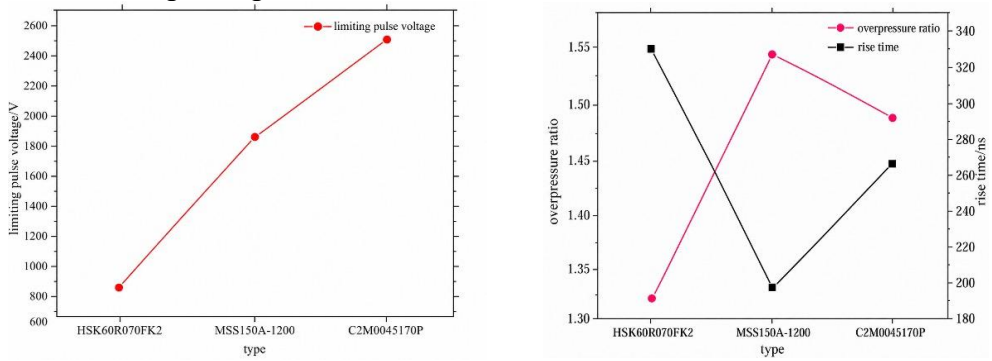


Fig. 8 Experimental comparison of single-pulse voltage limits：(a) limiting pulse voltage amplitudes；(b) overvoltage ratios and voltage rise times

The overvoltage capability under a single pulse is primarily limited by the device's ability to withstand transient high electric fields. SiC's wide bandgap provides a higher critical breakdown electric field. This gives SiC devices a larger margin above their rated voltage. In contrast, the internal electric field in Si devices is already near its limit when operating close to the rated voltage. It is important to note that the selected Si (600 V) and SiC (1200 V/1700 V) devices are not perfectly decoupled in voltage rating. The lower OVR of the Si device may be partly due to its higher drift region doping concentration and edge termination limitations. Therefore, the OVR difference cannot be attributed solely to the material type. However, comparing SiC devices with different voltage ratings shows that voltage rating is not the only dominant factor. Overall, the OVR is closely related to the material's critical breakdown electric field margin. Furthermore, package parasitic inductance mainly affects the dynamic current response. Its direct impact on the steady-state avalanche breakdown voltage is limited. Thus, it plays a secondary role when evaluating transient overvoltage limits.

4.2 Packaging-dominated overcurrent ratio analysis

Since the devices have different rated currents, we introduce the OCR for normalized comparison, as shown in Fig. 9. The OCR is defined as $OCR = I_{D,peak}/I_{D,rated}$. Devices with low-inductance designs, such as MSS150A-1200 and C2M0045170P, achieve $OCRs$ of 9.6 and 8.8, respectively. These values are significantly higher than the 7.1 measured for the traditional 3-pin plastic-packaged Si device (HSK60R070FK2). Furthermore, the current rise times of the two low-inductance devices are similar, both at the ~200 ns level. In contrast, the rise time of the traditional plastic-packaged device exceeds 300 ns.

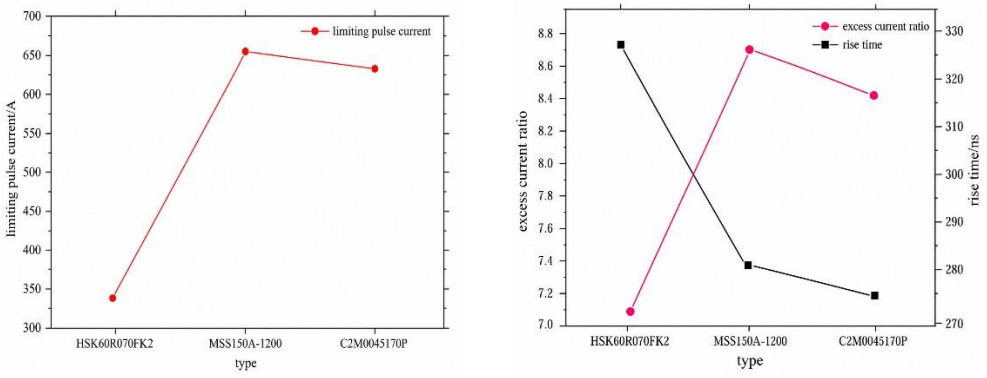


Fig. 9 Experimental comparison of single-pulse current limits：(a) limiting pulse current amplitudes；(b) overcurrent ratios and current rise times

The peak current rise rate (di/dt) is primarily constrained by the total loop inductance (V=L·di/dt). Within this loop, the package parasitic inductance, particularly the common source inductance (CSI), exerts the most significant impact. Metal packages effectively reduce this inductance by utilizing shorter internal bond wires. Meanwhile, 4-pin Kelvin packages drastically minimize the CSI by separating the power source from the gate drive source.

Comparing SiC devices of the same material but different packages reveals that low-inductance designs generally yield a higher OCR. Similarly, among plastic packages, the 4-pin device demonstrates superior dynamic performance due to its minimal CSI. Consequently, these results clearly demonstrate that the OCR and current rise rate are predominantly governed by the package parasitic inductance, whereas the influence of the semiconductor material is relatively limited.

4.3 Transient overdrive gain and ultimate limits

As shown in Fig. 10, increasing the gate drive voltage enhances the charge density in the channel inversion layer. This reduces the on-state resistance. Consequently, both the transient peak current and the current rise rate are improved. To quantitatively describe this gain effect, we define the transient overdrive gain K (in V^{-1}) as follows:

$$K_{VGS} = \Delta(I_{peak}/I_{rated})/(\Delta V_{GS}) \quad (1)$$

We perform a linear fit on the experimental data for gate drive voltages ranging from 25 V to 40 V. The results are as follows:

C2M0045170P (SiC/4-pin): I_{peak}=24.7 V_{GS}−100. The OCR increases from 7.5 to 12.6, yielding K≈0.35.

MSS150A-1200 (SiC/metal): I_{peak} =14.7 V_{GS}+146. The OCR increases from 7.8 to 10.9, yielding K≈0.22.

HSK60R070FK2 (Si/3-pin): I_{peak} =2.7 V_{GS} +274. The OCR increases from 7.2 to 8.1, yielding K≈0.06.

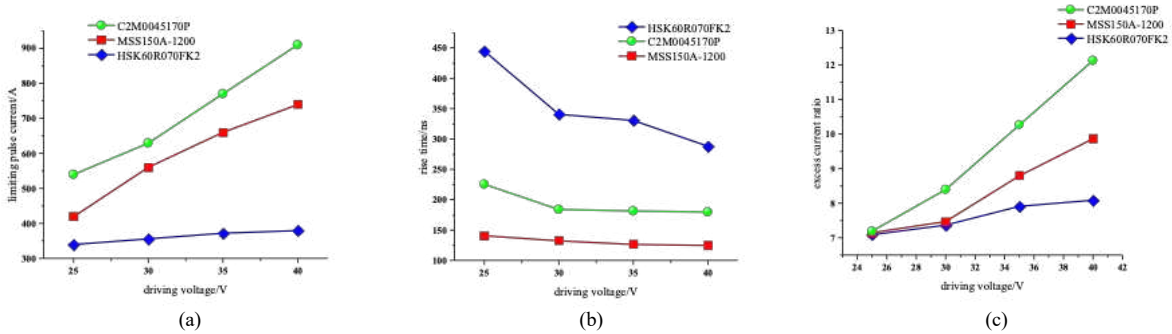


Fig. 10 Comparison of limiting pulse current amplitudes, current rise times, and overcurrent ratios among the three MOSFET models：a limiting pulse current amplitudes；b current rise times；c overcurrent ratios

The transient overdrive gain of SiC devices is approximately four times that of Si devices. This advantage largely stems from the higher carrier mobility and better temperature stability of the channel in SiC. Consequently, SiC devices respond

more significantly to gate voltage variations. When VGS exceeds 35 V, the growth of the peak current gradually slows down and approaches saturation. This phenomenon is primarily driven by two factors: the loop parasitic inductance limiting the maximum d*i*/d*t*, and the carrier velocity saturation effect. It is important to note that exceeding the rated gate drive voltage significantly increases the electric field stress across the gate oxide. This elevated stress can increase the risks of threshold voltage drift and gate oxide degradation [22]. Therefore, we recommend applying high gate drive voltages cautiously. This strategy should only be used during single narrow-pulse operations and must be combined with gate voltage clamping protection.

4.4 Inference of failure mechanisms based on waveform characteristics

Under extreme pulse stress, it is often difficult to directly determine if a device has suffered irreversible failure. However, the inflection points in the transient waveforms offer a viable method for the non-destructive inference of underlying physical mechanisms.

Voltage mechanism inference: Avalanche triggering and self-clamping effect. Based on the "voltage overshoot → drop → stabilization" waveform observed in Section 3.1, the underlying physical mechanism can be inferred as follows. When the drain-source voltage exceeds the dynamic avalanche breakdown threshold, impact ionization occurs in the depletion region. This causes a surge in avalanche current and a sharp drop in the device's equivalent impedance. Consequently, the initial overshoot voltage cannot be maintained and begins to fall. The subsequent voltage stabilization phase is primarily driven by the positive temperature coefficient of the breakdown voltage in SiC materials. A slight local temperature rise shifts the breakdown threshold upward. This helps suppress local current crowding and thermal runaway, manifesting as a voltage self-clamping effect. This complete response sequence “overshoot-drop-stabilization” accompanied by the eventual return of the leakage current to zero, indicates that the device experienced a soft avalanche breakdown without irreversible damage. Based on this characteristic, the stable voltage value following the overshoot can serve as a reliable reference for inferring the single-pulse ultimate withstand voltage boundary, all without damaging the device.

Under a single pulse, the device's ultimate limit is constrained by both internal semiconductor physics and the macroscopic energy conservation of the external circuit. The extreme pulse current waveform typically decays exponentially after reaching its peak. Since the single-pulse width (in the microsecond range) is much shorter than the device's thermal time constant, thermal dissipation is rarely the primary factor driving this current decay. From a circuit topology perspective, this current decay primarily stems from the natural voltage drop of the energy storage capacitor during the discharge process. Meanwhile, the loop parasitic inductance limits the di/dt. This significantly affects the slopes of both the current rise and fall. Consequently, the overcurrent limit under a single pulse is not primarily dictated by thermal failure. Instead, it is largely governed by the dynamic conversion of the system's electromagnetic energy, specifically the interplay between the initial capacitor energy and the loop inductance.

5 Limitations and future work

This study investigates the decoupling effects of material and packaging on the single-pulse ultimate capability. However, several limitations should be acknowledged. First, the selected Si and SiC devices are not perfectly decoupled in terms of voltage ratings. The OVR of the Si device may be partly due to its higher drift region doping concentration and edge termination limitations. Consequently, the OVR difference cannot be attributed solely to the material type. This voltage mismatch constitutes a major limitation of the present comparison. Future studies could employ Si and SiC devices with identical voltage ratings to isolate the specific impact of voltage ratings on the decoupling characteristics. Second, this study focuses exclusively on single narrow-pulse stress. It does not address the thermal accumulation effects under repetitive pulsing conditions. In practical pulsed power applications, electro-thermal coupling failures under repetitive pulses can significantly alter the device's ultimate limits. Therefore, investigating how thermal accumulation affects these decoupling

characteristics is a key focus for our future work. Finally, while this study verifies the gain effect of transient overdrive on the peak current, exceeding the rated gate drive voltage significantly increases the electric field stress across the gate oxide. This paper does not quantitatively evaluate the long-term threshold voltage drift and gate oxide degradation caused by this high stress. However, the long-term threshold voltage drift and gate oxide degradation induced by such high electric-field stress remain unquantified in this work. Future work must develop long-term reliability degradation models for the gate under transient overdrive stress to clarify the safe engineering boundaries for applying this driving strategy.

6 Conclusion

This study addresses the evaluation of the ultimate capability of power MOSFETs in pulsed power systems. By conducting multi-dimensional extreme pulse tests on three typical material-package combinations, we investigated the decoupling relationship between materials and packaging under single-pulse conditions.

The results demonstrate a clear decoupling between the overvoltage and overcurrent capabilities under single-pulse stress. Regarding overvoltage characteristics, the OVR is closely related to the margin of the material's critical breakdown electric field. Due to its wide bandgap, SiC devices typically exhibit a higher OVR (1.5–1.6) than Si devices (1.3), with a lower risk of thermal runaway. In contrast, package parasitic parameters have a limited direct impact on the steady-state avalanche breakdown voltage. Conversely, the OCR and current rise rate are predominantly governed by package parasitic inductance. Low-inductance packages (metal and 4-pin Kelvin plastic) shorten bond wires and eliminate common source inductance. This allows for a higher current rise rate, yielding a superior OCR (8.8–9.6) compared to traditional 3-pin plastic packages (7.1). Furthermore, the proposed transient overdrive gain model quantifies the enhancement of overcurrent capability by the gate drive voltage. The gain in SiC devices is approximately four times that of Si devices. However, at high drive voltages (> 35 V), this gain shows a diminishing marginal return due to loop inductance and carrier velocity saturation. Additionally, the waveform characteristic of “overshoot-drop-stabilization”, accompanied by transient leakage current, provides a non-destructive method to infer soft avalanche breakdown. This offers a valuable reference for evaluating the SOA of devices.

Based on these decoupling characteristics, this study offers practical guidelines for pulsed power system design. Wide-bandgap materials should be prioritized for applications with high transient overvoltage requirements, while low-inductance packages are preferable for high overcurrent and dynamic response needs. Since a single SiC device in a low-inductance package possesses both high overvoltage and overcurrent potential, it can reduce the need for series/parallel connections in system design. This helps simplify the topology and mitigate system-level parasitic issues. Finally, moderately increasing the transient gate drive voltage is a viable approach to enhance pulsed current capability, if gate oxide reliability is ensured and combined with a gate voltage clamping protection mechanism.

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Declarations

Ethics, Consent to Participate, and Consent to Publish declarations: not applicable. The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request. On behalf of all authors, the corresponding author states that there is no conflict of interest.

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