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Real-Time Hardware Implementation and Experimental Evaluation of a Modified dqPLL Architecture for Harmonic-Robust Three-Phase Grid Synchronization

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Abstract

This paper presents a real-time implementation and experimental evaluation of a modified synchronous reference frame phase-locked loop (dqPLL) for three-phase grid synchronization under harmonic distortion. The proposed architecture extends the conventional dqPLL with a dedicated harmonic compensation block designed to attenuate selected low-order harmonics while preserving the fundamental positive-sequence component required for accurate phase and frequency estimation. Real three-phase voltage signals acquired from the Spanish electricity grid using a Digilent Analog Discovery device were processed and implemented on a Real-Time Digital Simulator (RT Box 240) through AccurateRTDS software, enabling real-time experimental validation under realistic grid conditions. A quantitative comparison between the classical and modified dqPLL architectures was conducted in terms of frequency tracking, harmonic attenuation, total harmonic distortion (THD), transient behavior, and computational execution time. Experimental results show that the proposed dqPLL architecture limits frequency deviations to approximately ± 0.2 Hz around the nominal 50 Hz, whereas the classical dqPLL exhibits oscillations of approximately ± 8 Hz under harmonic

distortion. The results demonstrate that the proposed modification provides a practical compromise between harmonic rejection, synchronization accuracy, and computational complexity, making it suitable for real-time grid-connected power electronic applications. The proposed harmonic compensation mechanism attenuates the 5th, 7th, 11th, and 13th harmonic components by more than 90% and reduces the measured THD from 2.27% at the input to 1.101%. The modified dqPLL also provides improved frequency stability and reduced oscillatory behavior compared with the conventional architecture, at the expense of increased computational execution time.

Keywords: Synchronous reference frame PLL, Three-phase grid synchronization, Harmonic compensation, Real-time implementation, Power quality, Modified dqPLL

1 Introduction

The synchronization of grid-connected converters with the utility grid is a critical requirement in modern power systems, particularly with the increasing penetration of renewable energy sources and distributed generation. Accurate phase and frequency detection ensures stable inverter operation, minimizes power quality issues, and prevents instability during grid disturbances[1]. Among the various synchronization techniques, the synchronous reference frame phase-locked loop (dqPLL) has become the most widely adopted solution due to its simplicity and robustness under nominal conditions[2].

Nevertheless, the classical dqPLL suffers from significant limitations when operating in distorted grid environments. Harmonics, voltage unbalance, and frequency fluctuations can lead to oscillations in the estimated phase angle and frequency, thereby degrading the performance of grid-tied inverters[3][4]. To address these challenges, several enhanced PLL structures have been proposed, including adaptive PLLs[5], decoupled double synchronous reference frame PLLs (DDSRF-PLL)[6], and harmonic compensation-based dqPLL architectures[7][8]. These approaches aim to improve harmonic rejection and enhance frequency stability, but they often increase computational complexity and require careful parameter tuning[9].

Recent studies have emphasized the importance of harmonic compensation blocks within dqPLL architectures to mitigate the impact of specific harmonic orders, such as the 5th, 7th, 11th, and 13th, which are commonly present in distribution grids[10][11]. Offline analyses have demonstrated that incorporating such compensation mechanisms significantly reduces total harmonic distortion (THD) and improves synchronization accuracy[12][13][14].

The advent of real-time digital simulation platforms, such as the RT Box 240, provides new opportunities to evaluate advanced dqPLL architectures under realistic operating scenarios. By enabling hardware-in-the-loop (HIL) testing, these platforms allow researchers to inject real grid signals into the simulation environment and assess the dynamic performance of synchronization algorithms[15]. This capability is particularly relevant for smart grid applications, where converters must operate reliably in the presence of harmonics, voltage sags, and other disturbances[16].

Building upon previous work[12], this paper presents a comprehensive real-time implementation and comparative study of two dqPLL architectures: the classical dqPLL and a modified dqPLL with harmonic compensation block. Real three-phase signals acquired from the Spanish electricity grid were processed and injected into the RT Box 240 using AccurateRTDS software. The study evaluates the architectures in terms of frequency stability, harmonic amplitude reduction, and THD, thereby providing new insights into the practical applicability of enhanced dqPLL structures for smart grid synchronization[17][18][19][20].

2 Modified dqPLL with Harmonic Compensator Block

2.1 Motivation

The classical dqPLL is widely used for grid synchronization due to its simplicity and robustness under nominal conditions. However, in distorted grid environments, the presence of harmonics (particularly the 5th, 7th, 11th, and 13th orders) introduces oscillations in the estimated phase angle and frequency. These oscillations degrade synchronization accuracy and increase the total harmonic distortion (THD) at the inverter output[3][4]. To address this limitation, a harmonic compensator block was integrated into the dqPLL architecture[12].

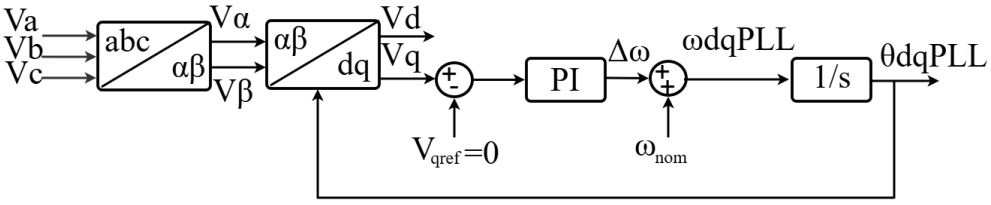


Fig. 1 Classical dqPLL architecture

The general synchronization principle considered in this work is illustrated in Fig. 1. The three-phase grid voltages are first measured and transformed into the synchronous reference frame (dq) using Park transformation. The q-axis component is then regulated to zero through a PI controller, allowing the estimation of the grid phase and frequency. This structure constitutes the classical dqPLL architecture, which serves as the reference framework for the modified and enhanced configurations proposed in this study. The figure highlights the fundamental operating principle upon which the comparative analysis of synchronization performance is based.

2.2 Modified dqPLL architecture

The modified dqPLL retains the main loop of the classical dqPLL(comprising the Park transformation, PI controller, and integrator), but introduces a parallel path

dedicated to harmonic compensation. This block processes the V_α and V_β signals, isolates specific harmonic orders (5th, 7th, 11th, and 13th), and subtracts them from the PLL input[12].

The modified dqPLL architecture is characterized by several key features that enhance its performance under distorted grid conditions. First, it incorporates selective harmonic detection, where the most critical harmonics (the 5th, 7th, 11th, and 13th orders) are identified to ensure accurate compensation. Second, a filtering stage (with red dots in Fig. 2) is introduced in which each harmonic order is isolated using appropriately tuned filters, allowing precise extraction of the unwanted components without affecting the fundamental frequency. Finally, in the compensation stage, the detected harmonics are subtracted from the dqPLL input signals, thereby yielding cleaner synchronization references for the PLL loop. Importantly, this compensation path operates in parallel with the main dqPLL loop, meaning that the primary control dynamics remain intact while harmonic rejection is significantly improved. As a result, the modified dqPLL achieves both enhanced frequency stability and reduced Total Harmonic Distortion (THD reduction from 9.052% to 0.36%), making it more suitable for three-phase grid-tied inverter applications operating under non-ideal grid conditions [12].

The modified dqPLL architecture presented in this section is proposed by the authors as part of this work. Its performance has been evaluated through offline analysis and validated experimentally using real-time digital simulation with real grid signals, ensuring its applicability under realistic operating conditions.

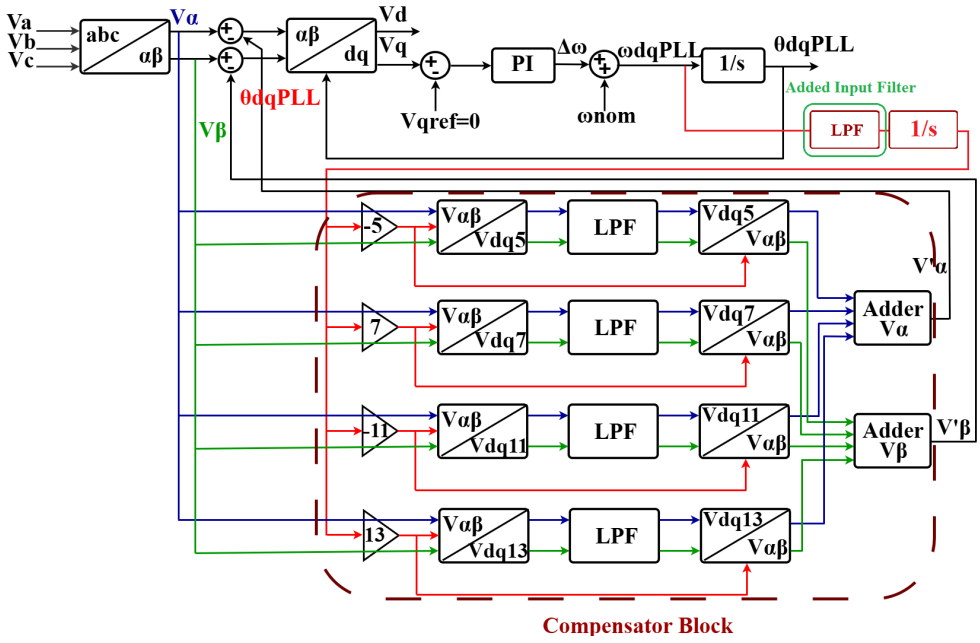


Fig. 2 Modified dqPLL architecture with compensator block

Although the modified dqPLL with harmonic compensation significantly improves frequency stability and reduces dominant harmonic amplitudes, residual oscillations remain observable in the instantaneous PLL frequency response. These oscillations propagate into the harmonic detection process, leading to small but persistent fluctuations around the nominal frequency.

To explicitly address this limitation, an input filter was introduced at the output of the PLL frequency before the harmonic compensation block. This filter aims to attenuate undesired frequency oscillatory components while preserving the fundamental synchronization dynamics. The inclusion of the input filter leads to a noticeable reduction of residual oscillations, and improved confinement of the frequency response around the desired central value of 50 Hz.

This design choice ensures that the compensator receives a cleaner signal, thereby minimizing oscillations in the frequency detection process. Importantly, the filter is not integrated into the main dqPLL loop, which preserves the dynamic response and stability of the PLL while enhancing harmonic detection accuracy.

The 5th, 7th, 11th, and 13th harmonic components are processed through their respective compensation branches using harmonic-specific coordinate transformations and filtering. The resulting compensation components are then combined to construct the harmonic compensation signal, which is used to mitigate the corresponding harmonic disturbances in the estimated grid synchronization variables.

The analytical formulation given in (1) clarifies the operating principle of the proposed harmonic compensation strategy. By performing selective dq transformation for each targeted harmonic, followed by low-pass filtering and inverse transformation, the method effectively isolates and attenuates dominant harmonic components without affecting the fundamental frequency.

$$V_{\alpha\beta i}(s) = \left[T_{dq}(i)\right]^{-1} f(s) \left[T_{dq}(i)\right] V_{\alpha\beta}(s) \tag{1}$$

where $V_{\alpha\beta i}$ represents the filtered output signals corresponding to the i-th harmonic component. In this study, the selected harmonic orders are $i = \{5, 7, 11, 13\}$, corresponding to the dominant low-order harmonics commonly observed under distorted grid conditions. $V_{\alpha\beta}$ represents the original $\alpha\beta$ input signals. The matrix $T_{dq}(i)$ denotes the Park transformation matrix associated with the i-th harmonic component and rotated by the θi angle, whereas $f(s)$ represents the transfer function of the low-pass filter implemented in the synchronous reference frame.

2.3 Theoretical Design and Parameter Selection of the Harmonic Compensation Filters

The harmonic compensation branches employ second-order low-pass filters to extract the selected harmonic components after the corresponding harmonic-specific synchronous-reference-frame transformation. The general transfer function of each filter is given by:

$$H(s) = \frac{\omega_c^2}{s^2 + 2\zeta\omega_c s + \omega_c^2} \tag{2}$$

where ω_c denotes the natural angular frequency of the filter and ζ is the damping ratio.

The filter parameters were selected according to two main requirements: harmonic selectivity and dynamic response. A sufficiently low bandwidth is required to attenuate undesired oscillatory components and isolate the low-frequency component associated with the targeted harmonic. However, an excessively narrow bandwidth increases the filter time constant and may introduce an undesirable delay in the harmonic compensation process.

The damping ratio determines the transient characteristics of the second-order filter. The theoretical percentage overshoot is expressed as

$$M_p = \exp\left(-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}\right) \times 100 \tag{3}$$

For $\zeta = 0.7$, the theoretical overshoot is approximately 4.6%, corresponding to a well-damped response. This value therefore provides a suitable compromise between transient damping and dynamic response and was adopted for all harmonic compensation filters.

The bandwidth was subsequently investigated to determine an appropriate compromise between harmonic extraction accuracy and synchronization dynamics. A parametric analysis was performed for several candidate bandwidths, namely 0.1, 0.2, 0.5, 1, and 2 Hz, while maintaining the remaining PLL parameters unchanged. For each configuration, the harmonic attenuation, THD, frequency error, and transient response were evaluated.

The results of this sensitivity analysis were used to select the final filter bandwidth. The selected value of 0.2 Hz provided a suitable compromise between attenuation of residual oscillatory components and the dynamic requirements of the harmonic compensation process. Lower cutoff frequencies provide stronger rejection of high-frequency residual components but increase the filter time constant and therefore slow down the compensation dynamics. Conversely, increasing the cutoff frequency improves the dynamic response at the expense of reduced filter selectivity. Then, the same bandwidth was adopted for the compensation branches associated with the 5th, 7th, 11th, and 13th harmonics.

2.4 Parameter Selection of the Input Filter

The cutoff frequency of the added input low-pass filter was selected according to the spectral characteristics of the synchronization signal rather than directly from the nominal grid frequency. In the synchronous reference frame, the low-order harmonic components considered in this study generate high-frequency oscillations in the synchronization variables. For a 50-Hz fundamental frequency, the dominant oscillatory components associated with the 5th and 7th harmonics occur around $6f_1 = 300$ Hz, whereas the 11th and 13th harmonics produce components around $12f_1 = 600$ Hz.

Consequently, the input filter should preserve the slowly varying information required by the synchronization and harmonic-compensation processes while attenuating these high-frequency oscillations. A second-order low-pass filter with a damping ratio of $\zeta = 0.7$ was therefore considered. The cutoff frequency of the input filter

was selected after evaluating several candidate values. The value of $f_c = 50\,\text{Hz}$ was retained for the final implementation based on the observed filtering performance and its impact on the PLL response. The obtained results showed that a cutoff frequency of $f_c = 50$ Hz provides an appropriate compromise between suppression of the high-frequency oscillatory components and preservation of the dynamic characteristics of the synchronization signal.

3 Methodology and Signal Processing

3.1 Signal Acquisition

The methodological process begins with the acquisition of a real three-phase voltage signal from the Valladolid electricity grid. To ensure safe measurement, the grid voltage of 230 V was reduced to 12 V using three transformers, followed by a voltage divider bridge composed of high-value resistors. This conditioning stage protected the acquisition hardware while preserving the waveform integrity. The Digilent Analog Discovery board, equipped with four 14-bit ADC channels, was used to capture the signals. Two channels were assigned to measure the grid phases and two channels to the neutral references, allowing acquisition of two phases at a time. The procedure was divided into two steps: acquisition of phases A and B, and acquisition of phases A and C. Each acquisition lasted 20 ms with a sampling interval of 2.5 µs, corresponding to one complete cycle of the grid signal. Longer acquisitions of 100 ms were also performed to capture multiple cycles for extended analysis.

The choice of resistor values was not arbitrary but based on achieving both safety and fidelity in the measurement process. The high-value resistors (220 kΩ) limited the current flowing into the acquisition circuit, thereby protecting the hardware from overload. Meanwhile, the lower-value resistors (8.2 kΩ) ensured that the voltage division ratio was appropriate to reproduce the waveform accurately without distortion. The resulting gain factor of approximately 0.036 was later used in the preprocessing stage to reconstruct the actual grid voltage from the scaled measurements. This calibration step was essential to guarantee that the signals processed in the measurement environment corresponded to the true grid conditions.

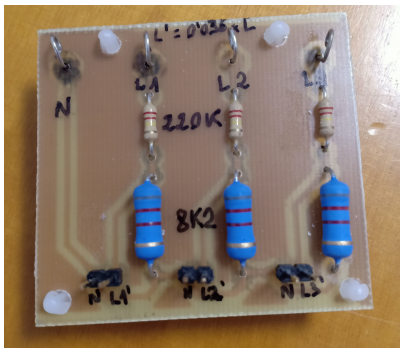


Fig. 3 Voltage divider stage prototype board

The voltage divider stage ensures that the measured voltage remains within the allowable input range of the acquisition system. This configuration guarantees safe operation while preserving waveform fidelity for harmonic and frequency analysis. The output voltage of each phase is obtained at the midpoint of the divider and can be expressed as:

$$V_{out} = V_{in} \frac{R_2}{R_1 + R_2} \tag{4}$$

Beyond its voltage range and resolution, the Digilent Analog Discovery board played a central role in ensuring flexibility and reliability during the acquisition stage. Its compact design integrates both oscilloscope and waveform generation capabilities, which allowed the experimental setup to be monitored and adjusted in real time without the need for additional laboratory instruments. Furthermore, its high sampling capability and USB-based communication interface facilitated accurate data transfer to the processing unit. This ensured precise synchronization between hardware measurements and real-time control implementation.

The electrical circuit corresponding to the voltage divider stage presented in Fig. 3 is depicted in Fig. 4. Each phase voltage is attenuated using a resistive divider consisting of a 220 kΩ series resistor and an 8.2 kΩ shunt resistor. The scaled voltage is extracted at the midpoint of the divider and supplied to the acquisition board.

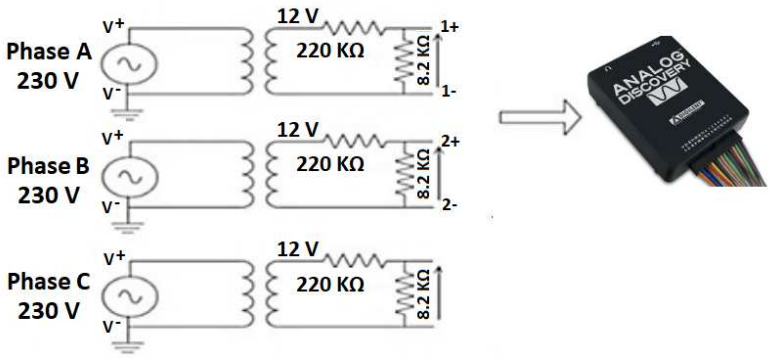


Fig. 4 Electrical circuit of the voltage divider stage

The acquisition experiment demonstrates the complete communication chain established between the grid interface and the processing unit. The three-phase voltage from the Spanish grid is first reduced by the isolation transformers to a safe level of 12 V, after which the voltage divider bridge further scales the signals to be adapted to the input range of the Digilent Analog Discovery.

In addition to the acquisition chain in Fig. 5, the test bench includes the RT Box 240 real-time simulator, which serves as the processing platform for implementing the proposed dqPLL algorithms. This unit enables real-time execution and validation of the synchronization strategies under realistic grid conditions. The combination of isolation transformers, passive conditioning circuits, high-resolution acquisition hardware, and real-time processing ensures both electrical safety and experimental accuracy.

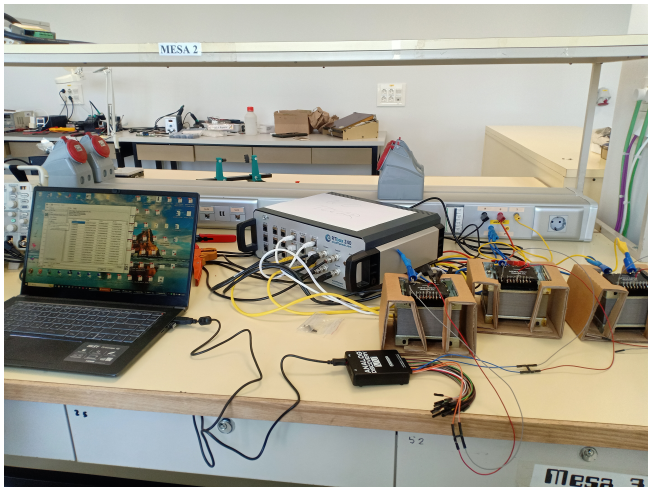


Fig. 5 Acquisition process experiment

The conditioned signal is then fed into the acquisition board, which digitizes the analog voltages and transmits them directly to the personal computer through its USB interface. The PC, equipped with the Analog ICs software, manages the configuration of the device, stores the acquired data in real time, and enables subsequent conversion into vector files for measurements. Each element of the setup therefore plays a specific role within the measurement–processing–validation loop, forming a coherent and reliable experimental platform.

3.2 Preprocessing of Data Vectors

After acquisition, the signals were exported into CSV format and processed in MATLAB and Excel environments. Preprocessing included offset removal and scaling by the resistance gain factor. To adapt the data to the memory and computational constraints of the RTDS hardware, the original 8192 samples were reduced to 8000, then down-sampled to 400 samples with an increased sampling interval of 50 µs. This resampling ensured efficient looping during simulation without introducing artificial noise or discontinuities. The resulting vectors represented the real grid signals in a format suitable for real-time digital simulation.

3.3 Implementation in AccurateRTDs

The real-time implementation was carried out using the RT Box 240 platform, which integrates a high-performance multi-core real-time processor operating at several hundreds of MHz and a dedicated FPGA module for deterministic real-time execution. The FPGA enables parallel processing and strict timing control, ensuring fixed-step execution without latency or jitter.

The processed vectors were integrated into the AccurateRTDS software environment, which interfaces directly with the RT Box 240 real-time digital simulation hardware. This architecture reproduces the dynamic behavior of grid synchronization

algorithms and evaluates their stability under realistic operating conditions, which cannot be fully captured using offline simulations alone.

The two architectures: classical dqPLL and modified dqPLL with harmonic compensation block, were implemented as embedded code modules. Each architecture was supplied with the same real grid vectors, ensuring a fair and consistent comparison. Each harmonic compensator sub-block was implemented using a second-order filter realized through a double-line coding structure. A uniform bandwidth of 0.2 Hz was selected as the cutoff frequency for all presented harmonic components. The AccurateRTDS platform enabled real-time execution of the algorithms, allowing the evaluation of instantaneous frequency, harmonic magnitudes, and total harmonic distortion (THD) under identical operating conditions.



Fig. 6 RT Box 240 real-time digital simulation hardware

3.4 Workflow Integration

The methodology thus establishes a closed loop from real grid acquisition to real-time digital simulation. By combining hardware-based signal conditioning, high-resolution acquisition, systematic preprocessing, and embedded implementation in RT Box 240, the study ensures that the comparison between the two dqPLL architectures is rigorous and representative of actual grid conditions. This methodological rigor provides the foundation for the subsequent analysis of frequency stability, harmonic suppression, and THD reduction.

4 Experimental Measurements and Discussion

This section presents the comparative analysis of the two dqPLL architectures: the classical dqPLL and the modified dqPLL with harmonic compensation. The evaluation was performed using real grid signals acquired in Valladolid, processed into data vectors, and implemented on the RT Box 240 hardware through AccurateRTDS software. We set the same PI regulator parameters for each dqPLL architecture, as well as the

tuning filter parameters of the compensator block. The results are discussed in terms of frequency stability, harmonic suppression, and total harmonic distortion (THD).

4.1 Acquired Signal Analysis

The acquisition of the real three-phase grid signals was carried out using the Digilent Analog Discovery board, and the data were subsequently processed and stored in CSV format for further analysis. After preprocessing of the data vectors, the signals were reconstructed in MATLAB by plotting the three voltage waveforms against time, which allowed a clear visualization of the sinusoidal behavior of the grid voltages, as shown in Fig. 7.

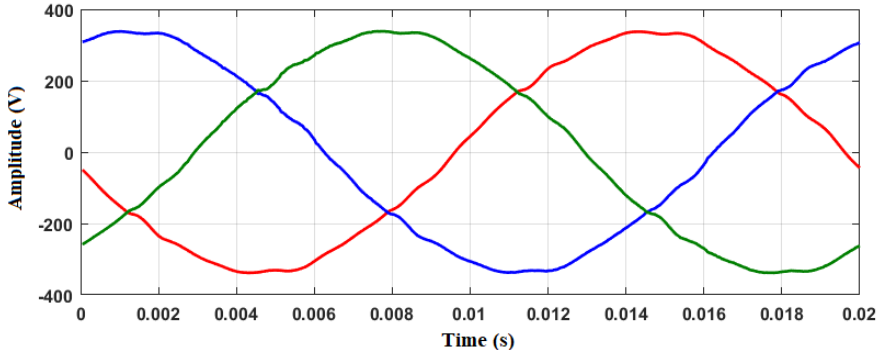


Fig. 7 Acquired three-phase signals

The reconstructed signals in Fig. 7 confirmed the expected periodicity of the grid with a nominal frequency close to 50 Hz, and the three phases exhibited the correct phase shift of approximately 120° between each other. These signals are not pure sinusoids, and the observed disturbances and deformations indicate the presence of harmonic components in the acquired signals.

The MATLAB representation provided a precise depiction of the acquired signals, ensuring that the data vectors were correctly synchronized and suitable for subsequent processing in the dqPLL architectures.

In addition to the time-domain representation, the harmonic content of the acquired signals was analyzed. The CSV vectors corresponding to one phase were imported into Excel, where the harmonic magnitudes were calculated and expressed in dBmV according to the following relation:

$$dBmV = 20 \times log_{10}(\frac{V}{1mV}) \tag{5}$$

The resulting harmonic spectrum was presented in the form of a bar diagram, showing the amplitudes of the fundamental component and the lower-order harmonics, as shown in Fig. 8. The diagram highlighted the presence of low-order harmonics such as the 5th, 7th, 11th, and 13th, which are typically observed in distorted grid

conditions. The fundamental component remained dominant, while the harmonic bars provided quantitative information about the distortion levels present in the acquired signal. This analysis established the baseline harmonic profile of the Valladolid grid signal, which served as the reference input for the comparative study of the two dqPLL architectures in the following subsections.

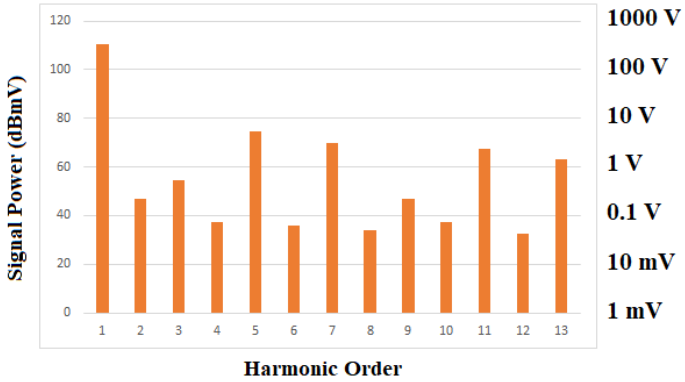


Fig. 8 Harmonic Power Spectrum

The power spectrum in Fig. 8 shows harmonic distortion in the acquired signal, with 1.57% from the fifth harmonic, 0.92% from the seventh harmonic, 0.69% from the eleventh harmonic, and 0.43% from the thirteenth harmonic.

Based on the harmonic amplitude vector extracted from the CSV file, the total harmonic distortion (THD) was computed to be 2.27% using the following equation:

$$THD\% = \frac{\sqrt{\sum_{n=2}^{N} V_n^2}}{V_1} \times 100 \tag{6}$$

4.2 Frequency Stability

This subsection evaluates the frequency stability of the two dqPLL architectures in real-time hardware implementation on the RT Box 240 under real-grid condition. The acquired three-phase signals from the Valladolid electricity grid were processed and used as inputs to the classical dqPLL and the modified dqPLL with harmonic compensation. The instantaneous frequency response was monitored and compared against the nominal grid frequency of 50 Hz as shown in Fig. 9.

The comparative frequency response in Fig. 9 highlights the improved dynamic performance of the modified dqPLL architecture relative to the classical dqPLL. Over the transient interval (0–0.9s), the classical dqPLL (Red curve) oscillates between 43 Hz and 59 Hz, corresponding to a maximum frequency error of ±8 Hz around the nominal 50 Hz (±16% of frequency error), while the modified dqPLL (Blue curve) achieves the most stable response, tightly bounded between 49.8 Hz and 50.2 Hz, i.e.,

an error margin of less than ±0.2 Hz (±0.4% of frequency error). These quantitative results confirm that the algorithmic improvements in the modified design significantly reduce frequency error and enhance synchronization robustness under dynamic grid condition.

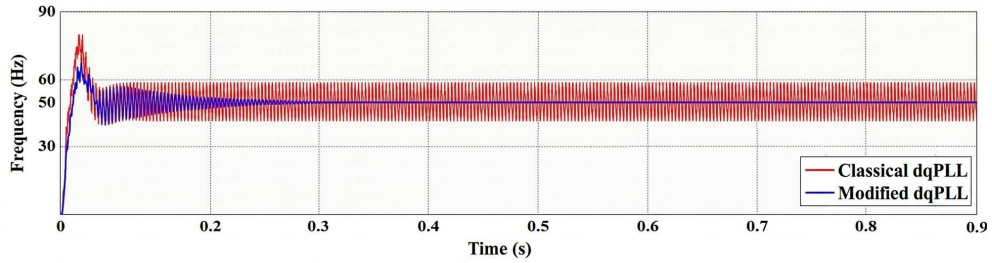


Fig. 9 Frequency responses of the considered dqPLL architectures

While the classical dqPLL exhibits significant oscillations and slower convergence following a disturbance, in Fig. 9, the modified dqPLL version demonstrates enhanced stability and faster settling behavior, and maintains a nearly constant frequency close to the nominal 50 Hz throughout the observation window, indicating robust tracking and minimal sensitivity to transient variations.

4.3 Harmonic Compensation

In addition to frequency stability, this sub-section evaluates the performance of the two dqPLL architectures in terms of harmonic power and magnitude reduction. After extracting the CSV file, we analyzed the power of each harmonic present in the V_α output signal. Using Excel software, we represented each harmonic power as a bar chart, as shown in Fig. 10.

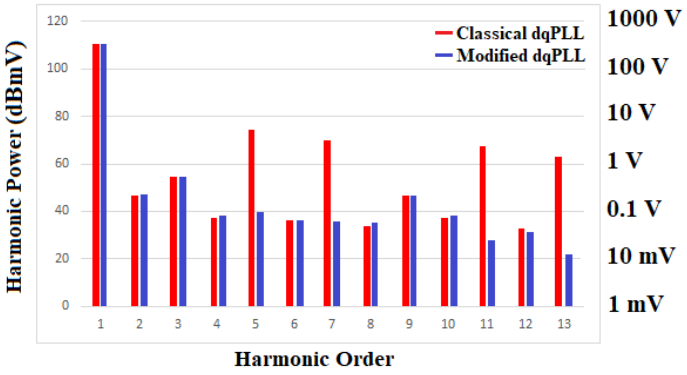


Fig. 10 Harmonic power spectrum (in dBmV) for harmonic orders 1–13 comparing two dqPLL architectures: Classical dqPLL (red bars), and Modified dqPLL (blue bars)

Fig. 10 presents a comparative bar graph illustrating the harmonic power levels (in dBmV) across harmonic orders 1 to 13 for the classical and the modified dqPLL architectures. Each harmonic order is represented by two bars: red and blue, corresponding respectively to the classical and the modified dqPLL. The red bars consistently show higher harmonic power, particularly at the 5th, 7th, 11th, and 13th orders, indicating that the classical dqPLL suffers from significant harmonic distortion. In contrast, the blue bars demonstrate substantial attenuation of these harmonics.

The modified dqPLL (represented by the blue bars) achieves the lowest power levels across all significant harmonic orders (5th, 7th, 11th, and 13th). This confirms that the addition of the filters attenuates harmonic content, while also preserving the fundamental frequency (harmonic order 1), which remains dominant in all cases.

The following table presents a comparative harmonic analysis of the input signal and the corresponding output signals obtained using the classical and the modified dqPLL designs:

Table 1 Harmonic amplitudes of input and output signals for different dqPLL methods

	Input Signal	Output Signal	
Harmonic	Amplitude (V)	Classical dqPLL Amplitude (V)	Modified dqPLL Amplitude (V)
1	335.52	335.52	335.44
5	5.26	5.25 (1.57%)	0.09 (0.02%)
7	3.07	3.07 (0.92%)	0.06 (0.01%)
11	2.33	2.32 (0.69%)	0.02 (0.007%)
13	1.44	1.45 (0.43%)	0.01 (0.003%)
THD	2.27%	2.27%	1.101%

In Table 1, the input signal is dominated by the fundamental component with an amplitude of 335.52 V, while relatively small amplitudes are present at the 5th, 7th, 11th, and 13th harmonics, resulting in an overall input THD of 2.27 %. The classical dqPLL reproduces the fundamental component almost exactly (335.52 V) and largely passes the harmonic components unchanged, as evidenced by harmonic amplitudes that closely match the input and an identical THD of 2.27%, indicating limited harmonic attenuation capability. In contrast, the modified dqPLL demonstrates a better harmonic suppression performance, further reducing the 5th and 7th harmonics to 0.09 V and 0.06 V, and almost eliminating the 11th and 13th harmonics to 0.02 V and 0.01 V, respectively. Consequently, the THD is slightly lowered to 1.101%, while the fundamental component remains effectively preserved at 335.44 V. Overall, the results clearly show that the modified dqPLL provides superior harmonic rejection and improved output signal quality.

In terms of computational burden, the classical dqPLL exhibits an execution time of 5.62 µs, whereas the modified dqPLL requires 25.40 µs. This increase in execution time is mainly attributed to the additional harmonic compensation block and filtering

stages introduced in the modified version, which significantly improve harmonic rejection and frequency stability under distorted grid conditions. Although the modified dqPLL presents the highest computational cost, its execution time remains well within the real-time constraints of typical digital control platforms used in power electronics applications. Therefore, the trade-off between improved synchronization performance and increased computational burden is justified, making the modified dqPLL a suitable candidate for practical implementation in smart grid and grid-connected inverter systems where robustness is a critical requirement.

5 Comparative Performance Analysis and Experimental Validation

To rigorously assess the performance, harmonic rejection capability, and dynamic response of the proposed modified dqPLL architecture, a detailed comparison with both baseline methods and state-of-the-art Phase-Locked Loop (PLL) algorithms was conducted. The evaluated architectures include the classical dqPLL (simulated in Matlab/Simulink and implemented in real-time HIL), the modified dqPLL (simulated and real-time HIL), as well as widely established grid synchronization algorithms from literature under similar experimental conditions, namely: the Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL)[6], the Single Second-Order Generalized Integrator PLL (SOGI-PLL)[21], the Dual SOGI-PLL (DSOGI-PLL)[22], and the Moving Average Filter-based PLL (MAF-PLL)[23]. The performance values reported for the SOGI-PLL, DDSRF-PLL, DSOGI-PLL, and MAF-PLL were obtained from the corresponding published studies. These values are included to provide a literature-based benchmark for the proposed Modified dqPLL. Since the results were reported under the test conditions of the respective studies, differences in input signals, parameter settings, and evaluation procedures are considered when interpreting the comparison.

The experimental real-time Hardware-in-the-Loop (HIL) implementation was executed on a high-performance RT Box 240 real-time digital simulator platform operating under realistic grid voltage harmonic disturbances (5^{th}, 7^{th}, 11^{th}, and 13^{th} order harmonics). Tables 2 and 3 synthesize the comprehensive quantitative and qualitative performance indicators across key metrics, including Total Harmonic Distortion (THD) attenuation, settling time (t_s), frequency estimation error (Δf), and harmonic rejection capability.

5.1 Discussion of Comparative Results and Key Contributions

As demonstrated in Tables 2 and 3, the proposed modified dqPLL demonstrates outstanding harmonic immunity, robust dynamic tracking, and high physical feasibility for real-time digital control applications:

1. **Harmonic Attenuation and Power Quality Enhancement:** Under real-time distorted grid-voltage conditions (input THD = 2.270%), the Classical dqPLL exhibits no measurable THD reduction in the RTDS experiment, with the output THD remaining equal to the input THD (2.270%). Traditional structures, such

Table 2 Harmonic power analysis of the proposed Modified dqPLL against simulated baselines and state-of-the-art PLL architectures

Architecture	Test Bed/Platform	Input THD (%)	Output THD (%)
Classical dqPLL	Matlab/Simulink	9.052	3.688
Modified dqPLL	Matlab/Simulink	9.052	0.3688
Classical dqPLL	RT Box 240 (RTDS)	2.270	2.270
Modified dqPLL (Proposed)	RT Box 240 (RTDS)	2.270	1.101
SOGI-PLL	Literature / HIL	2.270	2.150
DDSRF-PLL	Literature / HIL	2.270	1.850
DSOGI-PLL	Literature / HIL	2.270	1.700
MAF-PLL	Literature / HIL	2.270	1.150

Table 3 Comparative performance analysis of the proposed Modified dqPLL against simulated baselines and state-of-the-art PLL architectures

Architecture	Settling Time (s)	Freq. Error Hz (%)	Harmonic Rejection
Classical dqPLL	-	±24.5 (±49.0 %)	Weak
Modified dqPLL	0.80	±0.04 (±0.08 %)	Good
Classical dqPLL	0.35	±8.0 (±16.0 %)	Weak
Modified dqPLL (Proposed)	0.25	±0.2 (±0.40 %)	Superior
SOGI-PLL	0.04	±1.2 (±2.40 %)	Weak ($5^{\text{th}}, 7^{\text{th}}$)
DDSRF-PLL	0.06	±0.8 (±1.60 %)	Moderate
DSOGI-PLL	0.05	±0.6 (±1.20 %)	Moderate
MAF-PLL	0.12	±0.3 (±0.60 %)	Good

as the SOGI-PLL and DDSRF-PLL, exhibit limited rejection of higher-order harmonics (11^{th} and 13^{th}), with output THD values above 1.700%. In contrast, the proposed Modified dqPLL effectively attenuates both low- and high-order harmonics, reducing the output THD to 1.101% in the RTDS experiment and 0.3688% in simulation, thereby outperforming both the DSOGI-PLL (1.700%) and the MAF-PLL (1.150%).

2. **Frequency Tracking Precision:** Under steady-state harmonic pollution, the classical dqPLL exhibits unacceptable frequency estimation ripple (±8.0 Hz or 16.0% relative error in HIL; ±24.5 Hz in simulation). In sharp contrast, the modified dqPLL bounds the steady-state frequency error to a mere ±0.2 Hz (±0.40%), demonstrating high precision suitable for strict microgrid grid-code compliance.
3. **Transient Response:** During dynamic grid startup transients, the proposed architecture achieves a settling time of 0.25 s. While this is faster than the classical dqPLL (0.35 s), it is noticeably slower than state-of-the-art alternatives. This temporal trade-off stems from the narrow bandwidth (0.2 Hz) of the harmonic compensation filters required to achieve superior selective harmonic attenuation. Consequently, the architecture trades a fraction of dynamic speed for exceptional harmonic rejection and steady-state frequency stability (±0.2 Hz), representing a well-balanced compromise for distorted distribution grids.

4. **Real-Time Implementation Overhead on RT Box 240:** Executed on the RT Box 240 platform, the proposed modified dqPLL algorithm requires an execution time (τ_{exec}) of 25.40 μs. While slightly higher than the classical dqPLL (5.62 μs) due to the presence of the compensator block and filtering stages, this execution window easily complies with real-time digital control loops operating at standard PWM switching frequencies (10–20 kHz), confirming its computational viability for commercial inverter controllers and real-time HIL applications.

6 Conclusion

This paper presented the design, real-time hardware implementation, and experimental validation of a modified synchronous reference frame phase-locked loop (dqPLL) architecture equipped with a dedicated selective harmonic compensation block. Real three-phase grid voltage signals acquired from the Spanish utility grid were conditioned and deployed on an RT Box 240 Real-Time Digital Simulator using AccurateRTDS software to rigorously evaluate synchronization performance under realistic distorted grid conditions.

The experimental Hardware-in-the-Loop (HIL) results demonstrated that the proposed modified dqPLL significantly enhances power quality and synchronization accuracy compared with the classical dqPLL and established state-of-the-art PLL architectures. Specifically, the proposed harmonic compensation mechanism effectively attenuates the dominant 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonic components by more than 90%, reducing the overall output Total Harmonic Distortion (THD) from 2.27% to 1.101%. Furthermore, the instantaneous frequency deviation under severe grid distortion was drastically suppressed from $\pm$8.0 Hz ($\pm$16.0%) in the classical structure to within a narrow boundary of $\pm$0.2 Hz ($\pm$0.40%), while maintaining a fast transient response time of 0.25 s.

Although the addition of the selective filtering stage increases the computational execution time to 25.40 μs (compared to 5.62 μs for the basic dqPLL), this computational overhead remains well within the real-time execution constraints of standard power electronic digital controllers operating at typical PWM switching frequencies. Consequently, the proposed modified dqPLL provides a highly effective and practical trade-off between harmonic rejection capability, dynamic tracking performance, and real-time execution feasibility. Future work will focus on integrating self-tuning adaptive algorithms to dynamically adjust the filter parameters under wide grid frequency fluctuations and evaluating the architecture within closed-loop grid-tied converter applications.

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