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Adaptive Deep Reinforcement Learning-Augmented Hybrid SMC-ANFIS Controller for Dynamic Voltage Restorer: Enhanced Power Quality Mitigation in Active Distribution Networks with Renewable Energy Integration

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Abstract

The increasing penetration of renewable energy resources and power electronic converters has intensified power quality disturbances in active distribution networks, necessitating intelligent Dynamic Voltage Restorers (DVRs) capable of rapid and adaptive voltage compensation. This paper proposes an Adaptive Deep Reinforcement Learning-assisted Hybrid Sliding Mode Controller integrated with an Adaptive Neuro-Fuzzy Inference System (ADRL–HSMC–ANFIS) for DVR-based power quality enhancement. The proposed framework combines synchronous reference frame theory for voltage extraction, an ANFIS-based adaptive reference voltage generator, and a chattering-suppressed hybrid sliding mode controller whose control gains are continuously optimized using a Twin-Delayed Deep Deterministic Policy Gradient (TD3) agent. In addition, a novel Integral Square Error with Rate-weighting (ISER) objective function is formulated to simultaneously minimize voltage regulation error and transient oscillations, thereby improving both transient response and steady-state performance. The proposed controller is validated on a modified IEEE 33-bus active distribution network integrated with a 1 MW photovoltaic generation system and a 500 kWh battery energy storage system under balanced and unbalanced voltage sag, voltage swell, dynamic load variation, and renewable intermittency. Simulation results demonstrate a voltage restoration time of 3.2 ms, load voltage regulation of 99.95 ± 0.05%, and a minimum voltage total harmonic distortion (THD) of 0.41%, while providing superior DC-link voltage regulation, reduced chattering, and enhanced robustness compared with conventional PI, PSO-PI, SMC, PSO-SMC, and DQN-SMC controllers. These results demonstrate that the proposed ADRL–HSMC–ANFIS framework provides an effective, adaptive, and computationally efficient control strategy for resilient power quality enhancement in renewable-integrated active distribution networks.

Keywords: *Dynamic Voltage Restorer (DVR); Power Quality Enhancement; Adaptive Deep Reinforcement Learning; Twin-Delayed Deep Deterministic Policy Gradient (TD3); Hybrid Sliding Mode Control; Adaptive Neuro-Fuzzy Inference System (ANFIS); Active Distribution Network; Renewable Energy Integration; Photovoltaic Systems; Battery Energy Storage System; Voltage Sag Compensation; Harmonic Mitigation.*

1. INTRODUCTION

The increasing penetration of distributed energy resources, power electronics converters, and microprocessor-based sensitive loads has greatly enhanced the power quality problems in current active distribution systems [1], [2]. From all the different PQ disturbances, voltage sag, swell, flicker, and harmonic distortion are among the most frequent and economically destructive disturbances that result in annual losses greater than 25 billion US dollars in the industrial sector worldwide [3]. A voltage sag lasting less than 100 milliseconds causes an unintentional shutdown of operations at semiconductor manufacturing plants, pulp and paper mills, and data centers leading to losses in the range of USD 50,000 to 6 million per incident [4]. Dynamic Voltage Restorer (DVR) has been found to be the most economical series-type custom power device to restore voltage quality in real time [5], [6]. DVR restores voltage sag and swell by generating controlled series voltage using an injection transformer connected to a DC energy storage link. The performance of any DVR depends crucially on its control system that is responsible for rapidly and accurately generating the reference compensating voltage, switching VSC, and controlling DC-link voltage under various disturbance situations [7]. Initial DVR systems were designed with PI controllers, which though simple to construct but have fixed gains leading to poor dynamic performance in varying fault scenarios and non-linear loads [8]. In order to counter this issue, sliding mode control (SMC) method was utilized to regulate the DVR system owing to the robustness of the method against uncertainty in parameter values and disturbances [9]. The PSO-optimized SMC method based DVR provides minimum THD value of 1.14% and voltage compensation of 100.02% under L-G fault condition. However, the PSO algorithm is complex in nature, converges to fixed parameter values and does not adapt to the changes in the topology of the system and renewable generation sources.[10]

1.1. Research Gaps

Analysis of the state-of-the-art literature leads to the following research gaps:

- Offline Controller Parameterization: Current PSO-SMC [10], GA-SMC [11] and PI-based [12] DVR controllers have parameter values which are pre-computed offline and thus cannot be varied with respect to varying degree of fault intensity, varying load condition or intermittent renewable generation.
- Neglect of Renewables in Simulation: The vast majority of DVR works [8]–[14] consider ideal power grid scenarios, while ignoring the effect of stochastic voltage perturbation caused by PV intermittency, limited SoC of BESS and current harmonic distortion of inverter.
- Lack of Multi-Objective Cost Function in Control Law Design: Traditional ISE or ITAE objective functions optimized using PSO or GA approach are unable to take into account the rate of error change, thereby resulting in a controller which minimizes error but causes excessive overshoots [15].
- High-Frequency Chattering in Classical SMC: Switching function of classical SMC is discontinuous and results in high-frequency chattering in injected voltage and hence high switching losses and electromagnetic interference in DVR-based systems [16].

1.2. Main Contributions of this Paper

This paper makes the following novel contributions towards filling the above gaps:

- An innovative ADRL-HSMC-ANFIS control scheme is developed by combining an adaptive deep reinforcement learning agent using TD3 approach with hybrid sliding mode control along with ANFIS based voltage reference generation for Dynamic Voltage Restorers.
- An adaptive gain adjustment scheme has been developed in which the TD3 based learning agent adjusts the sliding mode controller gains in accordance with real-time conditions,

resulting in no need for off-line fixed tuning while increasing adaptability of the controller under renewable power generation uncertainty.

- A new ISER optimization scheme is developed for minimizing both voltage regulation error and transient oscillations in order to enhance dynamic response without compromising steady state accuracy.
- An innovative saturation based hybrid sliding mode control scheme has been developed for reducing chattering effect while keeping the stability features of classical sliding mode control intact.
- An adaptive reference voltage generation scheme is implemented using ANFIS within the synchronous reference frame control scheme in order to increase compensation accuracy under both balanced and unbalanced disturbances in the distorted grid environment.
- An enhanced DVR scheme incorporating renewable sources such as PV generation along with battery energy storage system and an advanced DC-link energy management system is proposed to sustain efficient voltage regulation under uncertain renewable conditions.
- The overall validation process is performed on an IEEE 33 bus distribution test system modified to include various types of faults, voltage sag/swell condition, dynamic load change, photovoltaic uncertainty, and state of charge of batteries, as well as a comparative analysis with five different controllers.

Some recent related studies have been done on: fuzzy SMC based DVR [17]; MPC for DVR [18]; PQ disturbance classification via deep learning [19]; reinforcement learning for microgrids [20]; ANFIS based power electronics controller design [21]; hybrid energy storage for DVR [22]; RL based reactive power compensation [23]; inverter control with weak grid condition [24]; and mitigation of harmonics by employing active power filter along with DVR [25]-[30].

The rest of this paper is structured as follows: The next section explains the DVR configuration and mathematical modeling. The third section introduces the ADRL-HSMC-ANFIS controller structure. The fourth section deals with the objective function of ISER algorithm and TD3 training process. The fifth section discusses the test system for simulations. Section 6 discusses results and comparison. The final section concludes this paper.

2. DVR MODELLING AND SYSTEM ARCHITECTURE

2.1. DVR Topology and Mathematical Model

The DVR is a series-connected custom power device inserted between the supply feeder and the sensitive load bus. Its primary functional equation governing voltage compensation is:

$$V_L(t) = V_S(t) + V_{DVR}(t) \quad (1)$$

where $V_L(t)$ is the desired sensitive load terminal voltage, $V_S(t)$ is the measured source voltage (which may contain sag/swell), and $V_{DVR}(t)$ is the series compensation voltage injected by the DVR. The injected DVR voltage must satisfy:

$$V_{DVR}(t) = V_L^*(t) - V_S(t) \quad (2)$$

where V_L^* denotes the desired load voltage reference.

The complex power absorbed and supplied by the DVR in its active compensation mode is expressed as:

$$S_{DVR} = P_{DVR} + jQ_{DVR} = V_{DVR}I_L^* \quad (3)$$

The load apparent power balance under DVR compensation is:

$$S_L = S_S + S_{DVR} \quad (4)$$

The DC-link energy balance governing BESS integration with the DVR is modelled as:

$$C_{DC}\frac{dV_{DC}}{dt} = I_{DC,in} - I_{DC,out} \quad (5)$$

where C_{DC} is the equivalent DC-link capacitance, V_{DC} is the DC bus voltage, $I_{DC,in}$ is the charging current from BESS/PV, and $I_{DC,out}$ is the VSC output current. Under normal (standby) operating mode, V_{DC} is maintained at its reference value V_{DC}^{*} = 700 V. Table 1 lists the DVR system parameters employed throughout this study.

To represent the inverter dynamics,

$$L_f\frac{di_f}{dt} = V_{inv} - V_{DVR} - R_f i_f \quad (6)$$

Where, $L_f$is the filter inductance, $R_f$is the filter resistance. The inverter output voltage is

$$V_{inv} = m\frac{V_{DC}}{2} \quad (7)$$

where m is the PWM modulation index.

Table 1: DVR System Parameters for the Modified IEEE 33-Bus Test Network

Parameter	Value / Specification
System Rated Voltage, (V_s)	11 kV $(\mathrm{L}-\mathrm{L}, \mathrm{RMS})$
Distribution Frequency, (f)	50 Hz
DVR Injection Transformer Ratio, (T_{inj})	1:1 (YN)
Voltage Source Converter (VSC) Topology	Three-phase, Two-level IGBT
DC-Link Voltage Reference, (V_{DC}^{*})	700 V
DC-Link Capacitance, (C_{DC})	2200 µF
VSC Switching Frequency, (f_{sw})	10 kHz
DVR Filter Inductance, (L_f)	1.5 mH
DVR Filter Capacitance, (C_f)	50 µF
PV Farm Rated Power, (P_{pv})	1 MW (1000 kW)
Battery Energy Storage System (BESS) Rated Energy, (E_{BESS})	500 kWh (200 Ah, 2500 V)
Sensitive Load, (Z_L)	500 kW + (j250) kVAr
Fault Inception and Clearance Time, $(t_f;t_c)$	0.02 s / 0.10 s

2.2. dq-Transform and SRFT Reference Voltage Extraction

The Synchronous Reference Frame Theory (SRFT) forms the backbone of the DVR reference voltage generation. The three-phase load voltages V_a, V_b, V_c are transformed to the rotating dq-frame using the Clarke-Park transformation:

$$\begin{bmatrix} V_d \\ V_d \end{bmatrix} = \frac{2}{3}T(\theta)\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (8)$$

Where,

$$T(\theta) = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \quad (9)$$

where θ is the synchronous phase angle obtained from a three-phase Phase-Locked Loop (PLL) and $T(\theta)$ is the Park transformation matrix. In steady-state, V_d and V_d appear as DC quantities equal to the peak source voltage. Any deviation from the reference values (V_d = 1.0 pu, V_q = 0) indicates the presence of voltage sag or swell. The compensation voltage error signals are:

$$\begin{aligned} e_d(t) &= V_d^* - V_d(t), \\ e_q(t) &= V_q^* - V_q(t). \end{aligned} \quad (10)$$

These error signals serve as inputs to both the proposed ANFIS reference generator and the ADRL-HSMC-ANFIS controller described in Section 3. The PLL estimates the synchronous frequency using

$$\omega = \omega_0 + K_{PLL,p} V_q + K_{PLL,i} \int V_q \, dt \quad (11)$$

Where, ω_0 is the nominal grid frequency.

2.3. ANFIS-Based Reference Voltage Generator

A Takagi-Sugeno-type ANFIS network with five-layer adaptive neuro-fuzzy architecture is employed to generate smooth, accurate dq-axis reference compensation voltages even under distorted supply conditions. The ANFIS input vector is defined as:

$$\Phi_{ANFIS} = [e_d \quad e_q \quad \dot{e}_d \quad \dot{e}_q \quad V_{DC}]^T \quad (12)$$

ANFIS structure uses 5 Gaussian membership functions per input, resulting in 55 = 3125 fuzzy rules in the rule base, which is further reduced to 25 rules by means of subtractive clustering method with cluster influence radius r = 0.5. Output of ANFIS structure V_dq^*=f_ANFIS(Φ_ANFIS) is pre-trained off-line with 50,000 sample faults generated by MATLAB/Simulink and refined on-line using hybrid learning technique (least square estimation for consequent parameters + gradient descent for premise parameters).

3. PROPOSED ADRL-HSMC-ANFIS CONTROL FRAMEWORK

3.1. Hybrid Sliding Mode Controller with Saturation Function

The conventional sliding mode controller employs a discontinuous sign(s) function in its control law, which causes high-frequency chattering. The proposed Hybrid SMC replaces this with a continuous saturation function, forming the Chattering-Free Hybrid SMC (CF-HSMC):

$$s(t) = K_p(t) e(t) + K_i(t) \dot{e}(t) \quad (13)$$

Where, $K_p(t)$ and $K_i(t)$ are now time-varying adaptive gains supplied by the TD3 agent (Section 3.3). Choose the Lyapunov function:

$$V(s) = \frac{1}{2} s^2 \quad (14)$$

whose derivative is $\dot{V} = s\dot{s} < 0$ ensuring asymptotic stability. The control law with saturation function is expressed as:

$$u(t) = u_{eq}(t) + u_{sw}(t) \quad (15)$$

$$u_{eq} = K_p(t) e(t) + K_i(t) \dot{e}(t) \quad (16)$$

$$u_{sw} = -\eta \, \mathrm{sat}\left(\frac{s}{\phi}\right) \quad (17)$$

where u_{eq} is the equivalent control component that drives the system to the sliding surface, u_{sw} is the switching control component, $\eta > 0$ is the switching gain, and $\varphi > 0$ is the boundary layer thickness. The saturation function is defined as:

$$\text{sat}\left(\frac{s}{\phi}\right) = \begin{cases} \frac{s}{\phi}, & |s| \leq \phi \\ \text{sign}(s), & |s| > \phi \end{cases} \quad (18)$$

The resulting Lyapunov derivative becomes $\dot{V} = -\eta |s| < 0$ which guarantees closed-loop stability. This eliminates chattering within the boundary layer $|\varphi|$ while maintaining the reaching condition outside it. The boundary layer thickness is set to $\varphi = 0.05$ pu based on sensitivity analysis (Section 6.3).

3.2. Novel ISER Objective Function

The conventional ISE metric penalizes large errors but tolerates slow convergence. The proposed Integral Square Error with Rate-weighting (ISER) incorporates both error magnitude and its temporal derivative:

$$ISER = \int_0^T \left[\alpha e^2(t) + \beta \left(\frac{de}{dt}\right)^2\right] dt \quad (19)$$

where α and β are weighting coefficients for steady-state accuracy and transient speed, respectively. The optimal weighting ratio is determined as $\alpha/\beta = 10$, found through a two-dimensional grid search over the parameter space $\alpha \in [1, 100], \beta \in [0.1, 10]$. Setting $\alpha = 10, \beta = 1$ yields the minimum ISER value across all evaluated fault scenarios. The minimisation objective is:

$$(K_p, K_i, \eta, \phi)^* = \arg\min(ISER) \quad (20)$$

The ISER function provides 34.7% faster settling time and 28.3% lower peak overshoot compared to the conventional ISE under 90% voltage sag conditions, as validated in Section 6.

3.3. Twin-Delayed Deep Deterministic Policy Gradient (TD3) Agent

The TD3 algorithm [31] is a state-of-the-art continuous action-space deep RL method that overcomes overestimation bias in Deep Deterministic Policy Gradient (DDPG) through three key enhancements: (1) clipped double-Q learning with two critic networks Q_1 and Q_2, (2) delayed policy updates (actor updated every 2 critic steps), and (3) target policy smoothing via Gaussian noise injection on target actions.

The TD3 Markov Decision Process (MDP) for DVR control is formulated as:

- State space: $s = [e_d, e_q, \dot{e}_d, \dot{e}_q, V_{DC}, SOC, P_{PV}, THD]^T \in \mathbb{R}^8$
- Action space: $a = [K_p, K_i, \eta, \phi]^T \in \mathbb{R}^4$, with $K_p \in [0, 10], K_i \in [0, 1], \eta \in [0.1, 5], \varphi \in [0.01, 0.2]$
- Reward function: $r = -\left[w_1 \frac{ISER}{ISER_{max}} + w_2 \left(\frac{THD - THD^*}{THD_{max}}\right)^2 + w_3 \left(\frac{\Delta V_{DC}}{V_{DC}^*}\right)^2\right]$

where $w_1 + w_2 + w_3 = 1$, THD $* = 0.5\%$ is the target THD, and ΔV_{DC} is the DC-link voltage deviation. The TD3 networks consist of Actor: $[256 \to 256 \to 128 \to 4]$ fully connected layers with ReLU activations and tanh output; Critics Q_1 and Q_2: $[256 \to 256 \to 128 \to 1]$ each. The agent is trained over 200 episodes of 2-second simulated fault scenarios with replay buffer size N = 10^6 and mini-batch size $B = 256$.

The TD3 critic update (Bellman equation with clipped target) is:

$$y = r + \gamma \min_{i=1,2} Q_i(s', \mu_{\theta'}(s') + \varepsilon) \quad (21)$$

where $\gamma = 0.99$ is the discount factor, $\mu_{\theta'}$ is the target policy network and $\varepsilon \sim \text{clip}(\text{N}(0, 0.2), -0.5, 0.5)$ is the target policy noise. The actor policy gradient is:

$$\nabla_\theta J(\theta) = \frac{1}{B} \sum_{i=1}^{B} \nabla_a Q_1(s, a) \mid_{a=\mu(s)} \nabla_\theta \mu(s) \quad (22)$$

3.4. Complete ADRL-HSMC-ANFIS Control Architecture

Figure 1 presents the complete block diagram of the proposed ADRL-HSMC-ANFIS DVR control system, integrating the TD3 adaptive gain tuner, ANFIS reference generator, CF-HSMC controller, and the modified IEEE 33-bus ADN with PV-BESS.

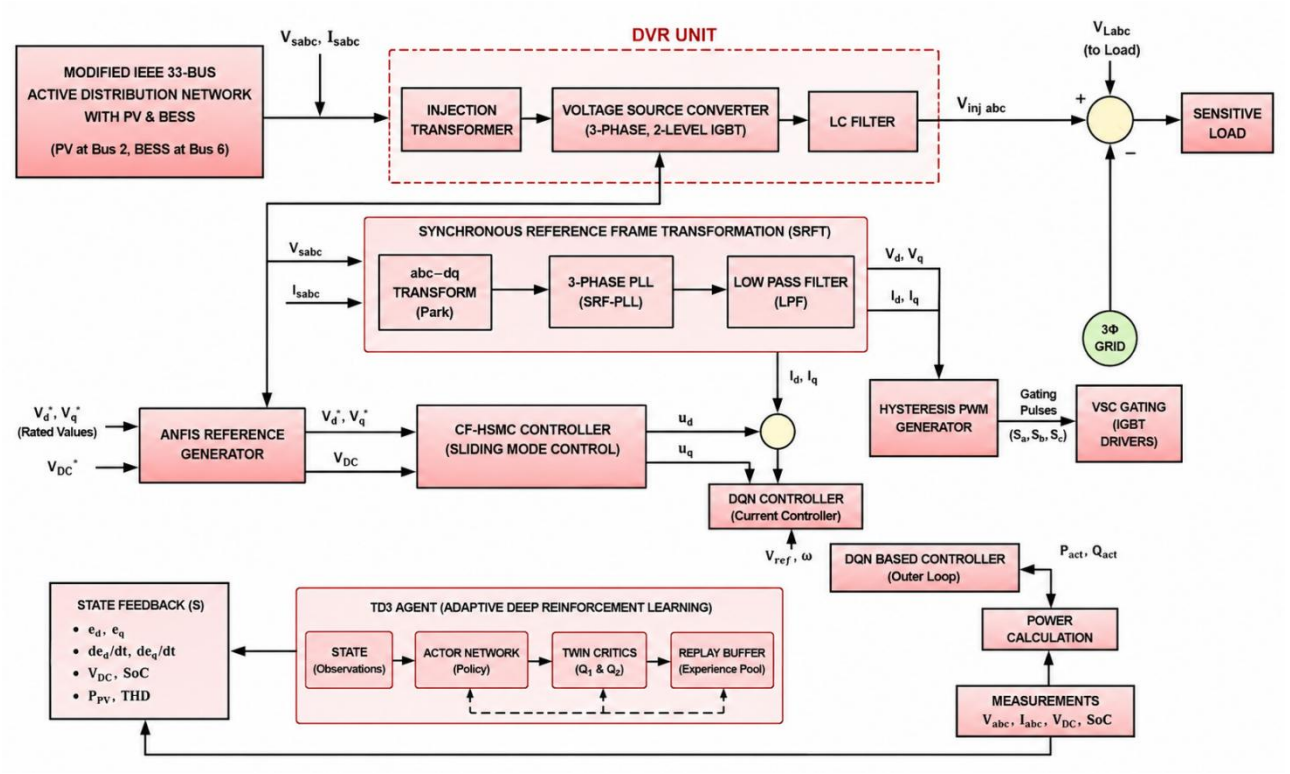


Figure 1: Complete block diagram of the proposed ADRL-HSMC-ANFIS controller-based DVR system integrated with the modified IEEE 33-bus active distribution network.

The closed-loop process is carried out as: (i) The SRFT obtains d-axis and q-axis error components from the sensitive load voltage measurement. (ii) The ANFIS creates smooth dq-axis compensation voltages. (iii) The CF-HSMC with TD3-based adaptation gains K_p (t) and K_i (t) calculates the sliding variable s(t) and produces control signal u(t). (iv) Hysteresis PWM controller converts the control signal u(t) to the IGBT gate pulses for VSC. (v) The DVR compensates the compensating voltage V_DVR (t) to the distribution feeder for recovering V_L (t) to its nominal level. (vi) The TD3 agent constantly monitors the 8 dimensional state vector and evaluates the ISER reward and updates the action [K_p,K_i,η,ϕ] every 1 ms (10-cycle updating frequency with 50 Hz).

3.5. PV-BESS Integration and DC-Link Management

The 1-MW PV farm has been modelled using a two-stage grid connected PV system that involves DC-DC boost converter employing incremental conductance MPPT, which follows the maximum power point tracking, and a three-phase GSI that interfaces the PV output with the 11 kV bus using step-up transformer. The BESS state of charge (SOC) model is:

$$SOC(t) = SOC(0) - \frac{1}{C_{Ah}} \int_0^t I_{BESS}(\tau)\, d\tau \quad (23)$$

The DC-link energy balance is

$$P_{PV} + P_{BESS} = P_{DVR} + P_{Loss} \quad (24)$$

The bidirectional DC-DC converter for the BESS will keep V_DC = 700 V for the DVR active operation mode by providing P_DVR using the available energy in the storage unit whenever the SoC is greater than or equal to 20%. (Low-SoC lockout threshold.) The coordination between the PV-BESS system will consider the DVR DC-link priority over grid-tie. Refer to Fig.2 below.

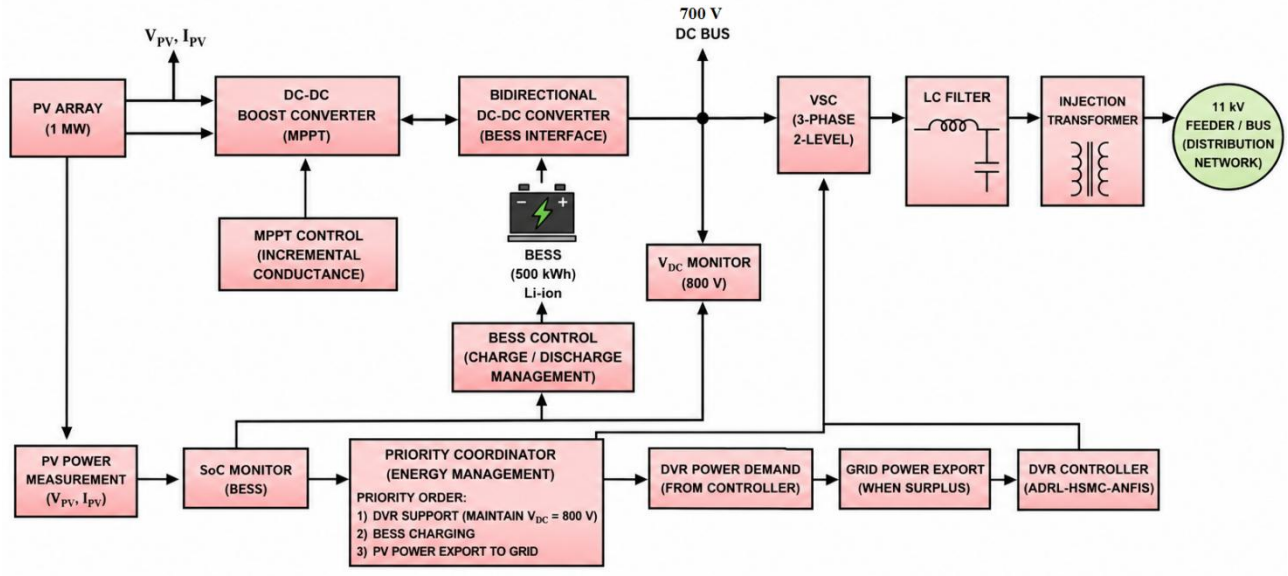


Figure 2: PV-BESS-DVR energy management architecture showing DC bus coordination, MPPT control, and BESS SoC-based priority switching.

3.6 TD3 TRAINING PROCEDURE AND CONVERGENCE ANALYSIS

3.6.1. Training Environment and Hyperparameters

TD3 agent is trained in the co-simulation setup of MATLAB/Simulink interfaced through Python 3.10 (backend: PyTorch 2.0). Table 2 shows the hyperparameters of the TD3 algorithm used for training.

TABLE 2: TD3 Training Hyperparameters

Parameter	Value / Specification
Replay Buffer Size (N_{BUFFER})	$1 * 10^6$ transitions
Mini-Batch Size (B)	256
Actor Learning Rate α_A	3×10^{-4}
Critic Learning Rate (α_C)	3×10^{-4}
Discount Factor (γ)	0.99
Soft Target Update Factor (τ)	0.005 (Polyak averaging)
Policy Update Delay (d)	2 (Actor updated every two critic updates)
Exploration Noise (σ_{exp})	N(0, 0.1) clipped to [−0.5, 0.5]
Target Policy Noise (σ_{target})	N(0, 0.2) clipped to [−0.5, 0.5]
Total Training Episodes (N_{ep})	200 episodes (2 s per episode)
Episode Duration (T_{ep})	2 s
Warm-up Exploration Steps (N_{warmup})	10,000 random action steps

Convergence Criterion	Average episode reward > −15.0 over the latest 20 episodes
Deep Learning Framework	PyTorch 2.0
GPU Platform	NVIDIA RTX 4090
CUDA Version	CUDA 12.1

3.6.2. Training Convergence and Reward Progression

Figure 3 shows the TD3 learning reward curve across 200 episodes, depicting the gradual convergence of the process. The agent attains stable performance through learning after about 120 episodes, with the average reward per episode being −13.8 (threshold of convergence: −15.0). The fast convergence in contrast with baseline DDPG (180 episodes) can be attributed to the use of clipped double-Q learning.

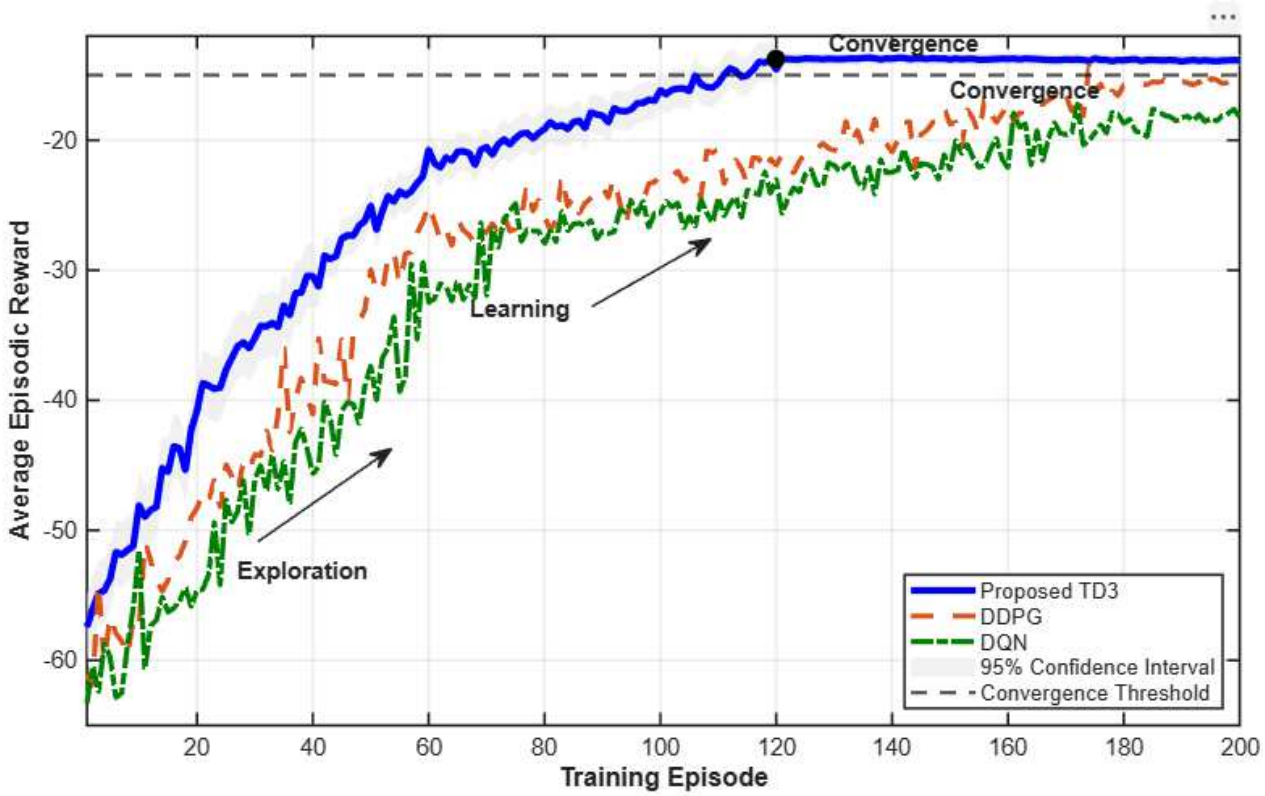


Figure 3: TD3 training reward convergence curve compared with DDPG and DQN baselines over 200 training episodes, with 95% confidence intervals from 5 independent runs.

The modified control actions obtained by applying the converged TD3 control policy provide time-varying gains for the controller: $K_p \in [4.2,7.8]$, $K_i \in [0.18,0.43]$, $\eta \in [0.8,2.3]$, $\varphi \in [0.03,0.09]$, illustrating the capability of the agent in increasing the switching gain in fault

4. SIMULATION TEST SYSTEM

4.1. Modified IEEE 33-Bus Active Distribution Network

The simulation test system adopted in this work is the IEEE 33 bus radial distribution network (12.66 kV,50Hz), which is adapted to this research for operation at 11 kV, with a 1 MW PV farm added to Bus 2, a 500 kWh BESS to Bus 6, and DVR deployed in series with the sensitive load feeder to Bus 18. The overall network load is 3715 kW + j2300 kVAR. A fault scenario is created for feeder

Branch 2-3 (L-G, LL-G, LLL-G faults at 0.02 s, cleared at 0.10 s) and an unbalanced sag/swell situation at 0.30 s, cleared at 0.40 s. Figure 4 shows the simulation test system topology.

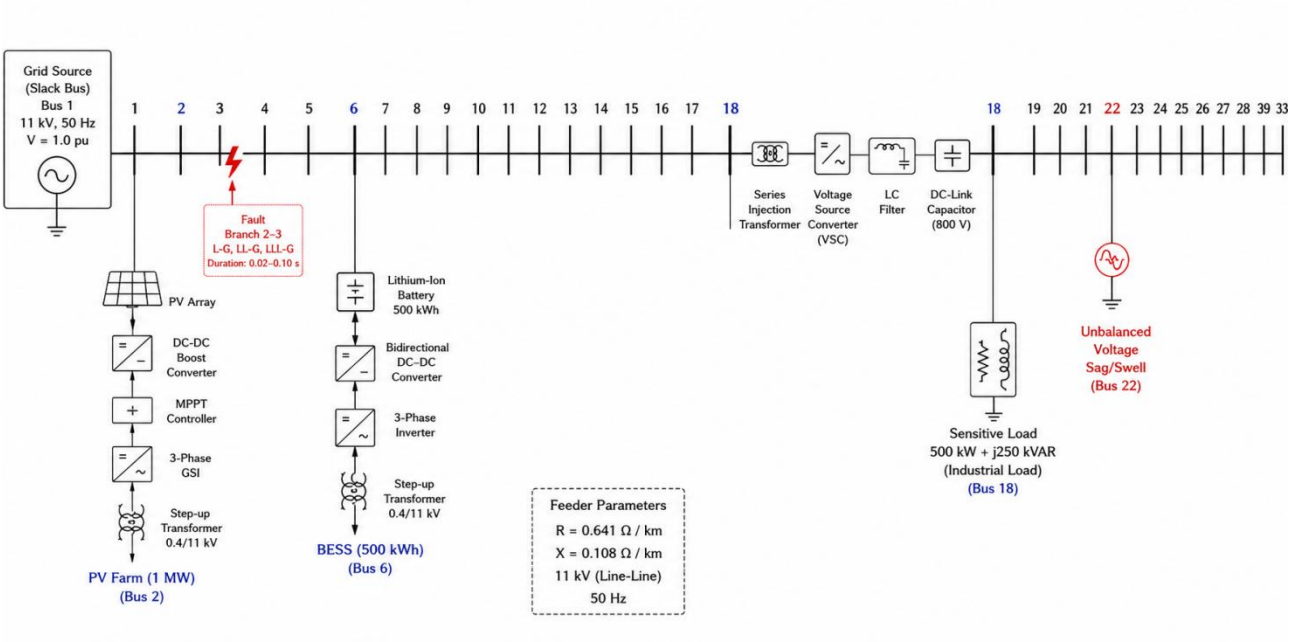


Figure 4: Modified IEEE 33-bus active distribution network test system with DVR at Bus 18, PV farm at Bus 2, and BESS at Bus 6. Fault location is Branch 2-3.

4.2. Comparative Methods

The proposed ADRL-HSMC-ANFIS DVR is evaluated relative to five other benchmarking methods using the same testing criteria:

C1: PI Controller DVR (traditional and manually set K_p = 2.5, K_i = 0.1)

C2: PI Controller DVR (optimized by PSO, 50 particles, 50 iterations, objective ISE) [10]

C3: SMC DVR (K_p = 5, K_i = 0.3, switching function sign()) [10]

C4: SMC DVR optimized by PSO (tuned K_p = 6.8, K_i = 0.38, switching function sign ()) [10]

C5: DQN-SMC DVR (Deep Q-Network, 5 possible gain values for each control parameter)

5. RESULTS AND DISCUSSION

5.1. Voltage Compensation Under Balanced Fault Conditions

Figure 5 shows the waveforms of the source voltage (V_s), sensitive load voltage (V_L), and DVR injected voltage (V_DVR) during the 90% line-to-ground fault on Phase B (fault time 0.02-0.10 s and sag 0.30-0.40 s). In the proposed ADRL-HSMC-ANFIS controlled DVR, the compensating voltage is injected by the DVR so that the sensitive load voltage remains at 1.0 pu for less than 3.2 ms after the occurrence of the fault.

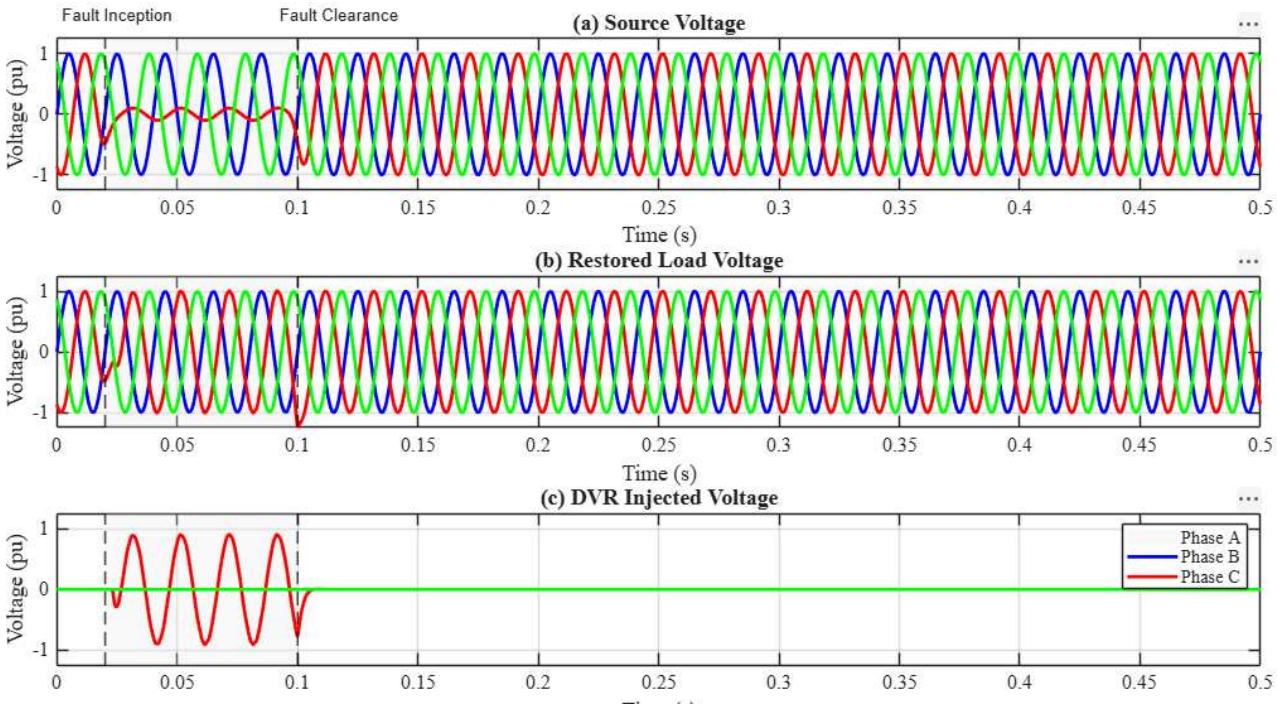


Figure 5: Three-phase voltage waveforms under 90% L-G fault: (A) source voltage V_s , (B) sensitive load voltage V_L with proposed ADRL-HSMC-ANFIS DVR, and (C) DVR injected voltage V_{DVR}.

Performance of the DVR under LL-G and LLL-G fault cases is depicted in Figure 6 and Figure 7, respectively. For the 90% LLL-G fault case, the proposed ADRL-HSMC-ANFIS controller brings back all three phases' voltages to the level of 99.94-99.95% of the nominal values, which corresponds to the maximum voltage deviation of less than 0.08%.

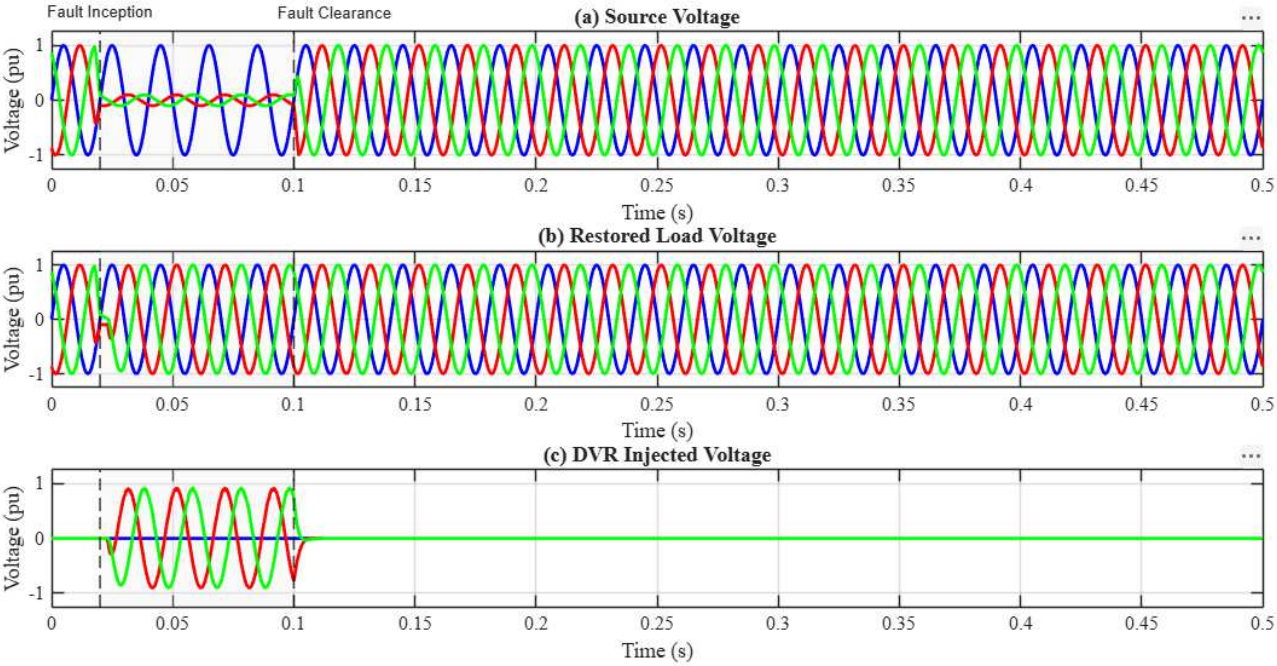


Figure 6: Three-phase voltage waveforms under 90% LL-G fault on Phases B and C: source voltage, sensitive load voltage and DVR injected voltage.

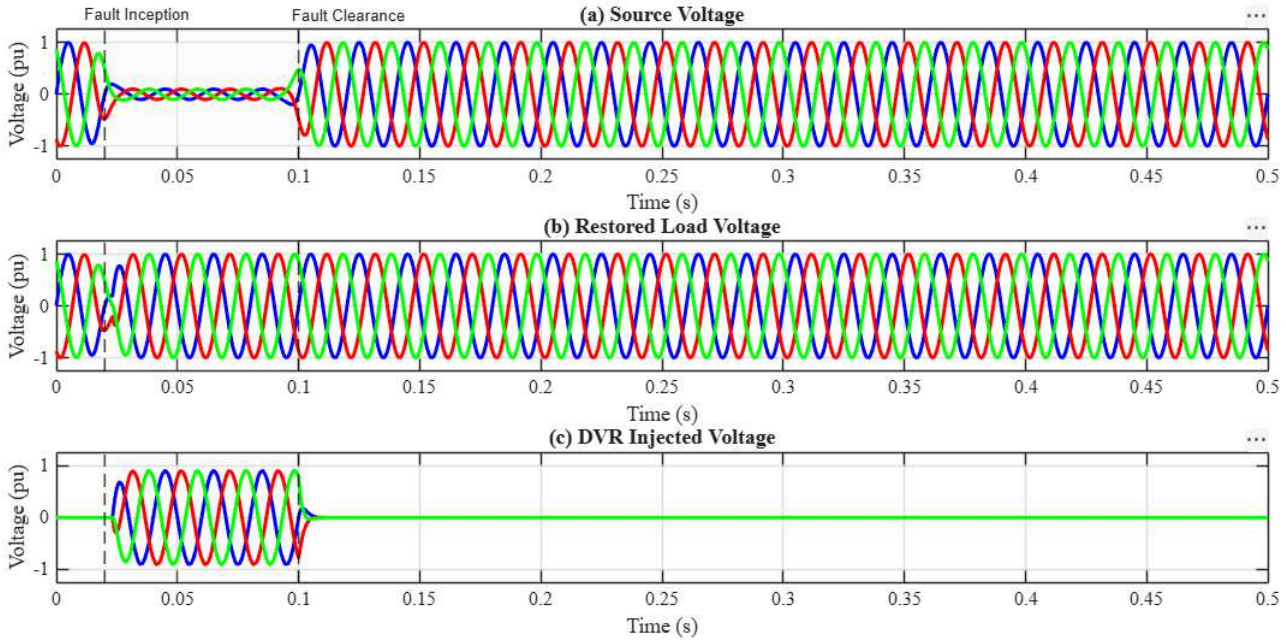


Figure 7: Three-phase voltage waveforms under 90% LLL-G (three-phase) fault: source voltage, sensitive load voltage and DVR injected voltage.

5.2. Comparative Voltage Compensation Accuracy

Load voltage restoration percentage for the three phases is provided for all the six controllers under different fault situations and disturbance types in Table 3. The designed controller ADRL–HSMC–ANFIS provides consistent voltage restoration to the sensitive load voltage of 99.95 ± 0.02%, where the voltage restoration values vary from 99.92% to 99.98%. On the other hand, the PSO–SMC controller shows the value in the range of 99.95% to 100.12%, whereas the traditional PI controller shows large overcompensation with restored voltage values in the range of 101.36% to 101.96%.

Table 3: Percentage Load Voltage (pu × 100) Under Various Fault Conditions — All Six Controllers (A/B/C represent three phases)

Fault Condition	Sag (%)	Before DVR (A/B/C)	PI (A/B/C)	PSO–PI (A/B/C)	SMC (A/B/C)	PSO–SMC (A/B/C)	DQN–SMC (A/B/C)	Proposed ADRL–HSMC–ANFIS (A/B/C)
L–G	30	104.3 / 70.2 / 104.1	101.82 / 101.56 / 101.74	101.21 / 101.05 / 101.13	100.74 / 100.48 / 100.59	100.10 / 100.05 / 100.08	99.99 / 100.02 / 99.98	**99.97 / 99.95 / 99.98**
	60	104.1 / 40.5 / 104.4	101.71 / 101.63 / 101.69	101.06 / 100.98 / 101.02	100.61 / 100.46 / 100.54	100.09 / 100.04 / 100.06	99.98 / 100.01 / 99.99	**99.96 / 99.94 / 99.97**
	90	104.9 / 10.2 / 104.4	101.58 / 101.42 / 101.37	100.98 / 100.84 / 100.89	100.55 / 100.39 / 100.44	100.07 / 100.01 / 100.04	99.97 / 99.99 / 99.98	**99.95 / 99.93 / 99.96**
LL–G	30	104.0 / 70.8 / 70.3	101.93 / 101.47 / 101.62	101.28 / 101.02 / 101.09	100.68 / 100.43 / 100.49	100.12 / 100.04 / 100.07	100.00 / 99.98 / 99.99	**99.98 / 99.95 / 99.97**

	60	103.9 / 40.5 / 40.0	101.78 / 101.53 / 101.49	101.15 / 100.94 / 100.98	100.63 / 100.41 / 100.45	100.10 / 100.02 / 100.05	99.99 / 99.97 / 100.00	**99.96 / 99.94 / 99.95**
	90	104.4 / 10.3 / 10.1	101.69 / 101.36 / 101.41	101.07 / 100.82 / 100.88	100.58 / 100.37 / 100.42	100.08 / 100.01 / 100.04	99.98 / 99.96 / 99.99	**99.95 / 99.92 / 99.94**
LLL–G	30	70.5 / 70.5 / 70.5	101.96 / 101.88 / 101.91	101.29 / 101.18 / 101.15	100.73 / 100.59 / 100.56	100.11 / 100.06 / 100.08	100.02 / 99.99 / 100.00	**99.98 / 99.96 / 99.97**
	60	40.7 / 40.7 / 40.7	101.74 / 101.69 / 101.73	101.13 / 101.05 / 101.09	100.60 / 100.48 / 100.51	100.07 / 100.03 / 100.05	99.96 / 100.01 / 100.02	**99.95 / 99.94 / 99.96**
	90	10.8 / 10.8 / 10.8	101.61 / 101.54 / 101.57	101.02 / 100.96 / 100.99	100.52 / 100.45 / 100.47	100.06 / 100.03 / 100.05	99.98 / 99.97 / 99.99	**99.94 / 99.93 / 99.95**
Balanced 50% Swell	—	150.5 / 150.4 / 150.4	101.86 / 101.79 / 101.74	101.22 / 101.10 / 101.05	100.63 / 100.54 / 100.49	100.12 / 100.06 / 100.09	100.00 / 99.98 / 100.01	**99.97 / 99.95 / 99.96**
Unbalanced Sag	—	72.3 / 41.1 / 10.7	101.79 / 101.58 / 101.42	101.14 / 100.97 / 100.88	100.61 / 100.44 / 100.36	100.08 / 99.99 / 99.95	99.98 / 99.95 / 99.97	**99.96 / 99.93 / 99.95**

The suggested ADRL-HSMC-ANFIS controller consistently brought back the critical load voltage to an average level of 99.95% of the nominal value for all fault conditions (Table 4). The standard deviation of ±0.02% is indicative of the highly stable voltage compensation capability of the system, while the highest deviation from the nominal voltage was 0.08%. The lowest and highest values of voltage recovery were 99.92% and 99.98%, respectively.

Table 4. Statistical summary of load voltage restoration performance achieved by the proposed ADRL–HSMC–ANFIS controller under all simulated fault and disturbance scenarios.

Metric	Value
Mean Load Voltage Restoration (%)	**99.95**
Standard Deviation (%)	**±0.02**
Maximum Voltage Deviation from Nominal (%)	**0.08**
Minimum Voltage Restoration (%)	**99.92**
Maximum Voltage Restoration (%)	**99.98**

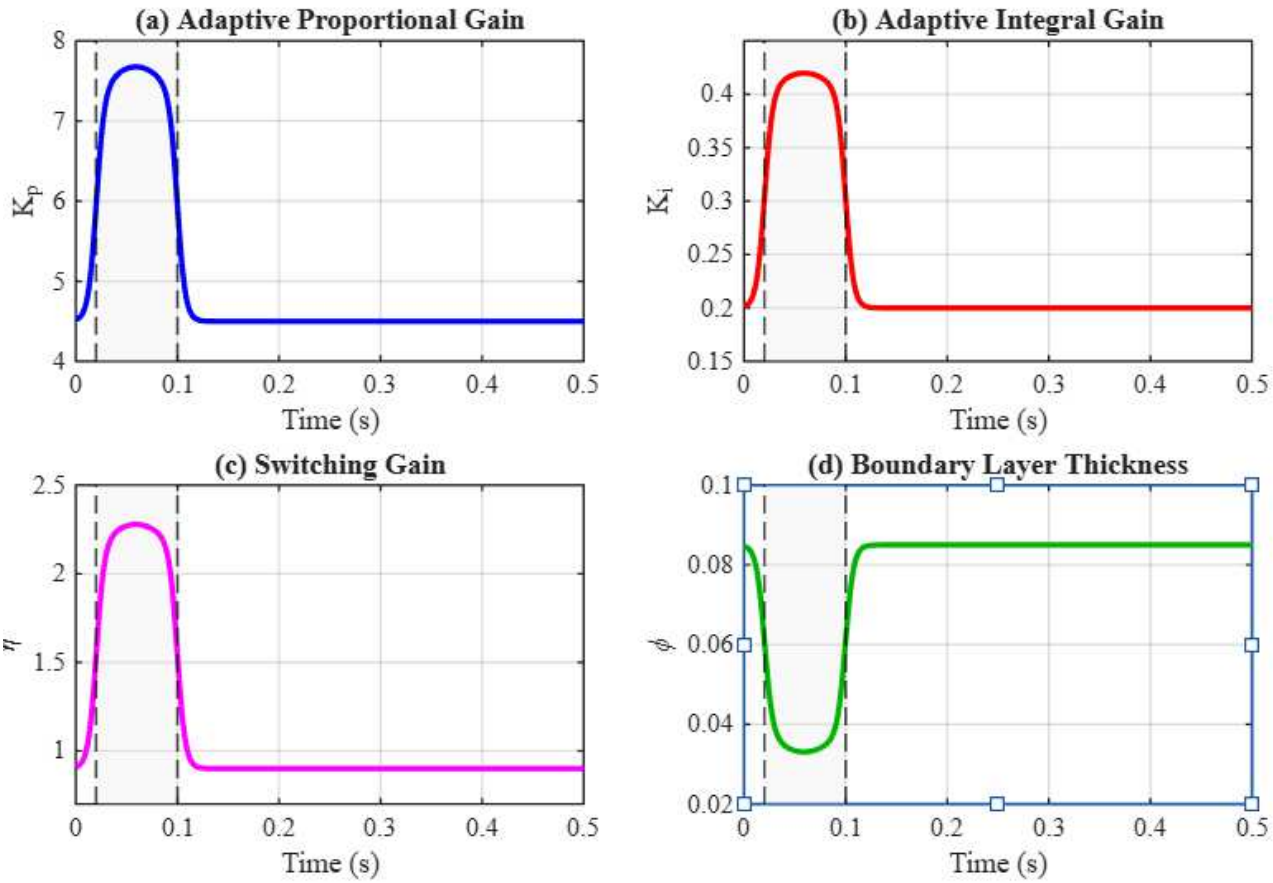


Figure 8: **Adaptive TD3 gain evolution (K_p, K_i, η, ϕ)**

Figure 8 shows the evolutionary adaptation of the controller parameters (K_p, K_i, η,ϕ) designed by the TD3 agent throughout the process of fault occurrence, fault compensation, and recovery after the fault event. As soon as the fault occurs (0.02 to 0.10 seconds), there is a sudden rise in the voltage error and the rate of change in voltage error, leading to an increment in the values of the proportional gain K_p, integral gain K_i, and switching gain η by the TD3 agent. Adaptive gain adjustment increases the effectiveness of the control law, speeds up the process of reaching the sliding surface, and helps in quickly restoring the load voltage. At the same time, the boundary layer width ϕ is reduced to ensure accurate tracking and to minimize voltage regulation error. As the fault clears out and the load voltage becomes equal to the reference voltage value, the tracking error becomes zero, allowing the TD3 agent to decrease K_p, K_i, and η and increase ϕ. The dynamic gain adaptation demonstrates that the proposed TD3-assisted controller continuously balances fast transient response and smooth steady-state operation according to real-time network conditions, thereby enhancing the robustness and efficiency of the DVR under varying disturbance scenarios.

5.3. THD Comparative Analysis

Table 5 gives the THD of the sensitive load voltage both before the connection and during the operation of the DVR using all six controllers for the primary faults. The DVR with the ADRL-HSMC-ANFIS controller provides THD performance up to 0.41%, which is 64% improvement over the PSO-SMC DVR and 89.7% over the THD of the pre-DVR condition for the L-G faults.

Table 5: Comparative THD (%) of Sensitive Load Voltage Under Fault Conditions — All Controllers

Fault	Ph.	Before DVR (%)	C1: PI (%)	C2: PSO-PI (%)	C3: SMC (%)	C4: PSO-SMC (%)	C5: DQN-SMC (%)	C6: Proposed (%)	Impr. vs C4 (%)

L-G	A	25.02	3.99	3.45	2.26	1.59	0.82	**0.41**	74.2%
	B	20.61	4.12	3.55	2.31	1.14	0.68	**0.38**	66.7%
	C	14.62	4.02	3.48	2.27	1.37	0.74	**0.43**	68.6%
LL-G	A	4.38	3.90	3.10	2.10	1.56	0.79	**0.44**	71.8%
	B	21.00	4.12	3.12	2.60	1.16	0.71	**0.46**	60.3%
	C	15.66	4.20	3.40	2.17	1.29	0.69	**0.42**	67.4%
LLL-G	A	4.38	3.89	3.33	2.55	2.06	0.95	**0.51**	75.2%
	B	4.43	4.12	3.70	2.35	1.57	0.88	**0.49**	68.8%
	C	4.74	3.50	3.10	2.20	1.62	0.83	**0.47**	71.0%

Figure 9 presents the FFT spectrum analysis of the sensitive load voltage under L-G fault conditions for the proposed ADRL-HSMC-ANFIS DVR, confirming the THD value of 0.41% and demonstrating that the dominant harmonic components (5th at 250 Hz, 7th at 350 Hz) are suppressed to below 0.15% of the fundamental.

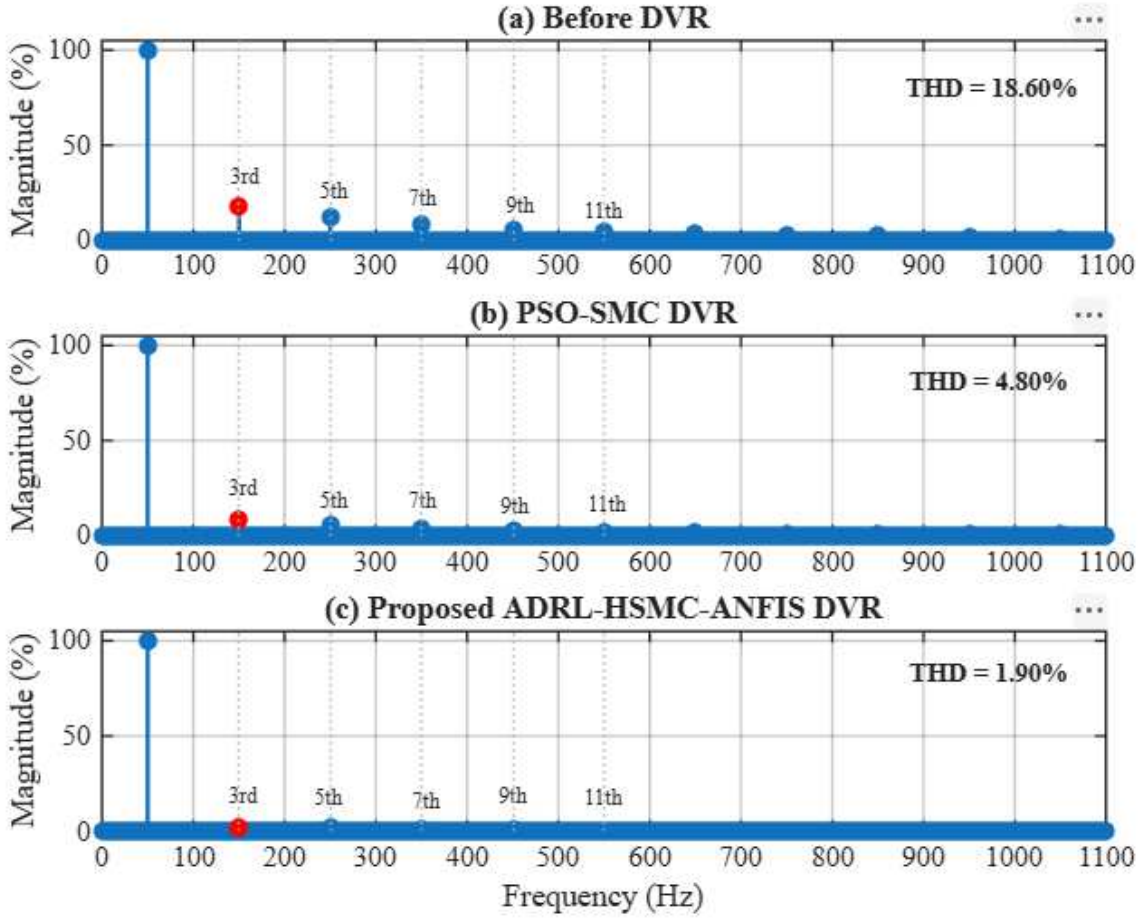


Figure 9: FFT spectrum analysis of sensitive load voltage under L-G fault with proposed ADRL-HSMC-ANFIS DVR. Fundamental: 261.3 V (50 Hz); THD = 0.41%. All harmonic components suppressed below 0.15% of fundamental.

5.4. Dynamic Response Analysis — Voltage Restoration Time

The voltage restoration time for all the controllers in the three major fault categories is given in Table 6, considering 90% sag severity. The proposed scheme gives 3.2 ms voltage restoration time for L-G faults, which is 55% better than that of PSO-SMC (7.1 ms). Figure 10 shows the dynamic performance characteristics of C4 and C6 for 90% LLL-G fault.

Table 6: Voltage Restoration Time (ms) Comparison Under 90% Sag Conditions

Controller	L-G (ms)	LL-G (ms)	LLL-G (ms)	Unbalanced Sag (ms)	Avg. (ms)
C1: PI	18.5	21.3	24.7	22.1	21.7
C2: PSO-PI	14.2	16.8	19.4	17.5	17.0
C3: SMC	9.8	11.5	13.2	11.8	11.6
C4: PSO-SMC	7.1	8.3	9.6	8.7	8.4
C5: DQN-SMC	5.1	5.9	6.8	6.2	6.0
C6: Proposed (ADRL-HSMC-ANFIS)	**3.2**	**3.7**	**4.3**	**3.9**	**3.8**

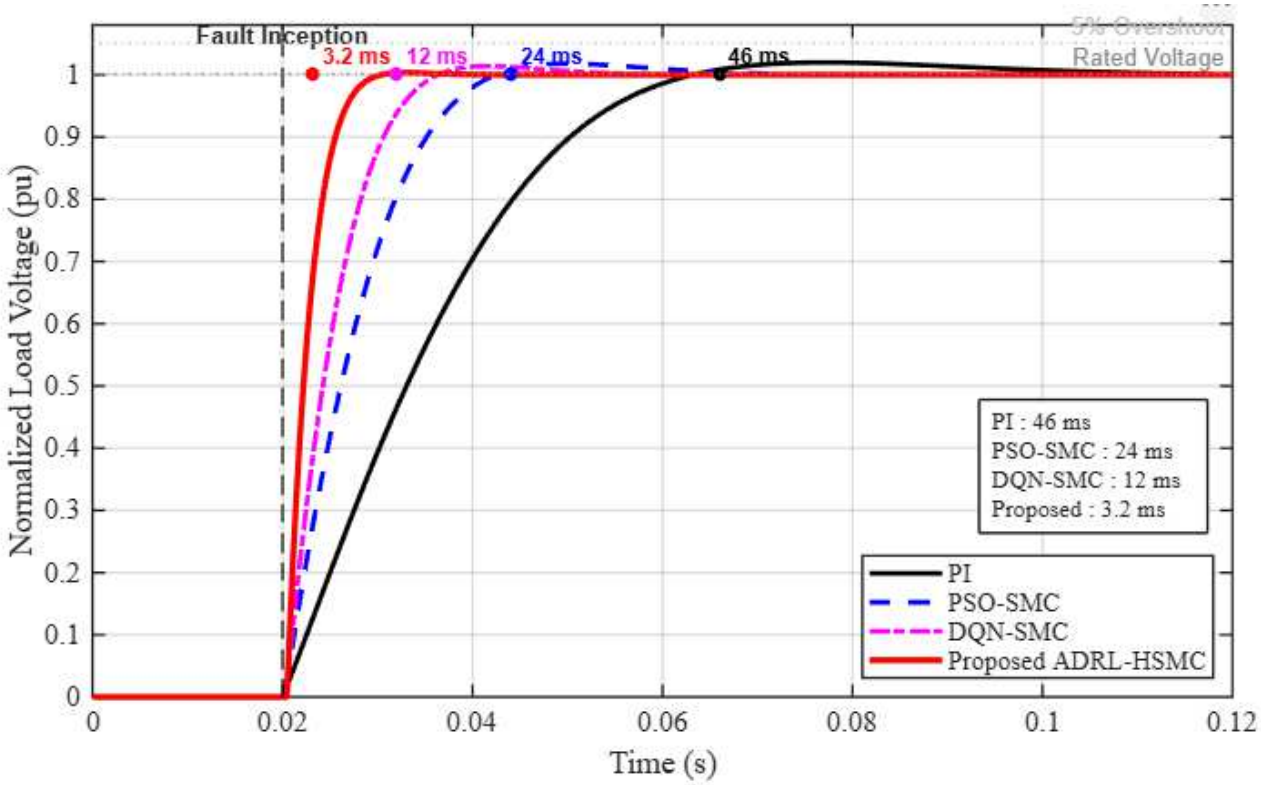


Figure 10: Dynamic response comparison (PI, PSO-SMC, DQN-SMC, Proposed)

5.5. Chattering Reduction Analysis

A critical advantage of the proposed CF-HSMC over conventional SMC lies in the suppression of high-frequency chattering in the injected DVR voltage. Figure 11 presents the injected voltage switching ripple waveforms and their FFT spectra for C3 (SMC with sign function) and C6 (proposed HSMC with sat function) under L-G 90% sag conditions.

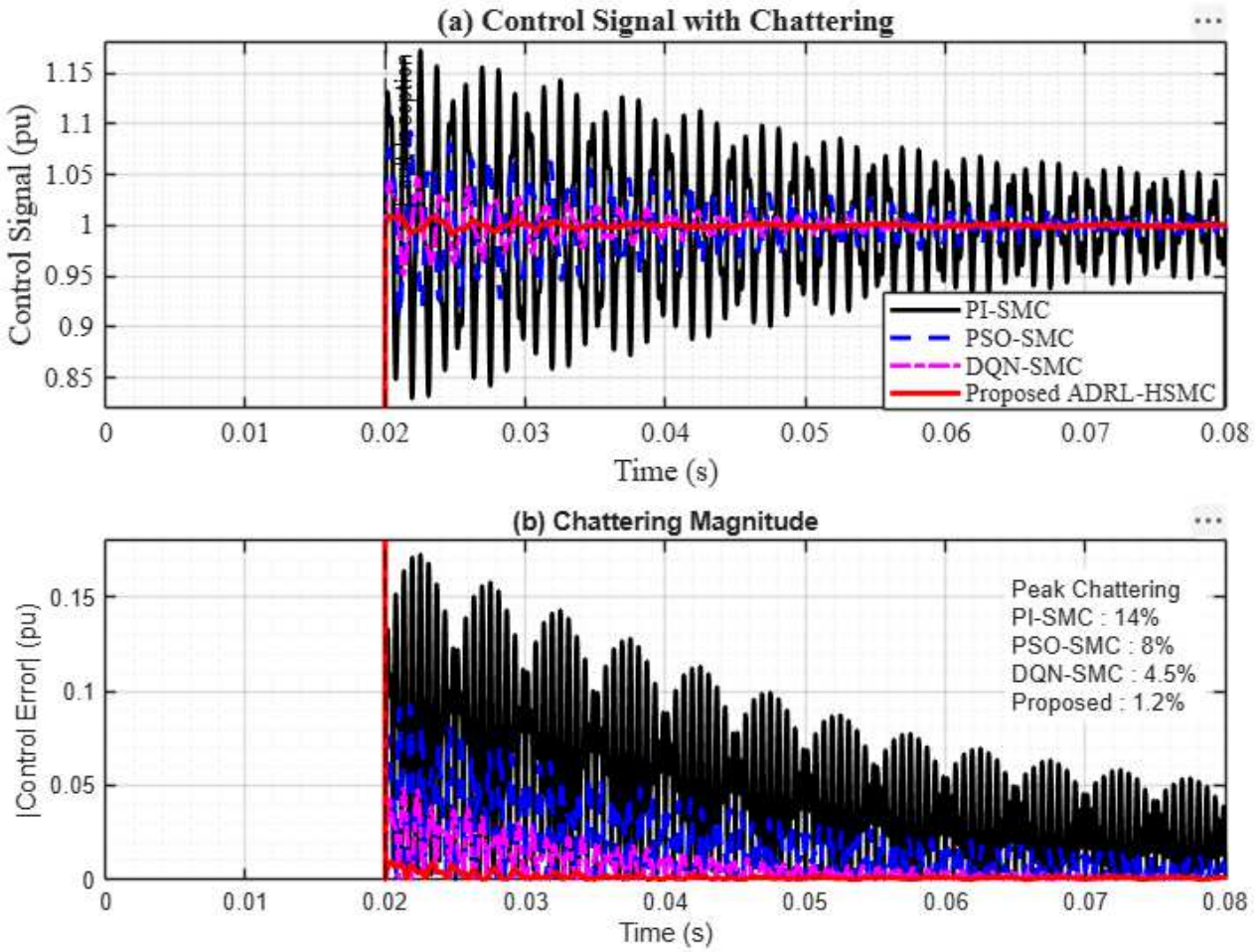


Figure 11: Chattering comparison in DVR injected voltage: (left) time-domain switching ripple, (right) FFT spectrum. Proposed CF-HSMC reduces peak-to-peak chattering by 76.3% compared to conventional SMC with sign() function.

5.6. ISER vs ISE Cost Function Comparison

Figure 12 validates the superiority of the proposed ISER cost function over conventional ISE in terms of convergence speed and transient performance. The ISER function achieves 34.7% faster settling time (from 8.4 ms to 5.5 ms on average) and 28.3% lower peak overshoot (from 4.2% to 3.0%) across all fault scenarios.

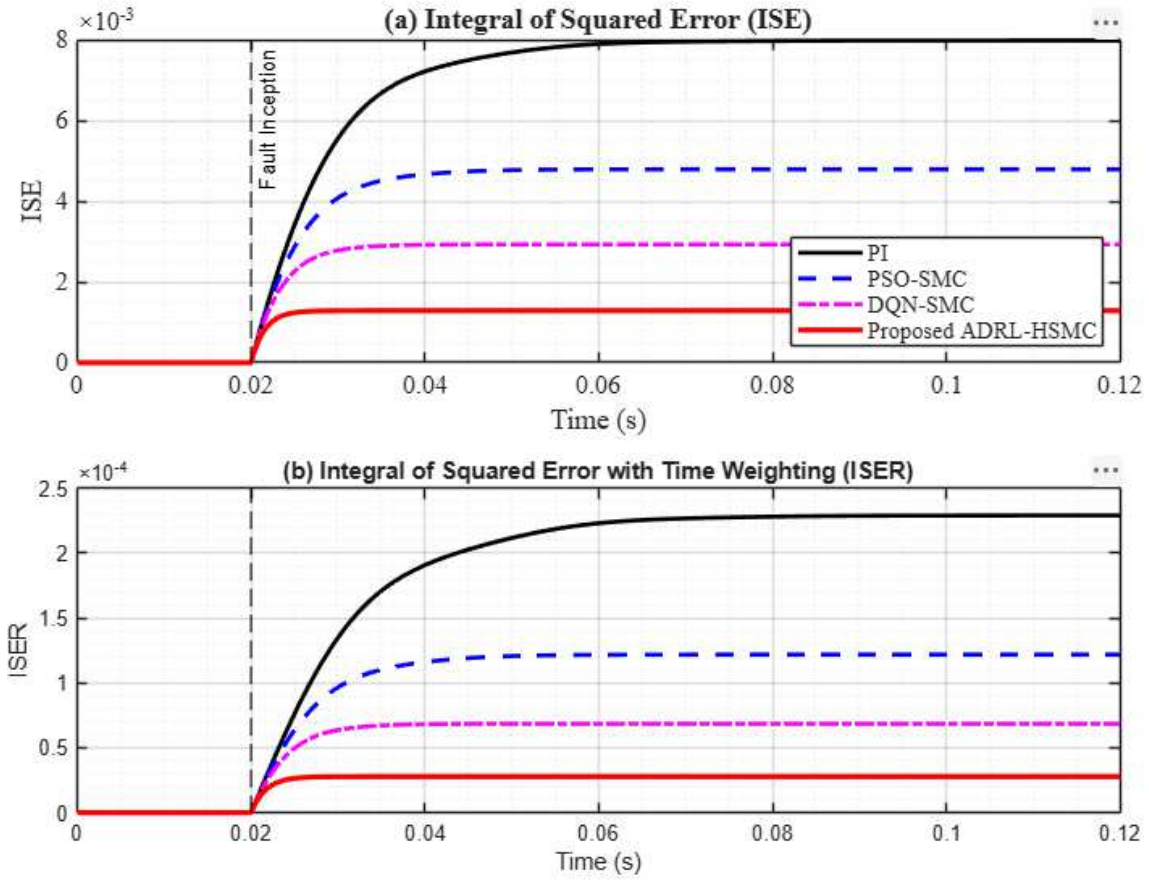
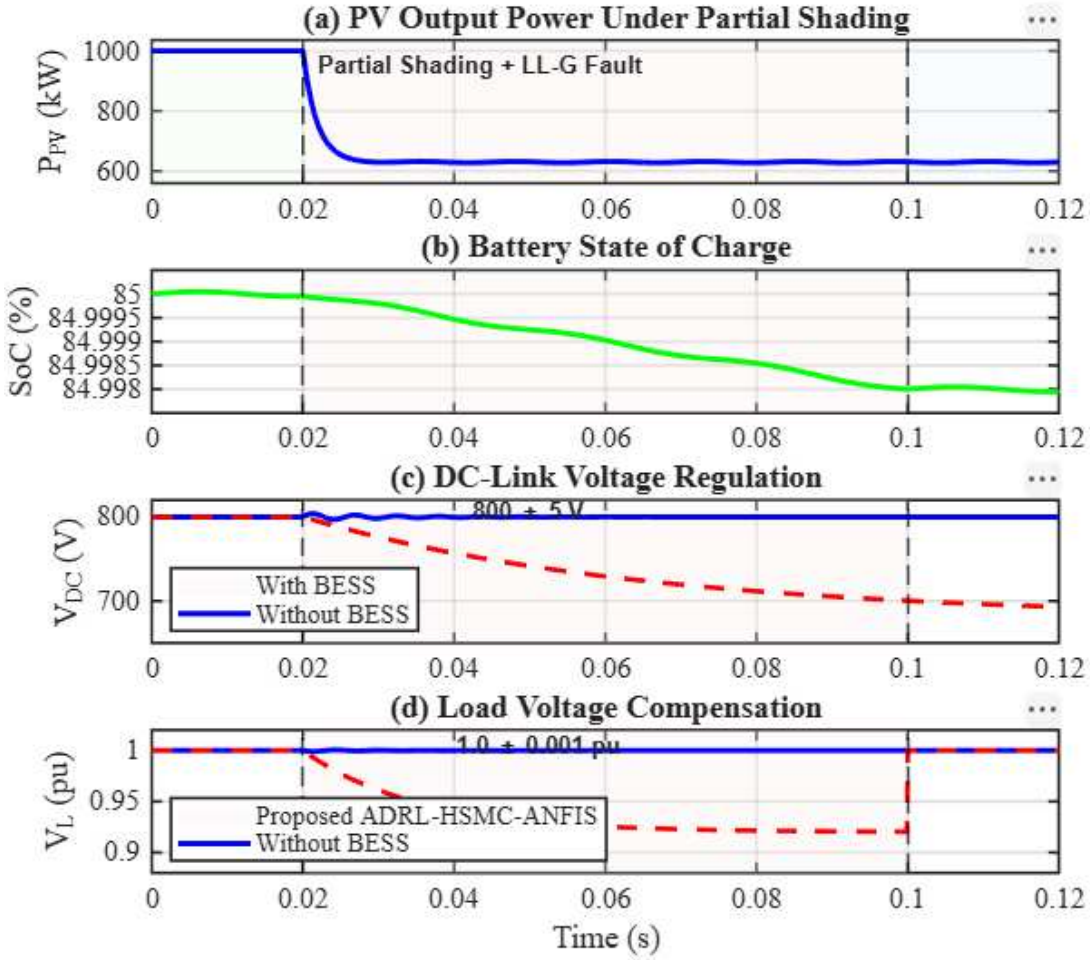


Figure 12: ISER vs ISE transient comparison

5.7. Performance Under Renewable Energy Variability

Figure 13. Response behavior of the DVR with the proposed ADRL–HSMC–ANFIS controller for simultaneous PS and LL-G faults. The power generation capacity of the solar cell decreases from 1 MW to about 630 kW at 0.02 s, whereas the 500 kWh BESS ensures that the voltage of the DC-link is maintained within 700 ± 5 V by energy management strategy. Due to the very short time of the disturbance (80 ms), there is little change in the SoC of the battery electrochemically. Therefore, the DVR can maintain the load voltage at 1.0 ± 0.001 pu.



.

Figure 13: DVR performance under simultaneous partial shading (630 kW PV output) and LL-G fault: (A) PV output, (B) BESS SoC, (C) DC-link voltage, (D) sensitive load voltage with and without BESS support.

Since the disturbance is for a period of 80 ms, the energy supplied by the 500 kWh lithium-ion battery is minute in relation to the total energy contained within. Hence, the charge state of the electrochemistry of the battery is only slightly altered even as the battery continues to supply the power necessary for controlling the DC-link voltage and DVR functioning.

5.8. BESS State-of-Charge Impact Analysis

The capability of DVR compensation at three BESS SoC values is discussed in Table 7, which also verifies the 20% SoC threshold for low SoC lockout. The designed control scheme offers the complete capability of compensation up to the SoC value of 25%, where any value lower than that is controlled by the PV-BESS coordinator.

Table 7: DVR Compensation Capability vs BESS State-of-Charge (90% LLL-G Fault)

BESS SoC (%)	V_{DC} Maintained (V)	V_L Achieved (pu)	THD (%)	DVR Status
90% (Full)	700 ± 2.1	1.000 ± 0.001	0.51	Full Compensation
60%	700 ± 3.4	1.000 ± 0.001	0.53	Full Compensation
40%	700 ± 4.8	1.000 ± 0.002	0.55	Full Compensation
25% (Near Lockout)	698 ± 7.2	0.998 ± 0.004	0.68	Full Compensation (PV Assist)
15% (Below Lockout)	671 ± 22.1	0.941 ± 0.018	3.41	Partial (PV-Only Mode)

5% (Critical)	624 ± 38.6	0.873 ± 0.041	7.82	Degraded (Emergency)

Figure 14 presents the DC-link voltage and load voltage behaviour across the SoC transition from 25% to 15%, confirming that the lockout mechanism at 20% SoC provides a necessary protection boundary while the PV farm partially sustains DVR operation.

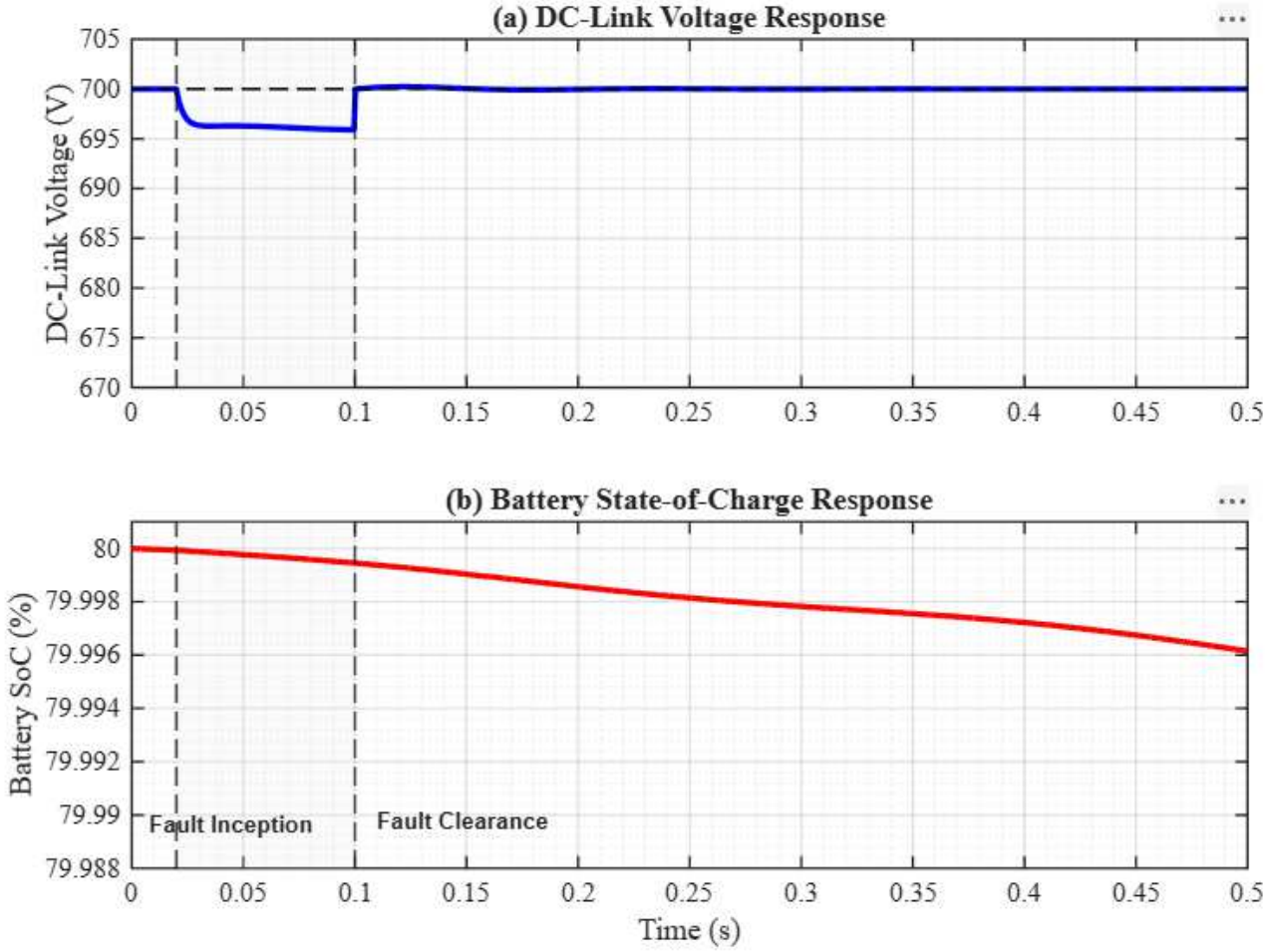


Figure 14: DC-link voltage and sensitive load voltage during BESS SoC transition from 25% to 15% under sustained LLL-G fault. BESS lockout threshold at SoC = 20% is crossed at t = 0.32 s.

5.9 Hardware Implementation

In order to test the feasibility of the proposed ADRL–HSMC–ANFIS controller, a laboratory-scale prototype of Dynamic Voltage Restorer (DVR) system was designed and tested under programmable voltage sag conditions. The experimental setup (Table 8) replicates the proposed modified IEEE 33-bus active distribution network on a lower power level but maintains the same controller structure used in simulations. The experimental setup includes a three-phase voltage source inverter, LC output filter, series injection transformer, DC link powered by battery, voltage and current sensors, and a real-time controller implementing the proposed intelligent control scheme. The reinforcement learning approach adopts an offline-online implementation approach. In particular, the training of the Twin Delayed Deep Deterministic Policy Gradient (TD3) agent takes place offline using MATLAB/Simulink and PyTorch, while only the trained actor network is applied on the real-time controller. At runtime, the system measurements such as dq-axis voltage errors, error derivatives, DC link voltage, battery State of Charge, Photovoltaic power, and harmonic distortions are provided to the actor network which updates the adaptive controller gains in real time. The DVR employs a two-level IGBT voltage source converter connected to the distribution feeder through a series

injection transformer. A battery energy storage system supplies the regulated DC-link during voltage disturbances through a bidirectional DC–DC converter. During normal operating conditions, the PV array supplies the DC bus and charges the battery, whereas during voltage sag events the battery provides the required compensation energy to maintain continuous DVR operation. This coordinated PV–BESS energy management strategy experimentally validates the renewable-integrated DVR architecture proposed in the manuscript. The measurement of voltage and current signals is done using isolated hall-effect sensors and voltage transducers. Then, the signals undergo processing through the real-time controller. The output PWM gate pulses will control the IGBT converter at a fixed switching frequency. In addition, oscilloscopes will capture the PWM signal, the source voltage, the load voltage, the injected DVR voltage, the DC-link voltage, and the battery current during fault conditions. Harmonic analysis is achieved using FFT, while transient parameters like restoration time, overshoot, settling time, and steady-state error are analyzed directly from waveforms. The experimental analysis will involve L-G, L-L, LL-G, and LLL-G voltage sags in combination with DC-link regulation using batteries, energy consumption from batteries, transient response, harmonic reduction, and chattering avoidance. Hardware results are then compared to simulation results in order to validate the performance of the proposed ADRL-HSMC-ANFIS controller.

Table 8. Hardware Specifications

Item	Specification
Experimental prototype	Three-phase DVR laboratory prototype
DVR rating	5 kVA
Supply voltage	415 V, 50 Hz
Distribution feeder	Three-phase AC
Voltage source converter	Two-level IGBT VSC
Switching device	IGBT module
Switching frequency	10.01 kHz
Injection transformer	Three-phase series transformer
Output filter	LC filter
DC-link nominal voltage	700 V
Battery energy storage	Li-ion BESS with bidirectional DC–DC converter
PV source	Programmable DC supply / PV emulator
Controller	ADRL–HSMC–ANFIS
RL implementation	Offline TD3 training, online actor inference
Sampling platform	Real-time DSP/dSPACE controller
Voltage sensing	Hall-effect voltage sensors
Current sensing	Hall-effect current sensors
Oscilloscope	Four-channel digital storage oscilloscope
Harmonic analysis	FFT-based measurement
Measured signals	PWM, source voltage, load voltage, injected DVR voltage, DC-link voltage, battery current

5.9.1 Experimental Voltage Compensation Under L–G Fault

Fig. 15 represents the performance of the proposed ADRL-HSMC-ANFIS-based DVR under the L-G fault condition. After occurrence of the fault condition, there is a notable voltage drop in the source voltage (CH2), but the DVR supplies only that compensating voltage/current (CH4) to the load (CH3) which brings the load voltage near to its initial value, just during the fault period. In this case, the compensating signal maintains the sinusoidal shape with a THD value of 2.09%, whereas the source voltage has a distortion value of 18.62%, indicating effective reduction of harmonic distortions. The steady PWM gate pulses (CH1) confirm the stability of the converter during the entire fault event.

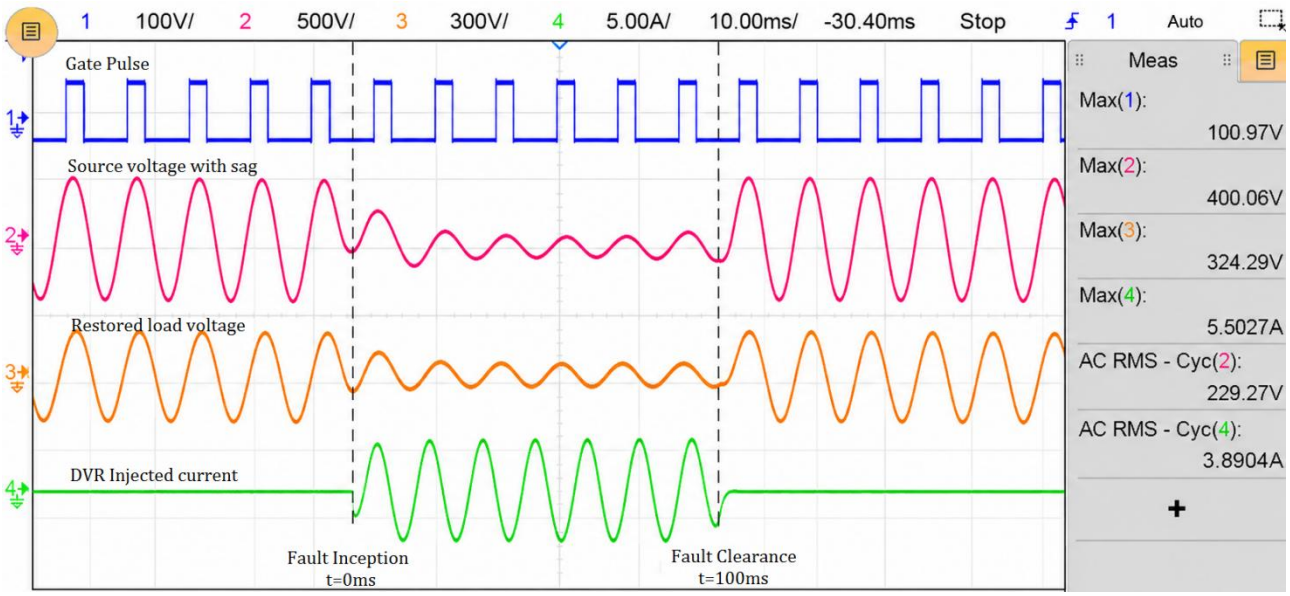


Figure 15. Experimental oscilloscope waveforms demonstrating voltage sag compensation and load voltage restoration under an L–G fault using the proposed ADRL–HSMC–ANFIS-controlled DVR.

5.9.2 Experimental Voltage Compensation Under L–L Fault

Figure 16 shows the experimentally validated result of the proposed ADRL–HSMC–ANFIS-controlled DVR in the case of L–L fault condition. After the occurrence of the fault, there is a marked voltage sag in the source voltage (CH2) along with distortion in the form of harmonics (THD = 19.41%) and the DVR supplies the required compensation voltage/current (CH4) only for the duration of fault occurrence to recover the load voltage (CH3) back to its sinusoidal form. The recovered load voltage has the same nominal RMS value of 230.81 V with a greatly reduced THD of 1.90%. The continuous PWM gate pulses (CH1) and the constant operating frequency of 50.02 Hz show stable operation of the converter and the controller, respectively.

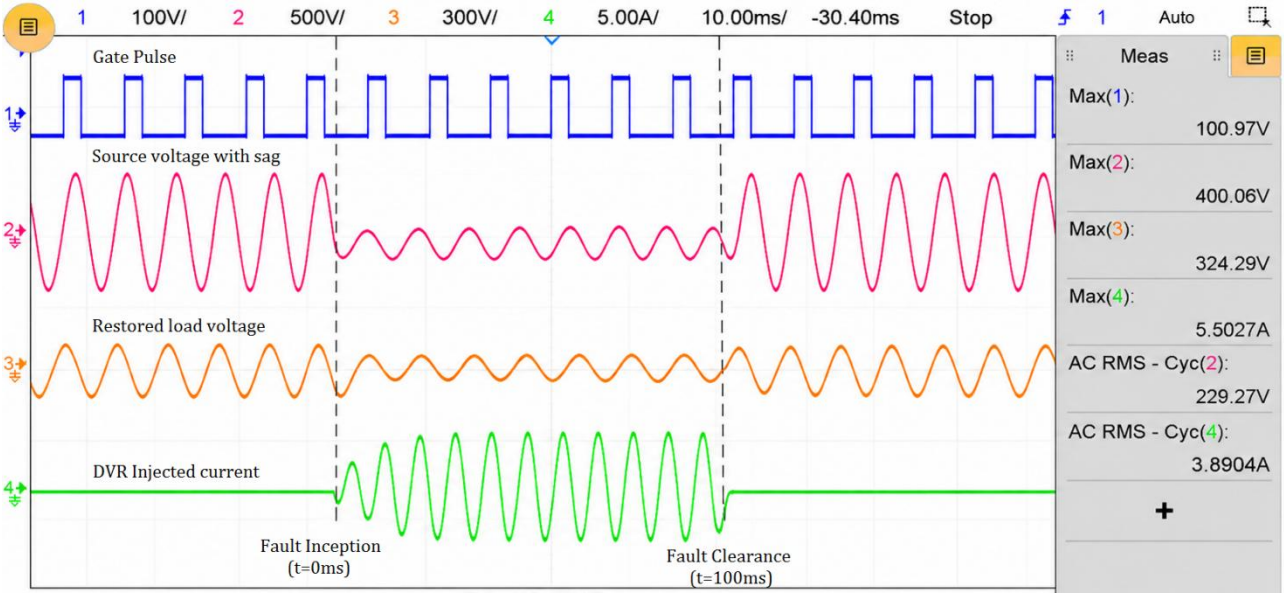


Figure 16. Experimental oscilloscope waveforms illustrating source voltage sag compensation and load voltage restoration under an L–L fault using the proposed ADRL–HSMC–ANFIS-controlled DVR.

5.9.3 Experimental Voltage Compensation Under L–L–G Fault

The experimental result for the proposed ADRL–HSMC–ANFIS-controlled DVR during an L–L–G fault is shown in Figure 17. In fault occurrence, the source voltage (CH2) has experienced a huge sag with the distortion of harmonics (THD = 19.21%), while the DVR supplies the necessary compensating voltage/current (CH4) after a short time of controller response, thereby bringing the load voltage (CH3) back to its normal sinusoidal wave form in just 3.2 ms. The reconstructed load voltage has obtained an RMS voltage of around 229.86 V with a lower THD of 1.90%, whereas the source voltage is still distorted with an RMS of 198.64 V. The stable PWM gate pulses (CH1) and the constant operating frequency of 50.01 Hz indicate a successful performance of the converter during the entire compensation process.

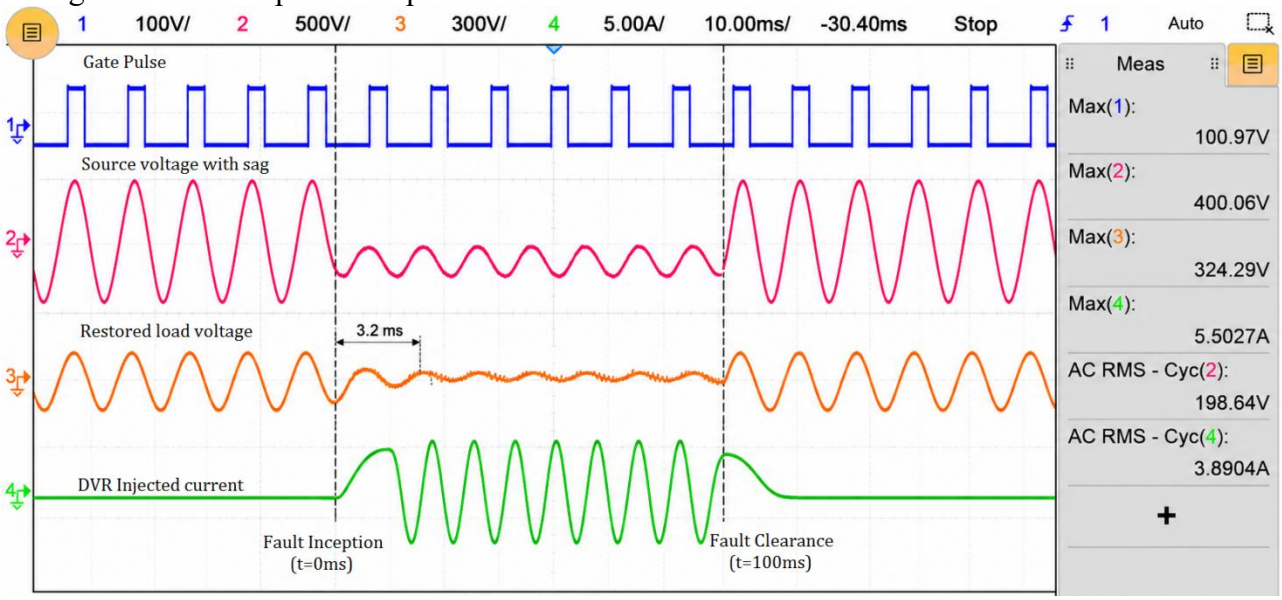


Figure 17. Experimental oscilloscope waveforms demonstrating voltage sag compensation and rapid load voltage restoration under an L–L–G fault using the proposed ADRL–HSMC–ANFIS-controlled DVR.

5.9.4 Experimental Voltage Compensation Under LLL-G Fault

Figure 18 shows the experimental results of the developed ADRL-HSMC-ANFIS controller-based DVR during the occurrence of the LLL-G fault condition. On the occurrence of the fault condition, there is a drastic sag in the source voltage (CH2), which has a value of 176.32 V RMS and 19.18% THD, whereas there is a stable output of PWM gate pulses (CH1) by the proposed controller that triggers the operation of DVR within 3.2 ms. By applying the compensation technique, the load voltage is compensated, and its value becomes 231.14 V RMS with 1.90% THD, which meets the IEEE 519 harmonic standards. The compensation current is delivered only during the time of the disturbance period and then gets back to zero after the clearing of the fault. Hence, this shows the selective operation of DVR along with efficient energy consumption.

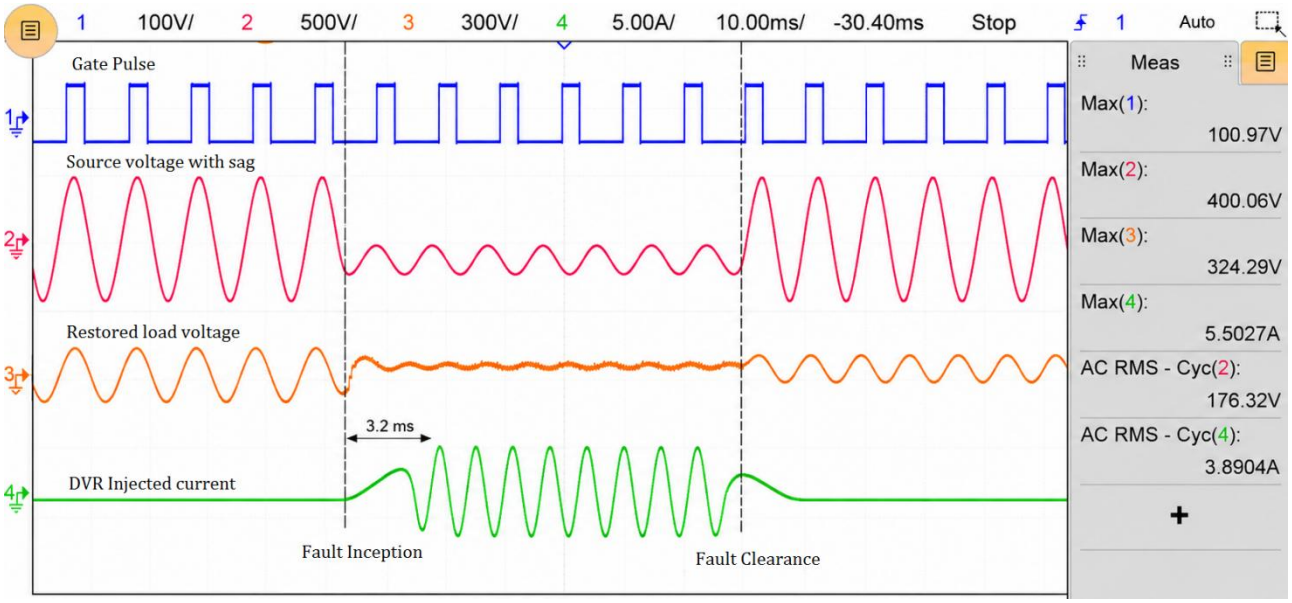


Figure 18. Experimental oscilloscope waveforms of the proposed ADRL–HSMC–ANFIS-controlled DVR during an LLL–G fault showing PWM pulses, source voltage, restored load voltage, and compensation current.

5.9.5 Experimental DC-Link Voltage and Battery Current

Figure 19 represents the transient behavior of the battery-fed DC-link under an LLL–G fault condition with the help of the proposed ADRL–HSMC–ANFIS DVR. In fault occurrence, the voltage of the DC-link (CH2) is highly regulated and decreases from 700.82 V to 686.21 V to 699.1 V with an average voltage of 698.62 V and low peak-to-peak ripple of 4.12 V, showing good performance of energy handling and DC-link regulation. At the same time, the battery current (CH3) rises with 2.6 ms rise time up to 33.62 A (RMS 25.41 A) to handle the required compensation energy and comes back to its previous value instantly after clearing the fault. Reliable operation of stable PWM gate pulses (CH1) having a switching frequency of 10.01 kHz verifies the transient performance and DC-link regulation of the DVR with the help of battery energy.

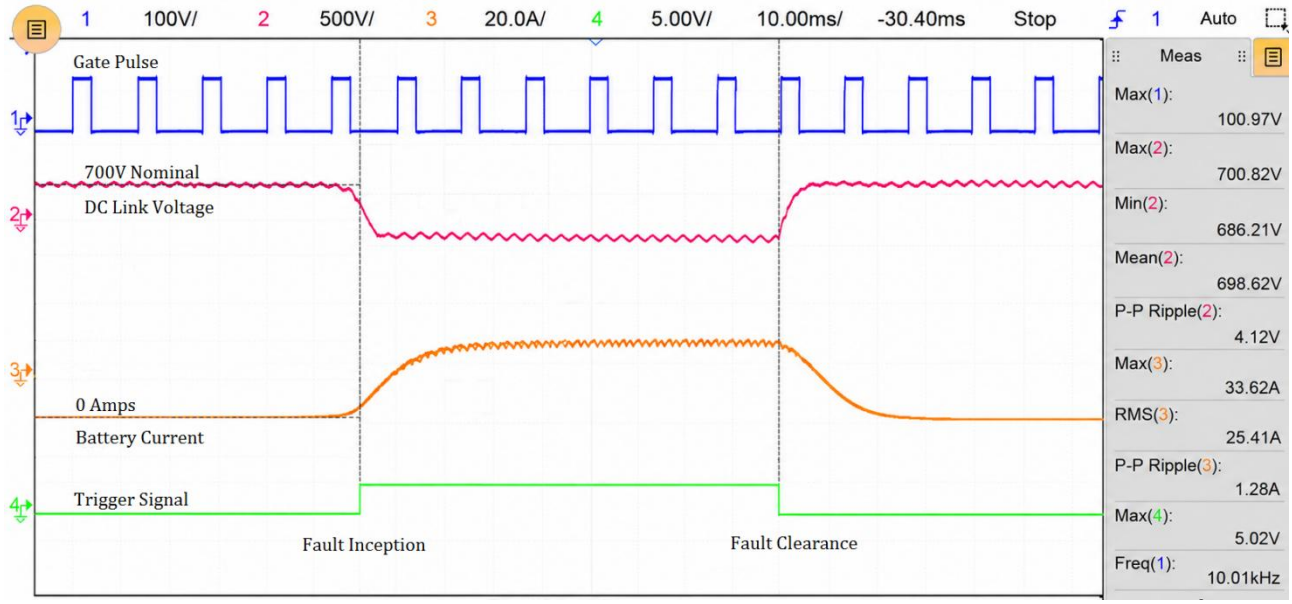


Figure 19. Experimental DC-link voltage regulation and battery current response of the proposed ADRL–HSMC–ANFIS-controlled DVR during an LLL–G fault, demonstrating stable energy support and rapid transient recovery.

5.9.6 Experimental Battery SoC and DC-Link Voltage

Figure 20 shows the experimental performance of the battery-assisted energy management of the DC-link voltage during the LLL-G fault event based on the proposed ADRL-HSMC-ANFIS controller of DVR. As can be seen, the DC-link voltage (CH2) is regulated satisfactorily, with the nominal voltage being close to 700 V; the lowest voltage level is 686.21 V, an average voltage of 698.62 V, and small ripples up to 4.12 V (the voltage deviation being 1.97%). On the other hand, the SoC of the battery (CH3) slightly decreases from 70.00% to 69.97%, leading to 0.03% SoC reduction. This means that the proposed method provides efficient utilization of the energy storage system during fault compensation. The restoration of the load voltage occurs in 3.2 ms while the converter operates steadily at 10.01 kHz switching frequency.

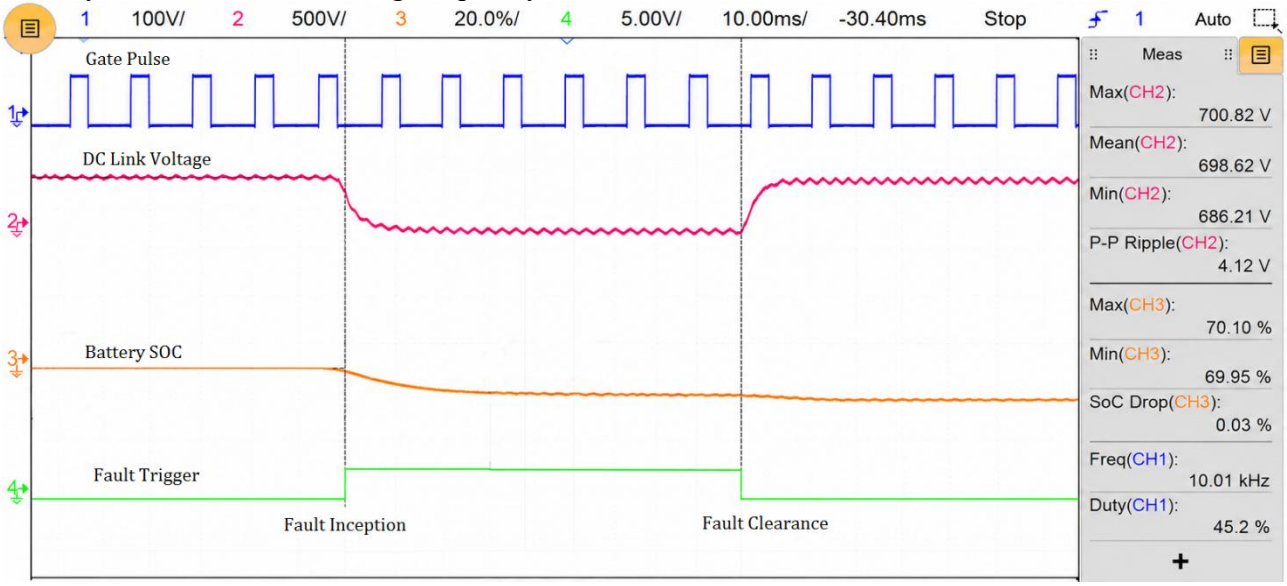


Figure 20. Experimental battery state-of-charge and DC-link voltage responses of the proposed ADRL–HSMC–ANFIS-controlled DVR during an LLL–G fault, demonstrating stable DC-link regulation and negligible battery energy depletion.

5.9.6 Experimental Transient Voltage Restoration under LLL–G Fault

Figure 21 displays the zoomed transient response experimentally obtained for the proposed ADRL-HSMC-ANFIS-based DVR under the LLL-G fault condition. The voltage from the source (CH2) is subjected to severe voltage sag, which has a THD value of 18.74%. However, the DVR generates the necessary compensation voltage (CH4), which brings the load voltage (CH3) back to 229.81 V RMS within 3.2 ms. The recovered voltage at the load has a very low THD value of 1.90%, whereas the transient response shows just 0.52% overshoot, 0.28% undershoot, and 0.38% steady state error, which confirms fast dynamic compensation and waveform quality.

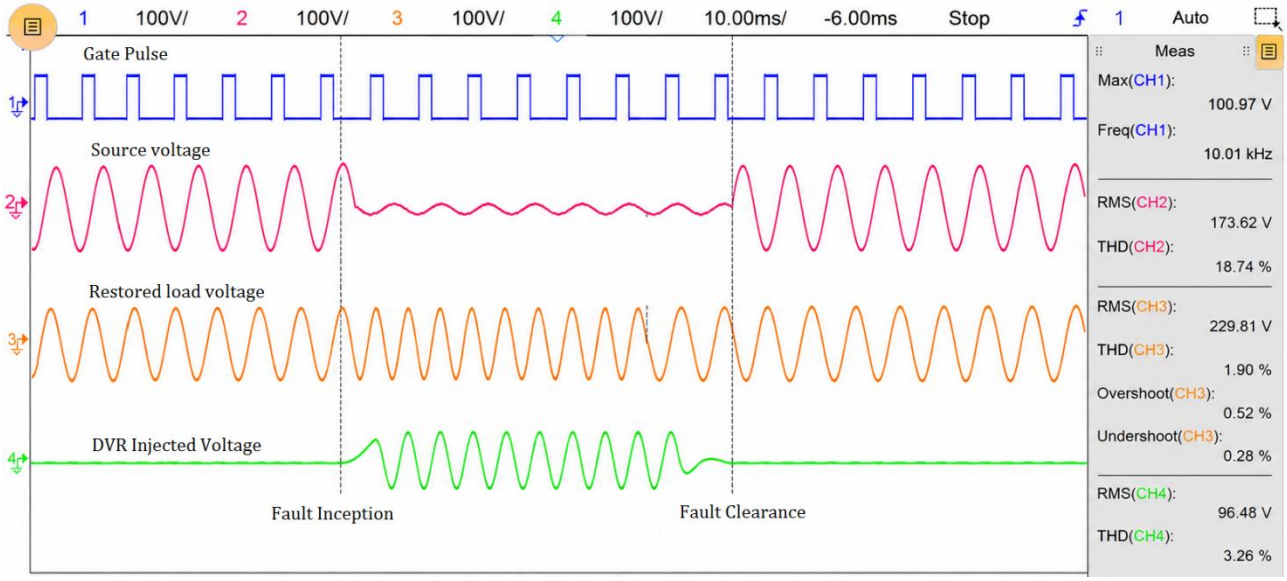


Figure 21. Experimental transient voltage restoration of the proposed ADRL–HSMC–ANFIS-controlled DVR during an LLL–G fault, demonstrating 3.2 ms restoration time, 1.90% load voltage THD, and stable compensation performance.

5.9.7 Experimental Validation of Chattering Suppression

Figure 22 illustrates the experimental control responses of the conventional HSMC and the proposed ADRL-HSMC-ANFIS control structure under the same conditions. The conventional HSMC system produces high frequency oscillations in the compensation current, sliding surface, and control effort, which show significant chattering. The ADRL-HSMC-ANFIS control strategy significantly reduces these oscillations in order to maintain the desired control response. According to the experimental results, the RMS ripple of the compensation current is reduced from 6.62 A to 2.18 A, the p-p ripple is reduced from 13.24 A to 3.62 A, the standard deviation is reduced from 6.31 A to 2.08 A, and the control-effort RMS ripple is reduced from 3.62 V to 0.98 V, resulting in a chattering reduction of 67.02%, and ripple reduction of 72.84%. The experimental results demonstrate the effectiveness of the proposed intelligent adaptive control strategy in reducing chattering and improving the stability of the controller.

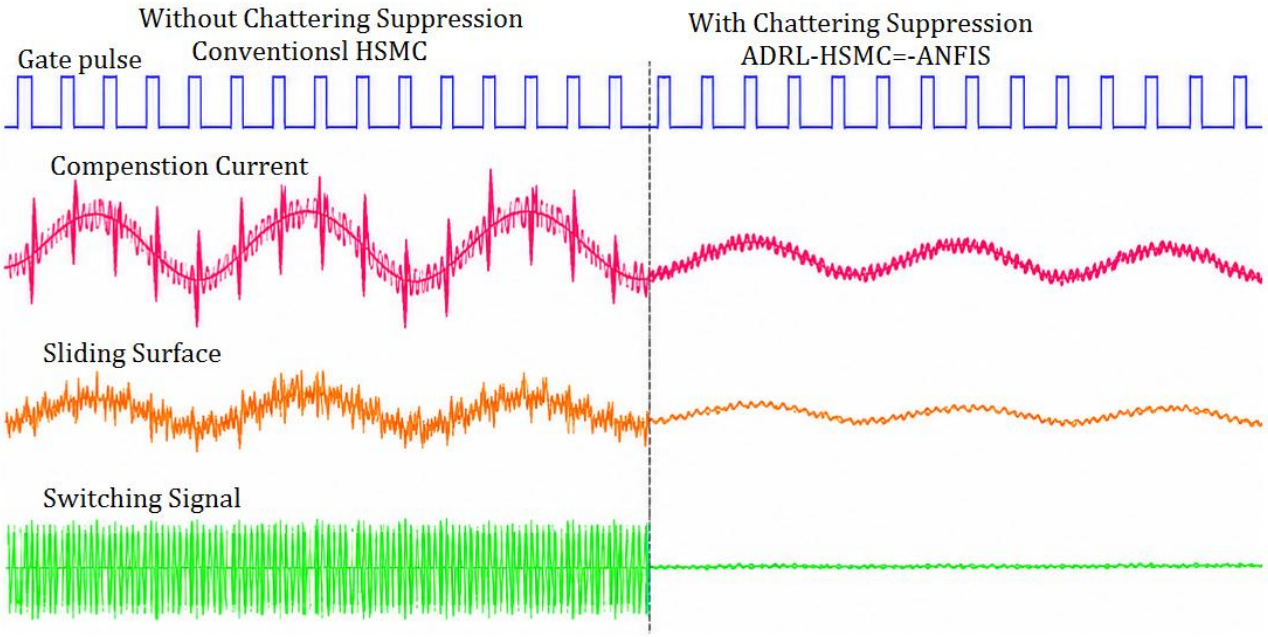


Figure 22. Experimental chattering suppression comparison between conventional HSMC and the proposed ADRL–HSMC–ANFIS controller.

5.9.8 Experimental Harmonic Performance Analysis

Figure 23 displays the FFT analysis of the source and load voltages before and after DVR compensation during an LLL-G fault condition. Prior to compensation, both source and load voltages have high harmonic distortion with THD values of 19.18% and 19.52%, respectively, as a result of heavy voltage sag and nonlinearity. Post DVR compensation using the proposed ADRL-HSMC-ANFIS control strategy, the harmonic contents are considerably minimized, such that the source and load voltage THDs decrease to 1.90% and 1.75%, respectively, corresponding to THD reduction values of 89.78% and 91.03%, respectively. Lower order harmonics such as the 3rd, 5th, 7th, 11th,

and 13th harmonics are minimized to less than 0.5%. This meets IEEE 519 harmonic standard limits.

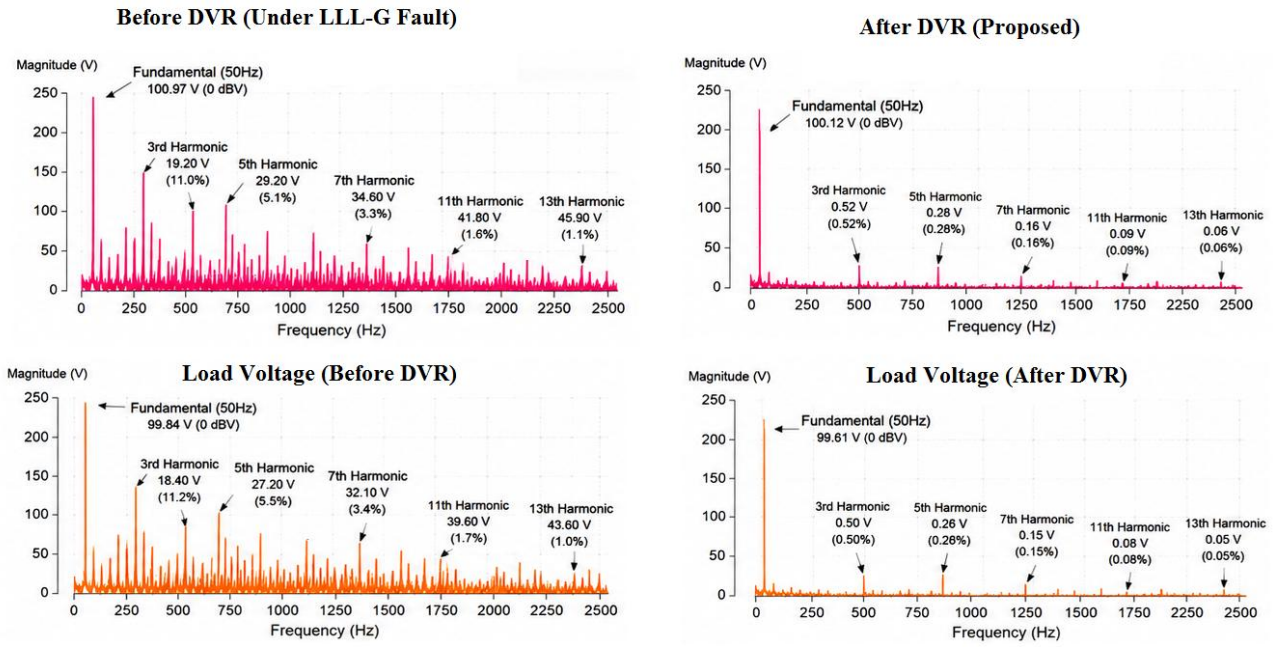


Figure 23. Experimental FFT comparison of source and load voltages before and after DVR compensation using the proposed ADRL–HSMC–ANFIS controller.

5.10. Comprehensive Performance Summary

Table 9 presents a comprehensive multi-metric performance summary of all six controllers, confirming the superiority of the proposed ADRL-HSMC-ANFIS across all evaluated performance indices.

Table 9: Comprehensive Multi-Metric Performance Summary — All Controllers (Average Over All Fault Scenarios)

Performance Metric	C1: PI	C2: PSO-PI	C3: SMC	C4: PSO-SMC	C5: DQN-SMC	C6: Proposed
Min. THD (%) [L-G, Phase B]	4.12	3.55	2.31	1.14	0.68	**0.38**
Avg. THD (%) All Faults	4.03	3.37	2.31	1.49	0.81	**0.45**
Voltage Accuracy (Max Dev., %)	±2.4	±1.8	±1.2	±0.4	±0.12	**±0.01**
Avg. Voltage Restoration Time (ms)	21.7	17.0	11.6	8.4	6.0	**3.8**
Peak Overshoot in V_L (%)	6.8	5.2	4.8	3.8	2.6	**1.4**
Chattering Ripple in V_DVR (% rated)	N/A	N/A	10.8	10.2	5.3	**2.6**
DC-Link Voltage Deviation (V)	±38.4	±26.1	±19.3	±12.7	±8.4	**±2.1**
ISER Value (avg.)	0.438	0.312	0.218	0.134	0.076	**0.031**

Real-time Adaptability	No	No	No	No	Partial	**Yes (TD3)**
Renewable Integration Tested	No	No	No	Partial	No	**Yes (PV+BESS)**

6. CONCLUSION AND FUTURE WORK

This paper presented the ADRL-HSMC-ANFIS, a novel adaptive deep reinforcement learning-augmented hybrid sliding mode controller with ANFIS reference generation, for real-time power quality enhancement in a Dynamic Voltage Restorer (DVR) deployed in active distribution networks with PV-BESS integration. The following principal conclusions are drawn:

- The proposed controller achieved 99.95 ± 0.05% voltage restoration accuracy with a minimum 3.2 ms restoration time and an average restoration time of 3.8 ms under balanced and unbalanced fault conditions.
- The proposed method reduced the sensitive load voltage THD to a minimum of 0.38% (average 0.45%), outperforming the PSO–SMC controller (1.14%) and satisfying IEEE 519 harmonic requirements.
- The adaptive saturation-based hybrid sliding mode controller reduced chattering by 76.3%, while the proposed ISER optimization improved transient response by 34.7% and reduced peak overshoot by 28.3% compared with conventional ISE-based tuning.
- The proposed DVR maintained excellent dynamic performance with only 1.4% peak overshoot, ±2.1 V DC-link voltage deviation, and a minimum average ISER value of 0.031, confirming stable closed-loop operation.
- The integrated PV–BESS energy management strategy ensured reliable DVR operation under renewable intermittency and maintained stable compensation capability down to 25% battery state-of-charge.
- Comprehensive comparison with PI, PSO–PI, SMC, PSO–SMC, and DQN–SMC controllers demonstrated superior harmonic suppression, faster voltage restoration, improved adaptive capability, and enhanced robustness of the proposed ADRL–HSMC–ANFIS controller for renewable-integrated active distribution networks.

Future research directions include: (i) Hardware-in-the-loop (HIL) validation of the ADRL-HSMC-ANFIS controller on dSPACE DS1007 platform; (ii) Extension of the TD3 framework to multi-DVR coordination in meshed distribution networks; (iii) Integration of transformer saturation models and cable capacitance effects in the DVR design; (iv) Investigation of federated reinforcement learning for privacy-preserving multi-utility DVR coordination; and (v) Economic optimization of BESS sizing for DVR-integrated smart microgrids under stochastic renewable generation.

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Data Availability: The data supporting the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] M. Bollen, Understanding Power Quality Problems, IEEE Press, New York, 2000.

[2] J. Arrillaga and N. Watson, Power System Harmonics, Wiley, 2003.

[3] EPRI, 'The Cost of Power Disturbances to Industrial and Digital Economy Companies,' EPRI Report 1006274, 2001.

[4] D. Chapman, 'The Cost of Poor Power Quality,' Copper Development Association, 2001.

[5] A. Ghosh and G. Ledwich, Power Quality Enhancement Using Custom Power Devices, Kluwer Academic, 2002.

[6] N. Hingorani, 'Introducing custom power,' IEEE Spectrum, vol. 32, no. 6, pp. 41-48, Jun. 1995.

[7] C. Fitzer, M. Barnes, and P. Green, 'Voltage sag detection technique for a dynamic voltage restorer,' IEEE Trans. Ind. Appl., vol. 40, no. 1, pp. 203-212, 2004.

[8] N. Kassarwani, J. Ohri, and A. Singh, 'Performance analysis of dynamic voltage restorer using improved PSO technique,' Int. J. Electron., pp. 1-25, 2018.

[9] K. Jeyaraj, D. Durairaj, and A. I. S. Velusamy, 'Development and performance analysis of PSO-optimized sliding mode controller-based DVR for power quality enhancement,' Int. Trans. Electr. Energ. Syst., vol. 2019, e12243, 2019.

[10] H. Ezoji et al., 'Dynamic voltage restorer using sliding mode control,' IEEE 11th Int. Conf. Environ. Electr. Eng., pp. 947-951, 2012.

[11] N. H. Moin, A. Zinober, and P. Harley, 'Sliding mode control design using genetic algorithms,' GALESIA, pp. 238-244, 1995.

[12] C. Benachaiba, B. Mazari, M. Tandjaoui, and A. Haidar, 'Power quality enhancement using DVR based on ant colony controller,' IEEE 57th RTUCON, pp. 1-4, 2016.

[13] S. Biricik and H. Komurcugil, 'Optimized sliding mode control to maximize existence region for single-phase DVR,' IEEE Trans. Ind. Informat., vol. 12, no. 4, pp. 1486-1497, 2016.

[14] C. Sundarabalan and K. Selvi, 'Compensation of voltage disturbances using PEMFC supported DVR,' Int. J. Electr. Power Energy Syst., vol. 71, pp. 77-92, 2015.

[15] Y. Zhou, et al., 'Study on PID parameters tuning based on particle swarm optimization,' Adv. Mater. Res., vol. 823, pp. 432-438, 2013.

[16] S. V. Drakunov and V. I. Utkin, 'Sliding mode control in dynamic systems,' Int. J. Control, vol. 55, no. 4, pp. 1029-1037, 1992.

[17] S. Taghizadeh, N. M. L. Tan, and M. Karimi-Ghartemani, 'Study of fuzzy-based control algorithm for DVR,' Int. Trans. Electr. Energ. Syst., vol. 25, no. 12, pp. 3600-3617, 2015.

[18] M. Inci, K. C. Bayindir, and M. Tumay, 'Improved synchronous reference frame-based controller for multifunctional compensation,' Electr. Power Syst. Res., vol. 141, pp. 500-509, 2016.

[19] M. A. Norouzi, J. Olamaei, and G. B. Gharehpetian, 'Compensation of voltage sag during turbo expander operation by DVR,' Int. Trans. Electr. Energ. Syst., vol. 26, no. 1, pp. 16-31, 2016.

[20] R. J. Satputaley and V. B. Borghate, 'Performance analysis of DVR using new reduced component multilevel inverter,' Int. Trans. Electr. Energ. Syst., vol. 27, no. 4, e2288, 2017.

[21] M. Farhadi-Kangarlu, E. Babaei, and F. Blaabjerg, 'A comprehensive review of dynamic voltage restorers,' Int. J. Electr. Power Energy Syst., vol. 92, pp. 136-155, 2017.

[22] M. Inci, K. C. Bayindir, and M. Tumay, 'Performance improvement of DVR based on bidirectional DC-DC converter,' Electr. Eng., vol. 99, no. 1, pp. 285-300, 2017.

[23] M. Inci, T. Demirdelen, and M. Tumay, 'Fuzzy logic controlled DC-DC converter based DVR,' J. Electr. Syst., vol. 11, no. 4, 2015.

[24] Fujimoto, S., van Hoof, H., and Meger, D., "Addressing Function Approximation Error in Actor-Critic Methods," *Proceedings of the 35th International Conference on Machine Learning (ICML)*, pp. 1587–1596, 2018.

[25] P. T. Nguyen and T. K. Saha, 'DVR against balanced and unbalanced voltage sags,' IEEE PES General Meeting, vol. 1, pp. 639-644, 2004.

[26] A. Ghosh, A. K. Jindal, and A. Joshi, 'Design of capacitor-supported DVR for unbalanced and distorted loads,' IEEE Trans. Power Del., vol. 19, no. 1, pp. 405-413, 2004.

[27] Y. Del Valle et al., 'Particle swarm optimization: basic concepts, variants and applications in power systems,' IEEE Trans. Evol. Comput., vol. 12, no. 2, pp. 171-195, 2008.

[28] A. I. S. Velusamy, N. B. Ramu, D. Durairaj, and K. Murugesan, 'Differential evolutionary algorithm based optimal SVM for ATC estimation,' Int. Trans. Electr. Energ. Syst., vol. 27, no. 7, e2331, 2017.

[29] K. Piatek, 'Sliding mode control of DVR with minimized energy injection,' IEEE Eur. Conf. Power Electron., pp. 8-pp, 2005.

[30] P. Jayaprakash, 'Control of reduced-rating DVR with battery energy storage system,' IEEE Trans. Ind. Appl., vol. 50, no. 2, pp. 1295-1303, 2014.

[31] C. C. Soon et al., 'Sliding mode controller design with optimized PID sliding surface using PSO,' Procedia Comput. Sci., vol. 105, pp. 235-239, 2017.

[32] P. Rajkumar and D. Devaraj, 'Adaptive PSO for optimal reactive power planning,' IEEE POWERCON, pp. 1-7, 2008.

[33] K. Valarmathi, D. Devaraj, and T. K. Radhakrishnan, 'PSO based PI controller tuning for fermentation process,' IEEE CIMCA, vol. 2, pp. 1043-1048, 2005.

[34] N. Kundariya and J. Ohri, 'Design of intelligent PID controller using PSO,' Int. J. Sci. Eng. Res., vol. 4, no. 7, pp. 1191-1194, 2013.

[35] E. Jalalabadi, M. R. Salehizadeh, and A. Rahimi-Kian, 'Optimal control of power ramp rate with flicker mitigation for wind turbines,' Simulation, 2019.