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# A Digitally Trimmable Bandgap Voltage Reference Using a Transmission-Gate Switched Resistor Ladder in 180-nm CMOS

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# A Digitally Trimmable Bandgap Voltage Reference Using a Transmission-Gate Switched Resistor Ladder in 180-nm CMOS

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***Abstract*—A bandgap reference is only as good as the silicon it is built on, and silicon never repeats itself exactly. This paper follows one bandgap circuit from its variation-limited state before trim to a digitally corrected one after trim. The core is a folded-cascode-regulated, mirror-based reference in a 180-nm CMOS process with VDD = 1.8 V; the correction is a 3-bit transmission-gate-switched resistor ladder placed in the output branch. Before trim, a 200-point Monte Carlo run swept over all eight codes (−50 °C to 125 °C) evaluates successfully at 199 points (99.5 %) and has a mean reference of 1.235 V with σ = 80.15 mV (6.5 %), a spread of 0.888–1.418 V and a temperature coefficient (TC) of 17.7–2570 ppm/°C, the upper extreme being a single outlier. After trim, a 20-point Monte Carlo run gives a mean of 1.193 V with σ = 51.69 mV (4.3 %), a 35 % reduction in σ, a spread of 1.112–1.297 V and a TC of 44.9–192.3 ppm/°C. At the nominal corner the reference falls from 1.206 V to 1.183 V over the range, about 105 ppm/°C. The trim step, switch-resistance effects and test-time code selection are analysed.**

***Index Terms*—Bandgap reference, digital trimming, Monte Carlo analysis, temperature coefficient, process variation, CMOS analog design.**

## I. Introduction

Every precision analog system quietly depends on a number it never questions: the reference voltage. The step size of an ADC, the output of a voltage regulator and the gain of a sensor front end all inherit the accuracy of one node that is expected to stay still while temperature, supply and fabrication spread move around it. The bandgap reference earned its place as that still point by cancelling two opposing temperature trends against each other, and it has remained the default choice for roughly fifty years [1]–[3].

The cancellation, however, is a balance struck on paper. On silicon, the balance depends on the absolute value of resistors, the saturation current of the junctions, the offset of the amplifier and the mismatch of the current mirrors, and none of these is identical from die to die [4]. Our own simulations tell this story plainly. Before trim, the reference of the circuit studied here spreads from 0.888 V to 1.418 V across Monte Carlo samples, a peak-to-peak range of 530 mV, and its temperature coefficient wanders from 17.7 ppm/°C to an outlier of 2570 ppm/°C. A design that is perfectly centred at the nominal corner can still be a poor reference on a particular die.

The remedy is to let each die be corrected after it is built. Trimming does this by adjusting one well-chosen parameter until the output sits where it should. Laser and fuse trimming need special processing or equipment; digital trimming, in which a few bits stored in a register or one-time-programmable memory select a resistor value, fits in standard CMOS and can be done at final test. This paper tells the story of one such design: a bandgap with a 3-bit transmission-gate (TG) switched resistor ladder, studied from its behaviour before trim, through its trim mechanism, to its Monte Carlo performance.

The contributions are: (i) a compact trim architecture with seven ladder segments and eight trim settings; (ii) an analytical description of the trim step and of the switch effects that limit it; and (iii) a Monte Carlo evaluation that quantifies the circuit before and after trimming. Section II reviews related work, Section III describes the circuit, Section IV the simulation and trimming method, Section V the results, and Sections VI and VII discuss them and conclude.

## II. Literature Review

### *A. From Zener Diodes to the Bandgap Principle*

The story of the bandgap reference begins with the shortcomings of its predecessor. Buried-Zener references offered good stability but needed supplies above 6–7 V and produced considerable noise, which made them a poor match for low-voltage integrated systems. In the early 1970s, Widlar and Kuijk independently showed that the base–emitter voltage of a bipolar transistor, which falls with temperature, could be added to a voltage proportional to absolute temperature (PTAT) to give an output near the extrapolated silicon bandgap of about 1.2 V [1], [5]. Brokaw then turned the idea into a practical three-terminal cell whose feedback arrangement is still widely copied [2]. Tsividis later gave an accurate account of the temperature dependence of the base–emitter voltage, showing that the residual curvature, not the first-order slope, limits what a simple bandgap can achieve [6].

### *B. Bandgap References in CMOS*

Bringing the principle into standard CMOS required a substitute for the bipolar transistor. The parasitic substrate diode or vertical bipolar device available in the process took that role, and Song and Gray demonstrated a CMOS

reference with curvature compensation on this basis [7]. Gunawan et al. showed a curvature-corrected low-voltage design [8], and Malcovati et al. reported a curvature-compensated reference operating from 1 V [9]. A different line of work addressed the supply limit. Banba et al. summed currents rather than voltages so that the output could be scaled below 1.2 V [3], and Leung and Mok achieved low supply operation without low-threshold devices [10]. The circuit in this paper sits in the more conventional family: its supply of 1.8 V comfortably accommodates a 1.2 V output, and the emphasis is on accuracy rather than on supply reduction.

### *C. Variation, Mismatch and Offset*

Why do fabricated references drift from simulation? Pelgrom showed that the mismatch of MOS devices scales inversely with the square root of their area [4], so the current mirrors and the amplifier input pair are bounded by area. A second, less obvious contributor is the amplifier offset. If the amplifier forces its inputs equal only to within an offset $V_{os}$, the PTAT voltage across the resistor $R_{11}$ is in error by $V_{os}$, and that error is multiplied by the resistor ratio on its way to the output, as derived in Section III. Pease documented this and other practical pitfalls of bandgap design in a well-known account [11].

### *D. Trimming Techniques*

Methods to correct these variations have grown more convenient over time. Laser trimming of thin-film resistors gives high resolution but needs special process steps and cannot be repeated after packaging. Zener-zap and fuse links are cheaper, but are one-way and need extra area or high-current pads. Digital trimming stores a code in non-volatile memory or fuses and uses it to switch resistors in or out, which is compatible with standard CMOS and allows post-package adjustment. Trimming at a single temperature fixes the absolute level; trimming at two temperatures can also reduce the TC, at a higher test cost. The price of digital trimming is the switch itself, whose on-resistance, leakage and temperature dependence enter the signal path.

### *E. Positioning of This Work*

The literature thus presents the problem and the tools, but a thin explanatory layer between them: how many bits are needed, how large the switch can be before it disturbs the step, and what a Monte Carlo run shows about the trimmed distribution. This paper fills that layer for a mirror-based, amplifier-regulated reference, with the analysis tied to simulated data (Table V summarises the results).

## III. Circuit Architecture

### *A. How the Core Works*

The core, shown in Fig. 1, can be understood as a loop that insists on one condition. A folded-cascode amplifier compares the voltage at the top of diode D0 with the voltage at the top of resistor R11, which sits in series with diode D1. Its output drives the common gate of three matched PMOS mirrors, PM0–PM2 (W = 2 µm, L = 180 nm each). The loop settles only when the two amplifier inputs are equal. D0 is a unit diode (m = 1) and D1 consists of eight parallel unit diodes (m = 8), so the equal-input condition forces R11 to carry the difference of the two junction voltages:

$$\Delta V_{BE} = V_T \ln(N), \quad N = 8 \tag{1}$$

This voltage is PTAT, and it sets the loop current $I = V_T \ln(N)/R_{11}$, with $R_{11}$ = 1 kfi. PM2 mirrors this current into the output branch, where it flows through a resistance $R_{tot}$ (the fixed resistor R6 = 4.445 kfi plus, in the trimmed circuit, the ladder) and then into diode D2. The output is the sum of a CTAT and a PTAT term:

$$V_{REF} = V_{BE,D2} + (R_{tot}/R_{11})\, V_T \ln(N) \tag{2}$$

The designer's task is to choose the ratio $R_{tot}/R_{11}$ so that the two slopes cancel. To first order, $V_{BE}$ falls with temperature as $-(V_{G0} - V_{BE})/T$, where $V_{G0} \approx 1.2$ V is the extrapolated silicon bandgap voltage, while $V_T = kT/q$ rises linearly. Setting the derivative of (2) to zero gives

$$(R_{tot}/R_{11}) \ln(N) = (V_{G0} - V_{BE}) / V_T \tag{3}$$

and, when (3) holds, $V_{REF} \approx V_{G0}$. This explains why the mean simulated reference of 1.193 V after trim (Table III) sits so close to 1.2 V. It also exposes the weakness that motivates trimming: the required ratio depends on $V_{BE}$, which depends on the junction saturation current, a process-dependent quantity. A fixed resistor ratio cannot follow it.

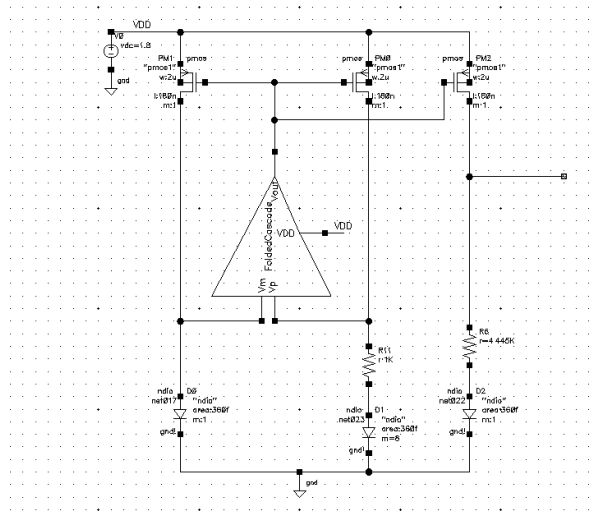



Fig. 1. Bandgap core: folded-cascode amplifier, PMOS mirrors PM0–PM2, PTAT branch (R11, D1 with m = 8) and output branch (R6, D2).

### *B. Amplifier, Offset and Start-Up*

A folded-cascode stage was chosen because it gives high single-stage gain, so the equal-input condition holds closely, and because its dominant pole at the high-impedance output node avoids a separate compensation network. Gain is not the only concern, though. Any input-referred offset $V_{os}$ unbalances the loop and produces an output error

$$\Delta V_{REF} \approx (R_{tot}/R_{11})\, V_{os} \tag{4}$$

so with $R_{tot}/R_{11}$ of about 4.4 an offset of 1 mV becomes about 4.4 mV at the output. A single-temperature trim can cancel this error at that temperature, but not its drift, which is one reason a residual TC remains after trimming. Like every bandgap loop, the circuit also has a second, undesired stable state with zero current. The schematic in Fig. 1 contains no

dedicated start-up cell; the DC temperature sweeps and the before-trim Monte Carlo run reported here settled into the intended operating point at 199 of 200 points, and a start-up circuit is left as future work.

### C. The Trim Ladder

The complete trimmed circuit is given in Fig. 2. Between the PM2 drain and diode D2, a fixed resistor and a series ladder of seven segments have been inserted. Every segment is bypassed by a transmission gate: when the gate is on, its segment is shorted out, and when it is off, the segment adds to the output resistance. A 3-bit code D2 D1 D0 is converted by a decoder into the enable signals, so that eight distinct values $R_{trim}(k)$, $k = 0…7$, are available. Equation (2) becomes

$$V_{REF}(k) = V_{BE,D2} + [(R_{fix} + R_{trim}(k)) / R_{11}]\ V_T \ln(N) \quad (5)$$

If each segment is a unit resistor $R_u$, one code step moves the reference by

$$\Delta V_{step} \approx (R_u/R_{11})\ V_T \ln(N) \quad (6)$$

At 300 K, $V_T \ln(8) \approx 53.7$ mV, so every 100 fi of $R_u$ gives a step of about 5.4 mV. The step depends on the ratio $R_u/R_{11}$ and not on absolute resistance, so it tracks process shifts of the resistors. Because the ladder carries the same current as the PTAT term, a longer series resistance also tilts the TC from negative towards positive, so the trim moves the level and the slope at once.

### D. Switches and Decoder

Each switch is a TG, chosen so that conduction does not depend on a single device type. The ladder nodes sit near 1.2 V while the supply is 1.8 V. At that level an NMOS alone has only a small gate overdrive, since its threshold in a 180-nm process is typically 0.4–0.5 V, whereas a PMOS with its gate at ground has a source–gate voltage of about 1.2 V and conducts well. The complementary pair therefore keeps the on-resistance $R_{on}$ reasonably flat as the node voltage shifts from code to code. Even so, $R_{on}$ adds to the ladder and varies with temperature, so it has to be small against $R_u$; otherwise the steps become non-uniform and may lose monotonicity. The design values are collected in Table I.

TABLE I
DESIGN PARAMETERS AND SIMULATION CONDITIONS

| Parameter | Value |
|---|---|
| Technology / supply | 180-nm CMOS / 1.8 V |
| PM0–PM2 (W/L) | 2 µm / 180 nm |
| D0, D1 (area ratio N) | m = 1, m = 8 (N = 8) |
| R11 / R6 | 1 kfi / 4.445 kfi |
| Trim ladder | 7 segments, TG-bypassed |
| Trim code / decoder | 3 bits (D0–D2), 3-to-8 |
| Amplifier | Folded cascode |
| Temperature range | −50 °C to 125 °C |
| Monte Carlo points | 200 (before trim), 20 (after trim) |

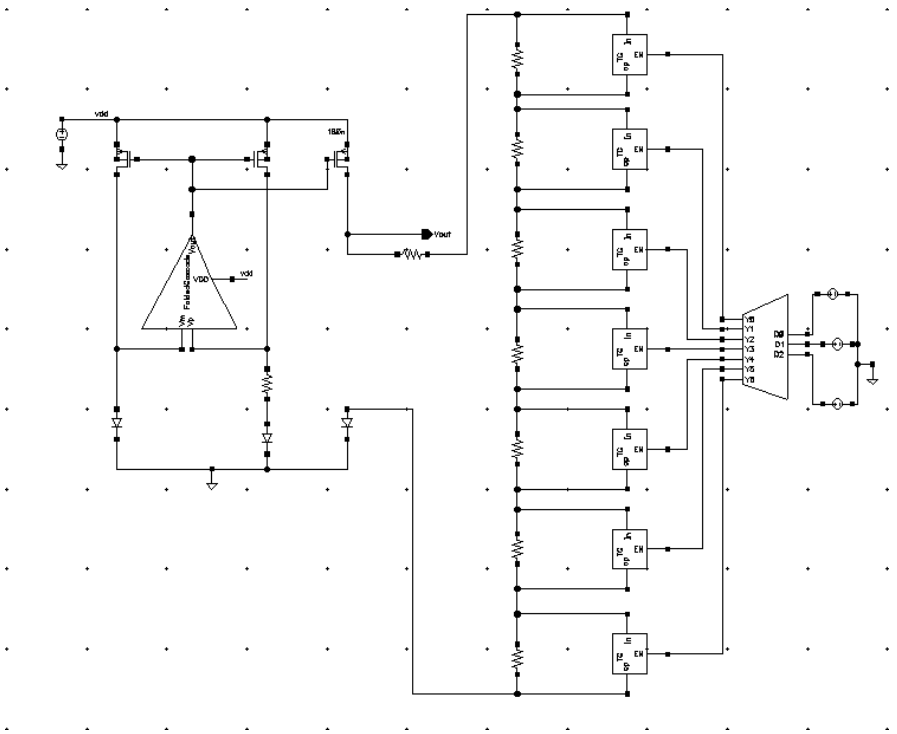



Fig. 2. Complete trimmed bandgap: core (left), resistor ladder with seven TG-bypassed segments (centre) and 3-bit decoder with code inputs D0–D2 (right).

## IV. SIMULATION AND TRIMMING METHOD

### A. Testbench

All simulations were run in Cadence ADE Assembler using a 180-nm CMOS process design kit with its foundry statistical models, which include process variation and device mismatch. The temperature was swept from −50 °C to 125 °C. The code was defined through global variables d0, d1 and d2 together with a combined variable, *code*. A natural plan was to sweep *code* from 0 to 7 inside the Monte Carlo run; the

tool, however, does not allow an active parameter sweep to run together with Monte Carlo sampling and rejects the setup with an error. The workaround was to enter the eight code values as eight corners, with the Monte Carlo sampling enabled over all of them. The result is a dataset in which every random die is evaluated at every code, which is precisely the information a tester needs. This 200-point run, with the code pooled over all eight values, is the before-trim data set; the after-trim data set is a separate 20-point Monte Carlo run.

### *B. Metrics*

The temperature coefficient is evaluated by the box method,

$$TC = [(V_{max} - V_{min}) / (V_{mean} (T_{max} - T_{min}))] \times 10^6 \quad (7)$$

in ppm/°C, where the extremes are taken over the swept temperature range. No specification window was applied to the outputs; a point is counted as passed when the simulation completes and all outputs are evaluated, so the percentage reported below is the share of points that evaluated successfully rather than a compliance rate against an accuracy limit.

### *C. Intended Trim Procedure*

A tester has no wish to explore all eight codes at every temperature; it measures a die at one or two temperatures and picks the best setting. The intended selection rule is to choose, for each sample *s*, the code

$$k^*(s) = \text{argmin}_k \, | \, V_{REF,s}(k; T_0) - V_{target} \, | \quad (8)$$

for a single-temperature level trim, or the code that minimises the sample's TC for a two-temperature trim. This procedure defines how the circuit is meant to be used; the results below report the code-pooled 200-point statistics as the before-trim state and a 20-point run as the after-trim state, and a larger trimmed sample with per-sample selection is listed as future work.

## V. Results

### *A. The Starting Point Before Trim*

The story starts from the 200-point Monte Carlo run in which the code is swept over 0–7; 199 of the 200 points evaluated successfully (99.5 %). Table II shows a mean reference of 1.235 V and σ = 80.15 mV, i.e. 6.5 % of the mean, with a range of 0.888–1.418 V (530 mV peak-to-peak, 42.9 %). The TC averages 102.4 ppm/°C with σ = 304.8 ppm/°C. The best sample, at 17.7 ppm/°C, shows that a good setting exists, but one outlier (TC = 2.57 kppm/°C) accounts for the large σ; an outlier of this size usually means that the loop biased at an off-nominal operating point for that sample and code, and the single point that did not evaluate may be related, although this was not examined further. The 200-point histogram of the reference is shown in Fig. 4(a), the upper histogram; the histogram tool reports a mean of 1.248 V and σ = 82.5 mV, within about 1 % and 3 % of the table values, with a longer tail towards low voltages than towards high ones. The distribution combines the process spread with the differences between codes and with the extra variation of the ladder and switches, and its mean sits well above the 1.2 V bandgap value. In short, process variation, not the topology, dominates the accuracy before trim.

TABLE II
BEFORE-TRIM MONTE CARLO STATISTICS (200 PTS, ALL CODES)

| Output | Min | Max | Mean | Std Dev |
|---|---|---|---|---|
| $V_{REF}$ (V) | 0.8881 | 1.418 | 1.235 | 0.0802 |
| TC (ppm/°C) | 17.67 | 2570 | 102.4 | 304.8 |

199 of 200 points evaluated successfully (99.5 %).

### *B. Behaviour Across Temperature and Code*

Fig. 3 shows the nominal reference over −50 °C to 125 °C with all eight codes on one graph. The reference falls monotonically from about 1.206 V at −50 °C to about 1.183 V at 125 °C, a drop of roughly 22 mV. The slope is small at the cold end (about −0.04 mV/°C) and steepens to about −0.25 mV/°C near 125 °C, which is the downward curvature that remains after first-order cancellation. By the box method of (7) this corresponds to a nominal TC of about 105–108 ppm/°C, in line with the Monte Carlo mean TC of 101.7 ppm/°C after trim and 102.4 ppm/°C before trim. In terms of (3), the nominal curve lies on the CTAT-dominated side of the optimum. The eight codes lie within about 1 mV of one another at the nominal corner, and the lowest curve, which the legend assigns to code 0, sits slightly below the rest.

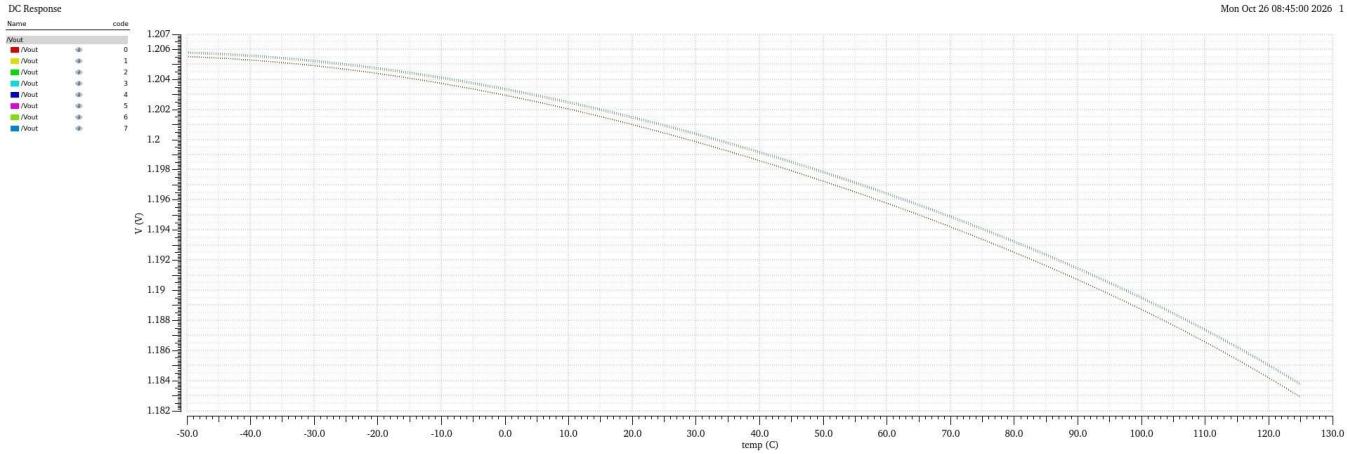



Fig. 3. Reference voltage versus temperature for all eight trim codes (nominal corner).

### C. Monte Carlo After Trim

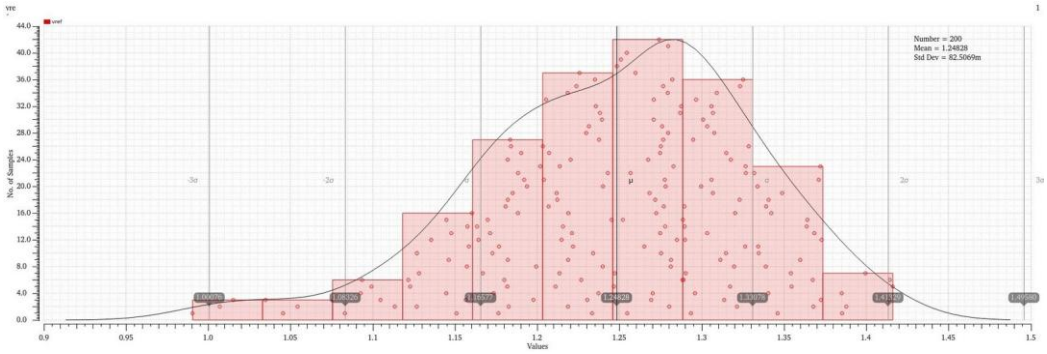
Table III gives the 20-point run after trim. The mean falls by 42 mV to 1.193 V, within 7 mV of 1.2 V, and σ drops from 80.15 to 51.69 mV, a reduction of 35 %, or 4.3 % of the mean. The spread narrows from 0.888–1.418 V to 1.112–1.297 V (185 mV peak-to-peak, 15.5 %, against 530 mV before trim), a reduction of 65 %. The 20-point histogram is shown in Fig. 4(b), the lower histogram; with so few points it is coarse, and the histogram tool reports a mean of 1.1926 V and σ = 52.83 mV, close to the values in Table III. Compared with the before-trim σ of 82.5 mV in Fig. 4(a), the distribution is clearly narrower and better centred.

Two details deserve attention. The TC range tightens from 17.7–2570 to 44.9–192.3 ppm/°C, and σ of the TC falls from 304.8 to 37.8 ppm/°C, so the outlier seen before trim no longer appears. The mean TC of 101.7 ppm/°C, however, is essentially unchanged from 102.4 ppm/°C, and the best sample (44.9 ppm/°C) is not as good as the best before trim (17.7 ppm/°C). Trimming here mainly re-centres the level and tightens the distribution, rather than lowering the average TC; reaching the best TC needs the two-temperature trim of Section IV. The after-trim run also has only 20 points against 200 before trim, so its tails are less well sampled and the comparison should be read as indicative.

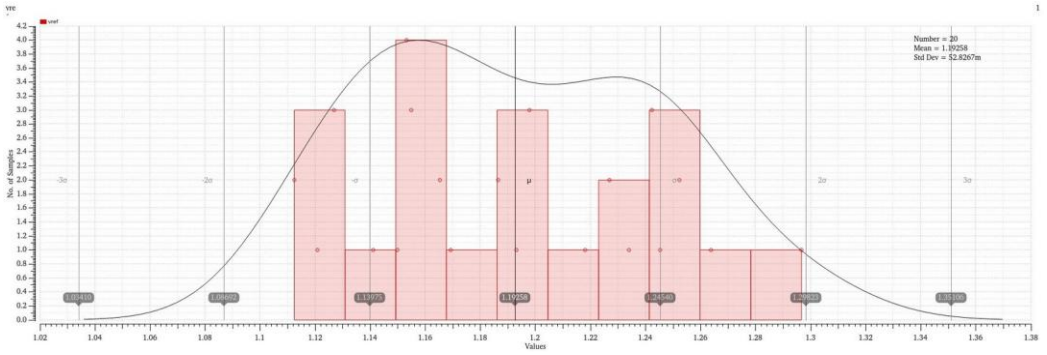
TABLE III
AFTER-TRIM MONTE CARLO STATISTICS (20 PTS)

| Output | Min | Max | Mean | Std Dev |
|---|---|---|---|---|
| $V_{REF}$ (V) | 1.112 | 1.297 | 1.193 | 0.0517 |
| TC (ppm/°C) | 44.93 | 192.3 | 101.7 | 37.8 |

N = 20 Monte Carlo points.




**(a) Before trim (above histogram)**




**(b) After trim (below histogram)**

Fig. 4. Monte Carlo histograms of the reference voltage: (a) before trim (top; N = 200, all codes, mean 1.2483 V, σ = 82.51 mV); (b) after trim (bottom; N = 20, mean 1.1926 V, σ = 52.83 mV).

### D. Comparison Before and After Trim

Table IV sets the two Monte Carlo runs side by side. Trimming lowers the mean reference by 42 mV, reduces σ from 80.15 to 51.69 mV (35 %) and narrows the range at both ends, while the maximum TC falls from 2570 to 192.3 ppm/°C. The mean TC is essentially unchanged, and the best TC is 44.93 ppm/°C after trim against 17.67 ppm/°C before. The runs also differ in size (200 points pooled over all codes before trim, 20 points after), so the table compares distributions rather than identical dies.

TABLE IV
BEFORE-TRIM VERSUS AFTER-TRIM MONTE CARLO

| Metric | Before trim (N = 200) | After trim (N = 20) |
|---|---|---|
| Mean $V_{REF}$ (V) | 1.235 | 1.193 |
| σ of $V_{REF}$ (mV) | 80.15 | 51.69 |
| Min / Max $V_{REF}$ (V) | 0.888 / 1.418 | 1.112 / 1.297 |
| Mean TC (ppm/°C) | 102.4 | 101.7 |
| Min TC (ppm/°C) | 17.67 | 44.93 |
| Max TC (ppm/°C) | 2570 | 192.3 |

### E. Summary of Results

Table V collects the figures obtained in this study. Supply sensitivity, power supply rejection, quiescent current, noise

and area were not evaluated here and belong to the next design iteration.

TABLE V
SUMMARY OF SIMULATED RESULTS

| Parameter | Value |
|---|---|
| Process / supply | 180-nm CMOS / 1.8 V |
| Temperature range | −50 °C to 125 °C |
| Trim resolution | 3 bits (8 codes) |
| $V_{REF}$ before → after trim | 1.235 V ± 80.2 mV → 1.193 V ± 51.7 mV (1σ) |
| TC range before → after trim | 17.7–2570 → 44.9–192.3 ppm/°C |
| Nominal TC (Fig. 3) | ≈105–108 ppm/°C |
| Mean TC before → after trim | 102.4 → 101.7 ppm/°C |
| Points evaluated, before-trim run | 199 / 200 (99.5 %) |

## VI. DISCUSSION

Several lessons come out of the simulations. First, the trim step needs closer study. At the nominal corner the eight codes differ by less than about 1 mV (Fig. 3), whereas the Monte Carlo σ falls from 80.15 mV before trim to 51.69 mV after trim, a change far larger than the nominal code spacing. The two observations are not fully consistent, and the sample sizes differ (200 against 20), so the nominal curves should be read as a lower bound on the step and the Monte Carlo statistics as an indication of the trim range; the unit resistor $R_u$ and the code mapping are the first parameters to re-examine, and a smaller $R_u$ gives finer steps but needs more bits to cover the same range. Second, trimming moved the mean down by 42 mV, from 1.235 to 1.193 V, which brings it close to the 1.2 V target; a code in the middle of the range should sit at the target so that the range is spent symmetrically.

Third, the TG deserves care. Its on-resistance varies with temperature and node voltage, and its leakage grows at high temperature, so a switch that is adequate at 27 °C may disturb the TC at 125 °C. Fourth, trimming addresses systematic spread of resistors and junctions; it cannot remove the temperature drift of the amplifier offset or the curvature of $V_{BE}$, which set the floor of the residual TC. Finally, there is a test-cost trade-off between a single-temperature trim, which centres the level, and a two-temperature trim, which also lowers the TC.

These observations translate into a short set of design guidelines for similar references. (1) Choose the unit resistor so that the full trim range is roughly twice the before-trim one-sigma spread of the reference, which leaves margin for the tails of the distribution without wasting bits. (2) Size the TG so that its on-resistance is below a few percent of $R_u$ at the hottest corner, and verify monotonicity there rather than at room temperature. (3) Place the ladder at the low-voltage end of the output branch where possible, so that the switch terminals sit at a favourable common-mode level. (4) Simulate every code with the Monte Carlo run switched on, as was done here with corners, so that bias-point failures such as the outlier in Table II are found before tape-out.

There are also limits to what this study can claim. The results come from simulation with foundry statistical models, which describe process spread and mismatch but not package stress, long-term drift or the noise of the trim memory itself. The trim code is assumed to be perfectly stored, and the leakage of the unselected switches was not examined separately. Silicon measurements are needed to confirm that the simulated results, including the after-trim σ of 51.7 mV and the 20-point sample behind it, carry over to fabricated parts.

## VII. CONCLUSION

This paper followed a 180-nm CMOS bandgap reference from its state before trim to a digitally trimmed one. Before trim, a 200-point Monte Carlo run over all codes gives a mean reference of 1.235 V with σ = 80.15 mV and a TC of 17.7–2570 ppm/°C, with 199 of 200 points evaluating successfully. After trim, a 20-point run gives a mean of 1.193 V with σ = 51.69 mV (a 35 % reduction) and a TC of 44.9–192.3 ppm/°C, while the mean TC stays near 102 ppm/°C. At the nominal corner the reference falls from 1.206 V to 1.183 V over −50 °C to 125 °C. A 3-bit TG-switched ladder in the output branch changes the PTAT contribution in eight steps. Future work includes a larger trimmed Monte Carlo run with per-sample code selection, a re-examination of the unit step, a start-up circuit, supply-sensitivity and power evaluation, a curvature-compensation term, characterisation of the switch at high temperature, and silicon verification.


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