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Multidimensional Bayesian Optimization of Nanosheet Double-Gate LDMOS for Enhanced Power Figure of Merit

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Abstract

This work investigates and optimizes a nanosheet-inspired Double-Gate Lateral Double-Diffused Metal-Oxide-Semiconductor (DG-LDMOS) architecture using Technology Computer-Aided Design (TCAD) simulations combined with Bayesian Optimization (BO), addressing the limitations of sequential manual tuning. By progressively expanding the optimization space from individual parameters to a six-dimensional design space, the optimized nanosheet DG-LDMOS intended for switched-mode operation achieves an intrinsic ultra-low specific on-state resistance of 0.17 $\mathrm{m\Omega{\cdot}mm^2}$ and a breakdown voltage of 11.32 V, corresponding to a power figure of merit (FOM) of 738 $\mathrm{kW/mm^2}$. The results reveal that FOM enhancement originates from coupled geometrical and doping optimization, which simultaneously shortens the conduction path, redistributes the lateral electric field, and enhances near-interface carrier transport. These findings demonstrate the importance of simultaneous optimization of strongly coupled device parameters and establish the nanosheet DG-LDMOS as a physics-based foundation for subsequent three-dimensional Gate-All-Around (GAA) LDMOS development.

Keywords: Bayesian optimization, Double-gate LDMOS, Figure of merit, Specific on-resistance, TCAD

1 Introduction

LDMOS devices remain central to BCD (Bipolar-CMOS-DMOS) power technologies because they combine low on-resistance, high switching efficiency, and CMOS compatibility. As lateral devices are scaled, however, short-channel effects and leakage become increasingly difficult to control. Multi-gate concepts such as double-gate (DG) and gate-all-around (GAA) structures improve electrostatic control and can enhance current drive while suppressing leakage [1–5].

At the same time, low-voltage power device design still requires a careful trade-off between breakdown voltage (BV) and specific on-resistance ($R_{\mathrm{sp,on}}$), where, as in lateral devices, BV is

enhanced by extending the drift region and optimizing its doping to satisfy the RESURF condition [6], while the on-resistance ($R_{\mathrm{ds,on}}$) is minimized by reducing the device length and optimizing its width.

This trade-off is captured by the specific on-resistance, $R_{\mathrm{sp,on}} = R_{\mathrm{ds,on}} \times \mathrm{Area}$, requiring careful balancing of $R_{\mathrm{sp,on}}$ and BV while controlling I_{leak} ($\leq 1 \times 10^{-13}$ A/µm) and ensuring reliability, which demands precise electrostatic engineering in DG structures [7].

Recently, machine learning (ML) has emerged as a powerful tool for semiconductor device optimization. By learning complex relationships between geometry, doping, and material parameters, ML models can efficiently predict key performance metrics such as BV and $R_{\mathrm{ds,on}}$. This data-driven approach accelerates design exploration and enables effective multi-objective optimization beyond traditional trial-and-error methods [8].

In this work, we first demonstrate the challenge of manually using Technology Computer-Aided Design (TCAD) simulations to determine the doping concentration and gate length that optimize the trade-off between $R_{\mathrm{sp,on}}$ and BV, and then apply Bayesian Optimization (BO) to show that simultaneous optimization of N_{d} and L_{g} along with four other parameters via BO yields a more uniform lateral field consistent with RESURF behavior, achieving a figure of merit (FOM) of 738 kW/mm^2.

The optimized device simultaneously maintains high BV and ultra-low $R_{\mathrm{sp,on}}$, representing a high-performance point in the BV–FOM landscape and demonstrating the clear advantage of integrating BO with DG-LDMOS design.

2 Simulation and optimization

The 3D GAA-LDMOS shown in Fig. 1a represents the target architecture, whereas this study optimizes the corresponding 2D DG-LDMOS cross section (A–A′) illustrated in Fig. 1b. This 2D structure is intended as a first-order approximation of nanosheet GAA devices, capturing the dominant electrostatics and relative device trends [9–11]. Width-direction and corner effects are deferred to future 3D studies. A DG configuration is employed within a 2D TCAD framework, with symmetrically biased top and bottom aluminum gates (work function 4.1 eV) controlling

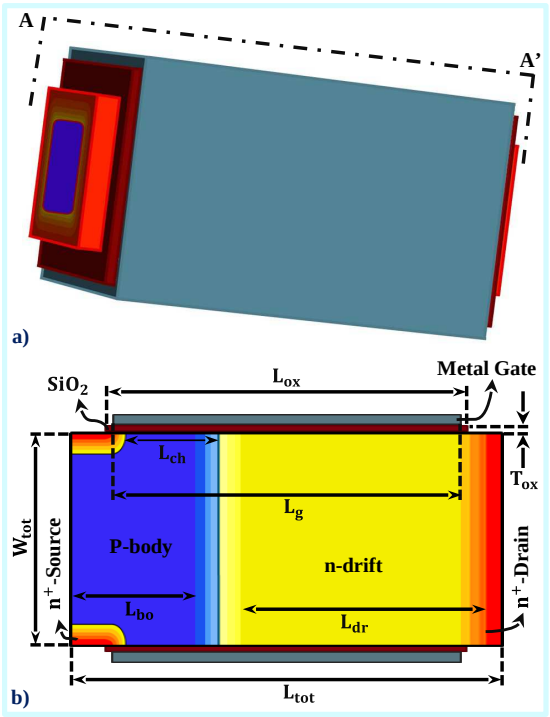


Fig. 1 (a) The proposed 3D GAA-LDMOS showing the A–A′ cross-section representing the studied DG-LDMOS. (b) A–A′ cross-sectional view of the optimized DG-LDMOS structure corresponding to the highest FOM, showing top and bottom 12 nm SiO_2 gate dielectrics and metal gates symmetrically. Gaussian doping profiles are applied in the source, drain, drift, and body regions

the laterally isolated channel and drift regions. The gate dielectric is 12 nm SiO_2, and the channel is formed in a p-body doped as N_{p}. The lateral channel length (L_{ch}) between the n^+ source and the p-body/n-drift junction is set by the p-body extension (L_{bo}) and the drift extension (L_{dr}), each defined by N_{p} and the n-drift doping N_{d}. L_{bo} is fixed to preserve the p-body–drift overlap, so the L_{ch} and depletion geometry are primarily controlled by L_{dr}, N_{p}, and N_{d}.

Simulations are performed using a commercial 2D drift-diffusion TCAD framework with proven predictive accuracy [12]. The model includes SRH and Auger recombination, Van Overstraeten impact ionization [13], mobility degradation, bandgap narrowing, and Fermi–Dirac statistics.

Gaussian doping profiles are a standard TCAD approximation of ion-implanted and annealed dopant distributions in silicon, used in key regions (p-body, n-drift, source, and drain) to capture implantation and diffusion effects [14]. The p-body

Table 1 Symbols, descriptions, and bounds of the six input parameters used in this work

Parameter	Description	Bounds
L_{tot}	Device length	400–800 nm
W_{tot}	Device width	200–500 nm
L_{dr}	Drift region extension length	150–550 nm
L_{g}	Gate length	300–700 nm
N_{p}	Body doping concentration	$(0.7\text{–}3) \times 10^{18}$ cm^{-3}
N_{d}	Drift doping concentration	$(0.8\text{–}8) \times 10^{17}$ cm^{-3}

peak concentration ensures strong electrostatic control, while the graded drift region enables efficient electric field distribution and a favorable BV–$R_{\mathrm{sp,on}}$ trade-off.

Electrical characteristics of the device are extracted from TCAD. BV is the V_{DS} at avalanche under off-state bias ($V_{\mathrm{GS}} = V_{\mathrm{BS}} = V_{\mathrm{SS}} = 0$ V). I_{leak} is measured at $V_{\mathrm{GS}} = 0$ V and $V_{\mathrm{DS}} = 5$ V. $R_{\mathrm{ds,on}}$ is obtained from $V_{\mathrm{DS}}/I_{\mathrm{DS}}$ at $V_{\mathrm{GS}} = 5$ V and $V_{\mathrm{DS}} = 0.1$ V, then used to compute $R_{\mathrm{sp,on}} = R_{\mathrm{ds,on}} \times \mathrm{HP}$, where the half pitch (HP) is the source-to-drain length (L_{tot}). $R_{\mathrm{ds,on}}$ is extracted from intrinsic TCAD simulations, excluding contact, silicide, and interconnect parasitics, consistent with standard FOM benchmarking. The estimated parasitic contribution is significantly smaller than the intrinsic $R_{\mathrm{ds,on}}$ and does not affect overall FOM trends. Finally, the FOM is obtained as FOM $= \mathrm{BV}^2/R_{\mathrm{sp,on}}$ (kW/mm^2).

Before applying BO, the effects of two key device parameters, N_{d} and L_{g}, are evaluated independently using TCAD simulations. N_{d} is varied from 1×10^{17} to 8×10^{17} cm^{-3}, while L_{tot}, W_{tot}, L_{g}, L_{dr}, and N_{p} are held constant at 800 nm, 200 nm, 700 nm, 550 nm, and 2×10^{18} cm^{-3}, respectively. L_{g} is then varied from 400 to 700 nm, while N_{d} is fixed at 3×10^{17} cm^{-3} and the remaining parameters retain the values used in the N_{d} sweep. The parameter boundaries are determined based on the device's structural and physical constraints, and the resulting insights significantly aid in defining suitable parameter ranges for BO.

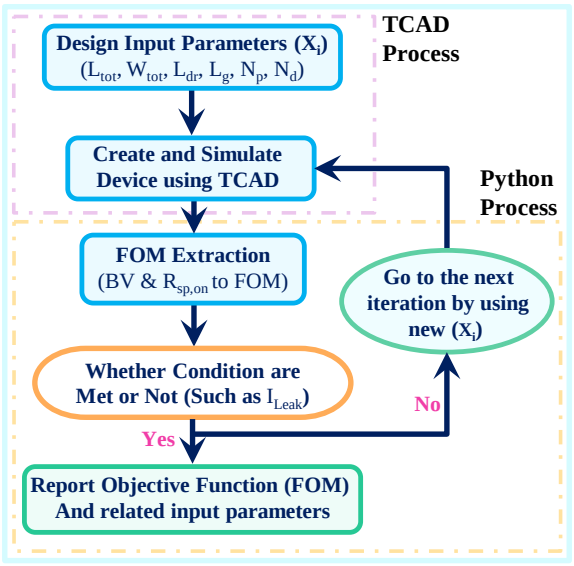


Fig. 2 BO–TCAD optimization flowchart

For BO, the objective function is Baliga's FOM [15], defined as

$$f(\mathbf{x}) = \mathrm{FOM} = \frac{\mathrm{BV}^2}{R_{\mathrm{sp,on}}}, \tag{1}$$

where $\mathbf{x} = [L_{\mathrm{tot}}, W_{\mathrm{tot}}, L_{\mathrm{dr}}, L_{\mathrm{g}}, N_{\mathrm{p}}, N_{\mathrm{d}}]$ denotes the design parameter vector. A Gaussian Process (GP) surrogate is used to approximate the FOM, guided by an Expected Improvement (EI) acquisition function, reducing the number of TCAD simulations and eliminating costly experimental iterations. The DG-LDMOS is defined by these six input variables ($\mathbf{x}$), summarized in Table 1, which determine the device geometry and electrostatics.

The optimization framework combines BO with TCAD simulations to identify optimal DG-LDMOS design parameters (Fig. 2). Extending prior BO-based transistor optimization studies [16], this optimization approach is applied to a nanosheet DG-LDMOS with coupled top and bottom gates, whose stronger electrostatic coupling and dual-channel conduction increase parameter interdependence. Optimization spaces ranging from single-parameter cases (N_{d} and L_{g}) and a three-parameter set (L_{tot}, W_{tot}, and N_{d}) to a full six-parameter set (L_{tot}, W_{tot}, L_{dr}, L_{g}, N_{p}, and N_{d}) are evaluated. Full co-optimization improves the BV–$R_{\mathrm{sp,on}}$ trade-off and achieves a peak Baliga's FOM of 738 kW/mm^2. BO is initialized with 20 uniformly sampled design points, and

TCAD results are used to train a GP surrogate model, with EI guiding iterative sampling [17].

3 Results and discussion

Figure 3a illustrates the effect of the drift region doping concentration, N_{d}, on BV and $R_{\mathrm{sp,on}}$ through a TCAD parameter sweep without BO. As N_{d} increases from 1×10^{17} to 8×10^{17} cm^{-3}, $R_{\mathrm{sp,on}}$ decreases steadily because the increased carrier concentration reduces the resistivity of the drift region. In contrast, BV exhibits a nonlinear dependence on N_{d}, reaching approximately 13.96 V at lower-to-intermediate doping concentrations before decreasing as the drift region becomes more heavily doped. This behavior reflects the conventional trade-off between drift resistance and depletion capability in an LDMOS structure. An N_{d} of approximately 7.2×10^{17} cm^{-3} provides a favorable compromise between the two performance metrics, but the single-parameter study also demonstrates that tuning N_{d} alone cannot simultaneously maximize BV and minimize $R_{\mathrm{sp,on}}$.

Similarly, Fig. 3b shows the influence of gate length, L_{g}, through a TCAD parameter sweep without BO. Increasing L_{g} from 0.40 to 0.70 µm reduces $R_{\mathrm{sp,on}}$ from approximately 0.82 to 0.66 m$\Omega \cdot$ mm^2, while BV increases to a maximum of approximately 13.45 V at $L_{\mathrm{g}} = 0.60$ µm and subsequently decreases slightly. The reduction in resistance occurs because the longer gate extends farther over the drift region, increasing electrostatic modulation of the underlying semiconductor while the channel length remains fixed. However, the nonmonotonic BV response indicates that simply maximizing gate length does not produce an optimum device. Instead, L_{g} must be coordinated with the drift geometry and doping profile to achieve an appropriate electric-field distribution.

Figure 4 presents the initial DG-LDMOS obtained through manual TCAD optimization, which achieves a maximum FOM of approximately 255 kW/mm^2 for $L_{\mathrm{tot}} = 800$ nm and $W_{\mathrm{tot}} = 200$ nm.

The corresponding electric-field profile exhibits substantial drain-side field crowding followed by a rapid decay through the drift region, indicating that the available drift length is not fully utilized for voltage support. Consistently, impact ionization is strongly localized close to the drain-side junction, where the peak electric field occurs. The on-state electron current density distribution is also confined to relatively narrow conduction paths. Together, these characteristics explain the limited BV–$R_{\mathrm{sp,on}}$ trade-off of the manually optimized structure and motivate simultaneous optimization of the coupled geometrical and doping parameters.

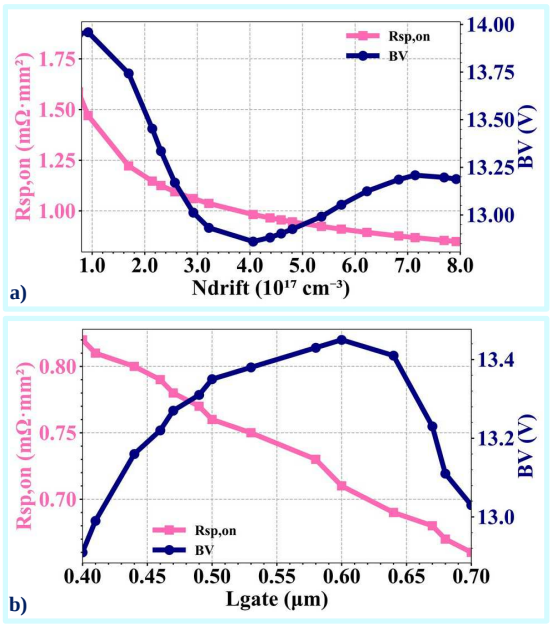


Fig. 3 TCAD-based optimization results illustrating the independent effect of two key parameters on the BV–$R_{\mathrm{sp,on}}$ trade-off: (a) n-drift doping concentration (N_{d}) and (b) length of the metal gate extension (L_{g}) over the oxide layer. In this step, the p-body doping (N_{p}), total device length (L_{tot}), total device width (W_{tot}), and drift region extension (L_{dr}) are kept constant

Figure 5 compares the results of 260 BO iterations for each parameter group, corresponding to more than 1000 TCAD-evaluated devices in total. The optimization begins with individual variation of N_{d} and L_{g}, followed by simultaneous optimization of three parameters, L_{tot}, W_{tot}, and N_{d}, and finally all six parameters, L_{tot}, W_{tot}, L_{dr}, L_{g}, N_{p}, and N_{d}.

Figure 5a demonstrates that increasing the dimensionality of the optimization space progressively expands the attainable BV–FOM envelope. In particular, the six-parameter optimization produces several designs with FOM values exceeding 700 kW/mm^2 and reaches a maximum of

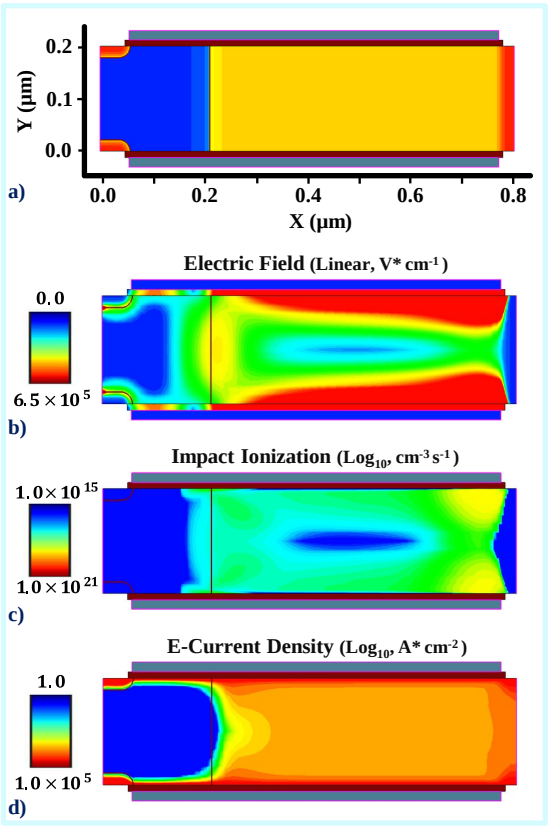


Fig. 4 Layout of the initial DG-LDMOS structure prior to computational optimization (device dimensions: 800 nm × 200 nm), along with the corresponding (a) doping profile, (b) electric field distribution, (c) impact ionization at breakdown voltage, and (d) electron current density at on-state, $V_{DS} = 0.1$ V and $V_{GS} = 5$ V, for the initial DG-LDMOS structure prior to BO

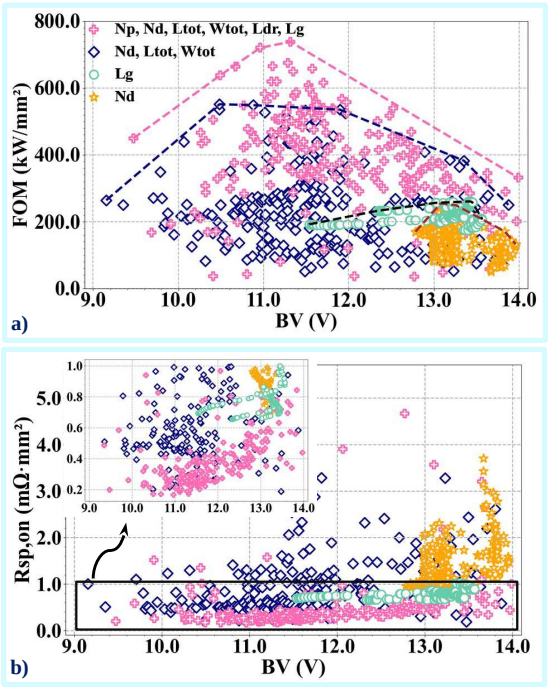


Fig. 5 (a) FOM versus BV for different parameter groups, with convex hulls showing the expanded optimization envelope as more parameters are included. (b) $R_{sp,on}$ versus BV for the same parameter groups, highlighting reduced resistance with multi-parameter optimization

738 kW/mm^2 while preserving the targeted low-voltage BV range. The convex hull boundaries further illustrate that the improvement results from access to combinations of parameters that cannot be reached through independent single-parameter tuning.

The corresponding BV–$R_{sp,on}$ distributions in Fig. 5b provide additional insight into this improvement. Increasing the number of simultaneously optimized parameters shifts the population toward lower $R_{sp,on}$ while retaining suitable BV, particularly in the region below 1 m$\Omega \cdot$ mm^2 highlighted by the inset.

This indicates that BO is not simply identifying designs with larger BV or lower resistance independently; rather, it learns combinations of structural and doping parameters that improve both sides of the competing trade-off. The increasingly favorable performance envelope therefore demonstrates the importance of accounting for interactions between geometry, drift-region design, and body/drift doping.

Figure 6a summarizes the maximum FOM obtained for the different BO parameter groups. The single-parameter optimizations of N_d and L_g achieve comparable maximum FOM values of approximately 254 and 260 kW/mm^2, respectively, indicating the limited improvement attainable through independent parameter tuning. Expanding the design space to three parameters (L_{tot}, W_{tot}, N_d) increases the maximum FOM to approximately 550 kW/mm^2, while simultaneous optimization of all six parameters (L_{tot}, W_{tot}, L_{dr}, L_g, N_p, N_d) further increases it to 738 kW/mm^2. This progressive improvement highlights the strong coupling among geometrical and doping parameters and demonstrates the

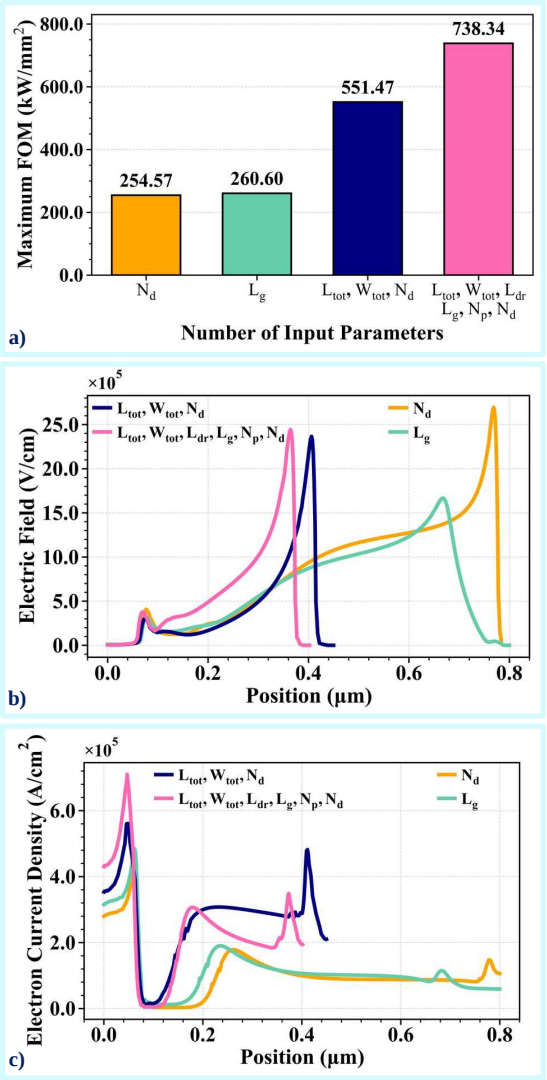


Fig. 6 (a) Maximum FOM obtained for different BO input-parameter groups, showing the performance improvement achieved by increasing the number of simultaneously optimized device parameters. (b) Lateral electric-field profiles in off-state for the optimum devices obtained from the different BO parameter groups. (c) Lateral electron current-density profiles in on-state for the optimum devices obtained from the different BO parameter groups

advantage of BO in identifying favorable parameter combinations that cannot be achieved efficiently through sequential single-parameter optimization.

Figure 6b compares the lateral electric-field profiles extracted 5 nm below the upper Si/SiO_2 interface for the optimum designs obtained from

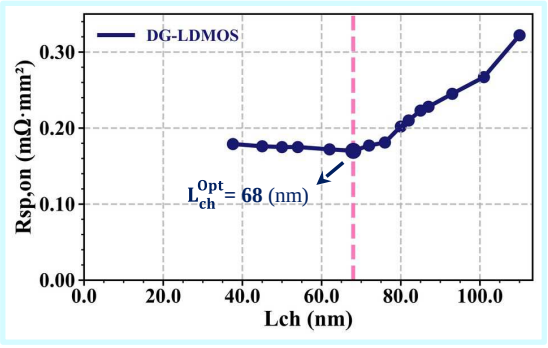


Fig. 7 $R_{sp,on}$ versus L_{ch} for the 5 V optimized DG-LDMOS

the different BO parameter groups. The single-parameter N_d and L_g cases retain the original 800 nm device length, whereas the three- and six-parameter optimizations shorten the device while simultaneously redistributing the lateral electric field. The multidimensional designs therefore achieve a more compact voltage-supporting region through coordinated adjustment of device dimensions and doping, demonstrating that the improved BV–$R_{sp,on}$ trade-off results from coupled electrostatic optimization rather than independent tuning of a single parameter.

Figure 6c compares the electron current-density magnitude along a lateral cutline located 5 nm below the upper Si/SiO_2 interface for the optimum designs obtained from different BO parameter groups. The single-parameter N_d and L_g cases retain the initial 800 nm device length and exhibit similar current-density profiles, whereas inclusion of the geometrical parameters reduces L_{tot} to approximately 450 and 400 nm for the three- and six-parameter optimum designs, respectively. The multidimensional designs exhibit substantially redistributed and enhanced near-interface current density along the shortened source-to-drain conduction path. Together with the corresponding reduction in $R_{sp,on}$, these profiles indicate that the FOM improvement arises from the coupled optimization of device geometry and doping rather than from variation of an individual parameter alone.

Figure 7 shows $R_{sp,on}$ as a function of the selected channel length, L_{ch}, for high-FOM DG-LDMOS designs identified through BO. The minimum $R_{sp,on}$ occurs near $L_{ch} \approx 68$ nm while the required BV is maintained. Interestingly, the

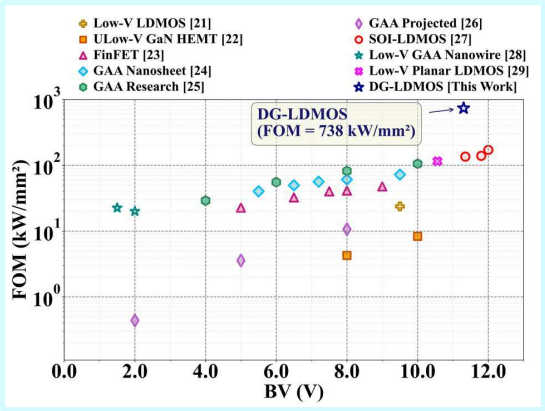


Fig. 8 BV–FOM benchmark of the optimized DG-LDMOS against reported low-voltage GAA, FinFET, and LDMOS devices, demonstrating a peak FOM of 738 kW/mm^2

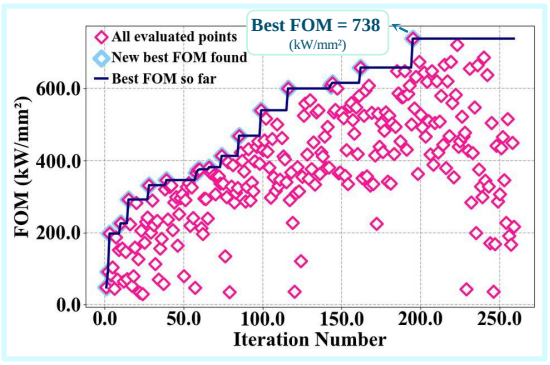


Fig. 9 FOM versus BO iteration number for the six-parameter optimization, showing convergence to near-maximum FOM within 260 iterations

shortest explored channel lengths, approaching approximately 38 nm, do not produce the lowest resistance. This result indicates that aggressive geometrical scaling alone is insufficient to maximize device performance. At very short L_{ch}, stronger short-channel effects and increased leakage require additional electrostatic control, including higher body doping, which can reduce carrier mobility and offset the resistance benefit expected from a shorter channel [18]. The optimum L_{ch} therefore emerges from the coupled optimization rather than from simple dimensional scaling. We recently compared the optimized DG-LDMOS with a manually optimized planar LDMOS baseline [19] and found an approximately fivefold reduction in $R_{\mathrm{sp,on}}$ without sacrificing BV, despite a longer optimal channel length (68 vs. 40 nm), highlighting the superior electrostatic control of the dual-gate structure.

Figure 8 compares the BV–FOM characteristics of the optimized DG-LDMOS with previously reported low-voltage power and logic devices [20–28]. The BO-optimized design occupies a high-FOM region of the low-voltage performance landscape, reaching 738 kW/mm^2 at a BV of 11.32 V. Relative to the performance envelope represented by the selected literature devices, the optimized structure extends the achievable FOM substantially while operating in a similar low-voltage range. This comparison emphasizes the potential of combining multi-gate electrostatic control with systematic optimization of the lateral device geometry. It should be noted that the reported $R_{\mathrm{sp,on}}$ is intrinsic and therefore excludes contact, silicide, and interconnect parasitic contributions, consistent with the TCAD-based benchmarking approach adopted in this work.

Figure 9 illustrates the convergence behavior of the six-parameter BO process. The best FOM of 738.3 kW/mm^2 is first identified at approximately the 195th iteration within a total of 260 TCAD evaluations. The rapid increase in the best-observed FOM during the earlier iterations indicates that the GP surrogate progressively learns the high-performance regions of the design space, whereas subsequent evaluations mainly refine the solution and verify the surrounding parameter region. The absence of substantial improvement after the optimum is reached suggests that optimization has approached a stable high-performance region.

It should be noted that the FOM of newly evaluated points is not expected to increase monotonically with BO iteration. Once a high-performing region is identified, the acquisition function continues to balance exploitation near the current optimum with exploration of uncertain regions, explaining the lower-FOM samples observed after approximately iteration 260. Moreover, because the optimization is performed with a finite evaluation budget, additional iterations could potentially identify a better design, although further improvement is not guaranteed.

These results are consistent with previous BO-based semiconductor-device studies [29, 30] and demonstrate the suitability of surrogate-assisted optimization for coupled device-design

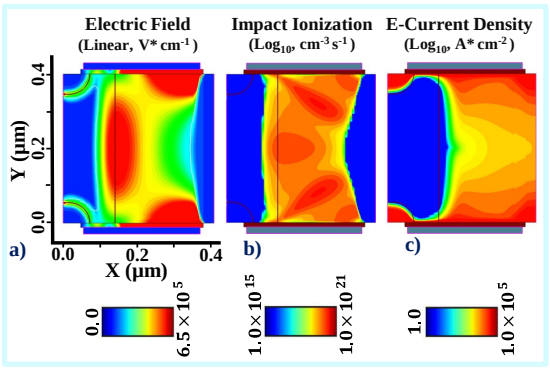


Fig. 10 (a) Electric field distribution, (b) impact ionization profile at breakdown voltage, and (c) electron current density at on-state, $V_{DS} = 0.1$ V and $V_{GS} = 5$ V, for the optimized DG-LDMOS, corresponding to the best FOM of 738 kW/mm^2

spaces where exhaustive TCAD sampling would be computationally expensive.

Figure 10 presents the electric field distribution, impact ionization profile, and on-state electron current density of the final BO-optimized DG-LDMOS corresponding to the maximum FOM. Compared with the initial manually optimized structure in Fig. 4, the electric field is distributed more smoothly through the drift region, with reduced localization near the drain.

The corresponding impact ionization profile is consequently distributed over a broader portion of the drift region rather than being concentrated strongly at the drain-side junction. This redistribution allows a larger portion of the lateral drift region to contribute to voltage support and is consistent with improved RESURF-like behavior. In the on-state condition, electron current is carried along both the upper and lower inversion interfaces created by the symmetric double-gate structure, increasing the effective conducting cross-section. These combined electrostatic and transport improvements enable an intrinsic $R_{sp,on}$ of 0.17 m$\Omega \cdot$mm^2 while maintaining a BV of 11.32 V.

Table 2 summarizes the highest FOM and corresponding device dimensions and doping concentrations obtained from single-, three-, and six-parameter BO, alongside those of the initial TCAD device. The single-parameter studies modify only the corresponding optimization variable, whereas the three-input BO jointly optimizes L_{tot}, W_{tot}, and N_d, resulting in a substantially more

Table 2 Evolution of key DG-LDMOS design parameters from the initial TCAD device through single- and multidimensional BO studies

Parameter	Initial	N_d BO	L_g BO	Three inputs	Six inputs
L_{tot} (nm)	800	800	800	450	400
W_{tot} (nm)	200	200	200	412	400
L_g (nm)	700	700	640	320	310
L_{dr} (nm)	550	550	550	225	174
N_p^a	2.0	2.0	2.0	2.0	1.6
N_d^b	5.5	7.4	5.5	5.9	2.8

[a]In units of 10^{18} cm^{-3}. [b]In units of 10^{17} cm^{-3}.

compact device. The accompanying reduction in L_g follows from the reduced L_{tot}, since the gate extends over the available lateral device region, rather than from L_g being an independent optimization variable. In the three-parameter study, L_{dr} is not an optimization variable; it is manually fixed at $0.5L_{tot}$. In the final six-parameter study, L_{dr} is explicitly included in the BO design space, enabling simultaneous optimization of the geometrical and doping parameters.

Figure 11a presents the full off-state I_D–V_D characteristic of the best optimized device from low drain bias through avalanche breakdown. The drain current remains below the imposed leakage criterion of 1×10^{-13} A/µm throughout the pre-breakdown operating range and increases sharply only as the device approaches BV. This result is important because it confirms that the improvement in FOM is not achieved by accepting excessive off-state leakage or premature punch-through. Instead, the optimized geometry maintains effective electrostatic isolation while supporting the required drain voltage.

The broader relationship between leakage and optimized performance is shown in Fig. 11b, where FOM is plotted against I_{leak} for the BO-generated designs. A substantial population of devices simultaneously exhibits FOM values above 400 kW/mm^2 and leakage currents below 5×10^{-15} A/µm. Thus, the BO search does not converge exclusively toward a narrow high-FOM/high-leakage region; rather, multiple high-performance solutions remain well within the leakage constraint. These results confirm that the optimized BV–$R_{sp,on}$ trade-off can be obtained while preserving low off-state current.

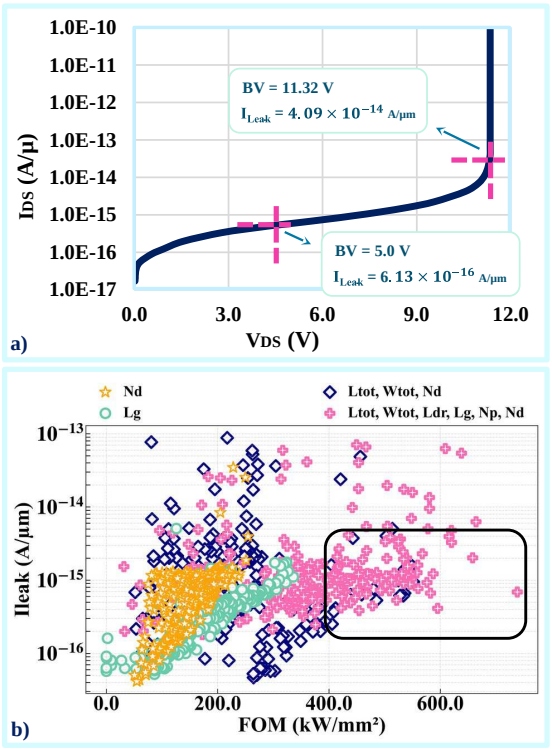


Fig. 11 (a) Off-state I_D–V_D curve of the optimized device up to breakdown, confirming that I_{leak} remains below 1×10^{-13} A/µm throughout the full operating window. (b) FOM versus leakage current for BO-generated devices, showing a large population satisfying the leakage criterion, with many achieving $I_{leak} < 5 \times 10^{-15}$ A/µm at high FOM

4 Conclusion

This work demonstrates a TCAD-assisted Bayesian optimization framework for systematically improving the performance of a nanosheet-inspired DG-LDMOS intended for low-voltage switched-mode applications. Beginning with individual studies of N_d and L_g, the analysis shows that single-parameter tuning provides only limited improvement because BV and $R_{sp,on}$ depend strongly on interactions among the device geometry, drift-region dimensions, and doping concentrations. Increasing the optimization space from one to three and ultimately six parameters progressively expands the achievable performance envelope, with the full six-parameter BO producing the highest FOM.

The final optimized structure achieves an intrinsic $R_{sp,on}$ of 0.17 m$\Omega \cdot$ mm^2 at $L_{ch} \approx 68$ nm while maintaining a BV of 11.32 V, corresponding to a maximum Baliga FOM of 738 kW/mm^2. Electrostatic analysis shows a smoother drift-region electric field distribution and reduced drain-side field crowding relative to the manually optimized device, while the dual inversion channels provide an increased effective current-conduction region. These results demonstrate that simultaneous optimization of coupled device parameters can substantially outperform sequential manual tuning and provide a systematic path toward high-performance nanosheet-based lateral power device design.

The present 2D DG-LDMOS serves as a physics-based approximation of the wide-nanosheet limit and establishes the design methodology required for subsequent three-dimensional GAA-LDMOS development. Extension of the optimization framework to full 3D structures can incorporate width-direction effects, nanosheet stacking, corner electrostatics, and fabrication-related geometrical constraints, providing a pathway toward more realistic nanosheet LDMOS optimization.

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