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A Single-Source Seven-Level Switched-Capacitor Multilevel Inverter with Three-fold Voltage Gain

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Abstract-This paper proposes a single-source, seven-level (7L) switched-capacitor (SC) inverter that triples (3×) the input voltage while maintaining a direct common-ground (CG) between the source and the grid, which suppresses the leakage current in transformerless operation for low-voltage grid-connected renewable energy sources. It uses 10 switches, 2 capacitors, and 1 diode. The SCs are balanced naturally to their nominal voltages in every fundamental cycle without voltage additional controls. The peak switch voltage stress (PSVS) is limited to 66.67% of output voltage, with a per-unit total standing voltage ($TSV_{p.u.}$) of 5, ensuring lower switch voltage stress profile and a longer predicted lifetime than existing common-ground seven-level topologies. Power-loss and reliability analysis are carried to estimate the efficiency and the expected mean time to failure. A detailed cost and size study is presented to show the best balance between voltage gain, cost and volume. Simulation test results using MATLAB and a 750-W laboratory prototype experimental results confirm the 7L, 3× boost, stable operation under different loads and other operating conditions such as step changes in load, input voltage and modulation index.

Index Terms—Common ground, multilevel inverter, reliability, seven-level inverter, switched capacitor, boosting.

1. INTRODUCTION

Multilevel inverters (MLIs) are widely used in photovoltaic (PV) systems, electric drives, and grid-connected energy storage. These converters generate a stepped output voltage with low harmonic distortion, reduced *dv/dt*, and smaller filter requirements compared with conventional two-level inverters [1]. The three conventional MLI structures are the neutral-point-clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) inverters. Although these topologies can generate multilevel output voltages, each has some limitations. NPC and FC inverters require more diodes or capacitors as the number of voltage levels increases, and voltage balancing also becomes more difficult. The CHB inverter requires multiple isolated dc sources [2]. In addition, these conventional structures cannot boost the input voltage. Therefore, an additional boost converter with an inductor or high frequency transformer is normally required when a low-voltage PV or battery source is used [3].

Switched-capacitor multilevel inverters (SC-MLIs) provide an attractive solution to these limitations. In an SC-MLI, capacitors are charged from the dc source and then connected in series with the source to increase the output voltage. Therefore, voltage boosting and multilevel inversion can be achieved in a single stage without magnetic components [4]. The early SC-MLIs reported in [1]-[4] use a single dc source and provide a moderate voltage gain. However, their capacitors are generally charged through the switching path, and the charging current can depend on the load and modulation method. The topology in [5] provides capacitor voltage balancing without sensors, while [6] achieves a higher voltage gain with more components. In general, these topologies have simple control, but their voltage gain may not be sufficient for

low-voltage sources. To achieve a higher voltage gain, another group of SC-MLIs uses different capacitor voltage combinations to obtain a three-times voltage boost from a single dc source. These topologies can be further classified based on their grounding arrangement [7]-[11]. The circuits in [12], [14], [15] and [16]-[22] achieve the required voltage gain using different combinations of switches and capacitors. However, they do not provide a common ground between the input source and load. This is an important concern in transformerless grid-connected PV systems. Without a common ground, leakage current can flow through the parasitic capacitance between the PV source and ground, which may cause safety and electromagnetic interference concerns [12], [16]. Some of these topologies also require more diodes or capacitors [17]-[19], while others impose higher blocking voltage on individual switches [20]-[22]. Higher voltage stress requires devices with higher voltage ratings and can increase the converter cost.

Recent SC-MLIs have attempted to improve these features. The seven-level topology in [23] provides a voltage gain of three using only six switches. However, it requires two inductors for soft charging of four capacitors. The topology in [24] generates up to eleven voltage levels from a single source with self-balanced capacitors, but it requires twelve switches and two dc-link capacitors. Among the grounded structures, the circuits in [25] and [26] provide a common ground for transformerless PV applications. The topology in [25] uses a quasi-Z-source cell to extend the input voltage range, while [26] generates five voltage levels without capacitor voltage sensors. The nine-level topology in [27] provides a voltage gain of four using twelve switches and three self-balanced capacitors. These studies show the continued development of single-source boosting MLIs. However, higher voltage gain or more output levels are often achieved by increasing the number of switches, capacitors, or magnetic components. Reliability is another important factor that has received less attention in SC-MLI studies. Each additional switch, diode, or capacitor introduces another possible point of failure. In many power converters, semiconductor devices contribute significantly to the overall failure rate. The MIL-HDBK-217 parts-stress method has been used to evaluate converter reliability and to study the effects of junction temperature and voltage stress on mean time to failure (MTTF) [28]. Reducing the number of components and limiting their voltage stress can therefore improve reliability and operating lifetime. Hence, a compact converter with moderate device stress is desirable for applications that require long-term operation. Based on these considerations, this paper proposes a single-source 7L-CGSC with a voltage gain of 3× with features as depicted in Fig. 1.

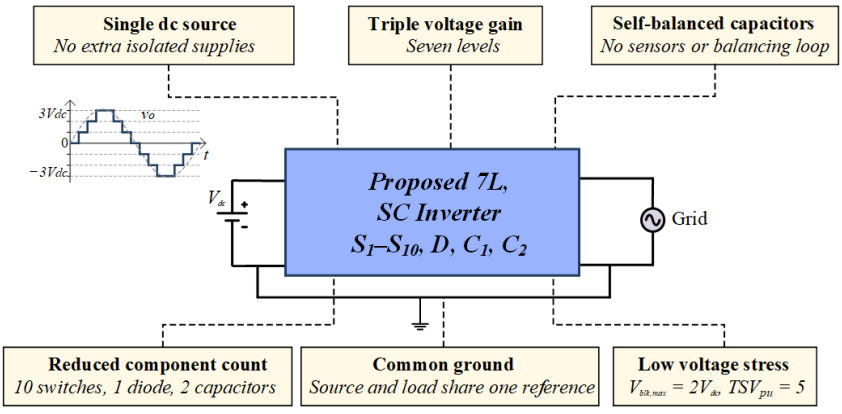


Fig. 1. Features of the proposed 7L-CGSC-3× inverter.

This paper is organized as follows. Section II describes the proposed topology, its operating modes, and the voltage stress on its devices. Section III presents the switching-angle selection and the design of the capacitors. Section IV analyses the power loss and efficiency, and Section V evaluates the reliability. Sections VI and VII compare the proposed inverter with existing

topologies in terms of component count, device stress, cost, and size. Sections VIII and IX present the simulation and experimental results, and Section X concludes the paper.

2. DESCRIPTION AND OPERATING PRINCIPLE OF 7L-CGSC-3× TOPOLOGY

A. Description

The proposed 7L-CGSC-3× inverter consists of a single dc source V_{dc}, ten switches (S_1-S_{10}), two capacitors (C_1 and C_2), and one diode, as shown in Fig. 2(a). The proposed inverter generates seven output voltage levels: 0, $\pm3V_{dc}$, $\pm2V_{dc}$, $\pm V_{dc}$, and the SCs are charged through parallel paths and discharged in series with the dc source to supply the load. The SC C_1 is charged to V_{dc}, while C_2 is charged to $2V_{dc}$. This arrangement provides a voltage gain of three without an additional dc source or any magnetic components. Different switching states combine the dc-source with SCs voltages to generate the positive and negative levels.

The switches in the load-current path of each mode, the switches that form the capacitor charging path and the state of each capacitor are summarized in Table I. A switch listed in either column is gated on during that mode.

TABLE I
SWITCHING TABLE OF THE PROPOSED INVERTER

Mode	Voltage level	Load-current path (switches ON)	Capacitor charging path (switches ON)	Capacitor status	
				C_1	C_2
1	$+V_{dc}$	S_1, S_4, S_7, S_9	S_1, S_3, S_4, S_6, S_7, S_8	Discharging	Charging
2	$+2V_{dc}$	S_2, S_3, S_4, S_5, S_8, S_9	—	—	Discharging
3	$+3V_{dc}$	S_1, S_4, S_5, S_8, S_9	S_1, S_2, D	Charging	Discharging
4	0	S_2, S_3, S_4, S_7, S_9	—	—	—
5	$-V_{dc}$	S_3, S_6, S_8, S_{10}	S_1, S_3, S_4, S_6, S_7, S_8	Discharging	Charging
6	$-2V_{dc}$	S_2, S_3, S_4, S_7, S_{10}	—	—	Discharging
7	$-3V_{dc}$	S_3, S_5, S_6, S_7, S_{10}	—	Discharging	Discharging

B. Operating Modes

The seven operating modes are shown in Fig. 2(b)-(h). The zero-voltage level is shown in Fig. 2(b), while ±Vdc, ±2Vdc, and ±3Vdc are shown in Fig. 2(c)-(h), respectively. In each subfigure, the conducting switches are shown in blue, the red line indicates the load-current path, and the solid orange line indicates the SCs-charging path.

First Positive Voltage Level ($+V_{dc}$):

The first positive level is obtained by turning on S_1, S_4, S_7 and S_9, as shown in Fig. 2(c). The load current leaves the positive terminal of V_{dc}, passes through S_1, S_4, S_7 and S_9 into the load, and returns to the negative terminal of the source through the common ground. In the same level, C_2 is placed in parallel with the series combination of V_{dc} and C_1 through S_1, S_3, S_4, S_6, S_7 and S_8, and is therefore charged to $V_{dc} + V_{C1} = 2V_{dc}$.

Second Positive Voltage Level ($+2V_{dc}$):

In this state the charged capacitor C_2 supplies the load on its own. Its positive terminal is connected to the load through S_9, and the load current returns from the common ground through S_3, S_2, S_4, S_5 and S_8 to the negative terminal of C_2, as shown in Fig. 2(e). The output voltage is therefore $V_o=V_{C2} = 2V_{dc}$.

Third Positive Voltage Level ($+3V_{dc}$):

In this state the source V_{dc} and C_2 are connected in series, which gives the maximum output $+3V_{dc}$. The current leaves the positive terminal of C_2 through S_9 and enters the load; it returns through V_{dc} and the series-connected switches S_1, S_4, S_5 and S_8 to the negative terminal of C_2,

as shown in Fig. 2(g). Meanwhile, C_1 is recharged from V_{dc} along the loop formed by S_1, S_2 and the diode.

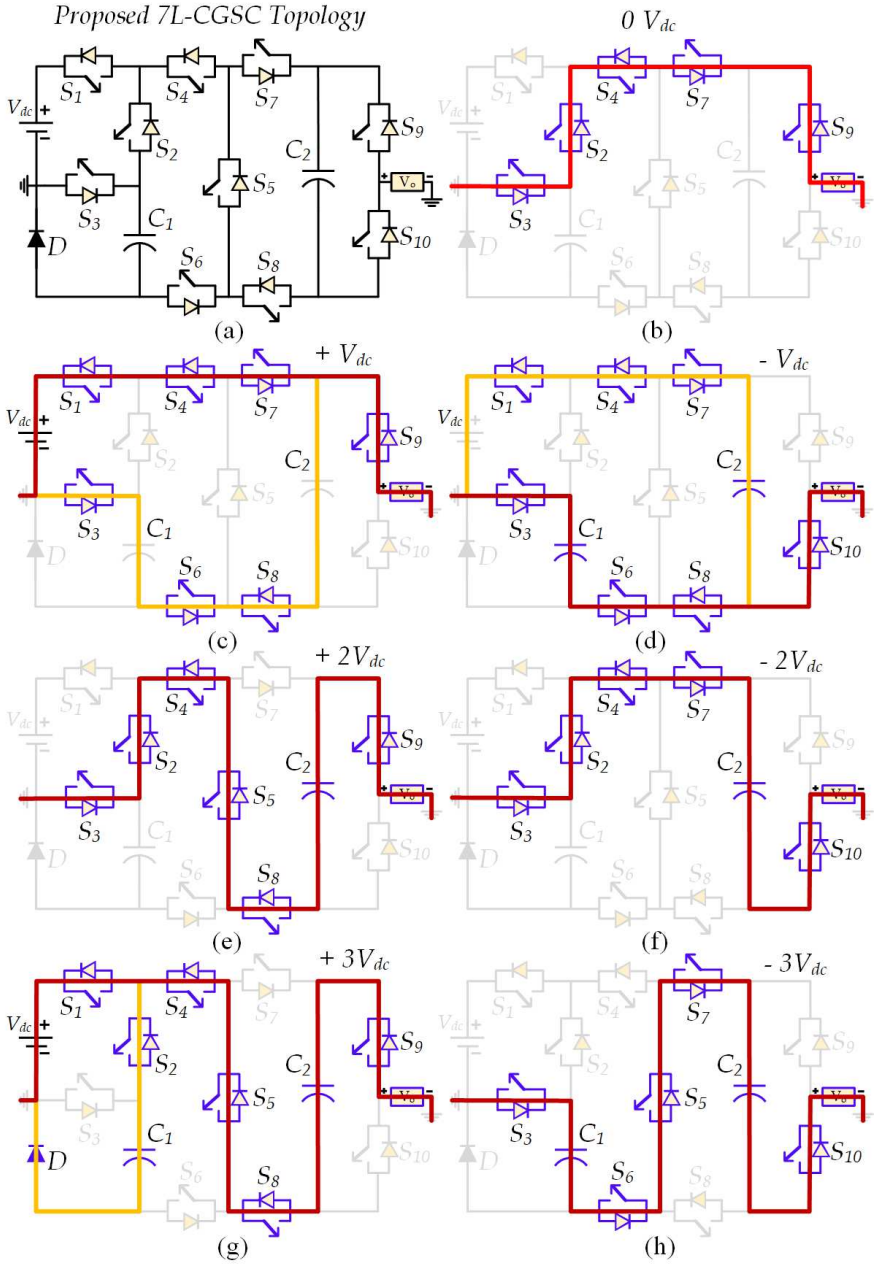


Fig. 2. Proposed 7L-CGSC inverter and its operating modes: (a) proposed topology, (b) zero level, (c) $+V_{dc}$, (d) $-V_{dc}$, (e) $+2V_{dc}$, (f) $-2V_{dc}$, (g) $+3V_{dc}$ and (h) $-3V_{dc}$.

Zero Output Level ($0V_{dc}$):

A zero output is produced by turning on S_2, S_3, S_4, S_7 and S_9. The output terminal is then tied to the common ground, and the load current circulates through these switches without drawing energy from either source or SCs, as shown in Fig. 2(b).

First Negative Voltage Level ($-V_{dc}$):

A negative output is produced by connecting C_1 across the load with reversed polarity. S_3, S_6, S_8 and S_{10} are turned on, as shown in Fig. 2(d): the positive terminal of C_1 is held at ground potential through S_3, while its negative terminal reaches the output through S_6, S_8 and S_{10}. The load therefore sees $-V_{C1} = -V_{dc}$. In the same interval, C_2 is recharged to $2V_{dc}$ through S_1, S_3, S_4, S_6, S_7 and S_8, which place it in parallel with the series combination of V_{dc} and C_1.

Second Negative Voltage Level (-$2V_{dc}$):

For the second negative level, S_2, S_3, S_4, S_7 and S_{10} are turned on, as shown in Fig. 2(f). The positive terminal of C_2 is tied to the common ground through S_7, S_4, S_2 and S_3, and its negative terminal is connected to the output through S_{10}, so the load receives $-V_{C2} = -2V_{dc}$. The diode is reverse biased and does not conduct in this state.

Third Negative Voltage Level (-$3V_{dc}$):

The peak negative level is obtained when C_1 and C_2 are connected in series with reversed polarity. S_3, S_5, S_6, S_7 and S_{10} are turned on, as shown in Fig. 2(h). The positive terminal of C_1 is held at ground through S_3, its negative terminal is linked to the positive terminal of C_2 through S_6, S_5 and S_7, and the negative terminal of C_2 reaches the output through S_{10}. The load voltage is thus $-(V_{C1} + V_{C2}) = -3V_{dc}$.

The voltage stress across the power components is shown in Fig. 3. The switches S_1, S_2, S_3, S_4, and S_6 form the input and capacitor-charging cell, and each switch blocks a maximum voltage of V_{dc}, whereas the switches S_5, S_7, S_8, S_9, and S_{10} are connected to C_2 or the output stage and block a maximum voltage of $2V_{dc}$. The diode has a peak reverse voltage of V_{dc}. Therefore, the total standing voltage (TSV) of the switches is $TSV = 5V_{dc} + 5(2V_{dc}) = 15V_{dc}$. With a peak output voltage of $3V_{dc}$, the per-unit TSV is $TSV_{pu} = 15V_{dc}/3V_{dc} = 5$. The maximum blocking voltage of any switch is $2V_{dc}$, which gives a maximum blocking voltage-to-gain ratio of $2V_{dc}/3V_{dc} = 0.67$. This reduced voltage stress allows the use of switches with lower voltage ratings and helps reduce the overall cost, as discussed in Section VII. Besides the primary switching states listed in Table I the proposed topology offers redundant switching states, in which the same output level is produced by different switch combinations. The redundant states do not increase the maximum blocking voltage of any switch, and they can be used for SC voltage balancing and to reduce the number of switching transitions.

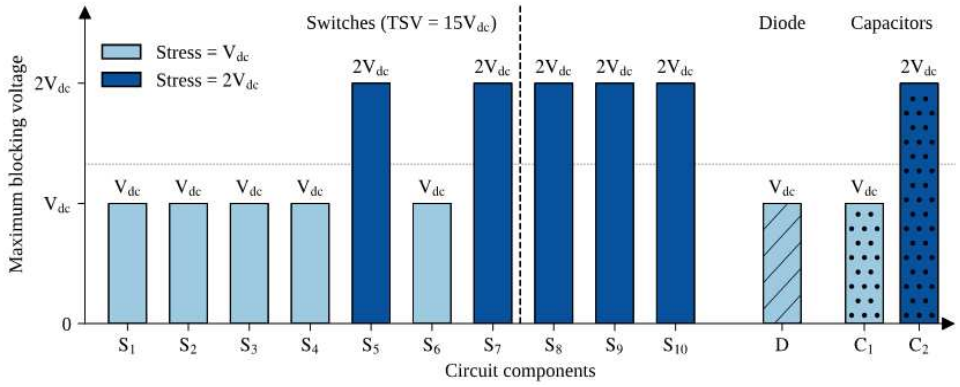


Fig. 3. Maximum blocking voltage of the switches, the diode and the capacitors of the proposed inverter.

3. SWITCHING-ANGLE SELECTION AND DESIGN OF PASSIVE ELEMENTS

For a 7L output the positive output levels are 0, V_{dc}, $2V_{dc}$ and $3V_{dc}$, so that the maximum output voltage is $V_o=3V_{dc}$. The sinusoidal reference is

$$V_{ref} = 3V_M \sin(\omega t)$$

The switching angle follows from the condition that the reference equals the boundary voltage at the switching instant,

$$3V_M \sin\theta_i = \frac{(2i-1)V}{2}$$

$$\theta_i = \sin^{-1}\left(\frac{2i-1}{6M}\right)$$

The three switching angles of the positive quarter-cycle are therefore

$$\theta_1 = \sin^{-1}\left(\frac{1}{6M}\right) \quad (1)$$

$$\theta_2 = \sin^{-1}\left(\frac{3}{6M}\right) = \sin^{-1}\left(\frac{1}{2M}\right) \quad (2)$$

$$\theta_3 = \sin^{-1}\left(\frac{5}{6M}\right) \quad (3)$$

The resulting staircase output over one fundamental cycle is shown in Fig. 4, which also shows the intervals in which the capacitors discharge. The SC C_2 discharges during the interval $\pi+\theta_2 \rightarrow 2\pi-\theta_2$, and C_1 discharges during the interval $\pi+\theta_3 \rightarrow 2\pi-\theta_3$.

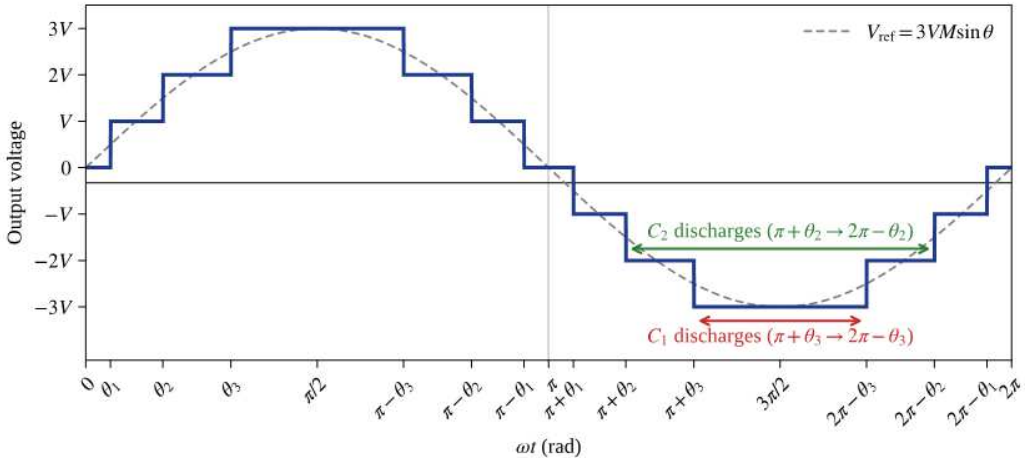


Fig. 4. Typical 7L staircase output voltage over one fundamental cycle and the discharge intervals of C_1 and C_2

The SC C_1 supplies the load during the interval $\pi+\theta_3 \rightarrow 2\pi-\theta_3$, so its ripple is,

$$\Delta V_{C1} = \frac{1}{C_1}\int_{(\pi+\theta_3)/\omega}^{(2\pi-\theta_3)/\omega} I_m \sin(\omega t - \phi)\, dt$$

The required capacitance is calculated as (4),

$$C_1 = \frac{I_m\sqrt{36M^2-25}\cos\phi}{6\pi f M\, \Delta V_{C1}} \quad (4)$$

The SC C_2 discharges during the interval $\pi+\theta_2 \rightarrow 2\pi-\theta_2$, so that the ripple is,

$$\Delta V_{C2} = \frac{1}{C_2}\int_{(\pi+\theta_2)/\omega}^{(2\pi-\theta_2)/\omega} I_m \sin(\omega t - \phi)\, dt$$

The required capacitance is calculated as (5),

$$C_2 = \frac{I_m\sqrt{4M^2-1}\cos\phi}{2\pi f M\, \Delta V_{C2}} \quad (5)$$

The two capacitance expressions (4) and (5), give the capacitances of SCs that are required to keep the voltage ripple of C_1 and C_2 within the chosen limits ΔV_{C1} and ΔV_{C2} for a given peak load current I_m, load angle φ, modulation index M and output frequency f.

4. POWER-LOSS ANALYSIS

The power-loss characteristics of the proposed inverter are evaluated with a state-dependent equivalent-circuit approach [34]. The analysis accounts for the conduction losses of the semiconductor switches and the diode, the equivalent series resistance (ESR) losses of the switched capacitors and the dynamic switching losses that are associated with the semiconductor transitions.

A. Conduction Loss

The conduction loss of each semiconductor device is determined from its RMS current and equivalent on-state resistance (R_{on}). For a resistive semiconductor conduction path, the corresponding loss is expressed as,

$$P_{cond,i} = I_{rms,i}^2 R_{on,i}$$

where $I_{rms,\,i}$ is the RMS value of the current carried by the i^{th} device during its conduction interval, and $R_{on,i}$ is its on-state resistance. The switches do not all have the same resistance: those with a lower voltage rating have a smaller on-state resistance than those that must block a higher voltage. Each capacitor branch is modelled by its equivalent series resistance (ESR), $R_{ESR,C1}$and $R_{ESR,C2}$, whereas the diode is represented by an equivalent resistance, R_D. Adding the losses of the switches, the capacitor branches and the diode give the total conduction loss of the inverter:

$$P_{cond,total} = \sum_{i=1}^{10} I_{rms,S_i}^2 R_{on,S_i} + I_{rms,D}^2 R_D + I_{rms,C1}^2 R_{ESR,C1} + I_{rms,C2}^2 R_{ESR,C2} \qquad (6)$$

Only the devices that conduct in a particular switching state are included in the corresponding state-level calculation. Since the number and identity of the conducting devices change with the generated voltage level, the conduction loss is obtained separately for each operating state. The equivalent circuits of the seven states are shown in Fig. 5, and the equations that follow from them, from which the conduction loss is calculated, are given below.

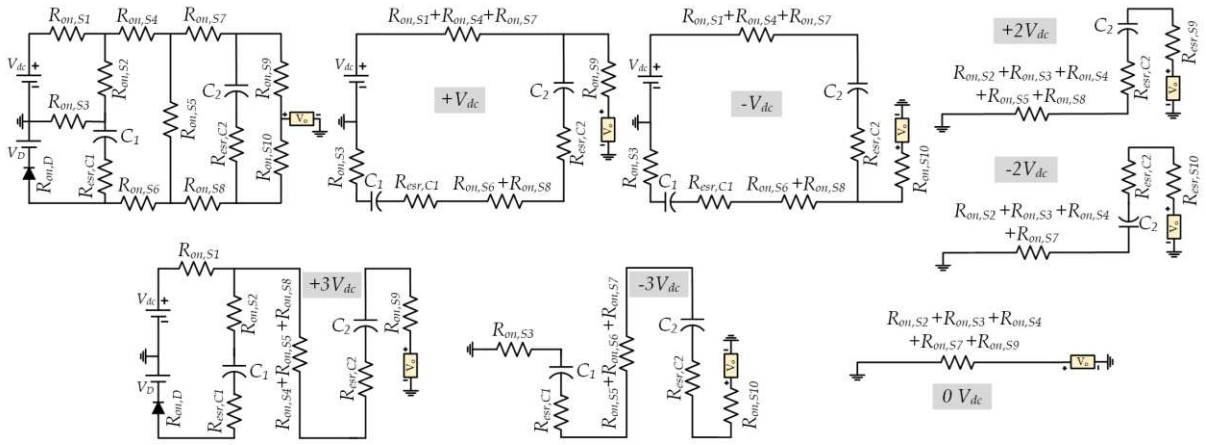


Fig. 5. Equivalent circuits of the proposed inverter for the seven operating states, used for the conduction-loss calculation.

$$
\begin{aligned}
P_{cond,+V_{dc}} &= I_{S1}^2 R_{on,S1} + I_{S4}^2 R_{on,S4} + I_{S7}^2 R_{on,S7} + I_{S9}^2 R_{on,S9} + I_{S8}^2 R_{on,S8} \\
&\quad + I_{S6}^2 R_{on,S6} + I_{S3}^2 R_{on,S3} + I_{C2}^2 R_{ESR,C2} + I_{C1}^2 R_{ESR,C1} \\
P_{cond,+2V_{dc}} &= I_{S3}^2 R_{on,S3} + I_{S2}^2 R_{on,S2} + I_{S4}^2 R_{on,S4} + I_{S5}^2 R_{on,S5} + I_{S8}^2 R_{on,S8} \\
&\quad + I_{S9}^2 R_{on,S9} + I_{C2}^2 R_{ESR,C2} \\
P_{cond,+3V_{dc}} &= I_{S1}^2 R_{on,S1} + I_{S2}^2 R_{on,S2} + I_{S4}^2 R_{on,S4} + I_{S5}^2 R_{on,S5} + I_{S8}^2 R_{on,S8} \\
&\quad + I_{S9}^2 R_{on,S9} + I_{D}^2 R_{on,D} + I_{C1}^2 R_{ESR,C1} + I_{C2}^2 R_{ESR,C2} \\
P_{cond,0} &= I_{S3}^2 R_{on,S3} + I_{S2}^2 R_{on,S2} + I_{S4}^2 R_{on,S4} + I_{S7}^2 R_{on,S7} + I_{S9}^2 R_{on,S9} \\
P_{cond,-V_{dc}} &= I_{S1}^2 R_{on,S1} + I_{S3}^2 R_{on,S3} + I_{S4}^2 R_{on,S4} + I_{S7}^2 R_{on,S7} + I_{S6}^2 R_{on,S6} \\
&\quad + I_{S8}^2 R_{on,S8} + I_{S10}^2 R_{on,S10} + I_{C2}^2 R_{ESR,C2} + I_{C1}^2 R_{ESR,C1} \\
P_{cond,-2V_{dc}} &= I_{S3}^2 R_{on,S3} + I_{S2}^2 R_{on,S2} + I_{S4}^2 R_{on,S4} + I_{S7}^2 R_{on,S7} + I_{S10}^2 R_{on,S10} \\
&\quad + I_{C2}^2 R_{ESR,C2} \\
P_{cond,-3V_{dc}} &= I_{S3}^2 R_{on,S3} + I_{S6}^2 R_{on,S6} + I_{S5}^2 R_{on,S5} + I_{S7}^2 R_{on,S7} + I_{S10}^2 R_{on,S10} \\
&\quad + I_{D}^2 R_{on,D} + I_{C1}^2 R_{ESR,C1} + I_{C2}^2 R_{ESR,C2}
\end{aligned} \tag{7}
$$

B. Switching Loss

The switching loss results from the simultaneous presence of voltage and current during the finite turn-on (T_{on}) and turn-off (T_{off}) intervals of the semiconductor devices. The energy that is dissipated during one switching transition can be approximated as (8),

$$E_{sw} = \frac{1}{6} V_D I_{peak} (T_{on} + T_{off}) \tag{8}$$

The individual turn-on and turn-off components are denoted as (9) and (10),

$$P_{on} = \frac{1}{6} V_D I_{peak} T_{on} f_{sw} \tag{9}$$

$$P_{off} = \frac{1}{6} V_D I_{peak} T_{off} f_{sw} \tag{10}$$

The total switching loss of the converter is consequently expressed as (11),

$$P_{sw,total} = \sum_{i=1}^{10} N_i \, P_{sw,i} \tag{11}$$

where N_i represents the effective number of switching transitions that the corresponding device experiences during one switching period.

C. Ripple Loss

When the capacitor voltage ripple is explicitly considered, the stored-energy variation can also be evaluated from (12),

$$\Delta E_C = C_1 \Delta V_{C1} + C_2 \Delta V_{C2} \tag{12}$$

Hence, the corresponding average ripple-related loss [33] may be obtained from the energy that is exchanged per cycle (13),

$$P_{ripple} = f_o \Delta E_C \tag{13}$$

where f_o is the fundamental output frequency.

Therefore, the total converter loss is obtained by combining the averaged conduction loss, the semiconductor switching loss and the capacitor ESR loss as (14),

$$P_{loss,total} = P_{cond} + P_{sw} + P_{ripple} \tag{14}$$

and the conversion efficiency is calculated as (15),

$$\eta = \frac{P_{out}}{P_{out} + P_{loss,total}} \times 100\% \tag{15}$$

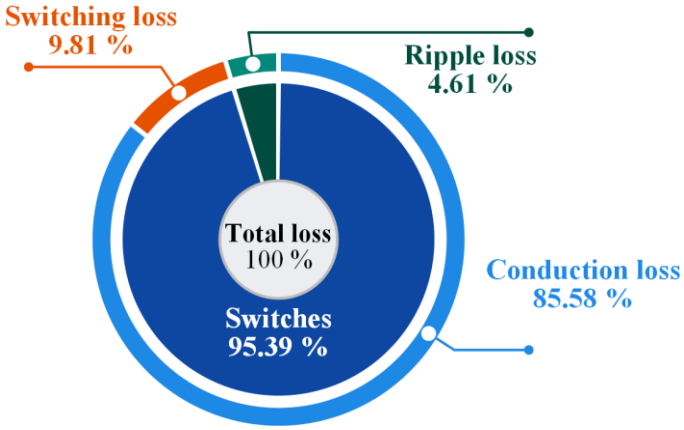


Fig. 6. Distribution of the analytical total power loss of the proposed inverter

The contribution of each loss to the total power dissipation at the rated output power of 750 W is shown in Fig. 6. The total loss at this operating point is 26.03 W. Conduction in the semiconductor devices is the largest contributor, at 22.27 W i.e., 85.58% of the total loss. This is to be expected, because in every output state the load current flows through five to seven series-connected devices, and the paths of the $\pm V_{dc}$ states, which carry the capacitor-charging current as well. Switching losses accounts for 2.55 W, i.e., 9.81% of the total loss. Most of it arises in the five switches that block $2V_{dc}$, since they commutate twice the voltage of the input-side switches. The remaining 1.20 W, or 4.61%, is the ripple loss related to the SCs C_1 and C_2 in every fundamental cycle.

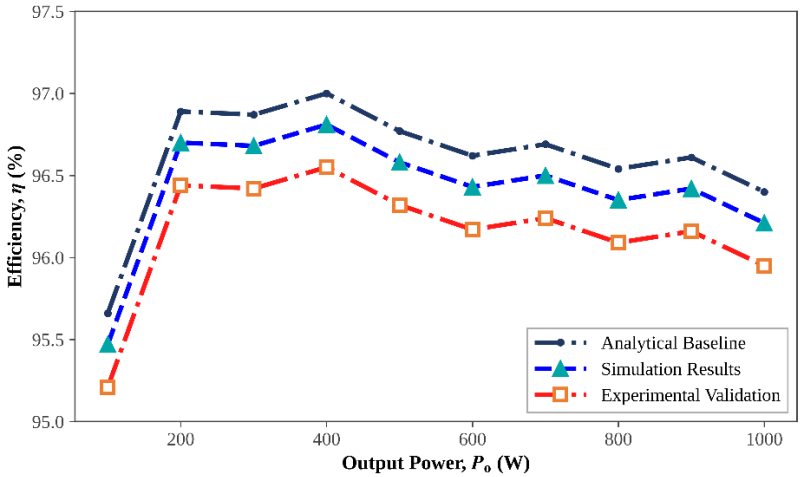


Fig. 7. Efficiency characteristics of the proposed converter under different output power levels

As observed in Fig. 7, the converter maintains an efficiency higher than 95% over the entire power range investigated. The efficiency rises from 100 W to 200 W and reaches its maximum of 97.00% at 400 W. Beyond this, the efficiency decreases gradually with increasing output power. It is approximately 96.6% at the rated power of 750 W. The lower efficiency at light load is mainly due to the nearly constant capacitor ripple loss and the switching loss, which form a larger fraction of the output power at low power levels. As the output current increases,

the semiconductor conduction loss becomes dominant. Since the conduction loss is approximately proportional to the square of the RMS current, its contribution becomes more significant at higher output power levels. The switching loss also contributes to the total loss and depends on the switching voltage, the current and the switching frequency. At lower power levels, the fixed and switching-related losses constitute a comparatively larger fraction of the output power, whereas at higher power levels the increase in conduction loss becomes more distinct. Nevertheless, the experimental efficiency of the proposed converter maintains to 96%, which demonstrates its suitability for medium-power applications. Thus, the efficiency characteristics validate the analytical power-loss evaluation and show that the converter maintains satisfactory energy-conversion performance over a broad operating range.

5. RELIABILITY ANALYSIS

Reliability is an important consideration in the design of power-electronic converters, particularly when the converter is intended for continuous operation. In the proposed converter, the reliability assessment is carried out at the component level with the MIL-HDBK-217 failure-rate approach [28]. The analysis considers the power switches, diode and the switched capacitors as the major components that contribute to the overall failure rate. The electrical losses are first determined for each component, followed by the estimation of the junction temperature and the corresponding reliability factors. The total failure rate and the mean time to failure (MTTF) are then obtained from the individual component failure rates.

A. Power Switches

The power losses of the individual switches are considered for the evaluation of their junction temperatures. The conduction loss of the i^{th} switch is determined from its RMS current and on-state resistance as,

$$\mathrm{P_{cond,i}} = \mathrm{I_{rms,i}^2 R_{DS(on),i}} \tag{16}$$

The switching loss is estimated from the voltage and current stresses during the turn-on and turn-off transitions. It is expressed as

$$\mathrm{P_{sw,i}} = \frac{\mathrm{V_{d,i} I_{d,pk,i} f_{sw}} \left(T_{\mathrm{on,i}} + T_{\mathrm{off,i}}\right)}{6} \times 10^{-9} \tag{17}$$

The total loss that is associated with each switch is consequently obtained as,

$$\mathrm{P_{loss,i}} = \mathrm{P_{cond,i}} + \mathrm{P_{sw,i}} \tag{18}$$

The power loss increases the semiconductor junction temperature and, consequently, influences its failure rate. The junction temperature is estimated from (19) as,

$$\mathrm{T_{J,i}} = \mathrm{T_A} + \mathrm{P_{loss,i}} \theta_{\mathrm{JC,i}} \tag{19}$$

where $\mathrm{T_A}$ is the ambient temperature and $\theta_{\mathrm{JC,\,i}}$ is the junction-to-case thermal resistance. The temperature factor that is used in the reliability calculation is given by (20),

$$\pi_{\mathrm{T,i}} = \exp\left[\frac{-2114}{\mathrm{T_{J,i}} + 273} + \frac{2114}{298}\right] \tag{20}$$

The failure rate of each switch is subsequently calculated as (21),

$$\lambda_{\mathrm{SW,i}} = \lambda_{\mathrm{BS}} \pi_{\mathrm{T,i}} \pi_{\mathrm{A}} \pi_{\mathrm{Q}} \pi_{\mathrm{E}} \tag{21}$$

where λ_{BS} denotes the base failure rate, and π_{A}, π_{Q} and π_{E} are the application, quality and environmental factors, respectively. The calculated failure rates of the ten switches are summed to obtain the total switch contribution (22),

$$\lambda_{\mathrm{SW}} = \sum_{\mathrm{i=1}}^{10} \lambda_{\mathrm{SW,i}} = 15.18586 \times 10^{-6} \text{ failures/h} \tag{22}$$

The obtained result shows that the switches account for the major portion of the calculated converter failure rate.

B. Diode

The proposed converter employs a single diode. The average current of the diode is calculated from

$$I_{D,avg} = \frac{2}{\pi} I_{D,pk} \tag{26}$$

The forward conduction loss is then determined as

$$P_F = V_F I_{D,avg}$$

The reverse-recovery loss is expressed as

$$P_{RR} = V_R Q_{RR} f_{sw} \tag{27}$$

where V_R is the reverse-voltage stress, Q_{RR} is the reverse-recovery charge and f_{sw} is the switching frequency. Therefore, the total diode power loss is

$$P_D = P_F + P_{RR}$$

$$P_D = 12.9267 \text{ W} \tag{28}$$

The thermal parameters of the selected diode are taken from the manufacturer's datasheet. The datasheet specifies a junction-to-case thermal resistance of 0.55 K/W and a case-to-heatsink thermal resistance of 0.3 K/W. The datasheet does not specify a sink-to-ambient thermal resistance θ_{SA}. Hence, no additional θ_{SA} value is introduced in the present calculation. The available thermal-resistance values are combined as (23),

$$\theta_{JC} + \theta_{CH} = 0.55 + 0.30 = 0.85 \text{ K/W} \tag{23}$$

The heatsink interface is considered to be approximately at the ambient temperature for the purpose of the present reliability estimation. Accordingly, the diode junction temperature is obtained from (24),

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CH}) \tag{24}$$

For an ambient temperature of 45 °C,

$$T_J = 45 + (12.9267)(0.85) = 55.99°\text{C}$$

The calculated junction temperature is well below the 175 °C maximum virtual junction temperature that is specified in the datasheet. The temperature factor for the diode is calculated as (25),

$$\pi_T = \exp\left[\frac{-3091}{T_J + 273} + \frac{3091}{298}\right] \tag{25}$$

Using T_J=55.99 °C gives

$$\pi_T = 2.6565$$

The voltage-stress factor is calculated from

$$\pi_S = \left(\frac{V_R}{V_{rated}}\right)^{2.43} \tag{26}$$

For V_R=125 V and V_{rated}=300 V,

$$\pi_S = \left(\frac{125}{300}\right)^{2.43} = 0.11915 \tag{27}$$

The resulting diode failure rate is

$$\lambda_D = \lambda_{BD}\pi_T\pi_S\pi_Q\pi_E$$

where $\lambda_{BD}=0.003\times10^{-6}$ failures/h, $\pi_Q=8$ and $\pi_E=1$. Thus,

$$\lambda_D = (0.003 \times 10^{-6})(2.6565)(0.11915)(8)(1) \quad (28)$$

$$\lambda_D = 0.007596 \times 10^{-6} \text{ failures/h} \quad (29)$$

Since only one diode is present in the proposed converter, this failure-rate contribution is included only once in the system reliability calculation.

C. Capacitor

The reliability of the switched capacitors is evaluated with the capacitance-dependent failure-rate factor. The capacitance factor is expressed as (30),

$$\pi_{CV} = 0.34\,C^{0.18} \quad (30)$$

For the SC C_1,

$$\pi_{CV1} = 0.10548$$

The corresponding failure rate is calculated as (31),

$$\lambda_{C1} = \lambda_{BC}\pi_{CV1}\pi_Q\pi_E = 0.05569 \times 10^{-6} \text{ failures/h} \quad (31)$$

Similarly, for SC C_2 the capacitance factor is

$$\pi_{CV2} = 0.10133$$

and the resulting failure rate is

$$\lambda_{C2} = 0.05350 \times 10^{-6} \text{ failures/h}$$

Hence, the combined capacitor contribution is calculated as,

$$\lambda_C = \lambda_{C1} + \lambda_{C2} = 0.10920 \times 10^{-6} \text{ failures/h}$$

By considering the independent failure of the individual components, the overall failure rate of the proposed converter is obtained from (32)

$$\lambda_{sys} = \lambda_{SW} + \lambda_D + \lambda_{C1} + \lambda_{C2} \quad (32)$$

Substituting the calculated component failure rates gives

$$\lambda_{sys} = (15.18586 + 0.007596 + 0.05569 + 0.05350) \times 10^{-6}$$

$$\lambda_{sys} = 15.30265 \times 10^{-6} \text{ failures/h} \quad (34)$$

The failure-rate contributions are summarized in Table II. The MTTF is calculated as (35),

$$\text{MTTF} = \frac{1}{\lambda_{sys}}$$

$$\text{MTTF} = 65348 \text{ h} \quad (35)$$

TABLE II
FAILURE-RATE CONTRIBUTIONS OF THE COMPONENTS OF THE PROPOSED INVERTER

Component	Number of devices	Failure rate ($\times10^{-6}$ failures/h)
Switches S_1–S_{10}	10	15.18586
Diode D	1	0.00760
Capacitor C_1	1	0.05569
Capacitor C_2	1	0.05350
Total converter (MTTF = 65348 h)	**13**	**15.30265**

For a constant failure-rate model, the reliability of the converter after an operating period t is expressed as (36),

$$R(t) = \exp(-\lambda_{sys} t)$$
$$R(t) = \exp[-15.30265 \times 10^{-6}\, t] \quad (36)$$

A lower total failure rate results in a slower reduction in reliability over time. Therefore, the reliability function R(t) = exp ($-\lambda_{sys}$ t) is used to compare the expected operating life of the inverters. Fig. 8(a) compares the reliability of the proposed inverter with the 7L inverters reported in [5]-[11]. Fig. 8(b) presents the corresponding MTTF values relative to that of the proposed inverter, providing a direct comparison of their expected operating life.

The proposed inverter maintains the highest reliability over the entire period. At 1×10^4 h, its reliability is 0.858, and it reaches 1/e at 65,348 h, which corresponds to its MTTF. The shaded region in Fig. 8(a) shows the reliability difference between the proposed inverter and the least reliable topology. This difference increases with operating time, indicating the benefit of a lower failure rate over a longer operating period. As shown in Fig. 8(b), the topologies in [8] and [7] have MTTF values closest to that of the proposed inverter, while [10] shows the largest difference.

The improved reliability is mainly related to the component count and device voltage stress. The proposed inverter does not use an inductor and requires only one diode. The diode operates at about 42% of its rated voltage and contributes only a small part of the total failure rate. The two capacitors contributed less than 1% of the total failure rate. As shown in Table II, the switches are the main contributors to λ_{sys}. However, the proposed inverter uses only ten switches, with a maximum blocking voltage of 2Vdc. These features reduce the overall failure rate and make the proposed inverter suitable for PV and other applications that require long-term continuous operation.

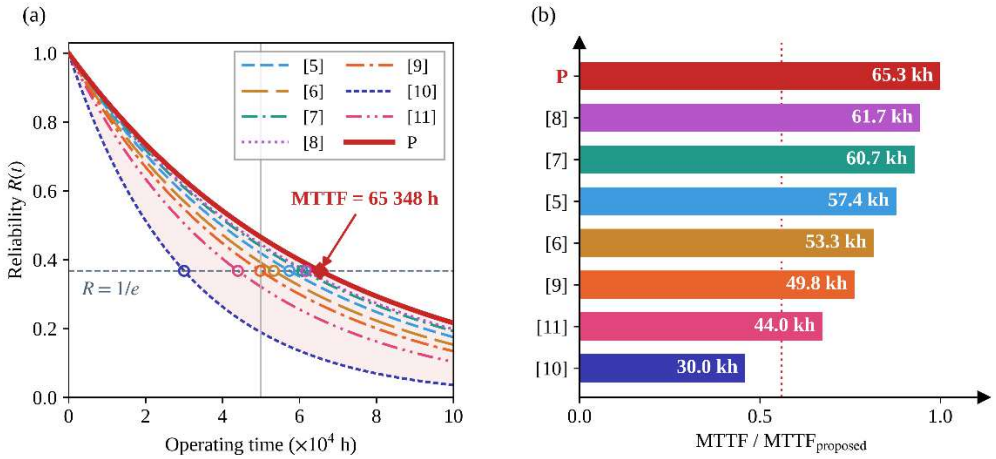


Fig. 8. Reliability comparison of the proposed inverter with the topologies in [5]-[11]: (a) reliability function R(t); (b) MTTF relative to that of the proposed inverter.

6. COMPARATIVE ANALYSIS WITH EXISTING 7L SC-MLIS

The proposed converter is compared with seven-level converters reported in the recent literature, [1]-[22], on the basis of the parameters summarized in Table III. In multilevel inverter design, an improvement in one figure of merit is frequently obtained at the expense of another: a reduced number of switches may require additional diodes, a lower capacitor count may sacrifice the common ground, and a high voltage gain may depend on an inductor. The evaluation is therefore performed across all parameters rather than on any single one. For every numerical parameter a lower value is preferable, with the exception of the boosting capability

β_g. Since β_g determines the minimum input voltage required by a converter, the references are classified according to their gain. Topologies [1]-[4] provide $\beta_g = 1.5$, [13] provides $\beta_g = 4$ and [6] provides $\beta_g = 6$. The remaining sixteen topologies, [5], [7]-[12] and [14]-[22], provide $\beta_g = 3$, identical to that of the proposed inverter, and therefore form the most direct basis for comparison.

A. Component Count

The proposed inverter achieves $\beta g = 3$ using $Q_{tot} = 10$, $G_{drv} = 10$, $C_{tot} = 2$, $D_{tot} = 1$, and $L_{tot} = 0$. Among the topologies with the same voltage gain, [5], [9], [11], [12], and [14] require more switches. In particular, [11] and [12] use fifteen and fourteen switches, respectively, while [8] and [15] use the same number of switches as the proposed inverter. Topologies [3] and [4] also use ten switches, but their voltage gain is limited to 1.5. Therefore, the proposed inverter provides twice the voltage gain with the same switch count.

A lower switch count is reported in [1], [2], [7], [10], and [16]-[22], but with some limitations. Topologies [1] and [2] provide a lower voltage gain, while [16]-[22] do not provide a common ground. Topologies [7] and [10] provide both $\beta g = 3$ and common-ground operation, but they require three diodes and have a maximum switch blocking voltage of 3Vdc. In most of the compared topologies, the number of gate drivers is equal to the number of switches. The exceptions are [14], which uses eleven gate drivers for twelve switches, and [22], which uses four gate drivers but does not provide a common ground.

Only [6] and [13] provide a voltage gain higher than that of the proposed inverter. However, [6] requires twelve switches, three capacitors, and one inductor, while [13] requires twelve switches and four capacitors and does not provide a common ground. Overall, the proposed inverter provides a good balance between voltage gain, component count, common-ground operation, and device voltage stress.

For the passive components, [1], [3]-[6], [9]-[11], [13], and [16] require more capacitors than the proposed inverter. Topology [15] uses only one capacitor, but it requires one inductor, has a maximum switch blocking voltage of 3Vdc, and has no common ground. Topologies [2], [7], [8], [12], [14], and [17]-[22] use two capacitors, the same as the proposed inverter. Among them, only [7] and [8] provide a common ground.

A higher diode count is required in [1], [4]-[7], [10], [16], [17], [21], and [22]. Topologies [8] and [18]-[20] use one diode, similar to the proposed inverter. Topologies [2], [3], [9], and [11]-[15] do not use any diodes, but they have other limitations. Topologies [2] and [3] have a lower voltage gain, [9] and [11] require twelve and fifteen switches, respectively, [12]-[14] do not provide a common ground, and [15] requires an inductor. Among the compared topologies, only [6] and [15] use an inductor. Therefore, the proposed inverter avoids the additional size, copper loss, and electromagnetic interference associated with magnetic components.

The proposed inverter has a total device count of NE = 23. A lower N_E is reported in [2], [15], and [18]-[22]. However, [2] has a lower voltage gain, [15] requires an inductor, and [18]-[22] do not provide a common ground. Topologies [1], [3], [7], [8], and [16] have the same N_E as the proposed inverter, while [4]-[6], [9]-[14], and [17] require more devices. The proposed inverter has a device-to-level ratio of $R_{dev/lev} = 1.85$. A lower value is reported only in [2], [15], [18]-[20], and [22], while [3], [8], and [21] have the same value. All the other compared topologies have a higher device-to-level ratio.

B. Voltage Stress

In the proposed inverter, capacitor C_1 is charged to V_{dc} and C_2 to $2V_{dc}$. The proposed inverter therefore does not offer the lowest capacitor voltage stress. Most of the referenced topologies limit their capacitor voltages to V_{dc} or less, [6], [7], [8], [13], [15] and [20] also reach $2V_{dc}$, and only [10] reaches $3V_{dc}$. The $2V_{dc}$ level across C_2 is intentional, since it enables $\beta_g = 3$ with only

two capacitors, and its benefit is reflected in the reduced switch stress examined below. The capacitor voltage diversity factor of the proposed inverter, $\sigma_{df} = 1$, is equal to that of [5]-[9], [11], [16] and [20], and lower than that of [1], [3], [4], [10] and [13]. A lower σ_{df} is obtained by [2], [12], [14], [15], [17]-[19], [21] and [22]. Of these, [2] has a low β_g, and the remaining topologies lack a common ground. The maximum blocking voltage of the proposed inverter is $V_{blk,\,max} = 2V_{dc}$. Lower values are found in [1]-[4], [11] and [12]. Of these, [1]-[4] provide $\beta_g = 1.5$ only, while [11] and [12] require $Q_{tot} = 15$ and 14, respectively. Topologies [8], [9] and [14] have the same $V_{blk,\,max}$, whereas the switches of all remaining topologies, [5]-[7], [10], [13] and [15]-[22], are subjected to a higher blocking voltage. When $V_{blk,\,max}$ is normalised by β_g, the proposed inverter attains $\rho_{MG} = 0.66$, a value equal to or lower than that of every reference except [11] and [12], both of which require a considerably larger Q_{tot}. The per-unit total standing voltage expresses the cumulative voltage stress of all switches as a single quantity. With $TSV_u = 5$, the proposed inverter performs better than [3], [4], [6]-[10], [13]-[15] and [17]-[22], and equals [2], [5] and [11]. Among the latter, [2] provides half the gain, [5] requires $Q_{tot} = 11$, $D_{tot} = 3$ and $V_{blk,\,max} = 3V_{dc}$, and [11] requires $Q_{tot} = 15$. Only [1], [12] and [16] exhibit a lower TSV_u; however, [1] provides half the gain, while [12] and [16] do not offer a common ground.

TABLE III
COMPARISON OF THE PROPOSED INVERTER WITH EXISTING SEVEN-LEVEL INVERTERS

Ref.	Q_{tot}	G_{drv}	C_{tot}	D_{tot}	L_{tot}	N_E	$R_{dev/lev}$	σ_{df}	$V_{blk,max}$	ρ_{MG}	TSV_u	β_g	ψ_{cf}		S_G	IT	CG
													$\alpha = 0.5$	$\alpha = 1.5$			
[1]	8	8	3	4	0	23	2.14	1.33	1	0.66	4.33	1.5	3.6	4.21	5.33	ANPC	No
[2]	9	9	2	0	0	20	1.57	0.66	1.5	1	5	1.5	3.21	3.93	6	SC	No
[3]	10	10	3	0	0	23	1.85	1.33	1	0.66	5.3	1.5	3.66	4.42	6.66	SC	No
[4]	10	10	3	2	0	25	2.14	1.33	1	0.66	6.2	1.5	4.01	4.9	6.66	ANPC	No
[5]	11	11	3	3	0	28	2.42	1	3	1	5	3	4.35	5.07	3.66	SC	Yes
[6]	12	12	3	2	1	30	2.57	1	4	0.66	5.33	6	4.52	5.28	2	SC	Yes
[7]	9	9	2	3	0	23	2	1	3	1	6.67	3	3.76	4.71	3	SC	Yes
[8]	10	10	2	1	0	23	1.85	1	2	0.66	6	3	3.71	4.57	3.33	SC	Yes
[9]	12	12	3	0	0	27	2.14	1	2	0.66	5.67	3	4.26	5.07	4	SC	Yes
[10]	9	9	3	3	0	24	2.14	2	3	1	6.67	3	3.9	4.85	3	SC	Yes
[11]	15	15	3	0	0	33	2.57	1	1	0.33	5	3	5.07	5.79	5	SC	Yes
[12]	14	14	2	0	0	30	2.28	0.66	1	0.33	4.66	3	4.62	5.29	4.67	SC	No
[13]	12	12	4	0	0	28	2.28	1.5	4	1	5.5	4	4.39	5.17	3	SC	No
[14]	12	11	2	0	0	25	2	0.66	2	0.66	5.3	3	3.95	4.7	4	SC	No
[15]	10	10	1	0	1	22	1.71	0.66	3	1	6.6	3	3.47	4.41	3.33	SC	No
[16]	9	9	3	2	0	23	2	1	3	1	4.33	3	3.59	4.21	3	SC	No
[17]	9	9	2	4	0	24	2.14	0.66	3	1	5.66	3	3.83	4.64	3	SC	No
[18]	8	8	2	1	0	19	1.57	0.66	3	1	5.66	3	3.11	3.92	2.66	SC	No
[19]	8	8	2	1	0	19	1.57	0.66	3	1	6.66	3	3.19	4.14	2.66	SC	No
[20]	8	8	2	1	0	19	1.57	1	3	1	5.66	3	3.11	3.92	2.66	SC	No
[21]	8	8	2	3	0	21	1.85	0.66	3	1	6	3	3.42	4.28	2.66	SC	No
[22]	8	4	2	2	0	16	1.71	0.66	3	1	5.33	3	2.66	3.42	2.66	SC	No
[P]	**10**	**10**	**2**	**1**	**0**	**23**	**1.85**	**1**	**2**	**0.66**	**5**	**3**	**3.64**	**4.35**	**3.33**	**SC**	**Yes**

Q_{tot}: switches; G_{drv}: gate drivers; C_{tot}: capacitors; D_{tot}: diodes; L_{tot}: inductors; N_E: total device count; $R_{dev/lev}$: device-to-level ratio; σ_{df}: capacitor voltage diversity factor; $V_{blk,max}$: maximum blocking voltage ($\times V_{dc}$); ρ_{MG}: MBV-to-gain ratio; TSV_u: per-unit total standing voltage; β_g: boosting capability; ψ_{cf}: cost function (inductors excluded from N_E); S_G: switches-per-gain ratio; IT: inverter topology; CG: common ground; SC: switched capacitor; ANPC: active neutral-point-clamped.

C. Cost Effectiveness, Topology Class and Grounding

The switches-per-gain ratio of the proposed inverter, $S_G = 3.33$, is lower than that of [1]-[5], [9], [11], [12] and [14], and equal to that of [8] and [15]. A lower S_G is obtained by [6], [7], [10], [13] and [16]-[22], each subject to a specific limitation. Topology [6] requires an inductor and $V_{blk,\,max} = 4V_{dc}$; [7] and [10] require $D_{tot} = 3$ and $V_{blk,\,max} = 3V_{dc}$; [13] employs $C_{tot} = 4$; and [13] and [16]-[22] lack a common ground.

The cost function is evaluated as $\psi_{cf} = (N_E + \alpha \cdot TSV_u)/N_L$, where N_L is the number of output levels and α is a weighting factor. The proposed inverter yields $\psi_{cf} = 3.64$ for $\alpha = 0.5$ and $\psi_{cf} = 4.35$ for $\alpha = 1.5$. These values are lower than those of [3]-[14] and [17] for both weighting factors, and lower than that of [15] for $\alpha = 1.5$. A lower ψ_{cf} is obtained only by [1], [2], [16] and [18]-[22] for both weighting factors, and by [15] for $\alpha = 0.5$. Of these, [1] and [2] provide a low β_g, whereas [15], [16] and [18]-[22] lack a common ground. With respect to the inverter topology (IT), twenty-one of the twenty-three circuits in Table III are switched-capacitor (SC) structures, whereas [1] and [4] are derived from the active neutral-point-clamped (ANPC) cell. A common ground (CG) between the source and the load is available only in [5]-[11] and in the proposed inverter. In transformerless grid-connected photovoltaic systems, this feature suppresses the leakage current that flows through the parasitic capacitance of the PV array; topologies [5]-[11] are therefore the most relevant for comparison. Within this group, the proposed inverter shares the lowest N_E with [7] and [8], the lowest $R_{dev/lev}$ with [8] and the lowest TSV_u with [5] and [11]. It also attains the lowest ψ_{cf} for both values of α and imposes a lower $V_{blk,\,max}$ than [5], [6], [7] and [10]. Topology [8] is the most comparable design, with the same Q_{tot}, C_{tot}, D_{tot}, β_g, $V_{blk,\,max}$ and capacitor voltage levels. It differs from the proposed inverter only in its higher TSV_u (6 against 5) and higher ψ_{cf} (3.71 and 4.57 against 3.64 and 4.35 for $\alpha = 0.5$ and 1.5, respectively). On this basis, the proposed inverter offers the lowest overall cost among the common-ground topologies considered.

TABLE IV
CATALOGUE OF CANDIDATE COMPONENTS WITH CODE DESIGNATIONS

Function	Part number	Package	Rating	Unit price ($)	Unit volume (cm^3)
Power MOSFET	STF40NF20	TO-220	200 V / 40 A	3.34	1.46
	SIHP065N60E-BE3	TO-220	600 V / 40 A	4.10	0.77
Gate driver	HCPL-3120	—	—	3.55	0.35
Diode	MBR40250G	TO-220	250 V / 40 A	3.05	0.78
	MUR4040	TO-247	400 V / 40 A	3.51	1.78
Heat sink	WA-T220-101E	for TO-220	—	3.33	8.90
	WA-T247-101E	for TO-247	—	4.02	11.90
DC-link / switched capacitor	MAL226932152E3	—	1.5 mF / 200 V	5.69	35.5
	LLS2D222MELC	—	2.2 mF / 200 V	10.12	43.2
	380LX122M400A082	—	1.2 mF / 400 V	14.76	76.9
	ALC70C272FP400	—	2.7 mF / 400 V	34.80	166.8

D. Cost and Size Assessment of The Compared Inverters

Counting switches, diodes and capacitors gives only a first impression of what an inverter will cost. Once each part is assigned a real voltage rating, package and capacitance, two circuits with a similar part count can differ widely in price and in size. The comparison in this section is therefore based on an actual component selection, following the cost-and-size procedure proposed in [30] and its use for seven-level switched-capacitor inverters in [31]. All seven

inverters are designed for the same voltage gain of three and the same output power of about 750 W. Each one is assembled only from the commercial parts in Table IV, and every discrete semiconductor is mounted on its own heat sink sized for its package. Because the same part families, voltage margins and cooling arrangement are applied to every circuit, the differences that remain come from the topologies themselves [30].

Table IV lists the parts from which every inverter is built, together with the code used for each part in Table V. Three MOSFET classes are available, rated at 200 V, 600 V and 800 V, so that every switch can be matched to the highest voltage it must block. With V_{dc} = 125 V, the 200 V device S_1 suits switches that block V_{dc}, and the 600 V device S_2 suits those that block $2V_{dc}$ or $3V_{dc}$. A separate isolated gate driver (HCPL-3120) is allotted to every switch, so the driver count of each circuit is equal to its switch count. The diode and heat-sink choices follow the package: TO-220 devices sit on the WA-T220-101E heat sink, and TO-247 devices on the larger WA-T247-101E. The capacitors show the largest spread of all the part groups. The 2.7 mF / 400 V unit (C_4) costs 34.80 $ and occupies 166.8 cm^3, close to four times the volume of the 2.2 mF / 200 V unit (C_2) and more than twice that of the 1.2 mF / 400 V unit (C_3). A circuit whose capacitors must hold $2V_{dc}$ or $3V_{dc}$, or must be large to limit the voltage ripple, therefore pays heavily in both cost and volume. This is especially true for switched-capacitor boosting inverters, where the capacitors must also carry the charging current spikes that occur when they are connected in parallel with the source [32].

TABLE V
NUMBER OF UNITS OF EACH COMPONENT REQUIRED BY THE COMPARED INVERTERS

Inverter	Switches		Driver	Diodes		Heat sinks		Capacitors				Switches / Total devices
	S_1 (V_{dc})	S_2 ($2V_{dc}$/$3V_{dc}$)	G	D_1	D_2	H_1	H_2	C_1 (V_{dc})	C_2 (V_{dc})	C_3 ($2V_{dc}$)	C_4 ($2V_{dc}$/$3V_{dc}$)	
[5]	7	4	11	1	2	12	2	3	–	–	–	11 / 14
[7]	2	7	9	–	–	9	–	–	1	–	1	9 / 9
[8]	4	6	10	1	–	11	–	–	1	–	1	10 / 11
[9]	7	5	12	1	1	13	1	–	3	–	–	12 / 14
[10]	6	3	9	2	1	11	1	–	1	–	2	9 / 12
[11]	15	–	15	–	–	15	–	1	2	–	–	15 / 15
[P]	**5**	**5**	**10**	**1**	**–**	**11**	**–**	**1**	**–**	**1**	**–**	**10 / 11**

TABLE VI
COST BREAKDOWN, VOLUME AND FIGURES OF MERIT OF THE COMPARED INVERTERS

Inverter	Group cost ($)				Total cost ($)		Size			Cost-based indices		Size index	
	Switch + driver	Diode	Heat sink	Capacitor	incl. HS	excl. HS	Volume (cm^3)	ρ incl. HS (W/cm^3)	ρ excl. HS (W/cm^3)	FGC	SGC	ISGC	ISGS
[5]	78.83	10.07	48.00	17.07	154	106	258.6	2.90	5.86	0.019	1.16	−0.34	−0.12
[7]	67.33	–	29.97	44.92	142	112	301.6	2.49	3.37	0.021	1.07	−0.15	−0.27
[8]	73.46	3.05	36.63	44.92	158	121	322.6	2.32	3.34	0.019	1.19	−0.41	−0.35
[9]	86.48	6.56	47.31	30.36	171	123	278.0	2.70	4.99	0.018	1.29	−0.62	−0.19
[10]	64.29	9.61	40.65	79.72	194	154	504.2	1.49	1.90	0.015	1.46	−1.00	−1.00
[11]	103.35	–	49.95	25.93	179	129	282.5	2.65	5.03	0.017	1.35	−0.75	−0.20
[P]	**72.70**	**3.05**	**36.63**	**20.45**	**133**	**96**	**225.7**	**3.32**	**5.87**	**0.023**	**1.00**	**0.00**	**0.00**

HS: heat sink; ρ: power density at 750 W; FGC: fractional gain–cost; SGC: subtractive gain–cost; ISGC: improved subtractive gain–cost; ISGS: improved subtractive gain–size. Group cost = quantity (Table V) × unit price (Table IV).

Table V gives the number of units of each coded part in every inverter. Two relations can be used to check each row: the number of gate drivers equals the number of switches ($G = S_1 + S_2$), and the number of heat sinks equals the number of switches plus diodes ($H_1 + H_2$). The proposed inverter [P] needs ten switches (five S_1 and five S_2), ten gate drivers, one diode, eleven TO-220 heat sinks and just two capacitors: a 1.5 mF / 200 V unit (C_1) for the V_{dc} level and a 1.2 mF / 400 V unit (C_3) for the higher level. On part count alone, [P] is not the leanest design. Inverters [7] and [10] manage with nine switches, while [11] needs fifteen, all of the 200 V class. The strength of [P] lies in the ratings rather than the numbers. It uses a single low-voltage diode, needs no TO-247 part and so no large heat sink, and is the only circuit that does without the bulky C_4. Its high-voltage capacitor is the smaller C_3, whereas [7] and [8] each use one C_4 and [10] uses two. Each group cost in Table VI is found by multiplying the unit count in Table V by the unit price in Table IV. For [P], for example, the switches and drivers cost $5 \times 3.34 + 5 \times 4.10 + 10 \times 3.55 = 72.70$ \$. In six of the seven circuits, the switches and their drivers form the largest cost group; only in [10] do the capacitors cost more (79.72 \$ against 64.29 \$). The cheapest switch-and-driver set belongs to [10] (64.29 \$), followed by [7] (67.33 \$) and then [P] (72.70 \$), while [11] reaches 103.35 \$ because of its fifteen switches and drivers. The diodes add no more than about 10 \$ to any design. The heat sinks account for 21 % to 31 % of the total price, so the cooling hardware clearly has to be included when topologies are ranked by cost. The capacitor cost varies the most, from 17.07 \$ in [5] to 79.72 \$ in [10]. When all the groups are summed, [P] has the lowest total cost, both with heat sinks (133 \$) and without them (96 \$). With heat sinks, the next cheapest circuit is [7] at 142 \$, and the most expensive is [10] at 194 \$. The proposed inverter is therefore about 6 % cheaper than its closest competitor and about 31 % cheaper than the costliest one. This result does not come from a single part group. In each group, [P] stays near the lowest value and avoids the expensive items, such as C_4 or a long chain of switches, that raise the totals of the other circuits. The volume in Table VI is the sum of the volumes of all the parts. The switches, diodes and drivers together occupy less than 10 % of the volume in every design; almost all the space is taken by the heat sinks and the capacitors. This is why [10] is by far the largest circuit, at 504.2 cm^3: its two C_4 capacitors alone take up 333.6 cm^3. The proposed inverter needs 225.7 cm^3, which is 12.7 % less than [5], the next most compact design, and about 55 % less than [10]. At the same output power, this gives [P] the highest power density [35], 3.32 W/cm^3 with heat sinks and 5.87 W/cm^3 without them. Without heat sinks, [5] is almost level with [P] (5.86 W/cm^3). Once cooling is counted, [P] moves clearly ahead because it needs eleven heat sinks, while [5] needs fourteen, two of them of the larger TO-247 type.

E. Gain-Based Cost and Size Indices

A lower price or a smaller volume means little unless it is set against what the circuit delivers. For this reason, the cost and the volume are combined with the voltage gain G through the indices defined in [30]:

$$F_{GC} = \frac{\alpha_G G}{\alpha_C C} \tag{37}$$

$$S_{GC} = \frac{C}{C_P} \tag{38}$$

$$ISG_C = \frac{\alpha_G (G - G_{min})}{G_{max} - G_{min}} - \frac{\alpha_C (C - C_{min})}{C_{max} - C_{\min}} \tag{39}$$

$$ISG_S = \frac{\alpha_G (G - G_{min})}{G_{max} - G_{min}} - \frac{\alpha_S (S - S_{min})}{S_{max} - S_{min}} \tag{40}$$

Here C is the total cost including heat sinks, S is the total volume and C_P is the cost of the proposed inverter, which serves as the reference for SGC. The minimum and maximum values are taken over the seven compared inverters, and all weight factors are set to $\alpha_G = \alpha_C = \alpha_S = 1$,

as in [31]. Since every circuit has the same gain of three, the gain term is zero for all of them. ISGC is then decided by cost alone and ISGS by volume alone. With this scaling, the cheapest or smallest circuit scores 0 and the costliest or largest scores -1, so values nearer to zero are better [30], [31]. The proposed inverter obtains the best value under every index: the highest FGC (0.023), the reference SGC of 1.00, and ISGC = ISGS = 0. The SGC of the other designs lies between 1.07 for [7] and 1.46 for [10], meaning that they cost 7 % to 46 % more than [P]. At the other extreme, [10] has the lowest FGC (0.015) and scores −1 on both ISGC and ISGS. The two improved indices do not rank the remaining circuits in the same order. Inverter [7] is second on cost (ISGC = -0.15) but only fifth on size (ISGS = -0.27), whereas [5] is second on size (ISGS = -0.12) but third on cost (ISGC = -0.34). This agrees with the observation in [30] that each index weights a design differently, so cost and size should both be examined before a topology is chosen for a given application. Of the seven circuits, only the proposed inverter ranks first under all of these measures. Fig. 9 shows the comparison of the proposed inverter with the inverters proposed in [5] and [7]-[11] on seven parameters: the maximum blocking voltage $V_{\mathrm{blk,\,max}}$, the device-to-level ratio $R_{\mathrm{dev/lev}}$, the cost function ψ_{cf} for $\alpha = 0.5$ and $\alpha = 1.5$, the power density including heat sinks PD_{hs}, the total device count N_{E} and the total cost including heat sinks TC_{hs}. Each axis is normalised to the largest value among the circuits, so that all quantities share one scale from 0 to 1. For every parameter except the power density a smaller value is preferable, so the power-density axis is inverted and a higher density is plotted closer to the centre. In this form, a circuit that performs well encloses a small area around the centre of the chart.

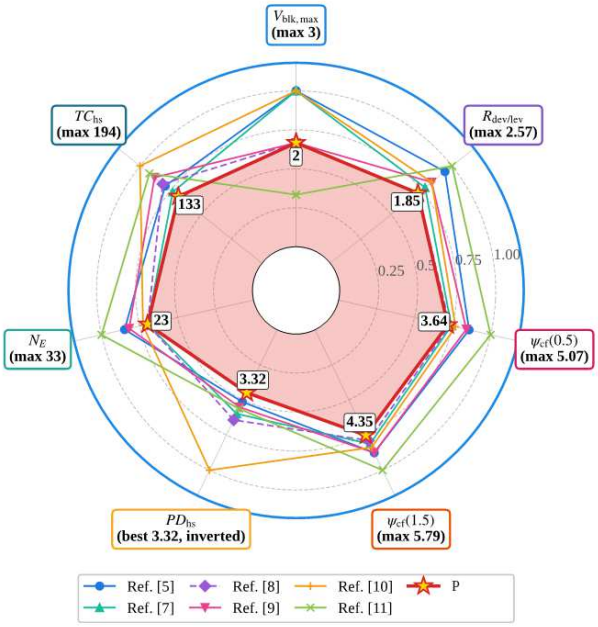


Fig. 9. Normalized multi-parameter comparison radar chart of the proposed inverter with the common-ground topologies [5] and [7]-[11]; a smaller enclosed area indicates better overall performance.

The proposed ten switch converter has the lowest cost function at both weighting factors (3.64 and 4.35), the lowest total cost (133 $) and the highest power density (3.32 W/cm^3), and it shares the lowest device-to-level ratio (1.85) with [8] and the lowest device count (23) with [7] and [8]. The only axis on which it does not lead is $V_{\mathrm{blk,\,max}}$: [11] limits the blocking voltage of its switches to V_{dc}, whereas the proposed circuit reaches $2V_{\mathrm{dc}}$, the same value as [8] and [9]. However, [11] needs fifteen switches to achieve this, which places it at the outer edge of the chart for device count and cost function. The chart also shows why a single index is not enough to rank topologies. Inverter [10], for example, is competitive in device count but has the lowest power density and the highest cost, and [11] avoids diodes but has the largest cost function and

device count. The proposed inverter is the only circuit that stays close to the centre on all axes at the same time, which confirms the balanced advantage indicated by Tables IV-VI.

7. RESULTS AND DISCUSSION

A. Simulation Results

The proposed seven-level boost inverter was modelled in MATLAB/Simulink and evaluated at a power rating of 750 W. Its steady-state and dynamic behaviour was examined under resistive and inductive loading, a step change in the dc input voltage, a sudden change in load, and a stepwise variation of the modulation index. The voltage stress imposed on each switch is also presented to validate the analysis of Section II-D.

Fig. 10 presents the steady-state waveforms of the proposed inverter supplying an 80-Ω resistive load from a 125-V dc source. The output voltage in Fig. 10(a) is a symmetrical seven-level staircase with levels of $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$ and 0. Its peak therefore equals three times the input voltage. This gain comes solely from the switched-capacitor cells, without a front-end dc-dc converter or a step-up transformer. Since the load is resistive, the load current in Fig. 10(d) follows the stepped shape of the output voltage, remains in phase with it and reaches a peak of about 4.2 A. Fig. 10(b) and (c) show the voltages across C_1 and C_2. Both remain at their nominal values over the entire interval: V_{C1} settles near the input voltage and V_{C2} near twice the input voltage. Each capacitor charges while it is connected in parallel with the source and discharges slowly while it feeds the load. This leaves a small ripple at the fundamental frequency. The corresponding capacitor currents are given in Fig. 10(e) and (f). The current of C_1 is bipolar, with a sharp charging pulse and a discharge interval in every cycle. In contrast, the current of C_2 consists of short charging pulses separated by a low, almost constant discharge current. With the inductor L placed in the charging path, the peak of these pulses is considerably lower than without it. Over one fundamental period, the mean current of each capacitor is zero, so the charge each capacitor absorbs equals the charge it releases. As a result, the capacitor voltages balance inherently, and neither voltage sensors nor an auxiliary balancing loop is required.

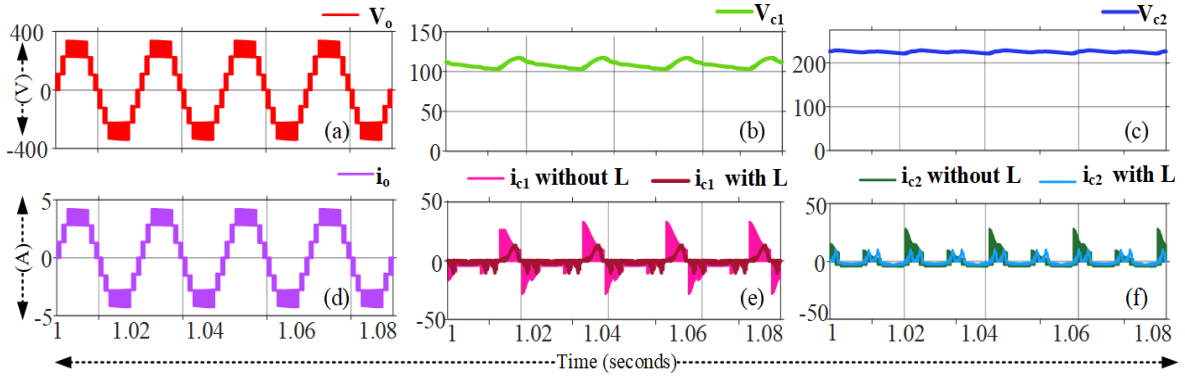


Fig. 10. Simulated waveforms with an 80-Ω resistive load: (a) output voltage V_o; (b) capacitor voltage V_{C1}; (c) capacitor voltage V_{C2}; (d) load current i_o; (e) capacitor current i_{C1} with and without inductor L; (f) capacitor current i_{C2} with and without inductor L.

To examine operation at lagging power factor, the inverter was tested with an RL load of $82 + j100$ Ω. The output voltage in Fig. 11(a) keeps its seven-level staircase shape, because the levels are set by the switching sequence and do not depend on the load. The load inductance suppresses the higher-order harmonics, so the load current becomes almost sinusoidal and lags the output voltage. Around each zero crossing, the output voltage and the load current have opposite polarities for a short interval. During this interval, the inductive current freewheels through the bidirectional conduction paths provided by the switches, and the voltage levels remain undistorted. The capacitor voltages in Fig. 11(b) and the capacitor currents in Fig. 11(c)

show the same behavior as under the resistive load: V_{C1} and V_{C2} stay close to their nominal values, and charge balance of both capacitors is preserved at reduced power factor.

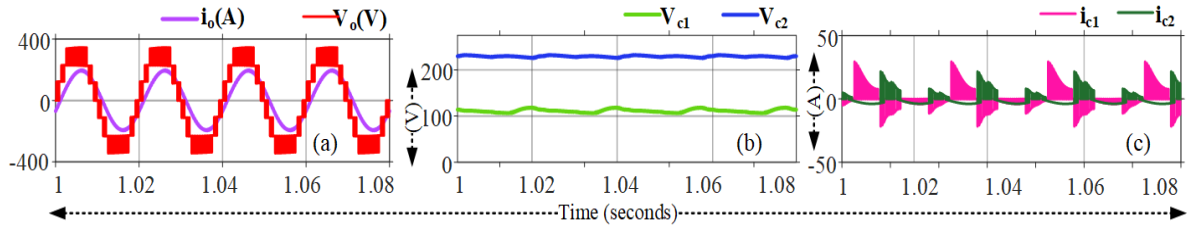


Fig. 11. Simulated waveforms under an RL load of 82 + j100 Ω: (a) output voltage V_o and load current i_o; (b) capacitor voltages V_{C1} and V_{C2}; (c) capacitor currents i_{C1} and i_{C2}.

Fig. 12 shows the response of the inverter when the dc input is reduced from 125 V to 100 V. After the step, the capacitor voltages move to the new operating point within a few fundamental cycles, and C_2 continues to hold twice the voltage of C_1. The output voltage keeps all seven levels while its amplitude decreases in proportion to the input, so the voltage gain of the topology is unaffected. The load current reduces in the same proportion and settles without noticeable overshoot or sustained oscillation. This confirms that the switched-capacitor stage tracks variations in the source voltage with no modification to the control scheme.

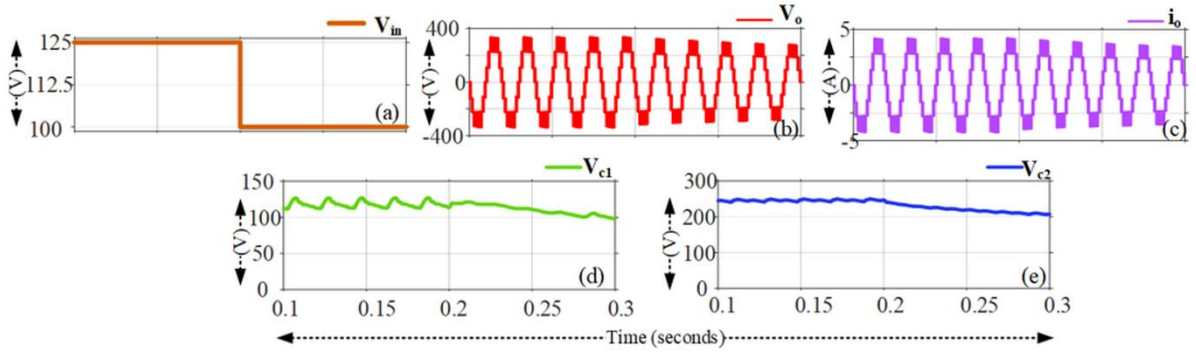


Fig. 12. Dynamic response to a step change in input voltage from 125 V to 100 V: (a) V_{in}, (b) V_o, (c) i_o, (d) V_{C1}, (e) V_{C2}.

Fig. 13 illustrates the behaviour of the inverter when the load changes suddenly from resistive to inductive and is subsequently restored to purely resistive. Under the resistive load, the load current follows the stepped profile of the output voltage and is in phase with it. When the inductive element is connected, the current changes to a smooth sinusoidal shape and lags the output voltage, since the load inductance filters the higher-order harmonics. Once the resistive load is restored, the current returns to its in-phase stepped form within the same fundamental cycle. Throughout both transitions, the output voltage keeps all seven levels without visible distortion. The capacitor voltages change only slightly during the RL interval and return to their earlier levels once the resistive load is restored. These results confirm that the inverter handles abrupt changes in load impedance while preserving output voltage quality and capacitor voltage balance.

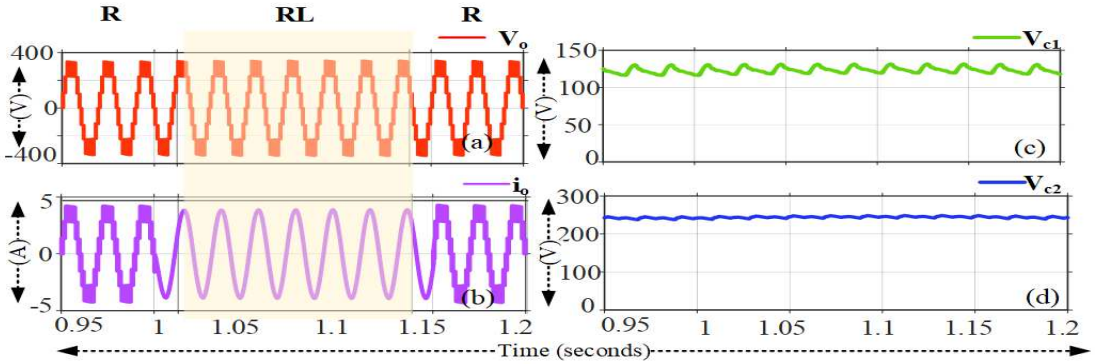


Fig. 13. Dynamic response to load change from R to RL and back to R: (a) V_o, (b) i_o, (c) V_{C1}, (d) V_{C2}.

The dynamic response of the inverter to changes in modulation index (MI) is shown in Fig. 14. MI was stepped down from 1 to 0.65, then to 0.5 and finally to 0.45. At MI = 1, the output voltage in Fig. 14(a) is a full seven-level staircase. When MI is reduced to 0.65, the outer levels are no longer reached and the output changes to a five-level waveform; the same five-level profile is retained at MI = 0.5 and 0.45 with a lower fundamental component. The change from one operating point to the next takes place within one cycle, without overshoot at the step instants. The load current in Fig. 14(b) settles to its new amplitude within about one cycle after each change in MI and remains nearly sinusoidal throughout. The peak current decreases as MI is reduced from 1 to 0.45, tracking the reduction in MI. These results confirm that the output voltage and load current can be regulated over a wide range simply by adjusting MI.

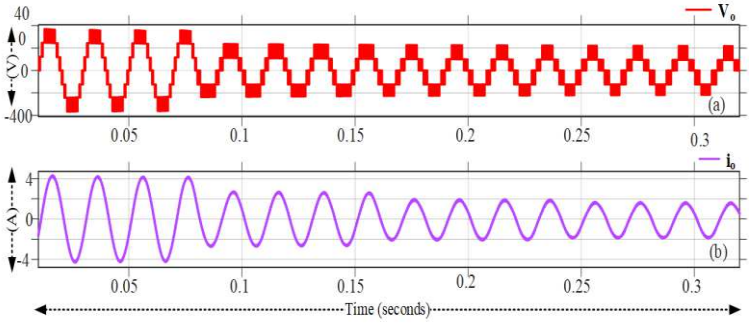


Fig. 14. Performance under stepwise modulation index variation (M_a = 1, 0.65, 0.5, 0.45): a) output voltage V_o, b) load current i_o.

The simulated blocking voltage across each of the ten switches is shown in Fig. 15. Switches S_1, S_2, S_3, S_4 and S_6 block a voltage equal to the dc input, whereas S_5, S_7, S_8, S_9 and S_{10} block twice the dc input. None of the switches is exposed to the peak output voltage, although the output reaches three times the input. The traces of S_5 and S_8 also contain an intermediate step at V_{dc}, because in some states only part of the C_2 voltage appears across them; their peak nevertheless remains $2V_{dc}$. These results agree with the stress distribution derived in Section II-D and plotted in Fig. 3, and confirm that the proposed topology can be realised with lower-rated semiconductor devices, which reduces conduction and switching losses as well as the cost of the converter.

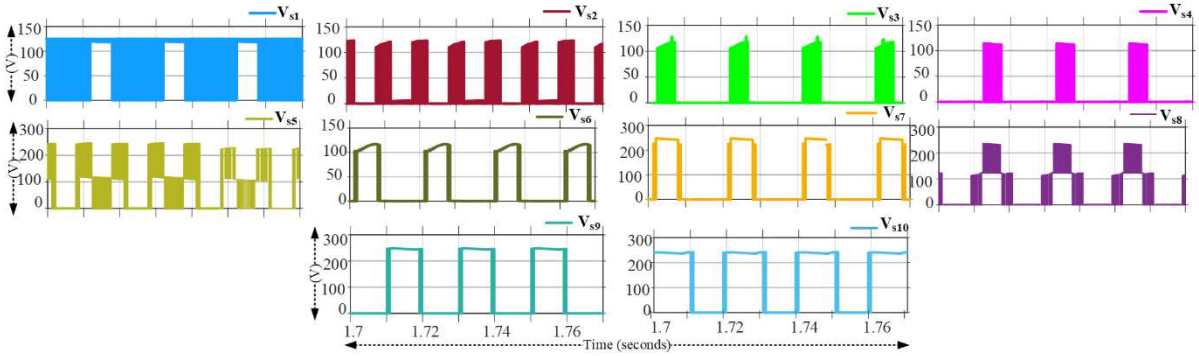


Fig. 15. Simulated voltage stress across switches S_1–S_{10}.

B. Experimental Results

A prototype of the proposed seven-level inverter was built to validate its operation. The parameters of the prototype are listed in Table VII. The waveforms were recorded with an oscilloscope model. The tests cover resistive and inductive loading, a step change in the dc input voltage, a change of load, a change of modulation index and the voltage stress on the switches. Fig. 16(a) shows the input voltage, output voltage and load current with a resistive load. The input is held at 125 V, and the output voltage is a seven-level staircase with a peak of about 375 V, that is, three times the input voltage. The load current follows the stepped output voltage, stays in phase. Fig. 16(b) gives the same quantities with an RL load. The seven voltage levels are unchanged, while the load inductance filters the higher-order harmonics, so the load current becomes nearly sinusoidal and lags the output voltage.

TABLE VII
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
Input dc voltage, V_{dc}	125 V
Peak output voltage ($3V_{dc}$)	375 V
Rated output power	750 W
Fundamental frequency, f_o	50 Hz
Switching frequency, f_{sw}	5 kHz
Switched capacitors C_1 / C_2	1.5 mF, 200 V / 1.2 mF, 400 V
Switches S_1–S_4, S_6	STF40NF20 (200 V, 40 A)
Switches S_5, S_7–S_{10}	SIHP065N60E (600 V, 40 A)
Diode D	MBR40250G (250 V / 40 A)
Resistive load	80 Ω
RL load	82 Ω-100 mH

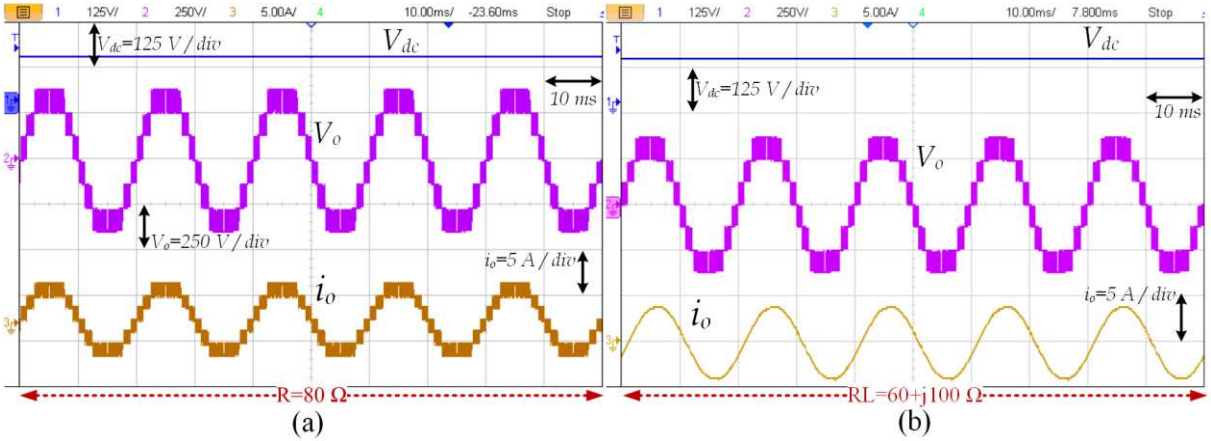


Fig. 16. Experimental steady-state waveforms of V_{in}, V_o and i_o (a) R load 80 Ω; (b) RL load 82 Ω–100 mH

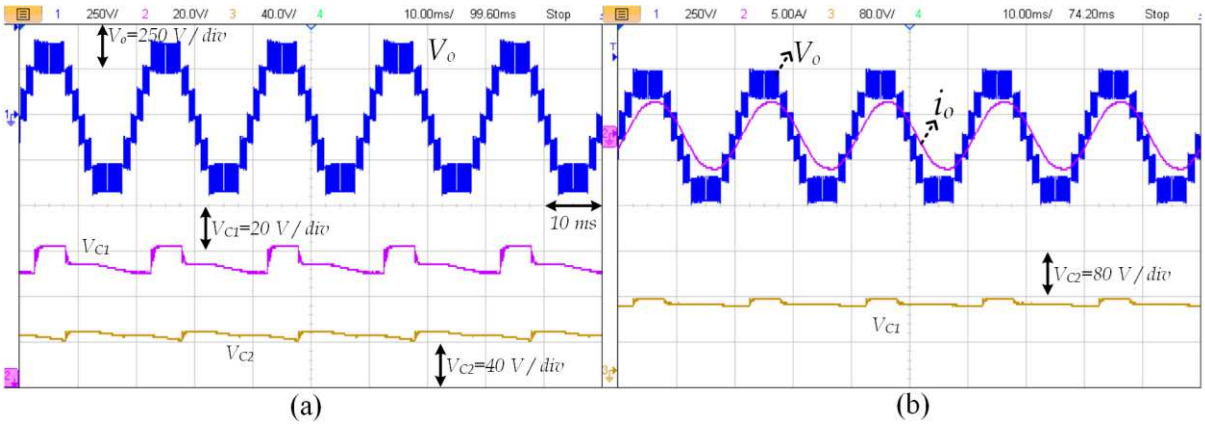


Fig. 17. Experimental capacitor waveforms (a) V_o, V_{C1} & V_{C2} with resistive load; (b) V_o, i_o & V_{C1} with RL load

Fig. 17(a) shows the capacitor voltages together with the output voltage under resistive loading, and Fig. 17(b) shows V_{C1} with the output voltage and load current under RL loading. In every fundamental cycle, each capacitor voltage rises sharply while the capacitor is connected in parallel with the source and then falls slowly while the capacitor supplies the load. The voltages return to the same value at the start of every cycle and do not drift over the recorded interval, which demonstrates that both capacitors balance themselves without voltage sensors or an auxiliary control loop. Fig. 18 shows the response when the dc input voltage is raised from about 100 V to 125 V. The output voltage keeps all seven levels before and after the step, and its peak rises in proportion to the input, so the voltage gain of three is maintained. As seen in Fig. 18(a) and (b), V_{C1} and V_{C2} move to their new operating values within a few fundamental cycles after the step. Fig. 18(c) shows both capacitor voltages together with the output voltage. No sustained oscillation or loss of capacitor balance appears after the transition.

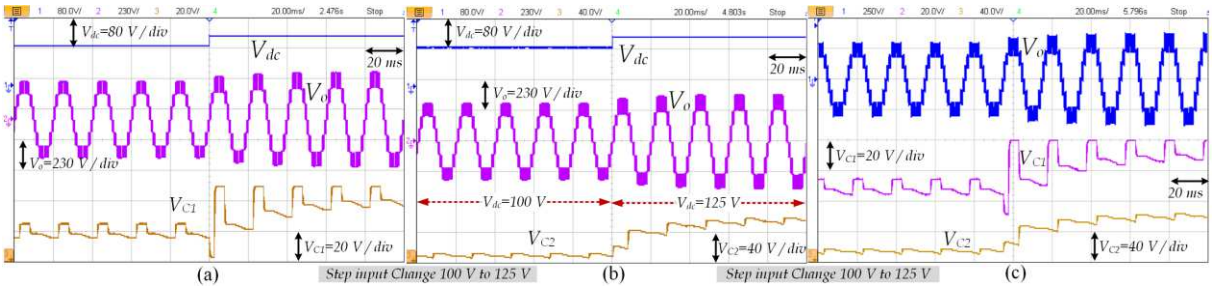


Fig. 18. Experimental response to a step change in input voltage from 100 V to 125 V (a) $V_{in,}$ V_o and V_{C1}; (b) V_{in}, V_o and V_{C2}; (c) V_o, V_{C1} and $V_{C2.}$

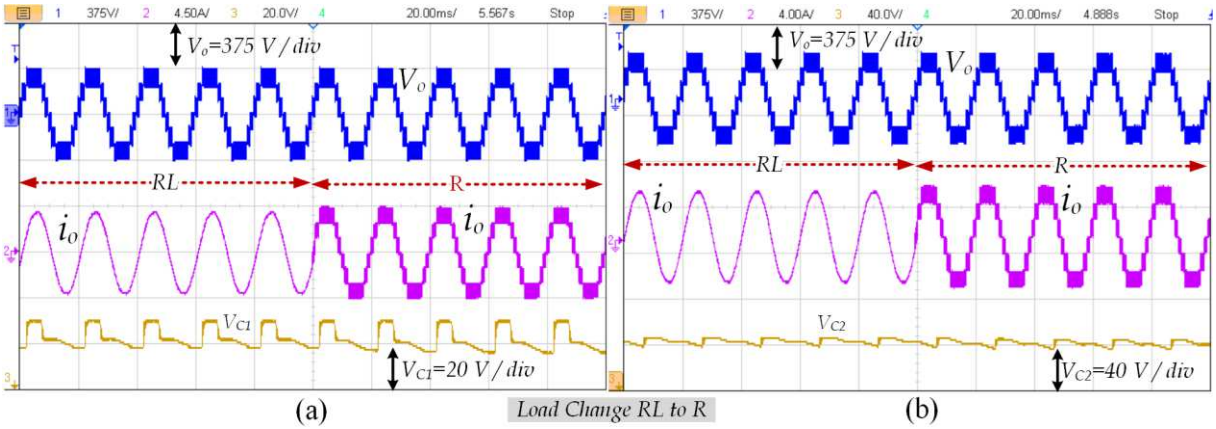


Fig. 19. Experimental response to a load change from RL to R, time (a) V_o, i_o and V_{C1}; (b) V_o, i_o and V_{C2}.

Fig. 19 shows the behaviour of the inverter when the load is changed from RL to purely resistive. Before the change, the load current is nearly sinusoidal and lags the output voltage. After the change, the current takes the stepped shape of the output voltage, comes into phase with it within the same fundamental cycle. The output voltage keeps its seven levels during the transition, and V_{C1} and V_{C2} continue their normal charge–discharge pattern without noticeable disturbance. Fig. 20 presents the output voltage and load current when the modulation index is reduced from 1 to 0.65. At the higher index, the output is a seven-level staircase with a peak of about 375 V. After the change, the outer levels are no longer generated and the output becomes a five-level waveform with a peak of about 250 V, equal to $2V_{dc}$. The load current moves to its lower amplitude within about one cycle, with no overshoot at the instant of change.

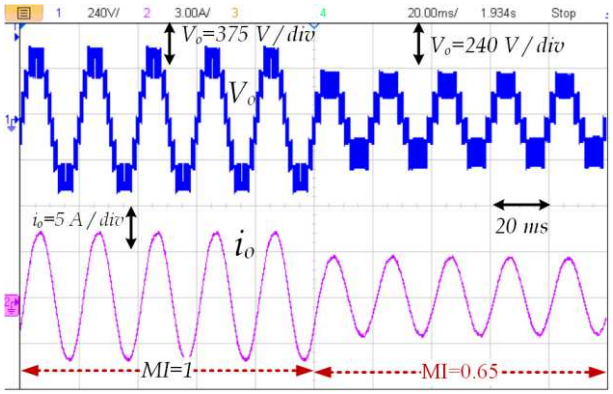


Fig. 20. Experimental output voltage V_o and load current i_o for a change in modulation index from 1 to 0.65.

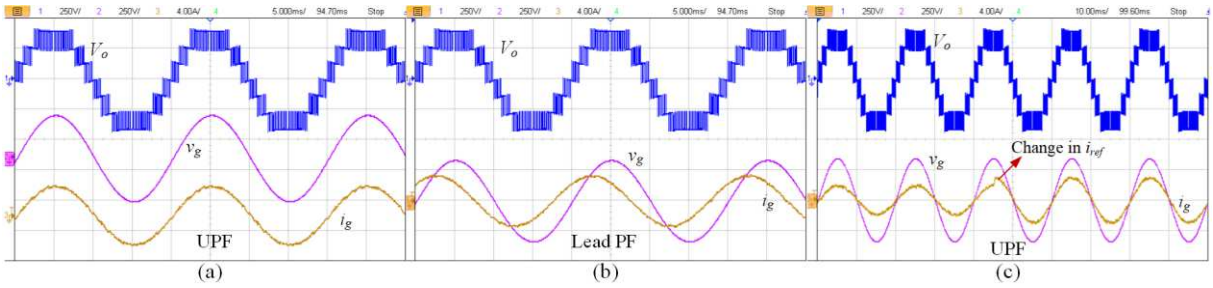


Fig. 21. Grid connected mode experimental results at, (a) UPF, (b) Leading PF, (c) Change of i_{ref}

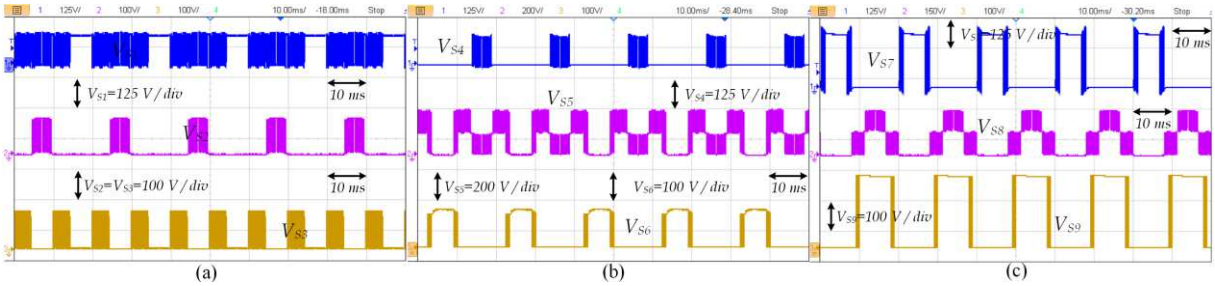


Fig. 22. Experimental voltage and current stress across the devices (a) v_{S1}, v_{S2}, v_{S3} (b) v_{S4}, v_{S5}, v_{S6}

Fig. 21(a)-(c) presents the experimental grid-connected responses of the proposed 7L-CGSC inverter topology while employing the closed loop control scheme as described in [31]. Under UPF operation, as shown in Fig. 21(a), the grid voltage (v_g) and grid current (i_g) exhibit ≈ zero phase angle, verifying synchronized active power delivery to the grid. In Fig. 21(b), the current waveform (i_g) leads the grid voltage, demonstrating the inverter's capability to inject reactive power with the grid. Fig. 21(c) examines the transient behaviour during a reference current (i_{ref}) variation from 3 A to 4 A under UPF operation. The grid current adjusts to the increased reference (i_{ref}) while preserving its sinusoidal profile and phase alignment with the grid voltage. Further, the blocking voltages of few of the power switches are depicted in Fig. 22. The switches S_1, S_2, S_3, S_4 and S_6 block a voltage equal to the input. None of the switches is exposed to the peak output voltage, which confirms the stress distribution derived in Section II.

All the experimental results agree closely with the simulation results presented in Section VIII. In both, the output voltage has seven levels with a peak of three times the input voltage, the load current is stepped and in phase with the voltage under resistive loading and nearly sinusoidal and lagging under RL loading, and the capacitors follow the same charge–discharge pattern with self-balanced voltages. The responses to the input-voltage step, the load change and the change in modulation index are also consistent, and the measured voltage stresses confirm that no switch or diode blocks more than $2V_{dc}$. The diode current pulses coincide with the capacitor-charging intervals, which verifies the self-balancing of the capacitor voltages. The small differences in peak values are attributed to the on-state voltage drops of the semiconductor devices, the equivalent series resistance of the capacitors and the tolerances of the passive components.

8. CONCLUSION

A seven-level switched-capacitor inverter has been proposed for low-voltage renewable energy sources. Fed from a single dc source, it triples the input voltage and maintains a common ground between the source and the load, which suppresses the leakage current in transformerless operation. The loss and reliability analyses showed that conduction loss dominates and that the proposed inverter achieves a longer predicted lifetime than other common-ground seven-level topologies. It also imposes a lower blocking voltage on its switches and offers the best balance between voltage gain, cost and volume. For the 750-W prototype, the analytical, simulated and measured efficiencies agreed closely. The experimental

results confirmed the threefold boost, the seven-level output, the self-balanced capacitor voltages and stable dynamic operation, making the topology a practical solution for transformerless PV systems.

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Data availability
The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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