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Posted Date: November 18th, 2026

DOI: https://doi.org/10.21203/rs.3.rs-11446085/v1

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Additional Declarations: No competing interests reported.

Interface Aware Quantum Dot Atomic Silicon Arithmetic for Verified Compression and Ripple Carry Addition

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Abstract—Quantum-dot atomic silicon provides a substrate for investigating arithmetic through the charge states of silicon dangling bonds. However, an isolated correct truth table does not establish a composable arithmetic circuit: charge-pair outputs and voltage-driven inputs use different interfaces, neighboring cells alter electrostatic conditions, and defects can produce incorrect or undecodable outputs. Direct ternary enumeration also becomes impractical as circuits grow. This study addresses these challenges with an eleven-site simultaneous full-adder cell, an explicit sensing and regeneration interface, and a complete reduced search that retains every potentially valid coupled configuration. The cell is composed into a 22-site 4:2 compressor and a 44-site four-bit ripple-carry adder. All 32 compressor and 512 adder input combinations satisfy their arithmetic identities. Across 64 compressor and 4,096 adder drive maps, independent implementations agree on the unique selected minimum, with exactly one consistent selected-state map per external input. Logical injection covers 18 and 34 single-net stuck-at faults; two tests detect every modeled fault, and three tests distinguish each faulty model from all others. Physical enumeration finds 27 of 88 omission cases and 209 of 352 displacement cases correct, while all 200 tested bias cases pass. SiQAD SimAnneal corroborates the selected configurations but exhibits a search-budget-dependent convergence gap. These results establish static arithmetic correctness and fault observability under a defined interface contract. Fabricated interfaces, metastable settling, delay, and operating energy require further investigation.

Index Terms—Quantum-dot atomic silicon; silicon dangling bonds; full adder; 4:2 compressor; ripple-carry adder; stuck-at faults; physical verification.

1 Introduction

Multioperand compression and carry-propagating addition perform different roles in arithmetic datapaths. Compressors reduce the number of equal-weight operands before a final adder resolves the carry representation, as occurs in multiplication and accumulation [1], [2]. Quantum-dot atomic silicon offers a physical setting for studying these operations using silicon dangling bonds (SiDBs) on a hydrogen-terminated surface. Experiments have demonstrated charge-position logic and elementary signal transmission [3], while SiQAD provides design and simulation support for larger exploratory structures [4], [5]. Arithmetic in this substrate therefore requires a description of both the Boolean computation and the physical representation of its signals [6], [7], [8].

Several obstacles prevent a collection of correct isolated gates from becoming a dependable arithmetic circuit. First, a voltage-conditioned input and a charge-position output are different physical interfaces; connecting their symbols does not establish signal transfer. Second, screened interactions couple neighboring cells and can change the selected charge configuration. A correct final output can also conceal an invalid intermediate pair or a disrupted input encoding, an issue highlighted by work on I/O integrity [9]. Third, omissions, displacement, and electrostatic perturbations affect the physical charge

solution, whereas a Boolean stuck-at model changes a decoded signal; their outcomes cannot be interpreted as the same reliability quantity [10], [11]. Finally, exact ternary enumeration grows exponentially with site count, and heuristic simulation need not recover the lowest valid configuration in every finite search [12], [13], [14].

The proposed response is to make the cell, its interconnections, and its verification conditions explicit. A newly generated eleven-site cell, denoted FA11-D, computes sum and carry simultaneously from the same three applied operands. Its ordered charge-pair outputs feed a specified sense–decode–wire–drive interface when another cell requires the result. Two cells implement a 4:2 compressor; four implement a four-bit ripple-carry adder (RCA). Complete local ternary catalogs and conservative interaction bounds reduce the coupled search without discarding any globally valid assignment. The resulting candidates are checked against the full interaction matrix. This responds to the composition and verification challenges while retaining a clear boundary between a simulated arithmetic core and proposed peripheral hardware, consistent with the need for physical I/O validation [9].

The principal contributions are an explicitly specified simultaneous full-adder geometry; connected compressor and RCA architectures with no directed output-to-upstream-input path; independent verification of every external input and every binary intermediate drive assignment; and separate logical and physical fault campaigns. The logical study additionally determines minimum detection and diagnostic suites. The physical study includes omissions, four defined lattice displacements per site, bias variation, screening variation, and the effect of intercell spacing. The results quantify failures as well as successful conditions. The two-adder compressor and the four-stage RCA are established architectures [15], [16], [17]; the contribution lies in their FA11-D implementation and the accompanying evidence, rather than a claim to the first compressor or RCA.

Section 2 defines the quantum-dot atomic silicon model and the signal encoding. Section 3 reviews relevant gate, arithmetic, simulation, and defect studies. Section 4 specifies the full adder, compressor, RCA, and interstage connections. Section 5 presents arithmetic verification, coupled-state analysis, SiQAD simulation, and fault characterization. Section 6 concludes with the remaining implementation requirements. The study concerns classical Boolean arithmetic encoded in quantum-dot charges; it does not demonstrate a coherent quantum algorithm or quantum computational speedup [18].

2 Quantum Dot Atomic Silicon Model

Removing a selected hydrogen atom from the H-Si(100)-2×1 surface creates a dangling bond whose localized electronic behavior can be modeled as an atomic quantum dot [3], [18]. In the charge-state description, a site can be negative, neutral, or positive. Binary-dot logic uses the position of an excess electron within an ordered pair [3], [7]. FA11-D uses this pair convention at its outputs and local external potentials at its three single-site inputs. Figure 1 identifies the physical sites; the dotted pair markers are annotations and do not represent fabricated metal wires or extra atomic sites.

The coordinates in Table I use integer lattice indices n and m and an intra-dimer index $l \in \{0,1\}$. Equation (1) converts these indices to nanometers and defines the Euclidean intersite distance r_{ij} used throughout the simulations. A translated cell adds a constant to n without changing its internal geometry.

$$x_i = 0.384\, n_i, \quad y_i = 0.768\, m_i + 0.225\, l_i \tag{1}$$
$$r_{ij} = \sqrt{[(x_i - x_j)^2 + (y_i - y_j)^2]}$$

For different sites i and j, the screened interaction coefficient W_{ij} is defined by Equation (2), with $W_{ii}=0$. Here $\kappa=1.4398375547444664$ eV·nm, ε_r is the relative permittivity, and λ is the screening length. The coefficient is positive; the signs of interacting charges enter through $q_i q_j$. The nominal parameters are $\varepsilon_r=5.6$ and $\lambda=5$ nm, consistent with the modeling framework used for SiDB logic [4], [9]. All pairwise interactions are retained in the coupled-array checks; there is no distance cutoff.

$$W_{ij} = \kappa \exp(-r_{ij} / \lambda) / (\varepsilon_r\, r_{ij}), \quad i \neq j \tag{2}$$

Let q contain the dimensionless site charges, $q_i \in \{-1,0,+1\}$, and let V contain the applied site potentials in the numerical convention used by the engine. Equation (3) defines the configuration energy E and the local energetic potential φ_i. With q dimensionless, a potential of one volt contributes one electronvolt per unit charge in $q^T V$. This expression is used to rank population- and hopping-valid configurations in the adopted model [4], [14]. It is not a measurement of energy dissipated in an arithmetic operation.

$$E(q) = \tfrac{1}{2}\, q^T W q + q^T V \qquad (3)$$
$$\varphi_i = -\Sigma_j\, W_{ij}\, q_j - V_i$$

TABLE I
FA11 D lattice coordinates

Site	Role	n	m	l
S0	Output	15	1	1
S1	Output	13	2	1
C0	Output	12	6	1
C1	Output	12	8	1
I0	Internal	12	10	0
I1	Internal	14	4	0
I2	Internal	9	11	0
I3	Internal	19	1	0
A	Input	6	8	0
B	Input	5	6	1
Cin	Input	6	4	1

Input bits apply local potentials only at A, B, and Cin. Output order is (S0,S1) for Sum and (C0,C1) for Carry.

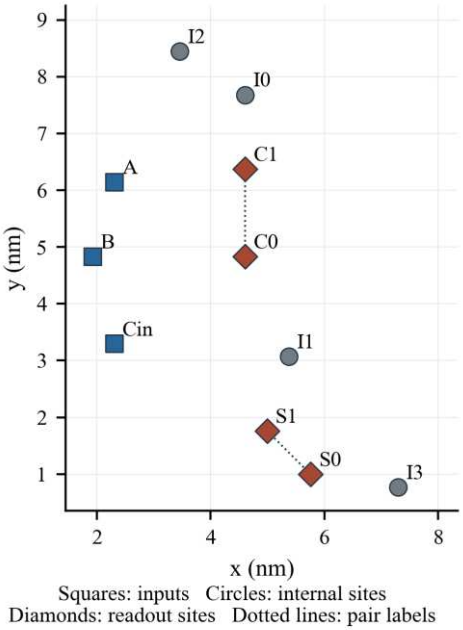


Fig. 1. FA11-D site geometry. Squares identify the three physical inputs, circles the four internal sites, and diamonds the four readout sites. Dotted segments identify ordered readout pairs; they are not wires. All coordinates are in nanometers.

The population conditions in Equation (4) use $m_i=\varphi_i+\mu_-$, $p_i=\varphi_i+\mu_+$, $\mu_-=-0.32$ eV, $\mu_+=-0.91$ eV, and a numerical tolerance $\tau=10^{-6}$ eV. Each site must satisfy the condition appropriate to its own charge. No input, internal, or output charge is clamped to an intended result. The tolerance-expanded inequalities

specify the acceptance rule; strict margins are reported separately so that numerical tolerance cannot be mistaken for a robustness budget.

$$q_i = -1: m_i < \tau; \quad q_i = +1: p_i > -\tau \qquad (4)$$
$$q_i = 0: m_i > -\tau \text{ and } p_i < \tau$$

Population-valid configurations must also pass the single-electron transfer check in Equation (5). A permitted ordered transfer changes q_i to q_i+1 and q_j to q_j-1 when $q_i<1$ and $q_j>q_i$. The corresponding energy change is ΔE_{ij}. Every permitted transfer must have $\Delta E_{ij} \geq -\tau$ [4], [9]. A physically valid configuration in this manuscript means a state accepted by these population and hopping criteria within the adopted static model. Among these states, the selected state has minimum E. All states within τ of the minimum are considered when checking output correctness.

$$\Delta E_{ij} = \varphi_j - \varphi_i - W_{ij} \geq -\tau \qquad (5)$$

The interface rule is given by Equation (6). An operand bit b applies $V=V_0(2b-1)$ to its designated input site, with V_0=0.30 V; zero potential is applied at all other sites. A readout pair (q_0,q_1) decodes to zero for (−1,0), to one for (0,−1), and to an invalid symbol ⊥ otherwise. A missing readout site is also invalid. Both sites and their order matter. In particular, pairs (0,0) and (−1,−1) are rejected rather than assigned a convenient Boolean value.

$$V_{input}(b) = V_0 (2b - 1) \qquad (6)$$
$$D(-1,0) = 0, \; D(0,-1) = 1, \; D(\text{other}) = \perp$$

These definitions specify a static simulation contract. Actual electrodes would need to realize the local potentials, and actual sensors would need to distinguish the two readout states without unacceptable loading. No electrode field solution or fabricated sensing circuit is included here. SiQAD geometry files and external-potential files are provided together because opening a geometry file alone does not reproduce the voltage-conditioned input cases. The SiQAD documentation explicitly separates configuration energy from dissipation and simulator occurrence counts from physical probabilities [14]. The same distinction is maintained in the results.

3 Related Work

Huff et al. [3] experimentally established binary atomic silicon logic using charge-position encoding, including elementary wiring and an OR function. This supports the physical basis of SiDB information representation. It does not experimentally validate the present full adder, active regeneration interface, or arithmetic arrays. Ng et al. [4] developed SiQAD for atomic silicon quantum-dot circuits, combining layout facilities with simulation engines. The current work uses SiQAD-format layouts and the SiQAD SimAnneal engine alongside independent enumerators; no fabrication claim follows from this software workflow.

Bahar et al. [6] investigated atomic silicon quantum-dot arrangements for logic design. Vieira et al. [7] developed a three-input NPN-class library that covers Boolean functions through equivalence transformations. These studies show that the spatial arrangement and pin conventions are central design variables. FA11-D differs in producing two arithmetic outputs simultaneously. Its eleven-site count is therefore not directly interchangeable with the count of an individual single-output gate in a library.

Walter et al. [8] introduced the Bestagon gate library and automated physical design for SiDB logic. Their routed-cell perspective is relevant because the boundary of a complete circuit includes placement and signal transport. An isolated site rectangle cannot represent the total area of a design with readout, drivers, and routing. Accordingly, the present manuscript reports the core count, the coordinate rectangle, and the interstage interface count separately.

The directly relevant architectural predecessor is the Miller-algorithm study by Ahmadpour et al. [15], which considers atomic silicon arithmetic including an FA, a four-bit RCA, and a 4:2 compressor. Consequently, cascading two full adders for compression is not claimed as a new Boolean architecture.

The proposed implementation instead uses the specific FA11-D geometry, voltage-to-charge interface convention, and complete coupled-state verification described here. Published site counts are available for selected earlier adders, but their complete layout and interface boundaries differ from the FA11-D core. Table II therefore compares the reported circuit functions and verification scope. A direct energy or reliability ranking would require matched physical parameters, signal interfaces, and evaluation protocols.

Ahmadpour et al. [10] studied a fault-tolerant majority gate and an adder, including atomic omission and displacement effects. Such analysis motivates reporting a clearly enumerated set of physical perturbations. The published full-adder assessment includes 36 selected single-omission scenarios, of which 16 are correct, and 198 double-omission scenarios, of which 70 are correct [10]. These scenario counts cannot be compared directly with a campaign that enumerates every physical site and input, including readout and input sites. The new results therefore state the eligible sites, perturbation directions, input counts, and invalid-output treatment. They do not infer fault tolerance from test coverage.

Rasmi et al. [16] proposed an ASDB full adder based on majority and XOR functions and extended the design to wider addition. Their later work [17] also treats a four-bit RCA and associated robustness considerations. These studies are arithmetic baselines, rather than evidence that a four-bit RCA is intrinsically novel. Table II summarizes the relevant scope without converting incompatible circuit boundaries or configuration-energy quantities into a power–performance–area ranking.

TABLE II
Comparison with published quantum dot atomic silicon studies

Work	Relevant object	Comparison scope
Huff et al. [3]	Binary logic and wires	Experimental elementary logic
Vieira et al. [7]	Three-input library	Single-output gate classes
Walter et al. [8]	Bestagon routing	Routed tile and placement
Ahmadpour et al. [15]	FA, RCA, compressor	Direct architecture predecessor
Ahmadpour et al. [10]	MV3 and adders	Omission and displacement study
Rasmi et al. [16], [17]	FA and RCA	Majority/XOR arithmetic
Drewniok et al. [9]	Automatic cells	I/O integrity and pruning
This work	FA11-D compositions	Exact map checks and stated fault sets

The table compares objects and evidence boundaries. The eight-input full-adder verification is reported in Table VIII. Interface-inclusive area, physical delay, and dissipated-energy reductions are not inferred across unmatched models.

QuickSim [12] and QuickExact [13] address the cost of physical simulation. The present exact checks are custom exhaustive and reduced-catalog implementations; they are not described as executions of either algorithm. The two independent implementations use the same stated physical model but different numerical organization. Ng et al. [11] further model fixed-charge defects and compare their formulation with experiment. That class of defect is distinct from removing a site, moving a site, or forcing a decoded net; the current campaigns are not presented as exhaustive coverage of all surface defects.

QuickCell [9] emphasizes that correct logical outputs can coexist with I/O integrity violations, such as kink states and overpopulated pairs. Its emphasis motivates checking the actual input-site charge encoding, both members of every output pair, and the consistency of each regenerated internal operand. The selected FA11-D geometry also underwent a bounded comparison against recovered earlier project records: thirteen records contained ten distinct complete geometries, and no congruent complete layout or noninput body was found by the recorded distance-signature tests. This is an audit of those available geometries, not proof of universal literature novelty.

4 Proposed Arithmetic Architecture

The FA11-D cell in Fig. 1 contains three input sites A, B, and Cin, four internal sites I0–I3, and four readout sites S0, S1, C0, and C1. The two output pairs represent Sum and Carry. All three input sites remain present for every operand combination. The cell evaluates the simultaneous full-adder relations in Equation (7), where ⊕ denotes exclusive OR, ∨ denotes Boolean OR, and juxtaposition denotes Boolean AND. The arithmetic identity in (7) is used as an independent integer check rather than as a substitute for the physical simulation.

$$\begin{aligned} &\text{Sum} = A \oplus B \oplus \text{Cin} \\ &\text{Carry} = AB \vee A\text{Cin} \vee B\text{Cin} \\ &A + B + \text{Cin} = \text{Sum} + 2\,\text{Carry} \end{aligned} \tag{7}$$

Figure 2 shows the selected charge configuration for every input state. For 000 through 111, the corresponding (Sum,Carry) outputs are (0,0), (1,0), (1,0), (0,1), (1,0), (0,1), (0,1), and (1,1). The charge arrangements are computed states, not drawn guesses or microscopy images. Each panel uses the same site coordinates and indicates the negative and neutral charge states. Positive charges are included in verification even though none occurs in the selected nominal states.

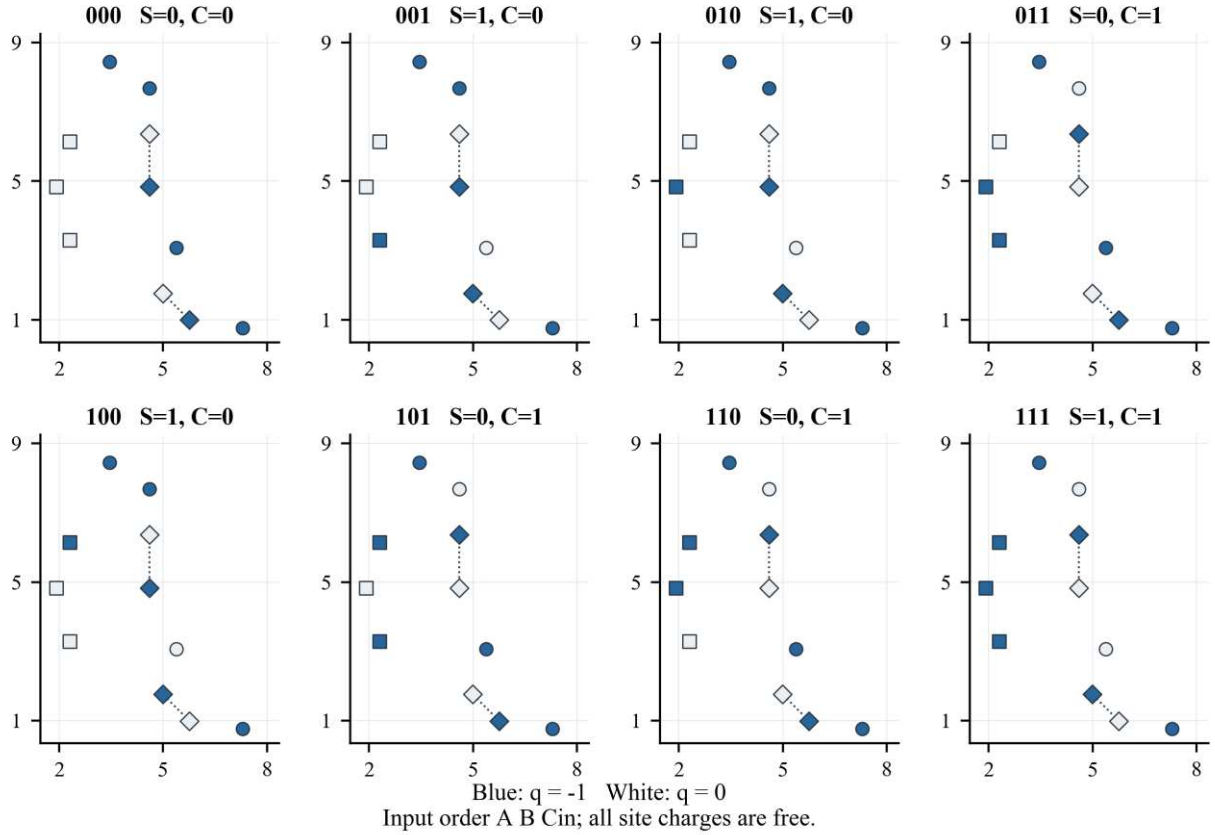


Fig. 2. All eight selected charge states of FA11-D in input order A B Cin. Blue sites are negative and white sites neutral. Each panel reports both simultaneously decoded outputs. Exact ternary enumeration permits positive charges and leaves all terminal charges free.

The geometry was selected by a randomized coordinate search with seed 2026101911, using 350,000 candidate rounds and selecting the recorded candidate at iteration 238779. The archived search was not initialized from a recovered previous layout. Candidate selection was followed by complete ternary verification. The coordinate rectangle measures 5.376×7.680 nm, or 41.28768 nm^2. This is the rectangle bounding the sites; it excludes electrodes, detectors, the surface clearance around a cell, and external wires. It is consequently a core geometry metric rather than device area.

The 4:2 compressor in Fig. 3 uses two instances of this cell. FA0 receives x1, x2, and x3 and produces an intermediate parity bit t and Cout. FA1 receives t, x4, and Cin and produces S and C. All five external

inputs have the same weight. The majority function is MV3(a,b,c)=abVacVbc. Equation (8) defines the two stages and the weighted conservation identity. The names C and Cout do not indicate successive binary positions: both have weight two. The output triplet is a redundant carry-save representation, and its numerical value is S+2C+2Cout.

$$t = x1 \oplus x2 \oplus x3, \quad Cout = MV3(x1,x2,x3) \tag{8}$$
$$S = t \oplus x4 \oplus Cin, \quad C = MV3(t,x4,Cin)$$
$$x1 + x2 + x3 + x4 + Cin = S + 2(C + Cout)$$

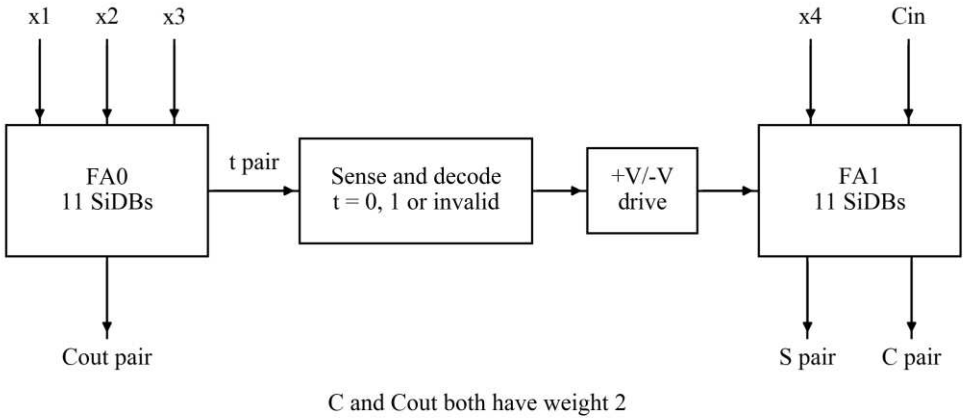


Fig. 3. Compressor connectivity. The parity pair from FA0 is sensed, decoded, transported electrically, and regenerated as a local input potential at FA1. The external sense, wire, and drive interface is proposed hardware. Primary operands also require local drivers; final output arrows identify readout pairs.

Cout is independent of x4 and Cin because it is obtained from FA0. This property avoids adding the second-stage parity dependency to that output. It does not establish a measured delay advantage. For example, input 00111 gives t=1 and (S,C,Cout)=(1,1,0), representing three; input 11111 gives (1,1,1), representing five. Table III lists all thirty-two states, including the intermediate t, so the distinction between output bits and their weights is visible for every case.

TABLE III
Complete compressor truth table

Input[1]	t	S	C	Cout	Value[2]
00000	0	0	0	0	0
00001	0	1	0	0	1
00010	0	1	0	0	1
00011	0	0	1	0	2
00100	1	1	0	0	1
00101	1	0	1	0	2
00110	1	0	1	0	2
00111	1	1	1	0	3
01000	1	1	0	0	1
01001	1	0	1	0	2
01010	1	0	1	0	2
01011	1	1	1	0	3
01100	0	0	0	1	2
01101	0	1	0	1	3
01110	0	1	0	1	3

Input[1]	t	S	C	Cout	Value[2]
01111	0	0	1	1	4
10000	1	1	0	0	1
10001	1	0	1	0	2
10010	1	0	1	0	2
10011	1	1	1	0	3
10100	0	0	0	1	2
10101	0	1	0	1	3
10110	0	1	0	1	3
10111	0	0	1	1	4
11000	0	0	0	1	2
11001	0	1	0	1	3
11010	0	1	0	1	3
11011	0	0	1	1	4
11100	1	1	0	1	3
11101	1	0	1	1	4
11110	1	0	1	1	4
11111	1	1	1	1	5

[1] Input order: x1 x2 x3 x4 Cin. [2] Value = S+2C+2Cout. Carry outputs C and Cout have equal arithmetic weight.

A single interstage path carries t. The FA0 sum pair is sensed, the ordered pair is decoded, an external electrical net transports the decoded bit, and a local driver applies the appropriate polarity to FA1 input A. The primary inputs also require local drive, and final outputs require readout. The sensing, routing, and drive circuitry is proposed peripheral hardware, not an additional set of verified atomic sites. The simulated potential maps represent its final action. An invalid pair prevents acceptance of a downstream result; the interface does not silently convert it to zero or one.

The four-bit RCA in Fig. 4 connects four FA11-D cells according to Equation (9). Operands A and B are unsigned integers from zero to fifteen, with A_i and B_i their binary digits. C0 is the external carry input; each cell supplies S_i and C_{i+1}. The final word is represented by four sum bits and C4. For example, A=15, B=1, C0=0 yields Sum=0000 and C4=1, while A=15, B=15, C0=1 yields Sum=1111 and C4=1. Omitting C4 would incorrectly turn exact five-bit addition into modular four-bit addition.

$$S_i = A_i \oplus B_i \oplus C_i,\ \ C_{i+1} = MV3(A_i,B_i,C_i) \qquad (9)$$
$$A + B + C0 = \Sigma_{i=0}^{3}\, 2^i S_i + 16\, C4$$

Three carry paths require the same sense–decode–wire–drive contract: the carry pair from FA0 drives Cin of FA1, FA1 drives FA2, and FA2 drives FA3. Each A_i and B_i is applied to its own designated input terminal. Sum outputs are read directly from their producing cell. The directed dependency graph is acyclic. No output is wired to an upstream operand, and no closed-loop combinational wire is introduced. The electrostatic interaction matrix is reciprocal, however, so the absence of a directed feedback wire does not imply the absence of physical loading.

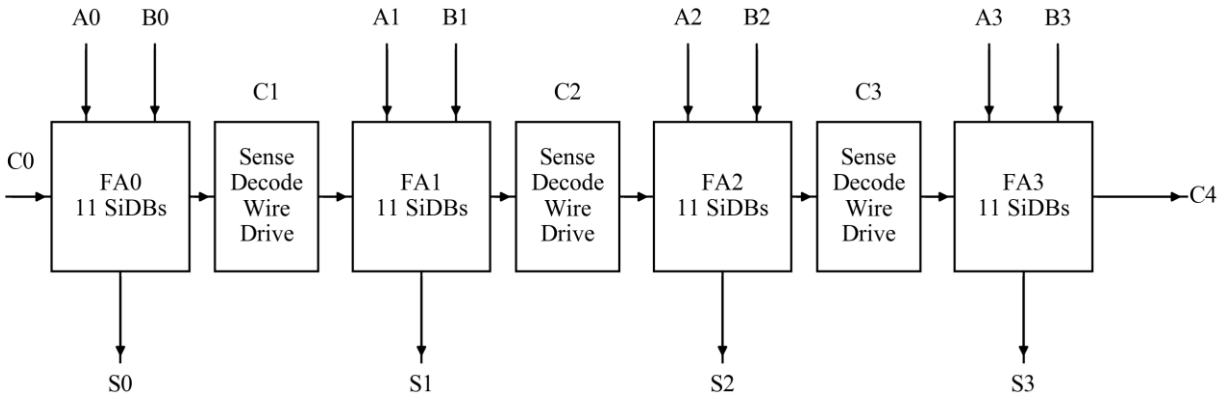


Fig. 4. Four-bit RCA with three explicit carry regeneration paths. Each path includes charge sensing, ordered-pair decoding, an external electrical wire, and local potential drive. The directed interstage network has no feedback loop. Primary-input drivers and final readout hardware are required but not included in the atomic-site count.

Figure 5 shows the actual translated atomic coordinates and a schematic overlay of the external interstage connections. The cell translation is 100 lattice units along n, corresponding to 38.4 nm. The compressor contains 22 SiDB sites and the RCA 44. Their site-bounding rectangles are 43.776×7.680 nm and 120.576×7.680 nm, respectively. These deliberately sparse placements separate active cores while preserving all screened interactions in the model. The drawn external routes are signal specifications, not solved electrode geometries or verified binary-dot wires. No crossing of atomic wires is needed in these layouts.

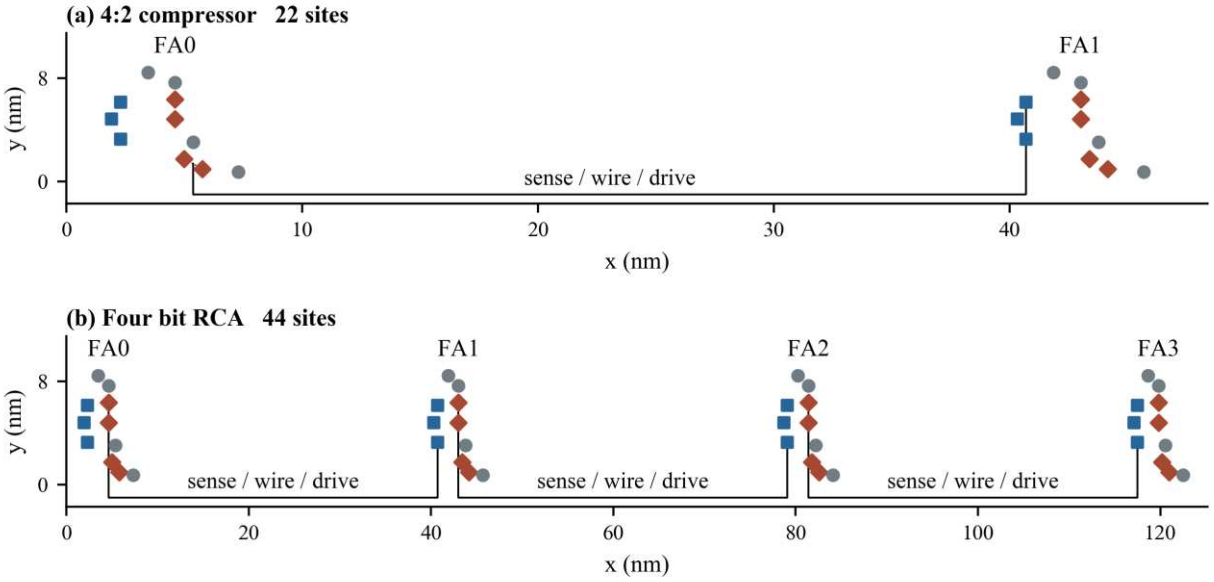


Fig. 5. Translated 22-site compressor and 44-site RCA coordinates at 38.4 nm cell pitch. Solid connection overlays specify proposed external sense–wire–drive paths from the source-pair midpoint to the designated next input. They are not atomistically modeled conductors. The detailed cell shape is given in Fig. 1.

The construction requires six driven terminals and four sensed output pairs for the compressor, including one regenerated internal input and its source pair. The RCA requires twelve driven terminals and eight sensed output pairs, including three regenerated inputs and three internal carry pairs. Counting only the final external outputs would hide these intermediate interface requirements. Table IV reports these quantities with the core site count and static search boundary. Neither the number of arithmetic stages nor the interstage wire count is converted into a clock period or switching energy.

TABLE IV
Implementation and exhaustive verification boundaries

Quantity	Compressor	Four-bit RCA
FA11-D instances	2	4
Atomic core sites	22	44
Site rectangle (nm^2)	336.19968	926.02368
Driven input terminals	6	12
Sensed output pairs	4	8
Internal regenerate paths	1	3
Primary input cases	32	512
All binary drive maps	64	4,096
Direct ternary space per map	3^{22}	3^{44}

Rectangle metrics exclude interface circuitry, electrodes, wire routing, and additional clearance. Sensed-pair counts include intermediate signals. Final selected pitch is 38.4 nm.

5 Results and Fault Characterization

The validation has four distinct levels: exact isolated-cell physics, complete reduced coupled-state selection, ideal-interface arithmetic, and fault injection. Physical campaigns modify the geometry or the model and then solve the charge problem again. Logical campaigns instead force one decoded scalar net. Conditional propagation of physical response maps is reported separately from joint physical verification of an entire defective array. This separation prevents the success of one abstraction from being attributed to another.

For the nominal full adder, all 3^{11}=177,147 charge configurations are enumerated for each of eight input states, totaling 1,417,176 state–input combinations. A scalar C++ implementation and a separately organized NumPy enumeration select the same unique minimum for every input; their configuration energies agree within 2×10^{-12} eV. The physical input charges also encode the applied operands in every selected state. This additional check is necessary because a correct decoded result alone would not reveal an unintended input-terminal state.

Figure 6 separates stability margins from the energy gap to an alternative valid configuration. The minimum population margin is 22.2326 meV, and the minimum allowed-hop margin is 15.4300 meV. The smallest finite alternative-state gap is only 0.307642 meV, for input 100. Input 000 has no alternative valid configuration in the enumerated model. The much smaller gap must not be replaced by the larger hopping margin when discussing state selection. None of these values establishes a physical operating temperature or switching-energy cost.

For coupled cells, direct enumeration would contain 3^{22}=31,381,059,609 assignments for the compressor and approximately 9.85×10^{20} for the RCA, per imposed potential map. Equation (10) bounds the remote contribution at a site in cell c by b_i, using $|q_j|\leq1$ and the positive interaction coefficients. This bound holds for any remote charge arrangement, including positive charges, not only the intended neighboring states.

$$b_i = \Sigma_{j\notin c} W_{ij}, \quad |\varphi_i\mathrm{global} - \varphi_i\mathrm{local}| \leq b_i \tag{10}$$

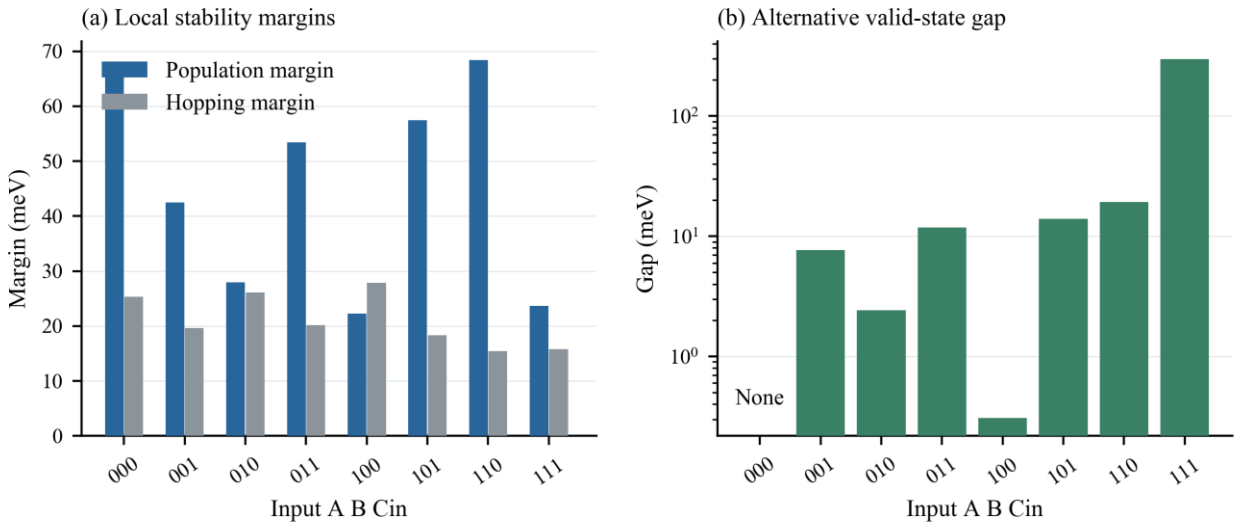


Fig. 6. Local stability margins and finite gaps to alternative valid configurations for FA11-D. Gap and stability margin are different quantities. No alternative valid configuration exists for input 000. The gap panel uses a logarithmic scale; values are configuration-energy differences, not dissipated energy.

Equation (11) defines the necessary local catalog Kc(Vc), where Vc is the imposed potential vector of cell c. Its population inequalities are relaxed by b_i, and its internal hopping inequalities by b_i+b_j. The functions m_i, p_i, and ΔE_{ij} in this equation are evaluated using the isolated local interaction block and the imposed local potentials. If a complete charge assignment is globally valid, each local restriction must satisfy these relaxed inequalities; otherwise even the largest permitted remote contribution cannot repair the violated local condition. Therefore every globally valid assignment is included in the Cartesian product K(V) in (12).

$$\begin{aligned} &\text{Kc(Vc):}\ \ q_i = -1 \Rightarrow m_i < \tau + b_i \\ &q_i = +1 \Rightarrow p_i > -\tau - b_i \\ &q_i = 0 \Rightarrow m_i > -\tau - b_i,\ \ p_i < \tau + b_i \\ &\Delta E_{ij}\text{local} \geq -\tau - b_i - b_j \quad \text{for allowed } i,j \in c \end{aligned} \tag{11}$$

Equation (12) defines the Cartesian product of necessary local catalogs and the selection of its minimum-energy valid state. Every product member is subsequently checked with the full array matrix W: all population inequalities, all permitted ordered transfers including transfers between cells, and the complete configuration energy. The selected valid minimum is then evaluated with the decoder in (6). This is a complete reduced search over potentially valid states, rather than a direct enumeration of all 3^N assignments or a cutoff approximation. Here k is the number of cells, with k=2 for the compressor and k=4 for the RCA. Forty-eight local catalogs, each built from all 177,147 local states, are sufficient for the two nominal array geometries. Their combined preprocessing examines 8,503,056 local state–input combinations.

$$\begin{aligned} &K(V) = K0(V0) \times K1(V1) \times \cdots \times Kk{-}1(Vk{-}1) \\ &q\text{selected} \in \arg\min \{E(q): q \in K(V),\ q \text{ valid}\} \end{aligned} \tag{12}$$

For the intended final potential maps, the compressor examines 183 product candidates across 32 inputs, with at most nine candidates in one map. The RCA examines 16,102 candidates across 512 inputs, with at most 81 in one map. All selected states are unique and match the arithmetic references. Their minimum finite alternative-state gaps are 0.302120 and 0.301653 meV, respectively. A simpler energy-envelope sufficient test passes the compressor but fails the RCA at the chosen pitch; the minimum RCA exclusion bound is −0.119874 meV. That failed sufficient bound is not used as evidence of correctness. The complete reduced search supplies the stronger result.

Checking only intended maps could overlook a different internal binary drive assignment. Equation (13) therefore defines consistency explicitly: each regenerated drive bit u_e must equal the decoded selected

source pair on edge e. The compressor has one such bit and hence 32×2=64 imposed maps; the RCA has three and hence 512×8=4,096. All maps are checked, including deliberately inconsistent carry or parity drives. The two circuits produce exactly 32 and 512 consistent selected-state maps, respectively, with one correct map per external input.

$$u_e = D(\text{qselected at source pair e}) \quad \text{for every edge e} \tag{13}$$

An independent scalar C++ reconstruction builds its own local catalogs, interaction matrix, energy calculation, and global checks directly from coordinates and parameters. It agrees with the NumPy search on all 4,160 maps, including 361 compressor and 130,321 RCA product candidates. Maximum selected-energy differences are 4.44×10^{-16} and 2.67×10^{-15} eV. Across all imposed maps, the smallest finite gaps are 0.301539068 and 0.301537650 meV. These differ slightly from the gaps over intended maps because the tested set includes inconsistent internal drives.

Selected-state uniqueness must be qualified. When every population- and hopping-valid state is retained, rather than only the minimum, the catalogs contain 179 consistent compressor map–state pairs and 15,839 consistent RCA pairs. Of these, 127 and 15,161 give incorrect weighted arithmetic; none relies on an invalid output pair. These are enumerated possibilities, not occurrence probabilities. The ground-state results therefore establish unique correct selected-state maps, not unique metastable equilibria or guaranteed settling. Explicit incorrect-state examples are included with the independent audit.

Table V summarizes the SiQAD SimAnneal corroboration. The engine receives the geometry, model parameters, and external potentials without any intended charge-state seed or fixed output charges. Its optimized profile uses portable population handling and a documented K6 refinement; the executable checksum, source, configuration, and logs accompany the results. At 30,000 annealing cycles and three requested restarts per case, the lowest exported valid state agrees with the exact reference for all 32 compressor inputs and 15 of 16 selected RCA inputs. With ten requested restarts, the RCA matches all sixteen. The individual FA runs also match all eight cases. The retained incorrect solver records show why a finite heuristic run is corroborating evidence rather than an exact certificate.

TABLE V
SiQAD SimAnneal selected state checks

Object	Cases	Restarts[1]	Exact selected match
FA11-D	8	10	8 / 8
Compressor	32	3	32 / 32
RCA sample	16	3	15 / 16
RCA sample	16	10	16 / 16

[1] Restarts per case, each with 30,000 cycles. Match: lowest exported valid state equals the reference and passes interface checks. Both RCA rows use the same sixteen inputs.

The numerical search budget is not a circuit clock. Exported record weights can also differ from the number of requested restarts and are not treated as measured state probabilities. The sixteen RCA samples are a stated heuristic sample; the exact search, not those sixteen runs, supplies the exhaustive 512-input result. No result is described as a fabricated device measurement.

The separate arithmetic evaluator decodes the eight physically selected full-adder states into a lookup and composes that lookup according to the netlist. It then compares the result with independent integer arithmetic. All thirty-two compressor cases satisfy (8), and all 512 RCA cases satisfy (9). Figure 7 displays the actual five-bit RCA result for both carry inputs over every A,B combination. In addition, 2,048 prefix identities pass: at each of four stages, the processed low-order operand bits equal the low-order sum plus the appropriately weighted outgoing carry.

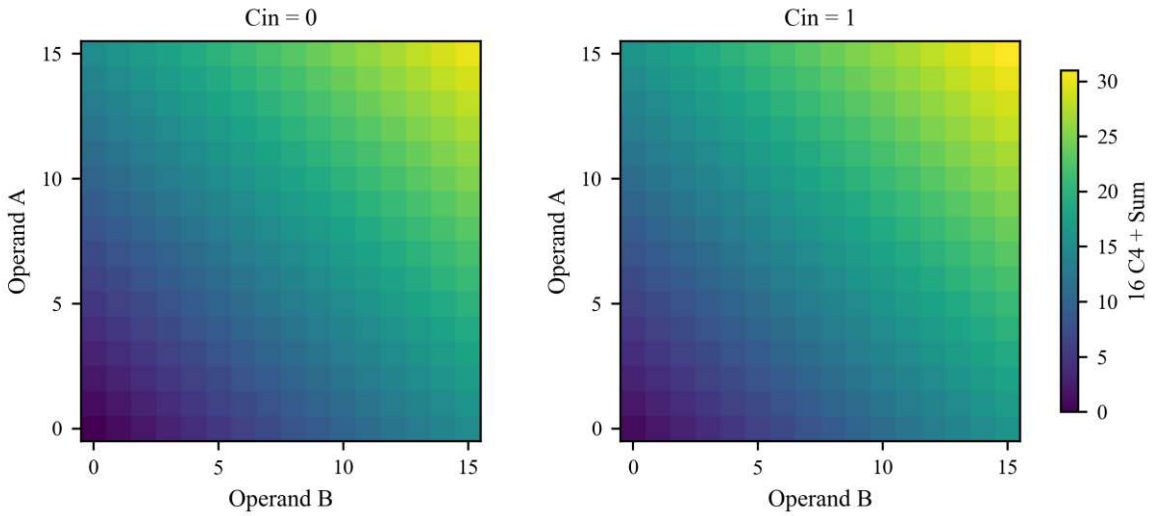


Fig. 7. All 512 unsigned RCA outputs. Each pixel is the computed five-bit value 16C4+Sum for one A,B,C0 combination. Every entry equals A+B+C0. This plot covers arithmetic behavior; exact coupled-state verification is reported separately.

Cout independence in the compressor is checked with 48 comparisons spanning variations of x4 and Cin at each fixed x1,x2,x3. For signed four-bit addition with C0=0, the same RCA produces the correct wrapped result for all 256 operand pairs. Equation (14) defines the signed interpretations a_s and b_s of A and B, $U=\Sigma_{i=0}^{3}2^{i}S_i$ is the unsigned sum word, s_s is its signed interpretation, and $O=C3\oplus C4$ is the overflow flag. The bracket [P] equals one when predicate P is true and zero otherwise. All sixty-four signed-overflow cases agree with the independent range test. This signed interpretation does not change the underlying unsigned conservation identity.

$$a_s = A - 16\cdot[A \geq 8], \quad b_s = B - 16\cdot[B \geq 8] \tag{14}$$
$$s_s = U - 16\cdot[U \geq 8]$$
$$O = C3 \oplus C4 = [a_s + b_s \notin \{-8,\ldots,7\}]$$

Logical stuck-at injection treats the entire named scalar net and every fanout consistently. The compressor net set is {x1,x2,x3,x4,Cin,t,S,C,Cout}, giving eighteen single faults. The RCA net set is {A0–A3,B0–B3,C0–C3,S0–S3,C4}, giving thirty-four. Each net is forced separately to zero and one. Inputs supplied to the reference arithmetic remain the originally requested operands; a fault on an input changes what the circuit receives, not the expected answer.

Equation (15) distinguishes fault coverage FC from the fault–input error fraction EF. F is the enumerated fault set and X the complete primary-input set. Df,x is one when the observed output word or triplet differs from the healthy result for fault f and input x. FC counts faults detected by at least one input; EF counts changed outputs over the Cartesian fault–input campaign. Both circuits have FC=100% and EF=50% in this model. There are 288 errors among 576 compressor trials and 8,704 among 17,408 RCA trials. The other trials do not activate the stuck value. Every activated fault changes the arithmetic value, so these results establish observability rather than inherent tolerance.

$$FC = (1 / |F|)\ \Sigma f\in F\ \max x\in X\ Df,x \tag{15}$$
$$EF = (1 / (|F|\ |X|))\ \Sigma f\in F\ \Sigma x\in X\ Df,x$$

Figure 8 shows the signed arithmetic-error distributions. The compressor's worst absolute error is two, with mean absolute error 0.611111 over all trials including nonactivated cases. The corresponding RCA values are sixteen and 2.235294. RCA errors occur at powers of two because a forced operand, carry, or sum net changes a defined arithmetic weight. Numeric errors are distinct from invalid charge-pair outcomes, which do not occur in this purely Boolean stuck-at model.

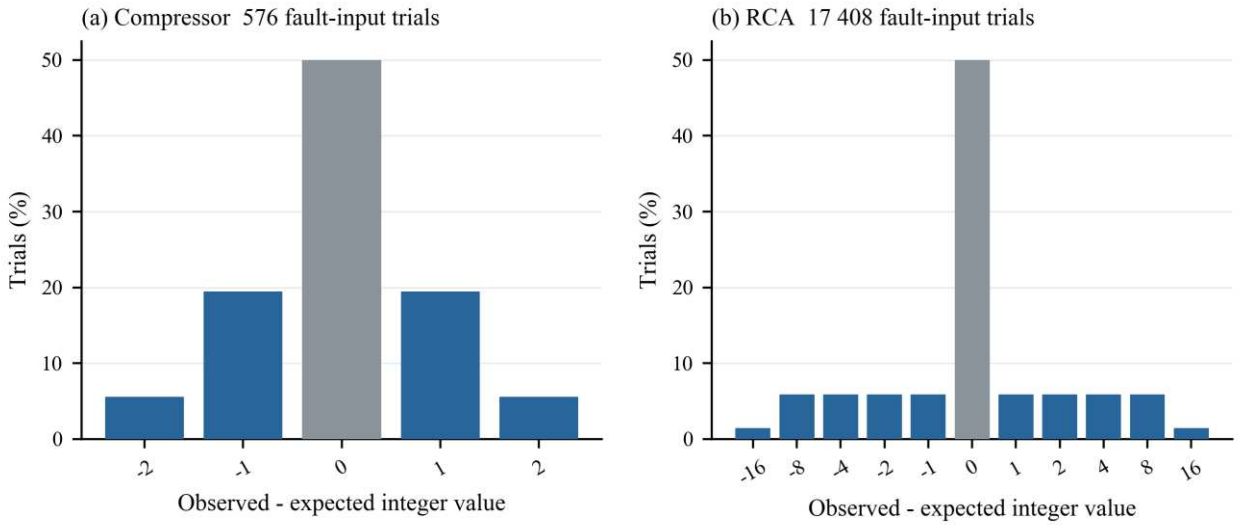


Fig. 8. Arithmetic error under every enumerated single-net stuck-at fault and input. Bars show fractions of trials, including nonactivated trials at zero error. All activated faults change the represented value. These distributions are deterministic fault-injection results, not device error probabilities.

Table VI provides compact tests. The all-zero and all-one input patterns detect every enumerated fault. Two tests are minimal because a single input cannot activate both stuck polarities on any one net. Detection does not identify which fault occurred. For diagnosis, complete output signatures distinguish the healthy circuit and every single-fault model. A set-cover formulation and exhaustive examination of every two-pattern pair establish a minimum of three patterns for both circuits. The compressor uses 01010, 01101, and 10000 in x1,x2,x3,x4,Cin order. The RCA uses (A,B,C0)=(0,7,1), (6,13,0), and (11,8,1).

TABLE VI
Minimum detection and diagnostic input suites

Purpose	Compressor[1]	RCA[2]
Detection	00000, 11111	(0,0,0), (15,15,1)
Diagnosis	01010, 01101, 10000	(0,7,1), (6,13,0), (11,8,1)
Models distinguished by diagnosis	19	35
Two-pattern suites ruled out for diagnosis	496	130,816

[1] Five-bit order x1,x2,x3,x4,Cin. [2] Triplet order (A,B,C0). Diagnosis assumes one persistent modeled fault or healthy operation. Full ordered output codebooks accompany the data.

For completeness, 496 compressor two-pattern suites and 130,816 RCA suites are checked and none diagnoses every model. The three-pattern codebooks distinguish nineteen and thirty-five models, including the healthy case. These results assume the modeled fault is persistent throughout testing and the test driver and observation paths are correct. They do not diagnose simultaneous faults, intermittent faults, or arbitrary analog interface failures.

The physical campaign in Table VII recomputes all ternary states for every perturbed cell. Single-site omission includes all eleven sites and all eight inputs, for 88 cases. Twenty-seven cases are correct, twenty-seven have wrong valid outputs, and thirty-four are invalid. Readout-site omissions account for 32 invalid cases because a complete ordered pair no longer exists. Restricting the denominator to the four internal sites gives 15 correct cases of 32; omitting physical input sites gives 12 of 24. No single-site omission preserves all eight input cases.

TABLE VII
Exact isolated cell physical campaigns

Campaign	Cases	Correct	Wrong valid	Invalid
Nominal	8	8	0	0
Single omission	88	27	27	34
Lattice displacement	352	209	121	22
Bias 0.240–0.360 V	200	200	0	0
Screening 3–7 nm	88	51	36	1

Each case is one perturbed geometry/model and one input. All eleven sites are eligible. Displacements track logical terminal identities; no fixed laboratory electrode misalignment is modeled. Bias and screening are one-parameter static sweeps.

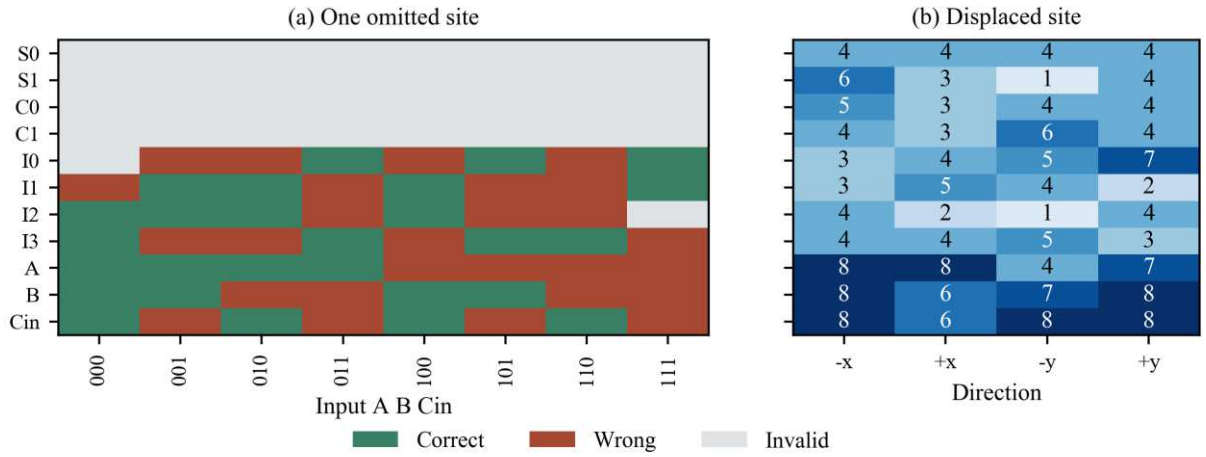


Fig. 9. Physical sensitivity of FA11-D. (a) Every omitted site against all eight inputs: green correct, red wrong, gray invalid. (b) Number of correct inputs out of eight after moving the indicated site by one defined step in each direction. Steps are ±0.384 nm in x and ±0.768 nm in y.

Displacement moves one site at a time by n±1 or m±1, keeping l fixed. These are structural steps of 0.384 nm along x or 0.768 nm along y, not isotropic random position noise. All forty-four perturbed geometries have distinct site positions. Across 352 input cases, 209 are correct, 121 are wrong valid, and 22 are invalid. Seven displaced geometries retain all eight cases. Site identity is preserved: ideal drive and readout follow the displaced terminal. Fixed laboratory sensor locations, electrode misalignment, and field spillover are not modeled. Figure 9 exposes the input-specific failures rather than concealing them in a single percentage.

Figure 10 separates the bias and screening tests. Twenty-five uniform input-bias amplitudes from 0.240 to 0.360 V in 0.005 V increments give 200 of 200 correct cell cases. This is a sampled passing interval, not a measured voltage noise margin or a claim that no failure occurs outside it. Eleven screening lengths from 3 to 7 nm give 51 correct cases of 88; three sampled lengths preserve every input. Screening variation is a change in the electrostatic model, not a temperature sweep. The nominal dielectric constant and charge-transition parameters remain fixed during these one-parameter sweeps.

The isolated physical response maps are also propagated through each hierarchy, with one affected cell at every eligible position. An invalid intermediate pair blocks acceptance of dependent outputs; no default bit is inserted. For compressor omissions, 216 trials are correct, 216 wrong, and 272 invalid out of 704. For the RCA, the counts are 6,912, 6,912, and 8,704 out of 22,528. Displacement gives 1,672 correct, 968 wrong, and 176 invalid compressor trials out of 2,816; the RCA gives 53,504, 30,976, and 5,632 out of 90,112. Figure 11 groups omission responses by terminal role.

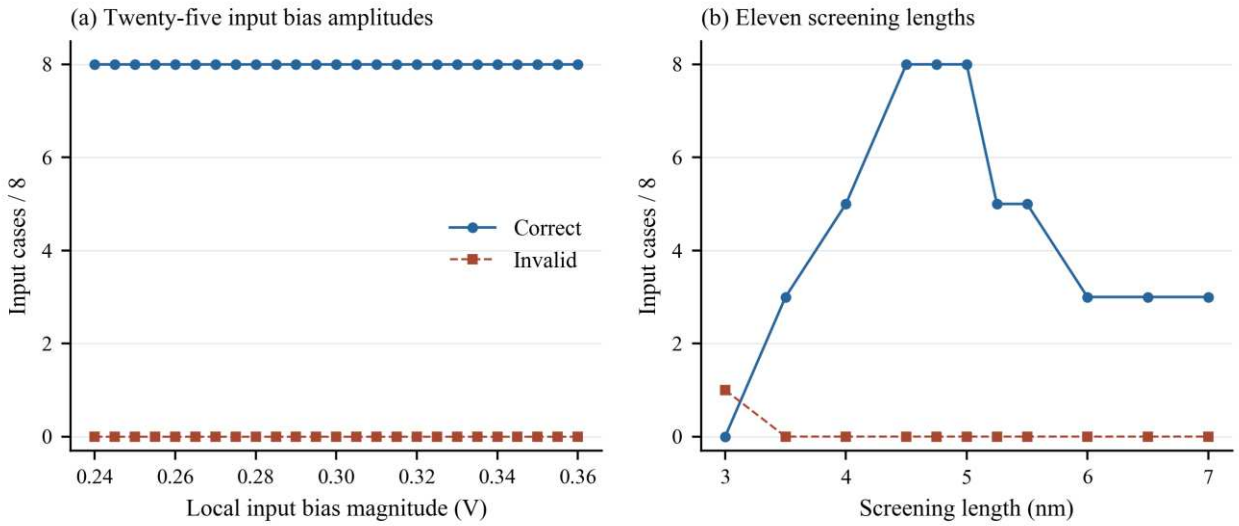


Fig. 10. Exact isolated-cell parameter sweeps. Twenty-five bias magnitudes cover 0.240–0.360 V in 5 mV steps. Eleven screening lengths cover 3–7 nm. Counts refer to correct or invalid input cases among eight at each sample. These are not temperature or fabricated-device yield measurements.

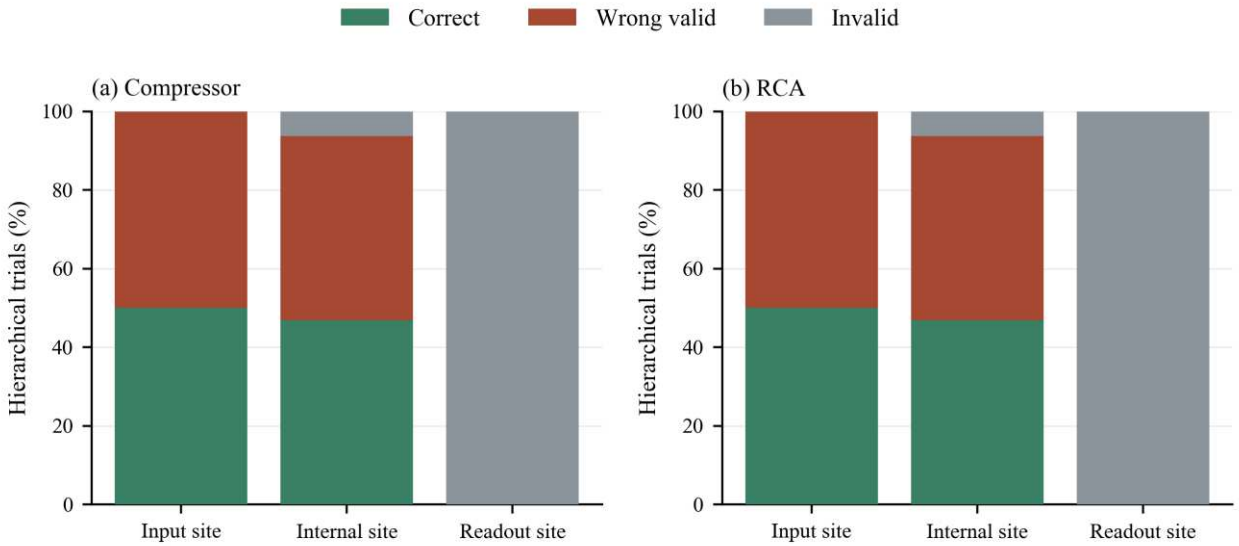


Fig. 11. Conditional omission-map propagation by site role. The decoder rejects a missing readout pair and blocks dependent outputs. Counts combine all input cases and every affected-cell position. Results use isolated defective-cell maps and ideal interfaces, not full coupled simulations of each defective array.

These propagated results assume ideal interfaces and use isolated defective-cell maps. The nominal coupled-array certificate does not automatically certify the defective arrays or arrays with changed screening. Weighted arithmetic correctness is also checked separately from exact compressor output-tuple equality: the two equal-weight carry outputs can exchange values without changing the represented sum. The global screening response-map experiment contains six such arithmetically masked output changes; the omission and displacement campaigns contain none. This distinction prevents carry-save equivalence from being confused with exact pin behavior.

Figure 12 quantifies placement sensitivity through complete reduced searches of all 512 intended RCA maps at six pitches. At 23.04 nm pitch, every intended reference state still passes population and hopping validity, but only 388 selected outputs are correct. Thus validity of the desired state alone is insufficient: a lower-energy valid alternative can change the arithmetic. All 512 cases pass at the tested pitches 26.88, 30.72, 34.56, 38.40, and 46.08 nm. The respective minimum alternative gaps are 0.222331, 0.272929, 0.293308, 0.301653, and 0.306567 meV; the failing 23.04 nm placement has a 0.093938 meV minimum selected-state gap.

The final 38.4 nm pitch is a conservative selected placement, not an area optimum. A 26.88 nm pitch also passes the intended-map sweep with a smaller site rectangle. Full all-drive-map consistency is established here for the final 38.4 nm design only. The spacing results do not provide an electrode routing area, a clock frequency, or an energy–delay product. Table II compares the architectural and verification scope of previous studies, while Table VIII collects the isolated full-adder verification results. The different implementation boundaries preclude an interface-inclusive area or energy ranking.

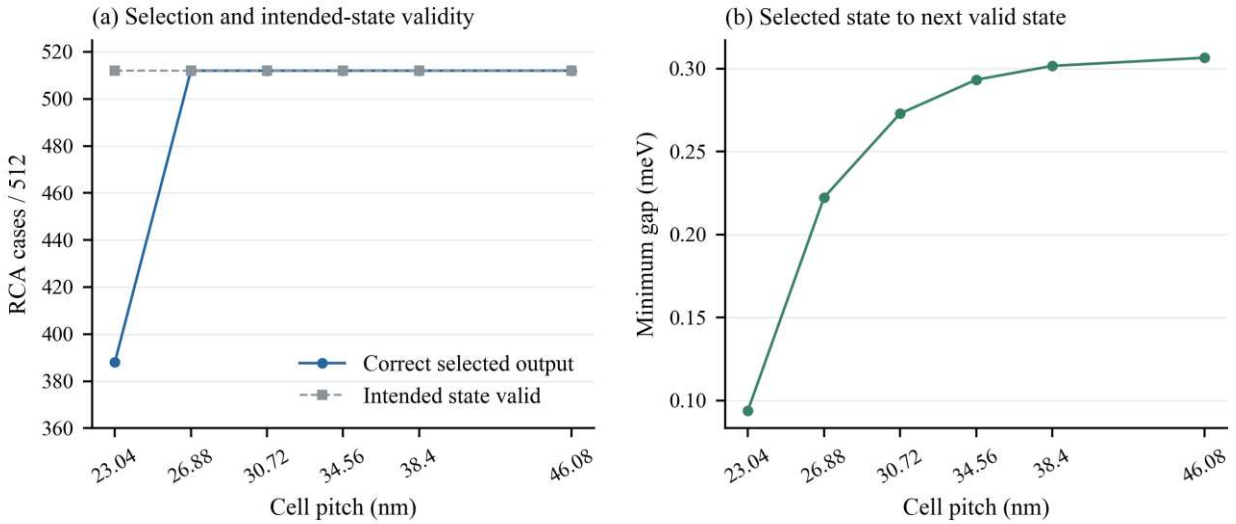


Fig. 12. RCA pitch sensitivity over all 512 intended maps at each spacing. At 23.04 nm the intended states remain physically valid, but 124 selected outputs are wrong. Larger tested pitches preserve all outputs. The gap is between the selected state and the next valid state; rectangles exclude interface and routing hardware.

Table VIII summarizes the verification of all eight full-adder input combinations. For each input, the simultaneously selected (Sum,Carry) pair agrees with the Boolean reference. The table reports one whole-configuration energy E* from Equation (3), exact uniqueness of the selected minimum, and the matching and total SiQAD exported record weights. The exported weight totals ten for each input, and every returned record matches both outputs. These finite solver records are not physical operation probabilities. The configuration energy belongs to the complete charge state and is not allocated separately to Sum and Carry or interpreted as switching dissipation.

TABLE VIII
Verification of every FA11 D full adder input state

ABC	Expected (S,C)	FA11-D (S,C)	E* (eV)	Unique minimum	SiQAD match / weight
000	0, 0	0, 0	0.677502	Yes	10/10
001	1, 0	1, 0	0.235588	Yes	10/10
010	1, 0	1, 0	0.236725	Yes	10/10
011	0, 1	0, 1	0.192539	Yes	10/10
100	1, 0	1, 0	0.282305	Yes	10/10
101	0, 1	0, 1	0.168788	Yes	10/10
110	0, 1	0, 1	0.256789	Yes	10/10
111	1, 1	1, 1	-0.036680	Yes	10/10

E* is the energy of the complete selected charge configuration from Equation (3). Uniqueness is checked by complete ternary enumeration. SiQAD entries are matching and total exported record weights from ten requested restarts per input; they are not physical operation probabilities. Configuration energy is not dissipated switching energy.

Overall, the strongest supported result is exact selected-state arithmetic under explicitly imposed potentials with a defined regeneration contract. The unresolved weakness is physical realization and convergence: sensors, voltage drivers, routing fields, transient trajectories, and nearby charged defects can alter operation. A reliable implementation will need to select or stabilize the desired state while

preserving interface integrity. The metastable counterexamples, finite-budget SiQAD outcomes, and tighter-spacing failures identify concrete targets for that next stage of development.

6 Conclusion and Future Work

An eleven-site simultaneous full adder has been composed into a 22-site 4:2 compressor and a 44-site four-bit RCA under an explicit voltage-input and charge-pair-output interface. Every arithmetic input passes, and independent coupled-state searches agree for all binary intermediate drive maps. The full-map analysis identifies exactly one controller-consistent selected-state map for each external input. It also makes clear why geometry, interface assumptions, and state selection must be specified together.

The fault results support testability and characterize sensitivity. Two patterns detect all enumerated single-net stuck-at models, and three distinguish every model from the healthy circuit. Omissions and displacements remain consequential: the nominal cell is not intrinsically tolerant of all such defects. The tested bias window is encouraging within the static model, whereas screening and placement sensitivity require attention. SiQAD search results corroborate the selected states but expose the practical importance of search effort and metastability.

Further work should realize and characterize the sensing and local drive hardware, solve electrode fields including their back-action, and model transient transitions under a defined clock or settling protocol. Defective coupled arrays, nearby fixed-charge defects, fabrication variability, and interface noise also require direct physical treatment. Measured end-to-end delay and dissipated energy are prerequisites for comparison with implemented arithmetic technologies. Within these limits, the supplied coordinates, SiQAD inputs, exact enumerators, complete truth tables, and fault records provide a reproducible basis for subsequent quantum-dot atomic silicon datapaths.

Data Availability—All data will be available upon request from the corresponding author.

Funding: NO

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