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Limiter-aware reset control of the power synchronization loop for fault recovery of grid-forming inverters

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Abstract

Grid-forming inverters synchronize through a power synchronization loop whose damping falls as the grid becomes stronger and whose transient stability suffers when a fault drives the converter into current limiting. This paper proposes a reset controller for this loop. A constant-in-gain lead-in-phase (CgLp) element, formed by a lead filter followed by a first-order reset element, replaces the linear droop path, so that a reset at a zero crossing of the power error clears the frequency deviation accumulated during a disturbance. A limiter-aware rule adds resets on the unfiltered power error while the current limiter is active. Outside current limiting, stability of the reset loop is certified with the H_β condition for short-circuit ratios from 1.5 to 50. The controller is compared with droop control, two lead compensators, and two virtual synchronous generator damping schemes, all tuned by one rule. On an averaged model it raises the critical clearing time of balanced dips by 42%-84% relative to droop control, and, together with the alternating-inertia scheme, it is the only design that rides through a 120 ms bolted dip at a short-circuit ratio of 10. A switching converter model with an LCL filter reproduces the averaged results within 0.2 percentage points of overshoot at a short-circuit ratio of 2. In a modified IEEE 9-bus system, post-fault power recovery falls from 0.73-0.84 s to 0.29 s. Frequency ramps, during which the power error keeps one sign and no reset occurs, remain a limitation.

Keywords Reset control · Grid-forming inverter · Hybrid dynamical systems · Transient stability · Current limiting · Constant-in-gain lead-in-phase

1 Introduction

Grid-forming (GFM) inverters behave as voltage sources behind an impedance and are expected to support power systems with few synchronous machines [1]. Their internal angle comes from a power synchronization loop that converts the active power error into a frequency deviation, through P-f droop, power synchronization control [2], or a virtual synchronous machine [3]. These schemes are reviewed in [4, 5].

The synchronization loop has two dynamic weaknesses. In small-signal terms it loses damping as the grid becomes stronger: the synchronizing power coefficient grows as the grid impedance falls, the crossover frequency moves towards the pole of the power measurement filter, and the phase margin shrinks [5, 6]. In large-signal terms, a fault drives the converter into current limiting, the loop no longer receives the power it commands, and the frequency deviation built up during the fault can carry the angle past its unstable equilibrium after clearance [7–9]. Linear remedies such as a smaller droop gain, a faster power filter, virtual damping, or a lead network address the first problem, but each trades damping against gain at high frequency, as any linear time-invariant compensator must.

Published remedies for the second problem modify either the current limiter or the angle dynamics. Current-limiting schemes have been designed to keep the converter synchronized during faults [8, 10], and an equivalent-circuit model of the circular current limiter makes the post-fault angle trajectory easier to assess [9]. A dynamic dq-axis current limit combined with a reference power control has been used to prevent repeated limiter activation after a fault [11]. On the angle side, a mode-adaptive power-angle control switches its structure during faults [12], transient damping adds a damping path that acts only during transients [13], and alternating inertia switches the virtual inertia according to the sign of

the acceleration [14]. Rule-based resets or restarts after fault clearance have also been proposed for current-limited GFM converters [15, 16]. In these methods, the frequency deviation accumulated during the fault either decays through the loop dynamics or is cleared by a rule applied after the fault.

Reset control offers a third option, in which the controller clears its own state at an instant set by its input. An integrator whose state is cleared at the zero crossings of its input keeps the gain of an integrator but has only 38° of phase lag [17]. The first-order reset element (FORE) [18], its stability theory [19–21], and describing-function tools [22, 23] led to the constant-in-gain lead-in-phase (CgLp) element [24]. The CgLp has a flat first-harmonic gain and a phase lead, and it has been used mostly in precision motion control [25, 26]. In power systems, reset ideas have been applied to frequency regulation [27, 28] and to the outer loop of a grid-following converter [29]. In a synchronization loop, a reset at a zero crossing of the power error removes the frequency deviation close to the instant at which the angle reaches its new equilibrium, which is the mechanism that matters for fault recovery.

This paper places a CgLp element in the synchronization loop of an AC GFM inverter and extends its reset law for operation in current limiting. The resulting controller, CgLp-L, is a hybrid dynamical system. The study asks whether the reset loop can be certified stable over a wide range of grid strength, whether it improves fault ride-through and post-fault recovery against benchmarks tuned as carefully as itself, whether its zero-crossing logic survives the switching ripple and sampling of a converter, and in which events it fails. The contributions are as follows.

1) A limiter-aware reset law for the synchronization loop. The shaping lead is placed ahead of the FORE so that one reset changes the internal frequency by a bounded amount, and additional resets on the unfiltered power error are enabled only while the current limiter is active.

2) A hybrid stability certificate based on the H_β condition, cast as a linear matrix inequality and shown to be feasible for short-circuit ratios (SCRs) from 1.5 to 50 outside current limiting.

3) A fault-recovery evaluation against droop control, two lead compensators, and two virtual synchronous generator (VSG) damping schemes, all tuned by one rule. CgLp-L raises the critical clearing time of balanced dips by 42%-84% over droop control and shortens post-fault power recovery in a modified IEEE 9-bus system from 0.73-0.84 s to 0.29 s.

4) Confirmation on a 1 MVA two-level converter model with an LCL filter, 10 kHz pulse-width modulation (PWM), and a sampled controller, and a grid-code test set that identifies the events in which the reset logic gives no benefit.

Extended results are given in Online Resource 1.

2 System and models

2.1 Outer control loop

Fig. 1 shows the GFM inverter. The controller filters the measured active and reactive powers with first-order filters of corner frequency ω_f, forms the error $e = P^* - p_f$, and sets the internal frequency through the droop gain m_p:

$$\omega = \omega_b + m_p u, \qquad \dot{\theta} = \omega \tag{1}$$

where u is the compensator output ($u = e$ for droop control). The voltage magnitude follows $E = E_0 + n_q\left(Q^* - q_f\right)$. Overcurrent is limited by a virtual impedance [10, 30]:

$$R_v = k_R(\bar{I} - I_{th})^+, \quad X_v = \sigma R_v, \quad \dot{\bar{I}} = \omega_I(|i| - \bar{I}). \tag{2}$$

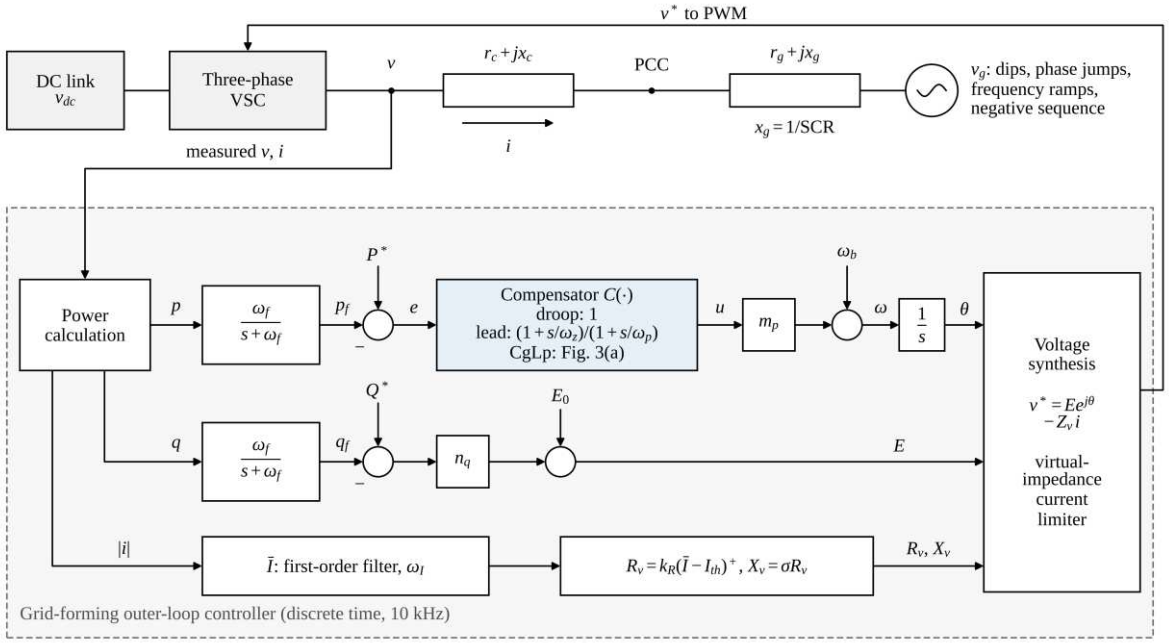

Fig. 1 Grid-forming inverter and outer-loop control structure. $C(\cdot)$ is unity for droop control, a lead network for the linear benchmarks, and the CgLp element of Fig. 3(a) for the proposed controller.

2.2 Averaged model

In per unit on the converter rating, with space vectors in the stationary frame, the averaged model is:

$$v = Ee^{j\theta} - (R_v + jX_v)i, \qquad \frac{x}{\omega_b}\frac{\mathrm{d}i}{\mathrm{d}t} = v - v_g - ri \tag{3}$$

where $x = x_c + 1/\mathrm{SCR}$ and $r = r_c + 0.1/\mathrm{SCR}$. The grid voltage v_g can dip, jump in phase, ramp in frequency, or contain a negative-sequence component. The network is integrated in Simulink with the ode4 solver at a step of 20 μs, and the outer controller runs as a discrete block at 10 kHz with a one-sample delay on its commands. Table 1 lists the parameters. A lead network with ratio a centered at ω_m has $\omega_z = \omega_m/\sqrt{a}$ and $\omega_p = \omega_m\sqrt{a}$.

Table 1 System and controller parameters

Parameter	Value
Base frequency; coupling impedance $r_c + jx_c$	50 Hz; 0.01 + j0.10 p.u.
Grid reactance x_g; ratio x_g/r_g	1/SCR p.u.; 10
Set-points P^*, Q^*	0.8 p.u., 0
P-f droop m_p; Q-V droop n_q; power filter corner ω_f	2%; 5%; $2\pi \cdot 2$ rad/s
Current limiter I_{th}, k_R, σ, ω_I	1.0 p.u., 1.5, 1, 1000 rad/s
Controller sample time; solver step	100 μs; 20 μs
Lead benchmarks: a, ω_m	3 and 4.6 at 25.6 rad/s; re-tuned: 8 at 51.2 rad/s
CgLp: ω_r, ω_t, $\omega_{r\alpha}$; γ; reset band δ_r	14.91, 213, 9.21 rad/s; 0; 0.02
VSG-TD: k_J, k_D, ω_d	0.5, 0.5, $2\pi \cdot 2$ rad/s
VSG-AI: k_J, inertia ratio ρ	1, 1.5

Note: all quantities are in per unit on the converter rating unless stated otherwise.

2.3 Switching model

The switching model in Fig. 2 is built in Simscape Electrical. A 1 MVA, 690 V two-level insulated gate bipolar transistor (IGBT) bridge on an ideal 1.2 kV DC link is modulated by a 10 kHz carrier with min-max zero-sequence injection. The LCL filter has $l_f = l_g = 0.05$ p.u. (75.8 μH) and $c_f = 0.15$ p.u. (1.0 mF), with a resistance of 0.005 p.u. per inductor, so that the two inductors reproduce the coupling impedance of the averaged model. The controller samples v_c, i_f, and i_g at the carrier valley, computes p and q from v_c and i_g, and runs the same outer-loop code. The converter voltage reference follows the power synchronization structure of [2]:

$$u = Ee^{j\theta} - Z_v i_g - R_a \mathrm{HPF}(i_f) \qquad (4)$$

where $R_a = 0.5$ p.u., acting through a 100 Hz high-pass filter (HPF), damps the LCL resonance and has no effect in steady state. A delay compensation of 1.5 samples is applied. Cascaded voltage and current proportional-integral (PI) loops were rejected because, in a discrete eigenvalue analysis, they either became unstable against the stiff grid or left a lightly damped mode of 1-2 Hz inside the bandwidth of the synchronization loop. With (4), the worst damping ratio of the electrical modes is 0.20 over the SCR range of 1.5-50. The power stage is solved with a step of 0.2 μs; Sect. 6.1 explains why a coarser step is not acceptable for a reset controller.

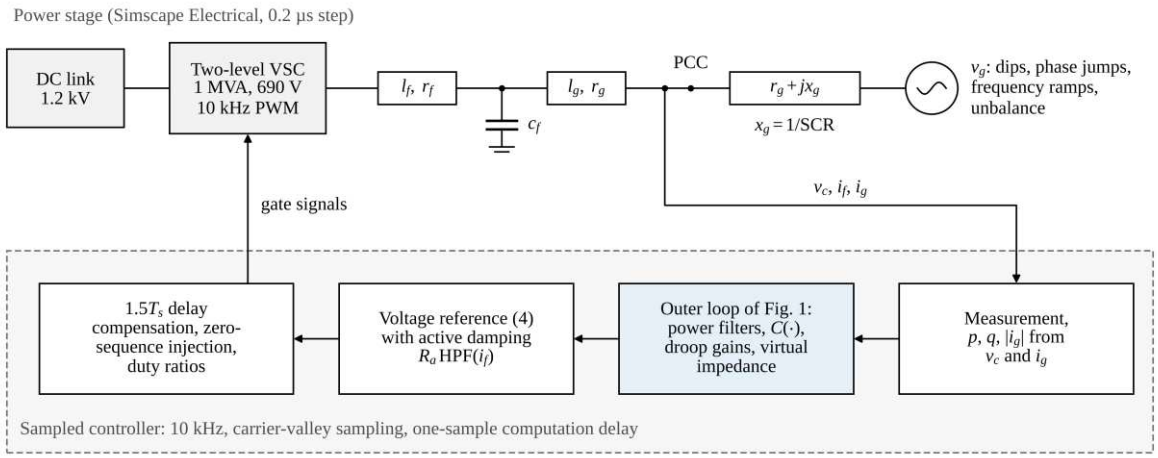

Fig. 2 Switching model: two-level converter with LCL filter on a Thevenin grid and sampled controller.

2.4 Strong-grid problem

Linearizing (3) for a quasi-static network gives the loop gain $L(s) = C(s)m_pK_s\omega_f/[s(s+\omega_f)]$ with $K_s = EV_g\cos\delta_0/x$ and the damping ratio $\zeta \approx 0.5\sqrt{\omega_f/(m_pK_s)}$. With droop control, the dominant mode has $\zeta = 0.58$ at an SCR of 2 and 0.27 at an SCR of 20, and the phase margin falls from 57.8° to 29.9°. A power step from 0.6 to 0.8 p.u. at an SCR of 20 overshoots by 41.8%. Lead networks with ratio a restore the margin but raise the gain above crossover by a factor of a (Fig. S1 in Online Resource 1).

3 Limiter-aware CgLp controller

3.1 Element and design

The FORE with corner frequency $\omega_{r\alpha}$ and reset coefficient γ is defined as:

$$\begin{cases} \dot{x}_r = -\omega_{r\alpha}x_r + \omega_{r\alpha}v & v \neq 0 \\ x_r^+ = \gamma x_r & v = 0 \end{cases} \quad (5)$$

Its first-harmonic describing function [22] is:

$$\begin{cases} N(j\omega) = \frac{\omega_{r\alpha}}{j\omega+\omega_{r\alpha}}(1 + j\Theta_D) \\ \Theta_D = \frac{2\omega^2(1-\gamma)(1+e^{-\pi\omega_{r\alpha}/\omega})}{\pi(\omega^2+\omega_{r\alpha}^2)(1+\gamma e^{-\pi\omega_{r\alpha}/\omega})} \end{cases} \quad (6)$$

which gives 38.1° of phase lag at high frequency for $\gamma = 0$, compared with 90° for the linear filter. A shaping lead $C_L(s)$ makes the first-harmonic gain flat between ω_r and ω_t [24]:

$$\begin{cases} C_L(s) = \frac{1+s/\omega_r}{1+s/\omega_t}, \quad \omega_{r\alpha} = \frac{\omega_r}{\alpha} \\ \alpha = \sqrt{1+\Theta_\infty^2}, \quad \Theta_\infty = \frac{4(1-\gamma)}{\pi(1+\gamma)} \end{cases} \quad (7)$$

The lead is placed ahead of the FORE, as shown in Fig. 3(a), so that $u = x_r$ and a reset changes the internal frequency by at most $m_p(1-\gamma)x_r$. With the opposite order, the lead would amplify each reset step by ω_t/ω_r, which produced a frequency spike of 3.7 Hz in a preliminary test. Equation (6) agrees with simulated FORE responses to within 0.035° and 0.035% (Fig. S2 in Online Resource 1).

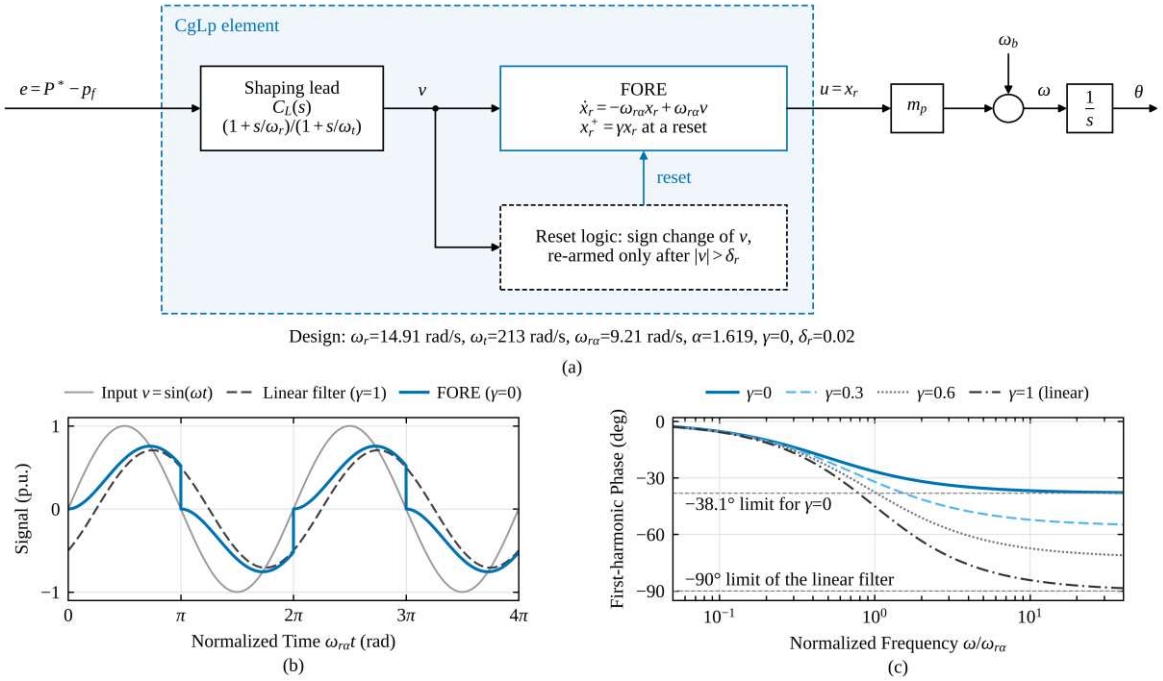

Fig. 3 CgLp element and FORE behavior. (a) CgLp element in synchronization loop. (b) Response of a FORE with $\gamma = 0$ to a sinusoid, compared with linear filter ($\gamma = 1$). (c) First-harmonic phase of FORE for several values of γ.

The design starts from the droop crossover at an SCR of 20, $\omega_c = 21.3$ rad/s, with $\gamma = 0$ ($\alpha = 1.619$), $\omega_r = k_r \omega_c$, and $\omega_t = k_t \omega_c$. A grid search over $\gamma \in \{0, 0.2, 0.4, 0.6\}$, $k_r \in \{0.35, 0.5, 0.7, 1.0, 1.4\}$, and $k_t \in \{10, 20\}$ with the rule of Sect. 5 selects $\gamma = 0$, $k_r = 0.7$, and $k_t = 10$. At ω_c, the element adds 16.7° of phase at a gain of 0.83, and its gain at 50 Hz is 0.55, compared with 2.97 and 4.53 for the leads with $a = 3$ and $a = 4.6$, respectively.

3.2 Reset band and limiter-aware reset

To prevent noise-driven resets, a reset is permitted only if $|v|$ has exceeded a band $\delta_r = 0.02$ since the previous reset [21]. The band only removes resets, so the analysis in Sect. 4 still applies.

The reset rule acts on the shaped error of the filtered power. During current limiting, this signal can keep one sign long after the instantaneous power has passed its set-point, because the power filter lags. This causes a loss of synchronism after large phase jumps (Sect. 7). The variant CgLp-L therefore also resets the FORE at the zero crossings of the unfiltered error $e_r = P^* - p$, but only while the limiter is engaged ($\bar{I} > I_{th}$). Outside current limiting, CgLp-L is identical to the CgLp. Holding the FORE state at zero during limiting was also tried and rejected, because the converter then remained in current limiting.

4 Stability analysis

For small deviations, the droop gain, network, power filter, and shaping lead form a linear plant $\dot{x}_p = A_p x_p + B_p u$, $y = C_p x_p$, with the FORE input $v = -y$. The closed loop with $x = \left[x_p^{\mathrm{T}}\ x_r\right]^{\mathrm{T}}$ is:

$$\begin{cases} \dot{x} = A_{cl}x & y \neq 0 \\ x^{+} = A_R x & y = 0 \end{cases} \quad (8)$$

where $A_{cl} = \left[A_p \; B_p; -\omega_{r\alpha}C_p \; -\omega_{r\alpha}\right]$ and $A_R = \mathrm{diag}(I, \gamma)$.

By the H_β condition [19], (8) is globally uniformly asymptotically stable if A_{cl} is Hurwitz, $|\gamma| \leq 1$, and there exist β and $\rho > 0$ such that $H_\beta(s) = \left[\beta C_p \; \rho\right](sI - A_{cl})^{-1}[0 \; 1]^{\mathrm{T}}$ is strictly positive real. With the Kalman-Yakubovich-Popov lemma, this becomes the linear matrix inequality (LMI):

$$A_{cl}^{\mathrm{T}}P + PA_{cl} \prec 0, \quad P = \begin{bmatrix} P_{11} & \beta C_p^{\mathrm{T}} \\ \beta C_p & \rho \end{bmatrix} \succ 0 \quad (9)$$

which is linear in (P_{11}, β, ρ). The LMI is feasible at every SCR between 1.5 and 50 (Table 2), and $\mathrm{Re}\, H_\beta(j\omega)$ is positive on 20000 frequencies from 10^{-3} to 10^{5} rad/s. The Lyapunov function $x^{\mathrm{T}}Px$ does not increase at any reset on $y = 0$, so any subset of these resets, including the reset band, preserves stability. The certificate is local and does not cover the current-limited mode in which CgLp-L adds resets.

The LMI was solved with the MATLAB LMI Lab (feasp). The smallest value of Re $H_\beta(j\omega)$ lies at the upper end of the frequency grid because Re H_β decays as ω^{-2}; the scaled quantity ω^2 Re $H_\beta(j\omega)$ evaluated at 10^6 rad/s is positive at every SCR (0.14 at an SCR of 2 and 3.07 at an SCR of 20). The scale of (β, ρ) differs between operating points only because feasp returns an arbitrary feasible point. The slowest eigenvalue of the base linear system moves from −3.98 s^{-1} at an SCR of 1.5 to −2.54 s^{-1} at an SCR of 50.

Table 2 H_β certificate for the CgLp loop ($\gamma = 0$). max Re $\lambda(A_{cl})$ is the slowest eigenvalue of the base linear system, $t_{min} < 0$ indicates feasibility, and the last column is the smallest value of Re $H_\beta(j\omega)$ on 20 000 frequencies from 10^{-3} to 10^{5} rad/s

SCR	max Re $\lambda(A_{cl})$ (s^{-1})	t_{min}	β	ρ	$\min_\omega$ Re $H_\beta(j\omega)$
1.5	−3.98	-1.89×10^{-3}	6.78×10^{-4}	5.43×10^{-2}	5.0×10^{-11}
2	−3.83	-2.27×10^{-5}	6.80×10^{-5}	1.54×10^{-2}	1.4×10^{-11}
3	−3.62	-3.28×10^{-4}	2.51×10^{-4}	4.81×10^{-2}	4.4×10^{-11}
5	−3.38	−0.170	0.217	50.6	4.7×10^{-8}
10	−3.07	−0.198	0.348	68.7	6.3×10^{-8}
15	−2.90	-1.97×10^{-3}	1.31×10^{-3}	0.171	1.6×10^{-10}
20	−2.79	-3.62×10^{-3}	2.22×10^{-3}	0.333	3.1×10^{-10}
30	−2.67	-2.33×10^{-3}	2.28×10^{-3}	0.290	2.7×10^{-10}
50	−2.54	−0.189	0.716	102.8	9.5×10^{-8}

5 Benchmarks and common tuning

Droop control with a first-order power filter is equivalent to a VSG with inertia $J = 1/(m_p\omega_f)$ and damping $D_p = 1/m_p$ acting on the unfiltered power. Two VSG damping schemes with the same static droop are added. With $\Delta\omega = \omega - \omega_b$ and $e_r = P^* - p$, they are:

$$\begin{cases} J\frac{\mathrm{d}\Delta\omega}{\mathrm{d}t} = e_r - D_p\Delta\omega - D_t(\Delta\omega - \Delta\omega_f) \\ \frac{\mathrm{d}\Delta\omega_f}{\mathrm{d}t} = \omega_d(\Delta\omega - \Delta\omega_f) \end{cases} \quad (10)$$

where $J = k_J/(m_p\omega_f)$ and $D_t = k_D D_p$. The VSG with transient damping (VSG-TD) [13] uses the term D_t. The VSG with alternating inertia (VSG-AI) sets $D_t = 0$ and switches the inertia [14]: J is multiplied by ρ while $|\Delta\omega|$ grows and is divided by ρ otherwise.

Every family is tuned with the rule used for the CgLp. Each candidate is simulated for a power step from 0.6 to 0.8 p.u. at SCRs of 20 and 2. A design is admissible if the overshoot of p_f is below 3% at both SCRs. Among the admissible designs, the one with the lowest integral of time-weighted absolute error (ITAE) at an SCR of 20 is chosen, provided that the root mean square (RMS) frequency jitter under 0.02 p.u. power measurement noise does not exceed 0.6 mHz. Otherwise, the smallest worst-case overshoot decides. The grids cover the corner frequency of the droop filter (×1 to ×4), the lead ratio (1.5-8) and center (0.5 to 2 times 25.6 rad/s), VSG-TD (k_J: 0.5-2; k_D: 0.5-8; $\omega_d/2\pi$: 0.5-2 Hz), and VSG-AI (k_J: 0.5-2; ρ: 1.5-4), with 132 designs in total (Fig. S3 in Online Resource 1).

Table 3 Designs selected by the common tuning rule (averaged model)

Controller	SCR of 20			SCR of 2		Jitter (mHz)	Admissible
	Overshoot (%)	Settling Time (s)	ITAE (10^{-3} p.u.·s^2)	Overshoot (%)	Settling Time (s)		
Droop, filter ×4	13.67	0.126	0.25	0.00	0.338	0.97	No
Lead, re-tuned	7.75	0.201	0.34	0.73	0.300	1.24	No
VSG-TD	0.00	0.230	1.38	3.99	0.689	0.57	No
VSG-AI	0.84	0.408	1.93	1.21	0.422	0.53	Yes
CgLp	0.29	0.247	1.06	2.34	0.459	0.45	Yes

Only the CgLp and VSG-AI meet the rule (Table 3). The CgLp has 45% lower ITAE, 39% shorter settling time at an SCR of 20, and 15% less jitter, whereas VSG-AI settles slightly faster at an SCR of 2. The re-tuned lead is the fastest but overshoots by 7.75% and has the highest jitter, and additional transient damping makes VSG-TD worse.

6 Single-inverter results

6.1 Power steps on averaged and switching models

On the averaged model (dotted lines in Fig. 4), the CgLp keeps the overshoot at 0.2%-2.3% for SCRs from 2 to 30 and the frequency excursion at 0.13-0.14 Hz, whereas the leads overshoot by up to 22% with a frequency kick of 0.6-1.6 Hz (Table 4). The first reset, 53 ms after the step at an SCR of 20, steps the frequency from 50.12 Hz to 50.00 Hz and removes the deviation that would carry the angle past its equilibrium. With the reset disabled ($\gamma = 1$), the overshoot is 58.6%. At an SCR of 2, the CgLp settles in 0.46 s, slower than the leads, because of the FORE pole.

With the reset disabled, the overshoot exceeds that of droop control at every SCR (Table 4, last column). The damping of the CgLp therefore comes from the reset action and not from its linear part.

Table 4 Power-step metrics versus SCR (averaged model): overshoot of p_f (%) / 2% settling time (s) / peak frequency deviation (Hz). The last column is the CgLp with the reset disabled ($\gamma = 1$)

SCR	Droop	Lead, a = 3	Lead, a = 4.6	Lead, re-tuned	VSG-TD	VSG-AI	CgLp	CgLp, reset off
2	10.9 / 0.536 / 0.20	0.6 / 0.280 / 0.60	0.0 / 0.367 / 0.92	0.7 / 0.300 / 1.60	4.0 / 0.689 / 0.11	1.2 / 0.422 / 0.10	2.3 / 0.459 / 0.14	21.6 / 0.945 / 0.14

SCR	Droop	Lead, a = 3	Lead, a = 4.6	Lead, re-tuned	VSG-TD	VSG-AI	CgLp	CgLp, reset off
5	26.6 / 0.522 / 0.20	6.2 / 0.252 / 0.60	0.4 / 0.114 / 0.92	3.5 / 0.287 / 1.60	3.7 / 0.434 / 0.10	3.2 / 0.391 / 0.08	1.3 / 0.537 / 0.13	41.1 / 1.086 / 0.14
10	35.6 / 0.564 / 0.20	12.2 / 0.188 / 0.60	6.6 / 0.137 / 0.92	4.9 / 0.227 / 1.60	1.2 / 0.222 / 0.09	2.4 / 0.437 / 0.07	0.2 / 0.200 / 0.13	52.0 / 1.248 / 0.13
20	41.8 / 0.610 / 0.20	19.1 / 0.162 / 0.60	15.4 / 0.142 / 0.92	7.8 / 0.201 / 1.60	0.0 / 0.230 / 0.08	0.8 / 0.408 / 0.07	0.3 / 0.247 / 0.13	58.6 / 1.278 / 0.13
30	44.3 / 0.585 / 0.20	22.2 / 0.157 / 0.60	18.7 / 0.145 / 0.92	10.7 / 0.200 / 1.60	0.0 / 0.284 / 0.08	0.3 / 0.391 / 0.06	0.2 / 0.247 / 0.13	60.3 / 1.367 / 0.13

With a solver step of 1 μs, the PWM edges are quantized to 1% of the period. This creates an RMS fluctuation of 0.018 p.u. in the measured power at an SCR of 20 and 18 resets in the 1.5 s after a step. With a step of 0.2 μs, the fluctuation falls to 0.0024 p.u. and the number of resets to 3. A digital CgLp therefore needs a PWM resolution well below 1%, which current digital signal controllers provide, or a reset band set from the measured ripple. All switching results use the step of 0.2 μs.

Table 5 and Fig. 4 compare the two models. At an SCR of 2, they agree for every controller within 0.2 percentage points of overshoot and 4 ms of settling time. At an SCR of 20, the agreement holds for droop control, the VSG schemes, and the CgLp (0.42% compared with 0.29%), but the leads lose damping on the switching model (25.8% compared with 15.4% for $a = 4.6$). Only the leads have a large gain above about 10 Hz, where the filter capacitor, active damping, and modulation delay act. The CgLp produces no resets in 1.5 s of steady operation, and its RMS frequency jitter (0.19 mHz) is below that of droop control (0.27 mHz) and the leads (0.91-1.20 mHz).

Table 5 Power step from 0.6 to 0.8 p.u. on switching (SW) and averaged (AV) models

Controller	SCR 20		SCR 2	
	SW	AV	SW	AV
Droop	45.31/0.608	41.77/0.610	11.11/0.536	10.90/0.536
Lead, $a = 4.6$	25.79/0.240	15.39/0.142	0.04/0.364	0.00/0.367
Lead, re-tuned	13.29/0.219	7.75/0.201	0.84/0.298	0.73/0.300
VSG-TD	0.22/0.235	0.00/0.230	4.02/0.689	3.99/0.689
VSG-AI	0.68/0.401	0.84/0.408	1.31/0.420	1.21/0.422
CgLp, CgLp-L	0.42/0.277	0.29/0.247	2.44/0.463	2.34/0.459

Note: each entry gives the overshoot of p_f (%)/the 2% settling time (s). Switching-model metrics use a 20 ms moving average of p_f.

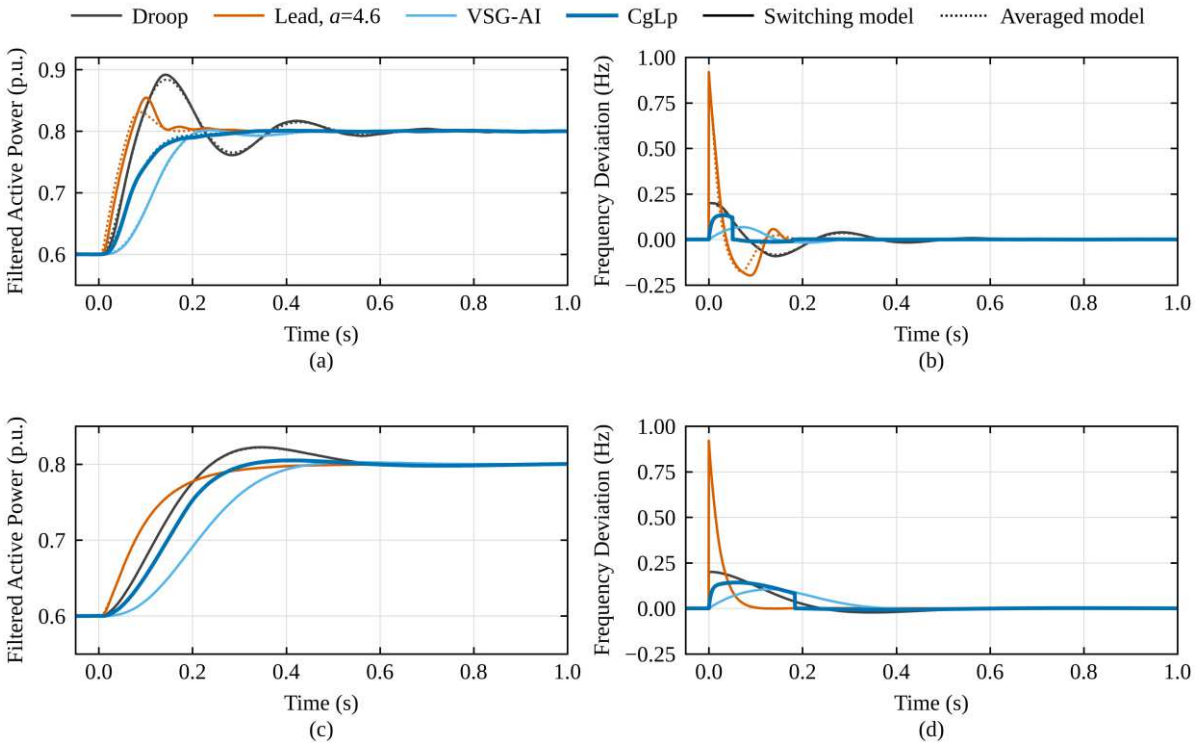

Fig. 4 Power step from 0.6 to 0.8 p.u. on switching model (solid lines) and averaged model (dotted lines). (a) Filtered active power at SCR of 20. (b) Internal frequency deviation at SCR of 20. (c) Filtered active power at SCR of 2. (d) Internal frequency deviation at SCR of 2.

6.2 Unbalance and faults

With a 5% negative-sequence grid voltage, the 100 Hz power ripple crosses the reset band and causes about 200 resets per second. A notch filter at twice the fundamental frequency on the measured power removes them and restores a step overshoot of 1.5% (Table S1 in Online Resource 1).

Table 6 gives the critical clearing time (CCT) for balanced dips, found by bisection over 0-600 ms with a 6 s run and settling tolerances of 0.02 Hz and 0.02 p.u.. The CgLp increases the CCT of droop control by 7%-11% for dips to 0.3 p.u. and by 12%-17% for bolted dips, whereas the hand-designed leads shorten it. CgLp-L increases the CCT much further, to 258-327 ms and 190-236 ms, respectively, which is 42%-84% above droop control and 29%-64% above the CgLp. After clearing, the instantaneous power crosses its set-point before the filtered power does, and the additional resets clear the FORE state earlier. A spot check (bolted dip, SCR of 20) confirms that all dips of 80-185 ms are cleared.

Table 6 Critical clearing time (CCT) on the averaged model

Dip	SCR	CCT (ms)					
		Droop	Lead, a=3	Lead, a=4.6	Reset Off	CgLp	CgLp-L
0.3 p.u.	2	229.7	227.9	226.8	235.6	253.7	327.0
	5	205.1	203.3	202.7	210.9	222.1	301.2
	10	179.3	177.5	177.0	185.2	192.8	275.4
	20	161.7	160.0	158.8	167.6	172.9	257.8
0 p.u.	2	143.0	136.5	133.6	150.0	167.0	236.1
	5	127.7	121.3	118.4	135.4	147.1	218.6
	10	113.1	107.2	104.3	120.1	128.9	201.6
	20	103.1	97.3	94.3	109.6	116.0	189.8

Note: "Reset off" denotes the CgLp with $\gamma = 1$; the dip column gives the residual grid voltage.

On the switching model, a 120 ms bolted dip at an SCR of 10 gives the same outcome as on the averaged model (Fig. 5(a) and (b)). Droop control, both leads, and VSG-TD slip a pole 1.0-1.6 s after the start of the dip, whereas VSG-AI, the CgLp, and CgLp-L recover and leave current limiting after 0.60, 0.57, and 0.15 s, respectively. The virtual-impedance limiter, tuned on the averaged model, is poorly damped with the LCL filter: the current oscillates between about 0.5 p.u. and 2.7 p.u. during limiting, which also triggers the additional resets of CgLp-L more often than on the averaged model.

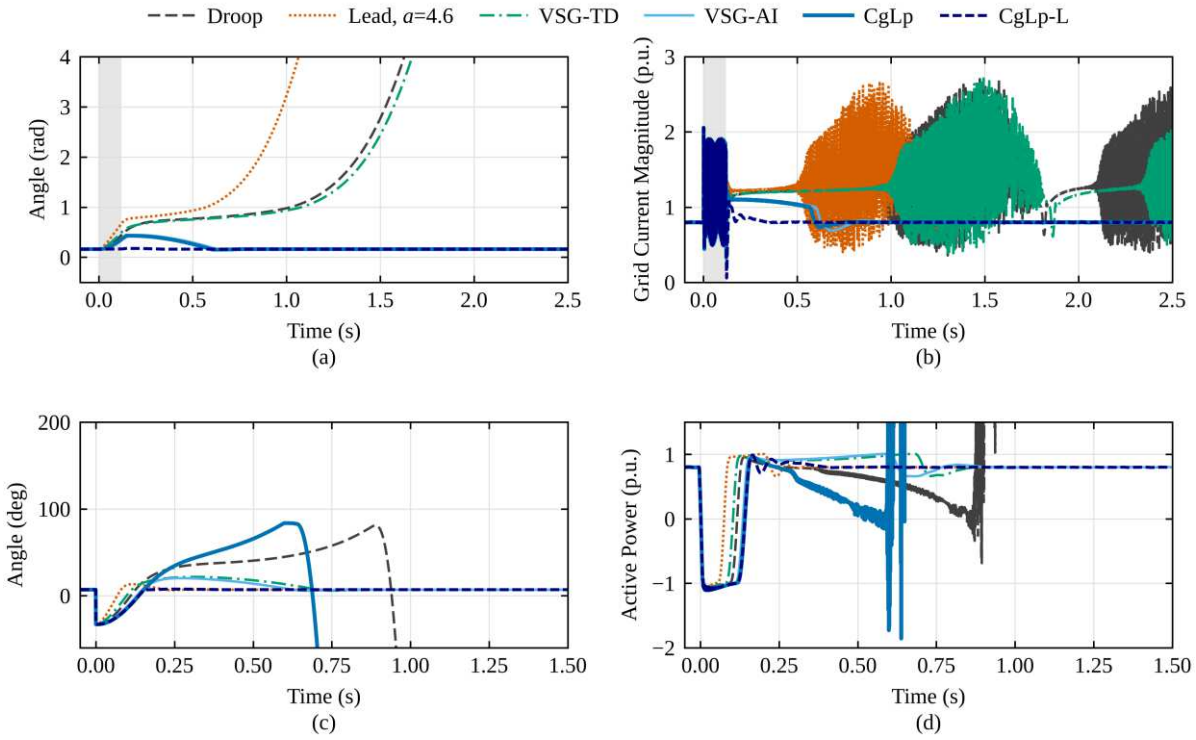

Fig. 5 Switching-model results. (a) Angle for a 120 ms bolted dip (shaded) at SCR of 10. (b) Grid current magnitude for the same dip. (c) Angle after a 40° phase jump at SCR of 20. (d) Active power (2 ms average) after the same jump.

7 Grid-code tests

The specifications of the Australian Energy Market Operator (AEMO) [31] and the North American Electric Reliability Corporation (NERC) [32] assess GFM plants by their responses to phase steps, frequency ramps, and voltage disturbances. The averaged model is extended with a frequency ramp and a step change of grid impedance. Every controller is tested with ramps of -0.5, -1, and -2 Hz/s (to a deviation of 0.5 Hz, from $P = 0.3$ p.u.), phase jumps of 10°-60° at SCRs of 20 and 5, dips to 0.5, 0.2, and 0 p.u. at SCRs of 2-10, and grid-strength steps between SCRs of 20, 2, and 1.5. The internal frequency is assessed with rate of change of frequency (RoCoF) meters with 100 ms and 500 ms windows, the range of averaging windows used in withstand requirements [33]. Table 7 gives the complete results.

Table 7 Grid-code test set (averaged model). Overshoot of active power relative to its change; angle overshoot and 0.5° settling time after phase jumps; time for p to stay within 0.04 p.u. of 0.8 p.u. after a dip; 2% settling

time of p after a grid-strength step; maximum RoCoF seen by a 500 ms meter. "Slip": loss of synchronism; "> 1.4": not settled within the 1.5 s run

Test and metric	Droop	Lead 4.6	Lead re-t.	VSG-TD	VSG-AI	CgLp	CgLp-L
Ramp −1 Hz/s: P overshoot (%)	13.9	0.8	4.4	13.8	24.3	28.1	28.1
Ramp −2 Hz/s: P overshoot (%)	24.7	1.7	8.7	27.3	40.6	41.1	41.1
Jump 10°, SCR 20: δ overshoot (deg) / 0.5° settling (s)	5.3 / 0.55	1.2 / 0.10	0.5 / 0.13	2.1 / 0.21	2.6 / 0.35	1.4 / 0.20	1.4 / 0.20
Jump 25°, SCR 20: δ overshoot (deg) / 0.5° settling (s)	17.9 / 1.02	2.6 / 0.13	1.3 / 0.20	7.2 / 0.52	8.2 / 0.56	3.6 / 0.30	3.6 / 0.30
Jump 40°, SCR 20: δ overshoot (deg) / 0.5° settling (s)	8.3 / > 1.4	3.1 / 0.16	2.0 / 0.23	12.3 / 0.74	12.0 / 0.71	slip	19.7 / > 1.4
Jump 60°, SCR 20: δ overshoot (deg) / 0.5° settling (s)	slip	3.2 / 0.19	3.0 / 0.29	18.5 / 1.07	15.6 / 0.88	slip	21.5 / > 1.4
Jump 40°, SCR 5: δ overshoot (deg) / 0.5° settling (s)	13.9 / 0.78	0.2 / 0.12	1.4 / 0.33	5.6 / 0.43	6.1 / 0.57	3.7 / 0.36	3.7 / 0.36
Jump 60°, SCR 5: δ overshoot (deg) / 0.5° settling (s)	20.1 / 1.00	0.1 / 0.15	2.0 / 0.37	9.1 / 0.73	8.6 / 0.67	5.5 / 0.43	5.5 / 0.43
Dip to 0.5 p.u., 150 ms, SCR 5: P recovery (s)	0.56	0.29	0.31	0.52	0.46	0.26	0.25
Dip to 0.2 p.u., 150 ms, SCR 5: P recovery (s)	1.16	0.95	0.91	1.09	0.71	0.47	0.42
Dip to 0.2 p.u., 150 ms, SCR 2: P recovery (s)	0.80	0.77	0.76	0.77	0.53	0.41	0.38
Dip to 0 p.u., 120 ms, SCR 5: P recovery (s)	1.38	slip	1.48	1.31	0.71	0.45	0.39
Dip to 0 p.u., 120 ms, SCR 10: P recovery (s)	slip	slip	slip	slip	0.80	0.58	0.47
SCR 20 → 2: 2 % settling (s)	0.52	0.33	0.28	0.58	0.46	0.46	0.46
SCR 2 → 20: 2 % settling (s)	1.12	0.66	0.75	0.86	1.04	0.91	0.91
SCR 20 → 1.5: 2 % settling (s)	0.60	0.47	0.40	0.67	0.37	0.51	0.51
0.2 p.u. set-point step, SCR 20: RoCoF, 500 ms (Hz/s)	0.41	1.84	3.20	0.17	0.13	0.26	0.26
Jump 10°, SCR 20: RoCoF, 500 ms (Hz/s)	0.94	1.46	1.69	1.00	0.78	0.80	0.80
Jump 25°, SCR 20: RoCoF, 500 ms (Hz/s)	2.23	3.16	2.75	2.14	1.75	1.79	1.79

The CgLp gives the fastest recovery after every dip (0.26-0.58 s, compared with 0.46-0.80 s for VSG-AI), and CgLp-L is faster still (0.25-0.47 s). Only VSG-AI and the two CgLp variants survive the 120 ms bolted dip at an SCR of 10 (Fig. 6(c) and (d)). After a set-point step, the resets of the CgLp register 0.26-0.29 Hz/s on a 500 ms meter, which is below droop control and far below the leads, whose frequency kick gives 1.84-3.20 Hz/s. The reset steps are 0.12 Hz after set-point steps and up to 0.95 Hz after phase jumps, with the angle remaining continuous.

The CgLp performs worst on frequency ramps (Fig. 6(a) and (b)). It overshoots the final power by 28% at -1 Hz/s and by 41% at -2 Hz/s, compared with 0.8%-1.7% for the lead with $a = 4.6$. No reset occurs during a ramp, because the error does not change sign, and the controller behaves as its base linear system, which is less damped than droop control. After phase jumps up to 25°, and up to 60° at an SCR of 5, the CgLp ranks behind the leads and ahead of droop control and the VSG schemes. At an SCR of 20, however, the CgLp loses synchronism after the 40° and 60° jumps (Fig. S4 in Online Resource 1). The jump drives the converter into current limiting. The instantaneous power passes its set-point within 0.15 s but the filtered power does not, so no reset occurs, and the FORE state holds the frequency about 1 Hz high until the angle runs away. Droop control also slips after the 60° jump. CgLp-L resets four to five times during limiting and holds the overshoot at 20°-22°, but its return to equilibrium through the FORE tail takes more than 1.4 s. On the switching model, the CgLp again slips after the 40° jump, droop control slips as well (a marginal case on the averaged model), and CgLp-L

resynchronizes with 0.6° of overshoot in 0.32 s (Fig. 5(c) and (d)).

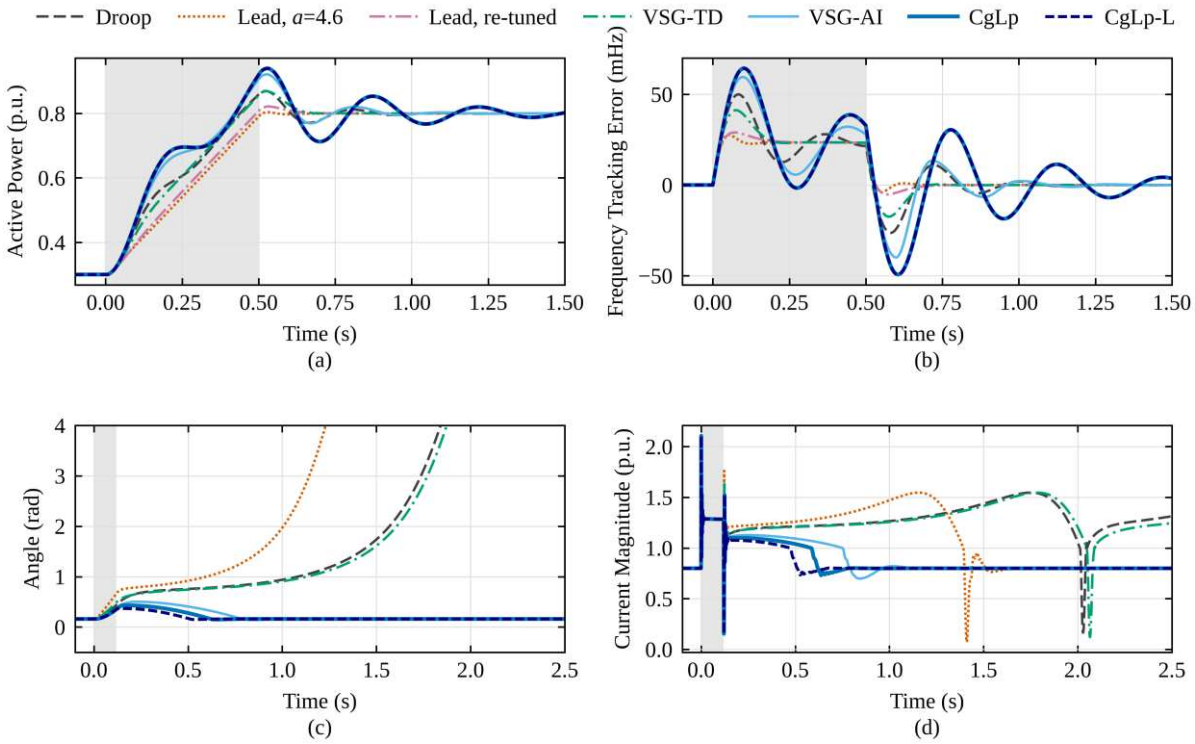

Fig. 6 Grid-code tests on averaged model. (a) Active power during a -1 Hz/s ramp (shaded) at SCR of 20. (b) Frequency tracking error during the same ramp; CgLp and CgLp-L coincide. (c) Angle after a 120 ms bolted dip (shaded) at SCR of 10. (d) Current magnitude for the same dip.

8 Multi-machine study

The IEEE 9-bus system [34] is modified as shown in Fig. 7 (100 MVA base). Bus 1 keeps the 247.5 MVA hydro unit as a classical machine (transient reactance of 0.0608 p.u., $H = 23.64$ s) with a 5% droop governor of 0.5 s [35]. GFM-A (192 MVA, 163 MW) and GFM-B (128 MVA, 85 MW) replace the units at buses 2 and 3. Each unit has its own 10 kHz controller, a coupling impedance of $0.01 + j0.10$ p.u. on its rating, and the original transformer. A 50 MW GFL PV plant (synchronous-frame phase-locked loop of 20 Hz, 2 ms current loop) is added at bus 8, whose load is raised by 50 MW. Lines include series R-L elements and half of their charging capacitance at each end, and the network is integrated in a common frame rotating at 50 Hz. A weak variant doubles all line impedances. The events are a conductance step of 0.3 p.u. at bus 5, a set-point step of $+0.2$ p.u. of GFM-B, a 100 ms fault at bus 7 (bus voltage of 0.21 p.u.), and the trip of line 5-7. Both GFM units use the same controller, and three mixed cases pair the CgLp with droop control and VSG-AI.

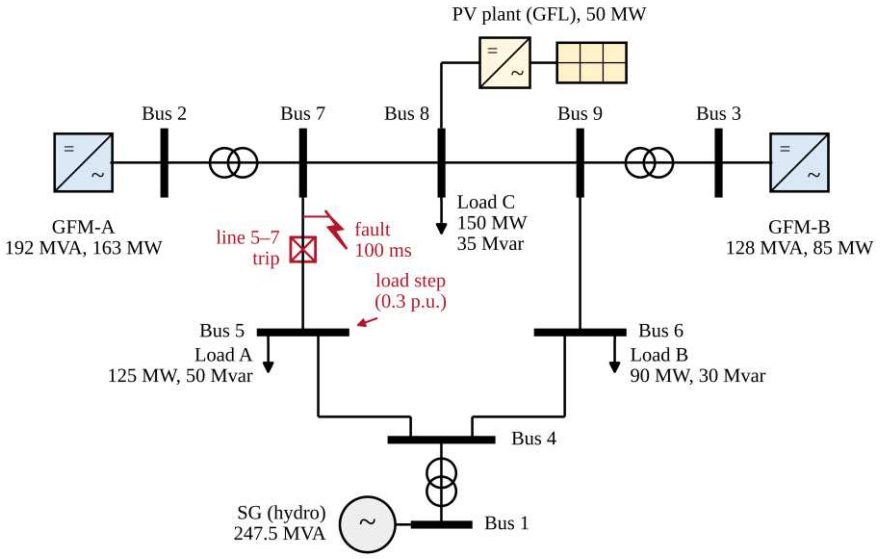

Fig. 7 Modified IEEE 9-bus system with an SG, two GFM inverters, and a GFL PV plant. Disturbance locations are marked in red.

Table 8 Multi-machine results on the nominal network

GFM-A and GFM-B	SG Nadir (Hz)	Overshoot of $p_{f,B}$ (%)	Recovery of p_A (s)	Settling of p_A (s)
Droop	49.934	48.2	0.82 (0.96)	1.71
Lead, $a = 4.6$	49.929	23.1	0.81 (0.91)	1.84
Lead, re-tuned	49.931	26.1	0.81 (0.93)	1.81
VSG-TD	49.934	24.1	0.84 (0.96)	1.74
VSG-AI	49.936	23.7	0.73 (0.36)	1.75
CgLp	49.937	25.1	0.31 (0.30)	2.29
CgLp-L	49.937	25.1	0.29 (0.27)	2.29
CgLp + droop	49.935	52.5	0.31 (0.29)	2.27
CgLp + VSG-AI	49.937	24.2	0.31 (0.29)	2.29
Droop + CgLp	49.935	22.3	0.83 (0.98)	1.72

Note: the SG nadir is for the load step, the overshoot for the set-point step of GFM-B, the recovery for the fault at bus 7 (weak network in brackets), and the settling for the line trip. Powers are on each unit's own base. Complete results for the nominal and weak networks are given in Table S2 of Online Resource 1.

No unit loses synchronism (Table 8, Fig. 8). The SG dominates the frequency nadir after the load step, which is 49.93-49.94 Hz for all controllers. The CgLp shortens the recovery of the GFM-A power after the fault from 0.73-0.84 s to 0.31 s and keeps the frequency difference between GFM-A and the SG lowest (366 mHz compared with 377-635 mHz). The set-point step of GFM-B overshoots by about 25% with the CgLp, close to the leads and the VSG schemes. The overshoot of 0.3% obtained on the infinite bus is not reproduced, because the step now moves the system frequency through the governor of the SG and the droop of GFM-A. After the line trip, the CgLp settles most slowly (2.29 s), through the FORE tail. In the mixed cases, a CgLp unit keeps its fast fault recovery, its neighbor behaves as in the uniform case, and the two GFM frequencies stay within 8.4 mHz of each other during the load step.

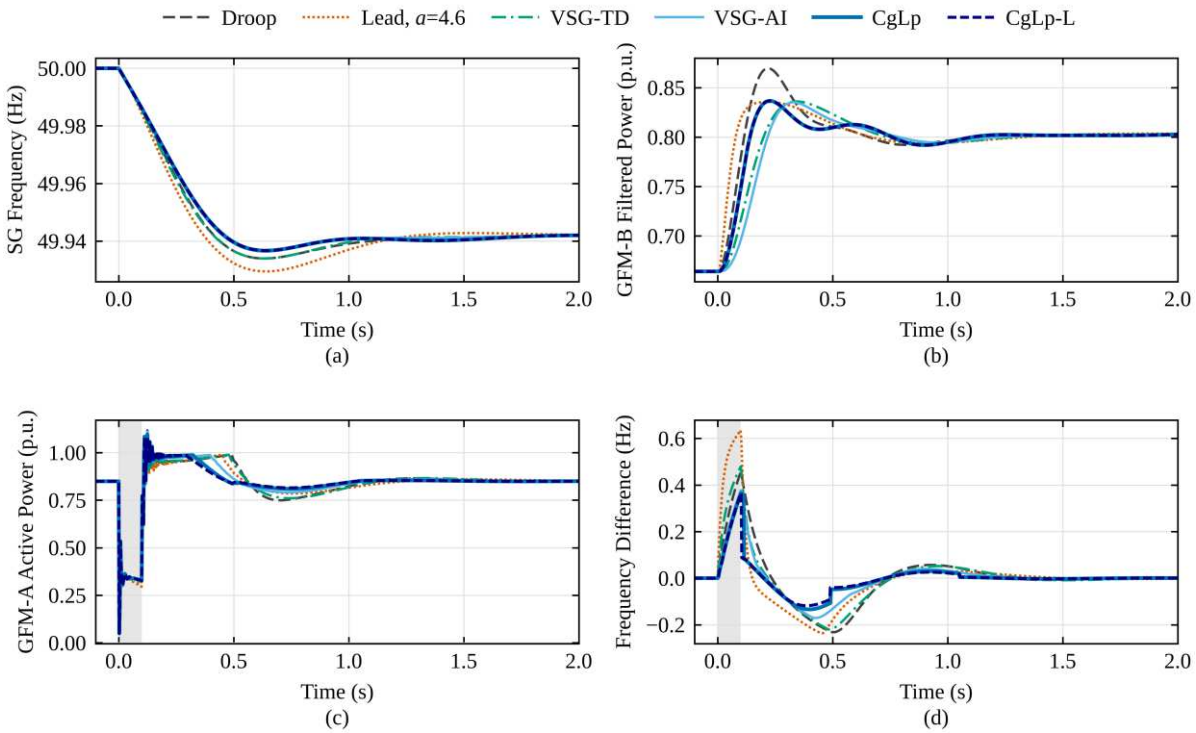

Fig. 8 Modified 9-bus system, nominal network. (a) SG frequency after load step. (b) Filtered power of GFM-B after its set-point step. (c) Active power of GFM-A for fault at bus 7 (shaded). (d) Frequency difference between GFM-A and SG for the same fault.

9 Discussion

The results separate the events in which the reset helps from those in which it does not. CgLp-L helps when a disturbance produces a large power error that later changes sign, as in voltage dips, faults, and set-point steps in strong grids. The first reset clears the frequency deviation accumulated during the transient when the power error crosses zero, close to the instant at which the angle reaches its post-disturbance equilibrium. This gives the longest CCT of the compared controllers (Table 6), the fastest recovery after every dip (Table 7), and a post-fault recovery of 0.29 s in the 9-bus system against 0.73-0.84 s for the other uniform cases (Table 8).

The reset gives no benefit when the error keeps one sign. During a frequency ramp no reset occurs, and the controller behaves as its base linear system, which is less damped than droop control (Table 4, last column); the ramp overshoot of 28%-41% follows from this. A large phase jump in a strong grid drives the converter into current limiting, where the filtered error lags the instantaneous one. The limiter-aware rule removes the resulting loss of synchronism, but the return to equilibrium through the FORE tail stays slow. A reset condition based on the frequency error, or a partial reset with $0 < \gamma < 1$, are possible remedies for the ramp case. The lead compensators remain better for phase jumps and grid-strength steps, and the CgLp settles most slowly after the line trip in the 9-bus system.

VSG-AI is the closest competitor. It meets the tuning rule, gives the lowest RoCoF after set-point steps, and survives the bolted dip at an SCR of 10. However, its switched inertia only slows the frequency change and does not remove the accumulated deviation, so it recovers 0.1-0.3 s more slowly after dips and has an 82% higher ITAE at an SCR of 20.

The reset logic reacts to ripple in the measured power, which a linear controller would only attenuate. Three sources of ripple appear in this study: white noise, handled by the reset band; double-frequency ripple under unbalance, handled by a notch filter; and PWM quantization in the switching model, which disappears at adequate resolution. A reset changes the internal frequency stepwise while the angle stays continuous. Measured with the 500 ms windows of RoCoF requirements, the steps of the CgLp are smaller than the frequency kicks of the leads. How internal frequency steps of a GFM inverter should be assessed against interconnection requirements [36] remains an open question.

This study has limitations. The switching model uses an ideal DC link, no dead time, and no cascaded inner loops, and its current limiter was not retuned for the LCL filter. The 9-bus study uses a classical machine and constant-impedance loads. The H_β certificate does not cover current limiting, so the benefit of the limiter-aware rule rests on simulation, and no hardware test has been made.

10 Conclusion

A CgLp reset element with a limiter-aware reset law was placed in the power synchronization loop of a grid-forming inverter. Outside current limiting, the reset loop satisfies the H_β condition for SCRs from 1.5 to 50. Under a common tuning rule it gives the lowest time-weighted error and frequency jitter among the admissible designs. With the limiter-aware rule it raises the critical clearing time of balanced dips by 42%-84% over droop control, rides through a 120 ms bolted dip at an SCR of 10, and cuts post-fault power recovery in a modified IEEE 9-bus system from 0.73-0.84 s to 0.29 s. A switching converter model reproduces the averaged results. The reset gives no benefit during frequency ramps, where the less damped base loop sets the response. Future work will address reset conditions for frequency ramps, a stability certificate that covers the current-limited mode, interaction with inner control loops, and hardware validation.

Statements and Declarations

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Competing interests The author has no relevant financial or non-financial interests to disclose.

Ethics approval and consent Not applicable.

Data availability The simulation models and data generated during this study are available from the corresponding author on reasonable request.

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