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Research Article

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Posted Date: November 25th, 2026

DOI: https://doi.org/10.21203/rs.3.rs-11414662/v1

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Additional Declarations: No competing interests reported.

Hardware Accelerated PS-PL Architecture for SPECAN SAR Imagery

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Abstract In wide-swath Synthetic Aperture Radar (SAR) modes, the Spectral Analysis (SPECAN) method is a vital processing tool for the rapid generation of medium-resolution SAR data. SPECAN employs deramp (dechirp) and spectral analysis to map radar echoes into focused SAR images by means of efficient frequency-domain operations such as the Fast Fourier Transform (FFT) and the Chirp Z-Transform (CZT). The framework combines range compression, azimuth deramping, Doppler centroid estimation and fast spectrum synthesis to produce azimuth profiles directly, without explicit interpolation or standard range cell migration correction (RCMC). The primary objective of SPECAN is to facilitate real-time processing of SAR image data, which makes it well suited to implementation on Field Programmable Gate Arrays (FPGAs). This implementation is intended to enhance the reliability of the hardware pipeline architecture in terms of resource availability, power constraints and processing speed for SAR comparative analysis. The proposed real-time, high-performance FPGA-based hardware PS-PL architecture integrates a floating-point IP core and a pipelined structure, reducing execution time, power consumption, hardware area and signal-processing requirements for SAR image-processing systems. The proposed PS-PL architecture was implemented for SPECAN, and its performance was compared and evaluated against the existing Range Migration Algorithm (RMA). The design reduced the utilization of resources such as Look-Up Tables (LUTs), Flip-Flops (FFs), BRAMs and DSP blocks while achieving a favourable trade-off between image quality and processing performance.

Keywords Synthetic Aperture Radar (SAR) · SPECAN · CZT · RCMC · FPGA · ZYNQ ZC706

1 Introduction

The Spectral Analysis (SPECAN) algorithm was developed as a result of the investigation of stretch processing and step-transform techniques employed to process linear Frequency Modulated (FM) radar signals. In the 1970s, researchers introduced the concept of deramping, which transforms a linear FM signal into a virtually constant-frequency sinusoid. The SPECAN algorithm for the formation of Synthetic Aperture Radar (SAR) images was subsequently established on the basis of this principle.

In 1979, the European Space Technology Center (ESTEC), Canada, and MacDonald Dettwiler (MDA) collaborated to develop the contemporary SPECAN algorithm. The primary objective of this work was to design a computationally efficient SAR processor capable of producing real-time SAR images. Several important innovations were introduced during this development, including:

- Linear Range Cell Migration Correction (RCMC);
- Descalloping for amplitude equalization;
- Deskewing for geometric correction;
- Multilooking to reduce speckle noise.

These innovations significantly reduced the computational requirements while maintaining acceptable image quality, making SPECAN an attractive solution for real-time SAR applications. Subsequently, comparative studies conducted at the University of British Columbia (UBC), Canada, further analysed various linear FM processing techniques and produced one of the earliest public descriptions of the SPECAN algorithm. Since then, SPECAN has become one of the most widely recognized quick-look SAR image formation algorithms.

Developed to facilitate the rapid generation of focused SAR images while retaining acceptable image quality, SPECAN is a computationally efficient SAR image formation technique. It is particularly well suited to wide-swath SAR systems, real-time imaging and quick-look processing, where processing speed is a critical requirement. In contrast to traditional SAR processing algorithms that rely on computationally intensive azimuth matched filtering, SPECAN implements azimuth compression through a deramping operation followed by a Fast

Fourier Transform (FFT). This significantly reduces computational complexity while maintaining the fundamental characteristics of SAR image formation.

The processing sequence of SPECAN commences with range compression, which is identical to the operation performed in the Range Doppler Algorithm (RDA). A linear Range Cell Migration Correction (RCMC) is then implemented to account for the migration of target reflections across range cells. While this linear approximation is computationally efficient, it may introduce minor limitations in image quality when compared with exact RCMC techniques.

The azimuth processing of SPECAN is its distinguishing characteristic. Rather than conducting convolution-based azimuth matched filtering, the algorithm first deramps the azimuth signal, transforming the quadratic phase history into an approximately linear frequency variation. An FFT is then employed to convert the Doppler spectrum directly into azimuth image coordinates. The amplitude variations introduced during spectral processing are compensated by a descalloping operation to further enhance image quality.

The algorithm can follow one of two paths, depending on the processing requirements. Multilooking is implemented to enhance radiometric quality and mitigate speckle noise during multilook image generation. Alternatively, a phase compensation stage is implemented for the construction of single-look complex (SLC) images in order to preserve the phase information that is necessary for applications such as coherent change detection and interferometric SAR (InSAR).

Finally, the geometric skew introduced by the linear RCMC approximation is corrected, and the processed data are combined into a geometrically consistent SAR image through deskewing and stitching. This final correction ensures improved spatial registration and overall image quality.

SPECAN provides numerous practical benefits, such as low computational complexity, reduced memory requirements and exceptional suitability for hardware implementation on FPGA, GPU and embedded processing platforms, owing to its dependence on straightforward frequency-domain operations. As a result, it has been extensively incorporated into airborne SAR, ScanSAR, UAV-based imaging systems and other applications that require rapid image generation. Although its approximation-based processing may result in slightly lower focusing accuracy than algorithms such as the Range Doppler Algorithm (RDA), Chirp Scaling Algorithm (CSA) and Range Migration Algorithm (RMA), SPECAN offers an exceptional balance between imaging performance and processing speed.

1.1 Literature survey

To meet the requirement for real-time image generation in airborne and spaceborne SAR systems, SPECAN was initially devised as a quick-look SAR processing technique. Its fundamental concept was developed in the 1970s from stretch processing and deramping methods for linear frequency-modulated (FM) signals. In 1979, researchers at the European Space Technology Center (ESTEC) and MacDonald Dettwiler (MDA) expanded these concepts into a practical SAR image formation algorithm by incorporating linear RCMC, descalloping, deskewing and multilooking operations. In comparison to conventional matched-filter-based methods, these innovations significantly reduced computational complexity and enabled efficient SAR processing. In detail, Wenna Fan et al. [1] proposed an enhanced fourth-order SPECAN algorithm. In this derivation, the high squint angle results in the correction and efficient processing of the azimuthal side-lobe defocusing (ASLD), the range cell migration (RCM) and the non-zero Doppler centroid. Cheng et al. [2] modified the SPECAN algorithm to address the imaging problem in the presence of a phase-coded signal, an extended synthetic aperture time and a large range migration. These modifications encompass the azimuth processing method, range curve correction and Doppler centroid compensation. V. Iglesias et al. [3] reported a real-time FPGA implementation of a spectrum analyzer employing a modified periodogram of the input signal. Given an analytical bandwidth, instantaneous dynamic range and frequency resolution, it can identify and estimate the power and frequency of up to NS narrow-band signals. L. Pei et al. [4] created a ScanSAR algorithm using a high-speed digital signal processing system, the space-borne SAR SPECAN imaging technique and a geometrical mosaic algorithm. High processing efficiency is possible owing to the parallel structure (SIMD software mode) of this system. A token rule is applied to boost the real-time performance of the DSP system and the speed of access to the local DSP bus on a board. G. Hu et al. [5] suggested a squint SAR image reconstruction algorithm based on SPECAN, which has the characteristics of high velocity, high efficiency and a wide squint angle range, and which addresses the fan-shaped distortion of the reconstructed picture and image geometric aberrations.

Z. Zhichao et al. [6] put forward a modified SPECAN method based on the Chirp Scaling principle. In the two-dimensional time domain, the received data are multiplied by the Chirp Scaling factor to remove the range walk. The conventional SPECAN technique is then used to obtain the two-dimensional focus of the image. C. Wang et

al. [7] suggested a real-time imaging technique for squint SAR based on SPECAN processing, which has high computational efficiency at medium resolution. They proposed a unified back-projection algorithm to address the problems of geometric distortion and fan-shaped distortion. The momentary Fourier transform (MFT) was introduced by S. Albrecht et al. [8] for SAR signal processing. In particular, these authors illustrate the benefits of the MFT algorithm for the SPECtral ANalysis (SPECAN) approach and burst-mode data processing. The problem is to maintain a constant azimuth resolution and output sampling rate because the azimuth FM rate of the signal is different in each range cell. They introduce SPECAN and present the advantages and drawbacks of the MFT compared to FFT algorithms.

X. Ye et al. [9] introduced an optimized squint imaging algorithm based on SPECAN for missiles. This algorithm is characterized by simple operation and low computational cost. It first processes echo signals by reducing the range walk, and then performs range FFT processing, range migration elimination and range compression. Y. Liao et al. [10] showed that mosaic SAR can perform high-resolution wide-swath (HRWS) imaging by flexibly steering its antenna beam. However, the classical imaging algorithm can suffer from spectrum ambiguity that finally leads to a defocused output owing to the data acquisition geometry. They therefore proposed a spectrum-analysis-based imaging approach for mosaic SAR imaging.

J. Sun et al. [11] proposed a SPECAN- and ECS (Extended Chirp Scaling)-based space-borne TOPS SAR full-aperture imaging technique. SPECAN is performed on the echo after range walk correction to provide a two-dimensional spectrum devoid of blur. The enhanced ECS algorithm is then used to adjust the range migration and range pulse compression. Finally, azimuth defocusing and the scaled Fourier transform (SCFT) are used for azimuth focusing. L. Fang et al. [12] proposed a modified SPECAN algorithm for missile-borne SAR in flat flight mode. The technique allows the processing of extended azimuth sequences under memory limitation, enabling real-time imaging without spectrum overlap. Zengliang Li et al. [13] proposed a computationally effective method for reconstructing a picture from the phase history data of Forward-Looking Bistatic SAR (FL-BSAR) and discussed the limitation on the size of the scene. The images obtained testify to the validity of the SPECAN algorithm. R. Lanari et al. [14] proposed a new phase-preserving approach for processing ScanSAR data, which complements the SPECAN procedure. The conventional SPECAN technique leads to an azimuth pixel size that is a function of range. The suggested solution avoids this problem by substituting the usual Fourier transform in SPECAN with a chirp z-transform, in whose kernel a range-dependent correction factor is included. The Terrain Observation by Progressive Scans (TOPS) mode, discussed by XiaoBei Wang et al. [15], overcomes the problems of the conventional ScanSAR mode by steering the antenna in the azimuth direction. An effective TOPS imaging technique for azimuth signal aliasing based on spectral analysis (SPECAN) is proposed to improve the sub-aperture division in the azimuth processing stage. The algorithm is very efficient because only a limited number of FFTs and complex multiplications are used for the complete SAR image processing.

Y. Li et al. [16] noted that SPECAN is a highly efficient method widely used to process SAR data, but that the Doppler rate is ignored, resulting in targets being defocused away from the scene center. Their approach equalizes the Doppler rate by using nonlinear chirp scaling (NCS) in the azimuth frequency domain, taking into account that the region of support in the azimuth frequency domain is distinct for targets within the same range gate. Consequently, an upgraded SPECAN method is proposed. In addition, the Doppler rate and its dependence are determined using a modified map drift (MD) autofocus approach. D. Wenzel et al. [17] developed two implementation strategies for range compression using the SPECAN methodology. The first approach, the Column Exploitation Method, uses a single deramping algorithm to demodulate signals; the transformed data are used to make the most of the calculated frequency-domain information for different look numbers, and the look number is calculated automatically from the system specifications. The second approach, the Multiple Deramping Method, takes the look number as a user-selected input value, and the lengths of the reference functions used for deramping are defined by the geometric resolution required. Both approaches are evaluated in terms of computing effort, geometric resolution, radiometric resolution and impulse response function.

S. Hamidi et al. [18] noted that the fundamental disadvantage of SPECAN is its lower resolution, but that its structure can be greatly improved by introducing a new method based on amplitude and phase estimation (APES) filter banks. SPECAN can scan a large coverage area quickly; however, its azimuth resolution is mediocre. Y. Lei et al. [19] created a method for mapping the detected and relocated positions of moving targets from the SPECAN-processed image to the SAR image generated through full azimuth compression. C. Wang et al. [20] and X. Ye et al. [21] suggested a successful image-based strategy that uses the SPECAN algorithm. The image was captured in circular SAR focus mode and processed using Terrain Observation by Progressive Scans (TOPS) and Inverse TOPS SAR.

1.2 Challenges and Gaps in the literature

SPECAN is computationally efficient and suitable for real-time processing, yet the literature reports several technical problems. The approach uses a linear approximation for Range Cell Migration Correction (RCMC), which sometimes causes residual migration errors in high-resolution and highly squinted SAR systems. Its azimuth compression method, based on deramping and FFT, can lead to inferior focusing accuracy, higher side-lobe levels and lower azimuth resolution compared with techniques such as RDA, CSA and RMA. Furthermore, standard SPECAN requires a relatively simple imaging geometry and is less effective for high-squint imaging, wide-swath SAR, spatially variable Doppler characteristics, platform motion errors and higher-order phase distortions. Challenges include a lack of sufficient support for 3D SAR imaging and for multi-channel and MIMO SAR systems, and an absence of adaptive techniques to improve image quality under different operating conditions. Although computationally advantageous, an effective implementation for ultra-high-resolution SAR with optimized hardware resource usage and energy efficiency remains a demanding task.

The literature shows various prospects for further study to address the existing constraints of SPECAN. Future studies should focus on the development of adaptive and nonlinear RCMC algorithms that can compensate the range migration without a major increase in computational complexity. There is also a need for higher-order phase compensation techniques, better autofocus algorithms and hybrid SPECAN systems that increase azimuth focusing while maintaining processing speed. Research on spatially adaptive processing, high-squint and wide-swath imaging and 3D/tomographic SAR extensions is still limited and needs further exploration. Furthermore, comparatively few studies have focused on FPGA- and ASIC-based real-time solutions emphasizing optimized pipelined designs, decreased memory utilization and low-power operation. Future research directions include the application of artificial intelligence and deep learning methods to phase error estimation, image enhancement and parameter optimization. A standard performance evaluation framework can be created with metrics such as SNR, PSLR, ISLR, processing time, memory usage and hardware resource utilization. Closing these research gaps will considerably improve the usefulness of SPECAN in next-generation SAR imaging systems.

1.3 Contributions of the study

The main objective of this work is to provide a unified framework for the evaluation of FPGA-optimized SAR image formation algorithms and to address the identified challenges, focusing on SPECAN in different operational modes, the hardware architecture, and the optimization of execution time, image quality and computational resource consumption. The work presents a complete simulation-to-hardware validation pipeline using Python, MATLAB and AMD Vivado HDL synthesis. This enables the conversion of algorithmic advances into operational real-time SAR imaging systems, providing the basis for future deployment on ASICs and next-generation reconfigurable platforms.

The remainder of this paper is organized as follows. Section 2 reviews SAR imaging algorithms. Section 3 presents the proposed methodology for hardware implementation. Section 4 provides the experimental results and a discussion of the proposed approach. Section 5 concludes the paper and outlines the future scope.

2 SAR imaging algorithm review

SAR techniques are highly specialized signal processing methods capable of transforming raw radar data into images with exceptional resolution of an observed scene. These methods utilize the motion of the radar platform, such as an aircraft or satellite, to synthesize a vast antenna aperture, thereby enabling a spatial resolution that is significantly finer than that of a physical antenna of the same size. The primary SAR algorithms are the Range Doppler, Chirp Scaling, Range Migration, Polar Format and SPECAN algorithms. Among these, the SPECAN algorithm is explained in detail in the next section.

2.1 SPECAN algorithm

The SPECAN processing flow is shown in Fig. 1 and consists of the following steps.

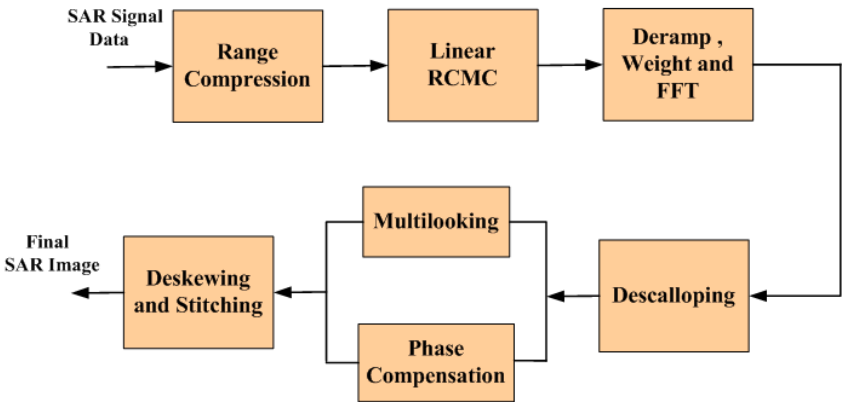

Fig. 1 SPECAN algorithm

1. *Range compression:* apply matched filtering (convolution with a reference chirp) in the range direction using an FFT-based approach, improving computational efficiency and leveraging FPGA-friendly parallelism [5].
2. *Corner turning:* rearrange the range-compressed data matrix by switching the columns and rows. In a hardware implementation, this step is essential for dataflow and maximizes memory access efficiency for azimuth processing.
3. *Azimuth deramping (dechirping):* mix (multiply) each azimuth line by a reference linear chirp signal to convert quadratic-phase (chirp) signals to a linear or stationary phase. Flattening the phase history makes rapid spectral analysis possible. This operation also prepares the data for segmentation into short bursts when operating in ScanSAR/wide-swath mode.
4. *FFT-based azimuth compression:* use an FFT (or chirp z-transform) on each deramped burst segment to synthesize the azimuth profile. By transforming to the frequency domain, SPECAN reduces memory and computational load, simplifies hardware design and allows focused azimuth compression without explicit range migration correction.
5. *Multilook and descalloping:* to improve radiometric quality, speckle and scalloping artifacts are reduced by averaging nearby frequency bins, a technique known as multilook averaging. As data move through the pipeline, streaming and accumulation can be used to optimize the hardware.
6. *Deskewing and output formatting:* to produce a geometrically correct SAR image and guarantee accurate target positioning, the processed data are realigned and deskewed. Results are mapped to output buffers, possibly with windowing or radiometric adjustments.
7. *Resource-aware implementation:* every operation (FFT, mixing, burst segmentation, accumulation) is optimized for FPGA parallel execution. For throughput and latency objectives, pipelines, DSP slices (for complex multipliers) and on-chip memory (BRAM) are carefully controlled [6].

This SPECAN flow creates a fully hardware-mappable pipeline and is particularly effective for real-time, medium-resolution SAR imaging, where speed and moderate radiometric fidelity are needed but computational and memory resources are limited. The key steps of the algorithm are:

a) Divide the SAR data into sub-apertures or processing blocks.

b) Apply a reference phase multiplication (deramping or phase compensation).

c) Perform an azimuth FFT.

d) Correct residual geometric errors.

e) Apply an inverse FFT or further focusing.

2.2 Mathematical analysis

Range compression. The received signal after demodulation is

$$s_r(n) = s(n) * h_r(n) \tag{1}$$

where s(n) is the raw SAR echo, $h_r(n)$ is the range reference (matched filter) and $*$ denotes convolution. In practice, range compression is performed in the frequency domain using FFTs:

$$S_r(f) = S(f) \cdot H_r(f) \tag{2}$$

Corner turning. The matrix is transposed so that azimuth lines are processed efficiently.

Azimuth deramping (mixing). Each azimuth column is multiplied by a reference chirp:

$$s_d(n) = s_r(n) \cdot e^{-j\pi\gamma n^2} \tag{3}$$

where γ is the azimuth chirp rate.

Azimuth FFT (spectral analysis). After deramping, an FFT is performed along the azimuth (burst) direction:

$$S_a(k) = \sum_n s_d(n)\, e^{-j2\pi\frac{kn}{N}} \tag{4}$$

Here, k is the frequency bin and N is the length of each azimuth burst.

Linear range cell migration correction (RCMC). Rather than complex interpolation (hyperbolic RCMC), SPECAN uses linear RCMC, aligning data by skewing azimuth lines based on a central reference:

$$R_{Align}(n,m) = R(n + \alpha \cdot m, m) \tag{5}$$

where α is the migration skew factor and n, m are azimuth/burst indices.

Deskewing and final image formation. After azimuth compression, the data are deskewed:

$$I_{final}(x,y) = R_{rearrange}(S_a(k)) \tag{6}$$

Parameter estimation. The Doppler centroid, the Doppler rate parameter γ and the pulse repetition frequency (PRF) are estimated from the platform velocity and antenna length:

$$PRF = \frac{2v}{D} \tag{7}$$

where v is the platform velocity and D is the antenna length. The hardware implementation follows the methodology of each of these algorithm steps.

3 Proposed methodology for hardware implementation

The Xilinx ZYNQ-7000 XC7Z045 System on Chip (SoC), which combines a dual-core ARM Cortex-A9 processor with FPGA programmable logic to enable the development of adaptable embedded systems, is installed in the ZYNQ ZC706 Evaluation Kit shown in Fig. 2. This makes the ZC706 appropriate for the development of detailed real-time processing systems in industries such as radar, communications and video processing.



Fig. 2 ZYNQ ZC706 board

3.1 Hardware Implementation Process Flow

The hardware implementation process flow is a hardware–software co-processing pipeline for SAR image formation (Fig. 3). The design leverages both Python scripts and hardware modules on the FPGA platform to process SAR images, using UART (Universal Asynchronous Receiver-Transmitter) for data communication between the PC and the hardware.

Input SAR image conversion. The input SAR image is first converted into a 32-bit hexadecimal data format using a Python script (Image_to_raw_dat.py). The output is a .mem file, in which each data point is represented in a 32-bit format suitable for hardware processing.

(1) Data transmission to hardware. A Python UART transmission script sends the hexadecimal data bytes serially from the PC to the hardware platform via the UART interface. The hardware module UART_Interface_32bit.v receives the serial data. The data are parsed such that the first 16 most significant bits (MSB) represent the real part and the next 16 bits represent the imaginary part of each complex data sample. The module reconstructs the 32-bit complex data for further processing.

(2) SAR algorithm processing. The reconstructed complex data are processed using one of several SAR focusing algorithms (RDA, CSA and RMA). These algorithms typically involve 2D FFTs, phase corrections and possibly Stolt interpolation, all aimed at converting raw radar echoes into a focused SAR image.

(3) Output buffering and data transmission. The focused SAR image data are stored in an output buffer, typically Block RAM (BRAM) within the hardware. This allows temporary storage and parallel access for further operations. The UART_TX_CORE module handles the transmission of the buffered output data back to the PC via the UART interface.

(4) Output data reconstruction. In Python post-processing, the data received from the UART interface are captured and stored back into a .mem file.

3.2 SPECAN pipeline architecture

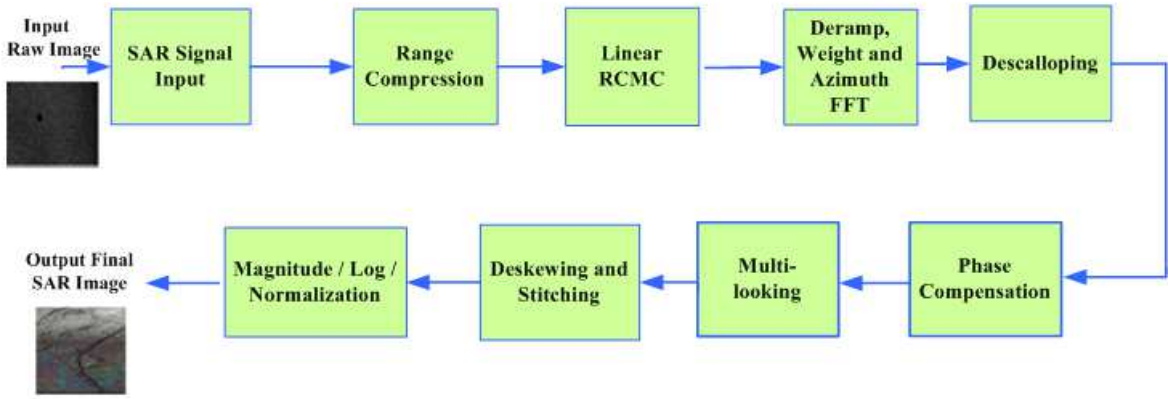

Fig. 3 SPECAN pipeline architecture process flow

Fig. 3 describes a ScanSAR/TOPS-mode SAR processing algorithm of the kind used for wide-swath SAR systems (such as the IW/EW modes of Sentinel-1), where the antenna beam is electronically steered across multiple sub-swaths and bursts, requiring extra steps beyond classic Range-Doppler processing (deramping, descalloping, deskewing, stitching) to handle burst discontinuities.

Input raw image. This is the unfocused raw radar echo data: a 2D matrix of complex-valued samples along fast time (range) and slow time (azimuth/pulse number). Each pixel encodes the amplitude and phase of the backscattered radar pulse, but no image structure is visible yet (it looks like structured noise, as in the input raw image thumbnail).

SAR signal input. The raw echoes are organized into a data matrix, and metadata (chirp parameters, PRF, platform velocity, orbit state vectors) are loaded. In burst-mode systems (ScanSAR/TOPS), this stage also separates the continuous raw stream into individual bursts per sub-swath, since the antenna cyclically switches beam pointing across sub-swaths.

Range compression. A matched filter (correlation with the complex conjugate of the transmitted chirp) is applied along the fast-time dimension. This collapses the long transmitted chirp into a narrow peak per target, giving fine range resolution independent of pulse length, which lets SAR use long pulses (for energy) while still achieving fine range resolution.

Linear range cell migration correction (RCMC). The energy of a target migrates across range bins as the platform moves during synthetic aperture formation, resulting in a small change in its range to the radar. This curved locus is referred to as the Range Cell Migration (RCM). Linear RCMC eliminates the range-varying component of this migration (typically through interpolation or a phase-domain shift in the range-Doppler

domain) to ensure that all azimuth samples of a specific target align in the same range bin prior to azimuth compression.

Deramp, weight and azimuth FFT. This step is specific to burst-mode (ScanSAR/TOPS) systems and distinguishes this pipeline from a simple stripmap Range-Doppler processor.

Deramping: in TOPS/ScanSAR, the antenna beam sweeps in azimuth during each burst, imposing an azimuth-varying Doppler centroid on the data. A deramping (azimuth phase multiplication) function removes this artificial chirp-like modulation, so the data behave like conventional stripmap data within each burst.

Weighting: a window function (Hamming, Hann, Taylor, etc.) is applied to suppress side-lobes in the final image, trading a small resolution loss for lower side-lobe and speckle artifacts.

Azimuth FFT: transforms the deramped, weighted azimuth data into the Doppler/azimuth-frequency domain, where azimuth focusing (matched filtering against the theoretical azimuth chirp) is performed more efficiently.

Descalloping. Because the antenna beam pattern is not uniform across a burst (it is strongest at beam center and weaker at burst edges), the resulting image has a scalloping artifact: a periodic intensity modulation across azimuth within each burst. Descalloping applies a correction (typically derived from the known antenna pattern or estimated empirically from calibration data) to flatten this intensity variation so that brightness is uniform across each burst.

Phase compensation. Residual phase errors (from imperfect deramping, orbit/timing inaccuracies or antenna phase-center variation across bursts) are corrected here. This step is critical for burst-mode SAR because inconsistent phase between adjacent bursts would cause visible discontinuities or ghosting at burst boundaries in the final stitched image, and it is essential for any downstream interferometric use, where phase must be preserved accurately.

Multilooking. Multiple independent looks of the same scene (typically from overlapping sub-apertures in azimuth, or adjacent range/azimuth pixel averaging) are incoherently averaged. This reduces speckle noise (the granular salt-and-pepper texture inherent to coherent radar imaging, caused by random constructive/destructive interference within a resolution cell) at the cost of reduced spatial resolution, a fundamental trade-off in SAR image quality.

Deskewing and stitching.

Deskewing: corrects for the fact that different bursts (and different sub-swaths) were acquired with slightly different antenna look angles and squint, which otherwise leaves geometric distortion (skew) between adjacent burst images.

Stitching: adjacent bursts (each independently focused) are joined into one continuous image along the azimuth direction. Because burst edges have lower SNR (antenna gain roll-off) and slight phase discontinuities, stitching typically uses a blended/overlapping region between bursts rather than a hard cut, to avoid visible seams.

Magnitude, log and normalization. The final complex focused image is transformed into a viewable and analysable form.

Magnitude: |pixel| ignores phase and retains backscatter intensity.

Log scaling: $20 \cdot \log_{10}|\text{pixel}|$ converts to decibels. Radar backscatter has an extraordinarily broad dynamic range (bright targets such as buildings or ships against dark targets such as calm sea may differ by more than 40 dB) that would be illegible on a linear scale.

Normalization: the dB values are rescaled into a common display range (e.g. 0–255 for an 8-bit display, or a set dB window such as [−30, 0] dB) so that the image can be rendered and compared consistently.

Output final SAR image. The result is a focused, speckle-reduced, radiometrically corrected SAR intensity image, geometrically continuous across burst and sub-swath boundaries and ready for visual interpretation or further analysis (classification, change detection, etc.), as shown in the colorized output thumbnail of the diagram.

3.3 SPECAN block design: PS-PL process flow

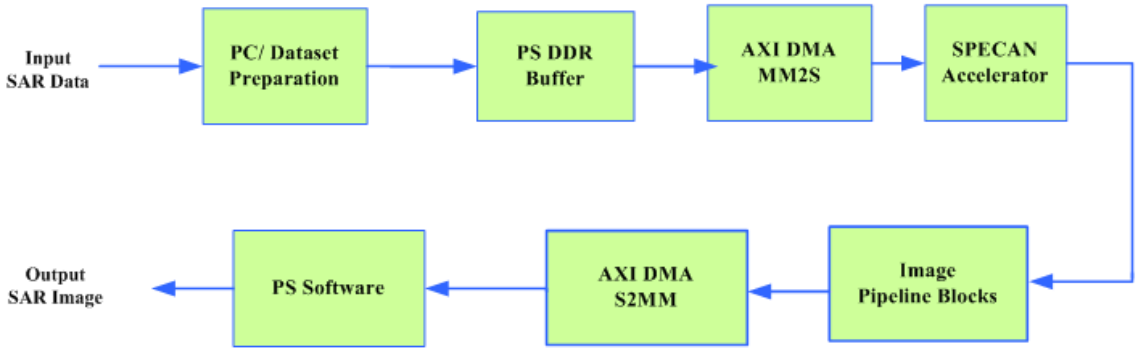

Fig. 4 SPECAN algorithm PS-PL process flow

Fig. 4 describes a hardware-accelerated SAR processing architecture implemented on a PS–PL hybrid SoC platform (such as a Xilinx/AMD Zynq or Zynq UltraScale+ device), in which the SPECAN algorithm is offloaded to programmable logic (FPGA fabric) for real-time or near-real-time processing, while the ARM processing system handles data management and final image output. The theory behind each stage is given below.

Overall architecture concept: PS–PL co-design. Modern SAR processors increasingly use System-on-Chip platforms that combine two parts. The Processing System (PS) is an ARM-based CPU running embedded Linux or bare-metal software, which handles data staging, control and post-processing. The Programmable Logic (PL) is FPGA fabric implementing the computationally intensive SAR focusing algorithm as custom, highly parallel hardware, handling the heavy signal processing that would be too slow on a general-purpose CPU. Data move between PS and PL via AXI DMA (Direct Memory Access) channels, which transfer large data blocks without CPU intervention, essential for the high throughput that SAR raw data requires.

Input SAR data. Raw SAR echo data (complex-valued, range × azimuth samples), either live from a radar receiver or from a pre-recorded dataset, is provided as the starting point.

PC/dataset preparation. Before hardware processing, the raw data are prepared on a host PC: reformatting (e.g. splitting real/imaginary components, fixed-point quantization for FPGA compatibility), byte ordering and packaging into a format the embedded system can stream, often written to an SD card or transferred over Ethernet/PCIe/JTAG to the SoC board.

PS DDR buffer. The prepared dataset is loaded into the DDR memory attached to the Processing System. This acts as the staging buffer: since FPGA on-chip memory (BRAM) is limited, DDR provides the capacity to hold full SAR data frames before and after PL processing.

AXI DMA MM2S (memory-mapped to stream). This is one direction of the AXI DMA engine: it reads data from PS DDR memory and streams it into the PL fabric as an AXI-Stream, feeding the accelerator continuously without CPU involvement, which is critical for sustaining the high data rates that SAR processing demands.

SPECAN accelerator. This is the core FPGA-based focusing engine implementing the SPECAN algorithm, a SAR image formation algorithm particularly suited to spotlight-mode or highly squinted SAR geometries. It is well suited to hardware implementation because its core operations are FFT-based rather than requiring the interpolation steps that Range-Doppler/RCMC algorithms need.

Image pipeline blocks. After SPECAN focusing, additional hardware pipeline stages typically handle range compression (matched filtering, if not already done before SPECAN); magnitude detection (converting complex focused data to intensity, $|s|$ or $|s|^2$); log scaling / dynamic range compression for display-ready output; speckle filtering or multilooking, if included; and format conversion to standard image pixel formats (e.g. 8-bit gray scale). These are implemented as further FPGA pipeline stages so that the entire chain from raw echo to displayable image stays in hardware, maximizing throughput.

AXI DMA S2MM (stream to memory-mapped). The reverse-direction DMA channel takes the processed image data streaming out of the PL pipeline and writes it back into PS DDR memory, making the result accessible to software running on the ARM cores.

PS software. The embedded ARM software (or Linux application) reads the focused image data from DDR, performs any final formatting (e.g. adding headers, colorization, file packaging) and prepares the output for storage, display or transmission.

Output SAR image. The final focused, detected SAR image is produced, as shown in the colorized output thumbnail, ready for visual interpretation, storage or downstream analysis.

3.4 SPECAN PS-PL pipeline architecture

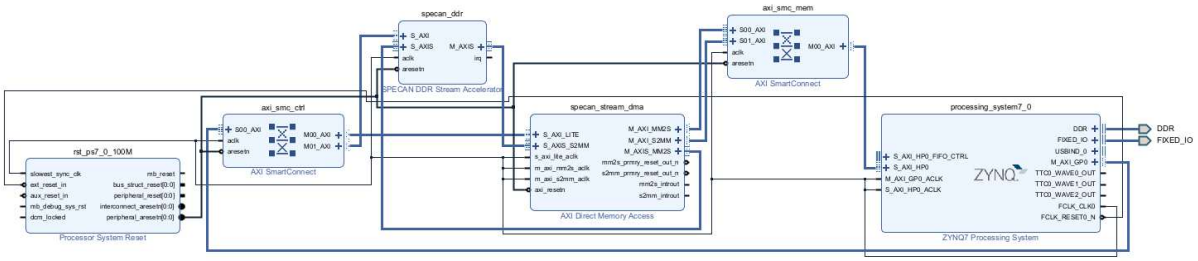

Fig. 5 SPECAN PS-PL pipeline architecture

Fig. 5 is the actual Vivado IP Integrator block design implementing the SPECAN hardware accelerator architecture described conceptually in the previous section, shown at the register-transfer/IP-core level and targeting a Xilinx Zynq-7000 SoC. The functionality and data flow are described below.

ZYNQ7 processing system (processing_system7_0). This is the PS core of the ZYNQ SoC: a hardened dual-core ARM Cortex-A9 with its memory controller. DDR and FIXED_IO are external pins connecting to the board's DDR3 memory chips and fixed ZYNQ I/O (clocks, MIO configuration). M_AXI_GP0 is a general-purpose AXI master port, letting the ARM CPU issue low-throughput control/configuration reads and writes to peripherals in the PL. S_AXI_HP0 (high-performance slave port) with its FIFO_CTRL is a high-bandwidth AXI slave port designed for high-throughput DMA traffic between the PL and DDR memory, essential for streaming large SAR datasets. The clock/reset outputs (FCLK_CLK0, FCLK_RESET0_N) drive the clock domain of the entire PL fabric.

Processor system reset (rst_ps7_zero_100M). A standard Xilinx reset-management IP that takes the raw reset signal from the PS and the FCLK clock, and generates properly synchronized, glitch-free reset signals (peripheral reset, interconnect_aresetn, bus_struct_reset) for every other IP block in the design. This ensures that all blocks come out of reset in a coordinated, stable state rather than each block resetting independently and causing bus lockups.

AXI SmartConnect (axi_smc_ctrl). This AXI interconnect/crossbar IP routes low-bandwidth control-plane traffic. It takes the single AXI-Lite-style master port from the PS (M_AXI_GP0) and fans it out to multiple slave (M00_AXI, M01_AXI) control interfaces, configuring both the SPECAN DDR stream accelerator and the register interface of the AXI DMA engine. This lets the ARM software set up DMA transfer descriptors and SPECAN algorithm parameters (deramp chirp rate, FFT size, etc.) via simple memory-mapped register writes.

SPECAN DDR stream accelerator (specan_ddr). This custom FPGA core performs the SPECAN algorithm itself (deramp multiply and FFT-based azimuth focusing). Its ports are: S_AXI, the control/configuration register interface (from axi_smc_ctrl); S_AXIS, an AXI-Stream slave input receiving raw SAR echo samples streamed from DDR via the DMA engine; M_AXIS, an AXI-Stream master output streaming the focused (processed) data onward; and irq, an interrupt line signalling the PS when a processing block (e.g. one burst or one FFT block) completes, so that software does not need to poll. Because the core operations of SPECAN (complex multiply for deramping, FFT for azimuth compression) are streaming, deterministic and highly parallelizable, implementing it as a dedicated AXI-Stream hardware core lets data flow through continuously at line rate rather than being processed sample by sample under CPU control.

AXI Direct Memory Access (specan_stream_dma). This is the data-mover engine bridging DDR memory and the AXI-Stream domain in which SPECAN operates. It has two independent channels. MM2S (memory-mapped to stream) reads raw SAR data from DDR (M_AXI_MM2S) and streams it (M_AXIS_MM2S) into the input of the SPECAN accelerator. S2MM (stream to memory-mapped) takes the processed output stream of the accelerator (S_AXIS_S2MM) and writes it back into DDR (M_AXI_S2MM). The mm2s_prmry_reset_out_n / s2mm_prmry_reset_out_n and introut signals manage per-channel reset and completion interrupts, so that the PS

can be notified independently when a read or write transfer finishes. This allows double-buffered, pipelined operation (loading the next burst while the previous one is still being written back).

AXI SmartConnect (axi_smc_mem). A second SmartConnect instance arbitrates the high-bandwidth memory-mapped traffic: it merges the two DMA master ports (S00_AXI and S01_AXI, corresponding to MM2S and S2MM) into the single M00_AXI port connected to the high-performance S_AXI_HP0 slave port of the PS. This is necessary because the HP ports of the PS are optimized for sustained, high-throughput burst traffic (exactly what streaming SAR data requires), and are separate from the low-throughput GP port used for control register access.

3.5 Salient features of the proposed work

1. Software running on the ARM cores (PS) configures the DMA and the SPECAN accelerator via the low-bandwidth control path: M_AXI_GP0 → axi_smc_ctrl → S_AXI (SPECAN) / S_AXI_LITE (DMA).
2. Raw SAR data, pre-loaded into DDR memory by software, is streamed out via DMA MM2S, through axi_smc_mem and the PS high-performance port, to the DMA engine, and into the AXI-Stream input of the SPECAN accelerator.
3. The SPECAN core performs deramp-multiply and FFT-based azimuth focusing entirely on the FPGA fabric, streaming out focused SAR samples.
4. The focused output stream flows back through DMA S2MM and axi_smc_mem into the HP0 port of the PS, and is written into DDR memory.
5. An interrupt notifies the ARM software that a processing block is complete; the software (or the PS software layer of the earlier system diagram) then reads the focused data from DDR for final magnitude/log/normalization and output image generation.

Advantage of the PS-PL design flow. This split, a low-bandwidth AXI-Lite control path plus a separate high-bandwidth AXI-Stream/DMA data path unified through two independent SmartConnect crossbars, is the standard Xilinx/AMD reference pattern for streaming DSP accelerators on ZYNQ. It cleanly separates configuration traffic (infrequent, small, latency-tolerant) from data traffic (continuous, large, throughput-critical), letting the high-performance AXI ports and the DMA engine sustain the full memory bandwidth that SAR processing needs, while the ARM cores remain free to handle sequencing, buffering strategy and final image post-processing without becoming a bottleneck in the streaming datapath.

3.6 Hardware Architecture Comparison

The proposed SAR hardware architecture integrates all processing stages into a unified pipeline, enabling continuous data flow and efficient resource utilization, as summarized in Table 1. It employs optimized RCMC handling and FFT-based processing to decrease computational complexity. This yields a high-throughput, low-memory, real-time FPGA implementation.

Table 1 Hardware architecture comparison

Parameter	RMA	SPECAN
Processing style	Full pipelined	Block-wise (burst/patch processing)
FFT usage	Streaming FFTs	Single-stage FFT (azimuth only)
RCMC handling	Inherent	Approximate / simplified (assumed negligible within a processed block)
Memory	High	Low
Computation complexity	$O(N^2 \log N)$ + Stolt interpolation	$O(N \log N)$
Throughput	Very high	High (for small-to-moderate scene sizes)

4 Results and Discussion

A comparative analysis of SPECAN and RMA is provided in terms of power consumption and resource utilization on the ZYNQ ZC706 board.

After processing of the SAR raw data image on the FPGA, the output images shown in Fig. 6 were obtained: the raw image, the contrast-stretched image and the equalized image. Raw SAR images are characterized by low contrast and grainy speckle noise because the coherent radar backscatter is concentrated in a restricted region

with a few very bright outliers. Linear contrast stretching linearly rescales the (typically percentile-clipped) intensity range to the full display range. This preserves relative brightness but does not adapt to the shape of the histogram. Histogram equalization remaps intensities non-linearly using the cumulative distribution function, so that densely occupied terrain values are spread out more, allowing improved visibility of detail at the cost of magnifying speckle.

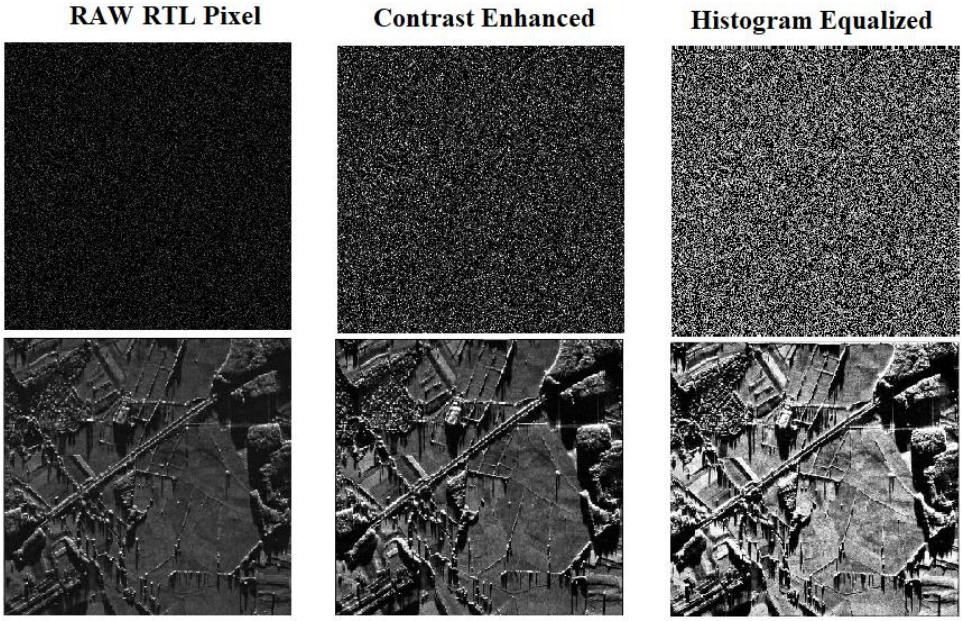

Fig. 6 SPECAN PS-PL Block Design Output Images

4.1 Power Consumption

Table 2 Power consumption

Algorithm	Static power (W)	Dynamic power (W)	On-chip power (W)	Junction temp. (°C)
Range Migration (Existing) [22]	0.110	0.262	0.372	29.3
SPECAN (Proposed)	0.216	1.616	1.832	28.2

Table 2 presents a comparison of the power consumption and thermal characteristics of the existing Range Migration Algorithm (RMA) and the proposed SPECAN algorithm implemented on an FPGA. The RMA design consumes 0.110 W of static power and 0.262 W of dynamic power, resulting in a total on-chip power of 0.372 W, with a junction temperature of 29.3 °C. In comparison, the SPECAN implementation consumes 0.216 W of static power and 1.616 W of dynamic power, leading to a total on-chip power consumption of 1.832 W, while its junction temperature is 28.2 °C. SPECAN therefore exhibits higher static, dynamic and total power consumption than RMA, mainly because of increased switching activity, hardware resource utilization, parallel processing and memory operations. Although SPECAN consumes approximately 4.924 times more total on-chip power, its junction temperature is 1.1 °C lower than that of RMA, which may be attributed to the thermal-analysis conditions, FPGA resource placement, ambient temperature and cooling assumptions. Overall, RMA provides better power efficiency, whereas the higher power consumption of SPECAN may be justified if it offers improved processing speed, throughput or real-time SAR image-formation capability (Fig. 7).

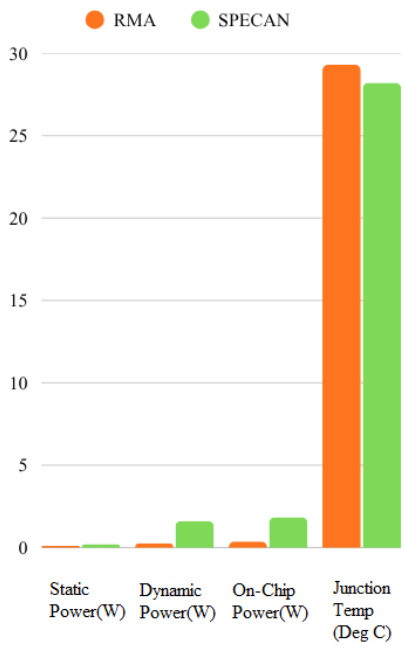

Fig. 7 Power consumption

4.2 Resource utilization

Efficient resource allocation ensures optimal performance, power efficiency and scalability in embedded SAR imaging systems.

Table 3 Resource utilization on the ZYNQ ZC706 board

Algorithm	**LUTs (218,600)**	**FFs (437,200)**	**BRAMs (545)**	**DSPs (900)**
Range Migration (Existing) [22]	4917 (2.24%)	9626 (2.20%)	7 (1.28%)	80 (8.88%)
SPECAN (Proposed)	4727 (2.1%)	6431 (1.47%)	2.5 (0.45%)	7 (0.77%)

Table 3 and Fig. 8 compare the FPGA resource utilization of the existing Range Migration implementation with that of the proposed SPECAN implementation on the target device (total available resources: 218,600 LUTs, 437,200 FFs, 545 BRAMs and 900 DSPs, consistent with a Zynq-7000 series device such as the ZC706/ZC702 class). The results directly validate the theoretical complexity comparison discussed earlier: SPECAN consumes noticeably fewer resources in every category, with roughly 4% fewer LUTs (4727 vs 4917), 33% fewer FFs (6431 vs 9626), 64% fewer BRAMs (2.5 vs 7) and 91% fewer DSPs (7 vs 80). This is because the single deramp-multiply-and-FFT azimuth focusing of SPECAN avoids the Stolt interpolation step that RMA requires, and interpolation is DSP- and BRAM-intensive (it needs multiply-accumulate units for coefficient computation and on-chip memory for storing intermediate wavenumber-domain data during resampling). The much lower DSP count of SPECAN is especially significant for real-time embedded SAR processors, since DSP slices are typically the tightest resource constraint on mid-range Zynq devices, and the much lower BRAM usage (0.45% vs 1.28%) confirms the smaller memory footprint of the block/patch-wise processing style of SPECAN compared with the need of RMA to hold larger 2D wavenumber-domain matrices for interpolation. Overall, these results provide hardware-level evidence for the algorithmic trade-off established earlier: SPECAN sacrifices the exact, wide-angle-capable range cell migration correction of RMA in exchange for a substantially smaller, more power- and area-efficient FPGA design, making it the more practical choice for resource-constrained, real-time onboard SAR accelerators where full RMA-level geometric accuracy is not strictly required.

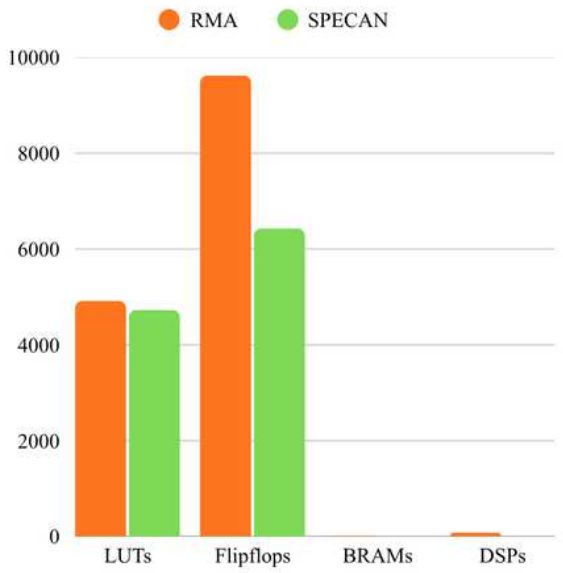

Fig. 8 Resource utilization

Table 4 Comparative analysis with reference work

Algorithm	Platform/ device	LUTs	FFs	BRAMs	DSPs	Power (W)	Reference
Range Migration [22]	ZYNQ 7000	53,200	10,6400	140	220	NA	[22] Existing work
SPECAN [Proposed]	ZYNQ ZC706 (proposed)	4727	6431	2.5	7	1.832	Proposed work

Table 4 extends the resource-utilization comparison with the platform/device, power consumption and reference columns, giving a fuller picture of the existing Range Migration implementation versus the proposed SPECAN implementation. Note that the two designs were implemented on different but related devices: Range Migration on a generic ZYNQ 7000 platform (existing work, reference [22]) and SPECAN on a ZYNQ ZC706 (proposed work). Some caution is therefore advised when directly comparing absolute resource numbers, as exact resource budgets can vary slightly by specific part number within the Zynq-7000 series. However, the ZC706 belongs to the same ZYNQ-7000 family, so the comparison remains broadly valid. The resource trend of the previous table also applies here: SPECAN requires far fewer LUTs (4727 vs 53,200), FFs (6431 vs 10,600), BRAMs (2.5 vs 140) and DSPs (7 vs 220). The FF count reported for RMA seems unusually low relative to typical implementations and may indicate a different reporting convention or scale in the source reference. This further illustrates that the simpler deramp-and-FFT-based azimuth focusing of SPECAN does not require the heavier Stolt-interpolation hardware needed by RMA.

A further metric of interest is power consumption. The reported power for SPECAN is 1.832 W, whereas the reported power for Range Migration in the source reference is not available (NA), so a direct power comparison cannot be made from these data alone. However, considering the dramatically lower DSP and BRAM utilization of SPECAN (both major contributors to dynamic power on FPGAs, as DSP slices and BRAM read/write operations consume proportionally more power under active switching), it is reasonable to infer that the actual power footprint of SPECAN would be substantially lower than that of RMA, were it measured, even accounting for platform differences. This combination of lower logic resource usage, lower memory usage and low absolute power consumption (under 2 W) makes SPECAN attractive for power- and area-constrained real-time onboard SAR systems such as small satellites, UAV-mounted radar or other platforms where every watt and every square millimeter of silicon is a hard constraint, even if this efficiency comes at the expense of the exact, wide-angle geometric accuracy of the Stolt-interpolation-based RCMC of Range Migration.

5 Conclusion and Future Scope

In this work, a comparative analysis of the standard Range Migration Algorithm (RMA) and the proposed SPECAN-based SAR image formation and PS-PL architecture has been presented, implemented and validated

on ZYNQ-7000 family FPGA platforms (ZYNQ 7000 and ZC706, respectively). Theoretical investigation demonstrated that the inherent wavenumber-domain Stolt interpolation of RMA provides accurate correction of range cell migration and wide-angle imaging, but suffers from high computational complexity ($O(N^2 \log N)$) and heavy hardware resource consumption. In contrast, azimuth focusing in SPECAN is based on deramping and FFT, which has O(N log N) complexity. It uses short processing blocks to approximate RCMC, which reduces the hardware cost significantly at the expense of some geometric precision. This trade-off was experimentally verified: the proposed SPECAN implementation used significantly fewer FPGA resources than the existing RMA solution, notably about 91% fewer DSPs and 64% fewer BRAMs, while operating at a measured power consumption of only 1.832 W. These results show that SPECAN, implemented on a PS-PL hybrid SoC architecture with AXI-Stream-based hardware acceleration and DMA-driven data movement, is a highly resource- and power-efficient alternative to RMA for SAR image formation, well suited to real-time, embedded and platform-constrained applications where full RMA-level accuracy is not strictly necessary.

Future work will include the following directions:

- *Direct RMA power benchmarking:* Conduct a fair comparison of power and hardware with SPECAN by implementing RMA on the same ZC706 platform.
- *Accuracy assessment:* Use resolution, SNR, PSLR, ISLR and geometric distortion metrics to evaluate the accuracy of SPECAN and RMA.
- *High-resolution and high-squint imaging:* Enhance SPECAN for wide-angle and high-resolution SAR by utilizing enhanced RCMC and phase compensation.
- *Validation on real SAR data:* Use genuine Sentinel-1 or other airborne/spaceborne SAR datasets to verify the SPECAN architecture.
- *Adaptive SPECAN–RMA processing:* Create a reconfigurable FPGA architecture that can switch between SPECAN and RMA depending on accuracy and processing needs.
- *Advanced FPGA platforms:* Enhance energy efficiency and increase throughput by extending the architecture to Zynq UltraScale+, RFSoC or Versal devices.
- *UAV/on-orbit testing:* Assess the performance of the processor under realistic UAV or spaceborne conditions, such as real-time, thermal, power and reliability constraints.
- *Application integration:* Combine the focused SAR output with interferometric processing, target detection, ship detection and change detection.

Data availability

The data generated and analysed during this current study are not publicly available but can be obtained from the corresponding author upon reasonable request.

Author Contribution Declaration

Srinivasulu Parri contributed to conceptualization, methodology, algorithm development, MATLAB simulation, Python scripts, FPGA architecture design, and manuscript preparation. Puli Kishore Kumar contributed to supervision, technical review, validation, interpretation of results, and critical revision of the manuscript. Both authors reviewed and approved the final version of the manuscript.

Funding

The authors received no specific financial support from any funding agency in the public, commercial, or not-for-profit sectors for this research.

Ethics Approval

Ethical approval was not required for this study because it did not involve human participants, animals, or the collection of personal or sensitive data.

Consent to Participate

Not applicable. This study did not involve human participants.

Consent to Publish

Not applicable. This study does not contain any individual person's identifiable data or images requiring consent for publication.

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