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Finite Control Set Model Predictive Control of a Five-Level Grid-Tied Transformer-less Inverter with Reliability Enhancement

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Abstract

This paper proposes a modified Model Predictive Control (MPC) strategy designed to address the issues of uneven capacitor voltage balancing, higher switching losses, and reduced reliability, making it applicable across different MLI topologies. The control utilises a modified cost function that adds an explicit switching frequency penalty term, allowing the controller to actively minimise unnecessary switching transitions and improve switch reliability while still maintaining accurate voltage tracking and capacitor balancing. The proposed control strategy is implemented on a 1kW five-level topology hardware prototype that reduces component count and stress. Both simulation and hardware validation are carried out under open-loop and closed-loop (MPC-based) operation across varying load conditions, and the results confirm that the proposed control approach delivers stable multilevel output waveforms, consistent

capacitor voltage balancing, and fast dynamic response, all while increasing reliability compared to conventional MPC. The reliability evaluation using the FIDES methodology shows that the reduced switching activity under the proposed control directly translates into a lower switch failure rate compared to open-loop operation. The proposed control strategy can be extended to other MLI configurations.

Keywords: MPC, MLI, Capacitor Voltage Balancing, Switching Frequency Optimization, FIDES Methodology, FCS-MPC.

Author Contributions

Aasiya Fatima contributed to the conceptualization and methodology of the study, conducted the investigation and formal analysis, curated the data, performed the visualization, and prepared the original draft of the manuscript. Mohammad Anas Anees contributed to the conceptualization, methodology, investigation, formal analysis, and validation of the study, and participated in reviewing and editing the manuscript. Saad Mekhilef contributed to the methodology, provided supervision and resources, and contributed to the review and editing of the manuscript. Addy Wahyudie contributed to the methodology and participated in reviewing and editing the manuscript. Houssem Jerbi contributed to the methodology and participated in reviewing and editing the manuscript. All authors reviewed and approved the final version of the manuscript.

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1 Introduction

The renewable energy systems are used against traditional methods, as they are convenient, environmentally friendly, and contribute to sustainable energy. Power electronic converters have found extensive use in diverse applications. The conventional applications employs various PWM-driven switching schemes and associated control frameworks [1–3]. Among them, linear control with PWM and hysteresis control have been widely preferred in practice due to their operational simplicity and reliability [4]. In earlier times, advanced control schemes that required substantial computational effort were impractical due to the limited processing capabilities of available hardware. However, with advances in high-speed, powerful processors, interest in such complex computational control methods has increased significantly among researchers.

Multi-level Inverters (MLIs) offer more advantages as compared to normal inverters. MLI has multiple voltage levels as compared to conventional two-level inverters. Multilevel inverters deliver a broad spectrum of advantages, including improved voltage stress profile across the switches, lower harmonics, small filter requirements in grid-connection, reduced on-state and switching losses, and modular design features

[5, 6]. Various Topologies such as Diode Clamped, H-bridge, Flying capacitors and Hybrid inverters are already researched and studied [7, 8].

Over the years, researchers have used many controllers, such as the PWM control scheme, hysteresis control, PI control and sliding mode control (SMC) but each one of them has its own limitation. In hysteresis control, the switching frequency keeps changing, which complicates filter design and increases electromagnetic interference (EMI) [9]. Other advanced methods, such as SMC, offer high accuracy but suffer from substantial implementation complexity, chattering, and sensitivity to measurement noise, making them complex to implement [10]. Most of the controllers are only suitable for linear systems.

Model predictive control (MPC) can effectively handle system nonlinearities and is therefore well-suited for a wide range of inverter topologies. Among modern control strategies, MPC has gained considerable attention because it uses an internal mathematical framework to forecast the system's upcoming response by minimising the cost function and selecting the optimised switching state. [11].

Among the multilevel inverter topologies for grid-connected applications, the five-level inverter has received much attention due to the trade-off between the quality of the output waveform and the implementation complexity. than the traditional three-level inverter, it has low total harmonic distortion (THD), low voltage stress and smaller output filters. The additional reduction in THD achieved by seven-level and higher-level inverters is at the expense of significantly increased circuit complexity, component count, control requirements, and cost. Therefore, the five-level inverter can be considered a promising and practical solution for grid-connected power conversion systems.

A. Tiwari et al. [7] reviews the integration of five-level multilevel inverters into grid-connected photovoltaic applications, highlighting their benefits such as higher efficiency, lower harmonic distortion, and better power quality. It also compares different control and modulation methods to help choose the most suitable approach for specific applications.

H. Le et al. [8] introduce a new five-level medium-voltage inverter with fewer components, no split DC-bus or isolated sources, and simple voltage regulation. It runs at low switching frequency, reducing switching losses and improving efficiency. A predictive current control (PCC) method is applied using discrete-time models to ensure fast response. Experimental results show that, compared to existing MLIs, the proposed inverter achieves lower switching frequency, reduced harmonics, lower power losses, and higher efficiency.

Another analysis [4] introduces a newly proposed three-phase, five-level (FLSDO) converter designed to interface with either a six-phase or dual three-phase load configuration. The design uses fewer switches than conventional setups but still generates all required voltage levels. It expands the operating range compared with earlier dual-output converters and employs a hybrid SPWM control technique. The converter is scalable to multiple loads by adding modules. A five-level inverter topology was previously proposed in [12]. As shown in Fig. 1, the topology includes 7 switches (some bidirectional), 2 capacitors, and 1 DC voltage source. It offers key advantages, including elimination of leakage current, minimal component count, high voltage gain, and

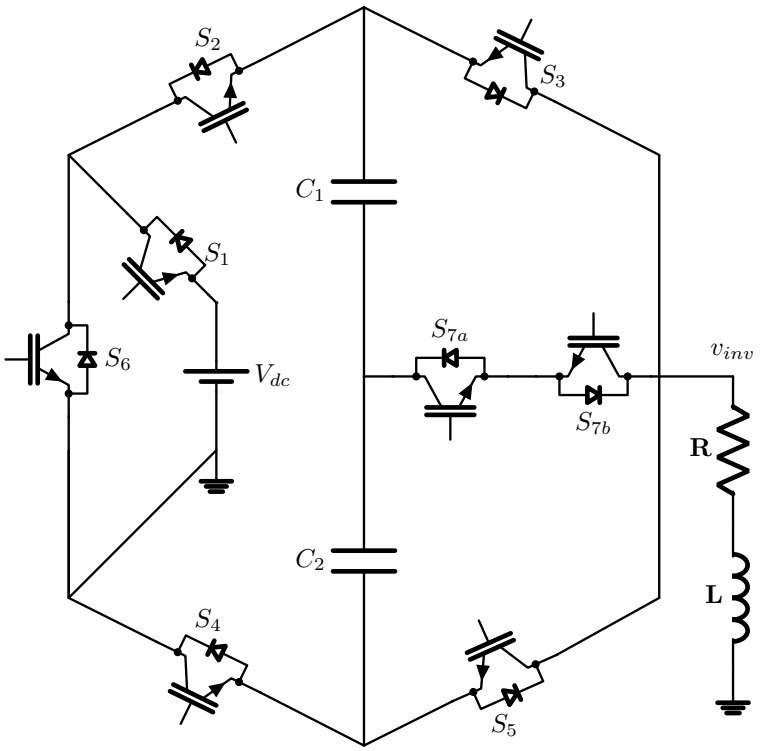


Fig. 1 Five-level inverter topology adopted from [12]

excellent efficiency. However, the original open-loop configuration suffers from limitations including poor dynamic response and higher total harmonic distortion (THD) under PWM control.

To the authors' knowledge, this is the first work in which model predictive control (MPC) has been integrated into the five-level topology proposed in [12] for its reliability improvement and has been validated using the FIDES standard. The main contributions are as follows:

1. A modified MPC cost function is proposed, incorporating an explicit switching-frequency penalty term in addition to the current-tracking objective. This minimises unnecessary switching transitions. The proposed approach reduces thermal and electrical stress on the power semiconductor switches without degrading current-control performance.

2. The failure rates of the switches (λ) are evaluated using the FIDES reliability prediction methodology. Results are presented for both open-loop PWM and the proposed modified MPC. The modified MPC exhibits a lower failure rate, thereby establishing a direct link between control-strategy design and long-term switch

reliability—an aspect that has received limited attention in the current multilevel inverter literature.

3. The topology proposed in [12] was previously demonstrated only under open-loop PWM operation. This work extends the topology to closed-loop operation using MPC. Simulation results demonstrate the feasibility of grid-tied operation, with a significant reduction in THD, as well as improved dynamic response and grid synchronisation compared to the open-loop baseline.

2 Model Predictive Control

The multilevel inverter topology generates five output voltage levels using a single DC source and two switched capacitors. The two capacitors, C_1 and C_2, holds significant importance in generating intermediate voltage levels and supporting the self-balancing mechanism during operation. The switching devices $S_1 - S_7$ are controlled in a manner that the inverter can generate the required levels as given in Table 1. These states are obtained by appropriate charging and discharging of the switched capacitors. The Model Predictive Controller selects the optimal switching state from the available valid states to minimise the error between the reference grid current/capacitor voltages and their corresponding predicted values. In Model Predictive Control (MPC), the first step is the prediction of the mathematical model of an inverter and load using equation 1 below.

$$i\left(k+1\right) = i\left(k\right) + \frac{T_s}{L}\left(V_{inv}(k) - V_{load}\left(k\right)\right) \tag{1}$$

where T_s is the sampling time, L is the load inductance, and V_{inv} is the predicted inverter output voltage. This model predicts the future current for each possible switching state to select the best switching state; the cost function is defined as given in 2:

$$g = \left|i_{ref}\left(k+1\right) - i_{pred}\left(k+1\right)\right| \tag{2}$$

The MPC evaluates all possible switching states and selects the one that minimises the cost. This ensures optimal tracking and low ripple. A secondary objective of MPC is to maintain capacitor voltages:

$$V_{C1} \approx V_{C2} \approx V_{dc}/2 \tag{3}$$

If an imbalance occurs, MPC penalises switching states that worsen the imbalance and favours those that correct it. This eliminates the need for additional balancing circuits. Firstly, MPC measures the current, voltage, and capacitor values. After that, it Predict future values for every switching possibility. Next, it Evaluates the cost function for each prediction. After that choose the switching level with the minimum cost. Apply the selected switching combination to the inverter. Repeat the operation at every sampling period. This results in an efficient, fast, and ripple-free control with excellent dynamic response. MPC reacts quickly to disturbances such as load changes or voltage sags. Another perk is reduced THD. Since switching states are selected optimally, the output waveform closely follows the reference sinusoid. By modifications in

the objective function, it can also lower switching losses. Unlike PWM, MPC switches only when required, reducing switching frequency and improving efficiency. Natural capacitor balancing is also observed. The controller automatically triggers switching states that restore capacitor voltage balance.

A grid-tied inverter is connected to the point of common coupling (PCC) through an RL filter. Closed-loop simulations are performed in this study for grid-tied as well as standalone operation. Let i_g be the grid current, v_{pcc} be the PCC voltage, and v_i be the inverter output voltage.

The continuous-time model is

$$L\frac{di_g}{dt} + Ri_g = v_i - v_g. \tag{4}$$

Using forward Euler discretization with sampling time T_s, the one-step prediction of the current of the grid is

$$i_{g,k+1} = i_{g,k}\left(1 - \frac{RT_s}{L}\right) + \frac{T_s}{L}\left(v_i - v_{g,k}\right). \tag{5}$$

The methodology described above is shown in the flowchart Fig. 4.

If the standalone operation is performed in a closed loop instead of a grid-tied operation, v_{pcc} can be removed from the equation. Also, R and L will now be the load resistances and inductances rather than filter resistances and inductances as shown in Fig. 2

3 Switching States and Output Voltage Levels

The inverter has five feasible switching states corresponding to five output voltage levels:

$$\{-V_{dc},\ -V_{dc}/2,\ 0,\ +V_{dc}/2,\ +V_{dc}\}.$$

The switching table (given) is summarised in (1). The charging and discharging states of the capacitors are also shown.

Table 1 Switching states and capacitor behavior (C: charge, D: discharge, N: no change).

S.No.	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Output level	Levels	C_1	C_2
1	0	1	0	0	1	1	0	$-V_{dc}$	1	D	D
2	0	1	0	0	0	1	1	$-V_{dc}/2$	2	D	N
3	1	1	0	1	1	0	0	0	3	C	C
4	0	0	0	1	0	0	1	$+V_{dc}/2$	4	N	D
5	0	0	1	1	0	0	0	$+V_{dc}$	5	D	D

The selected topology produces its five output levels through five distinct switch combinations, as shown in Fig. 3.

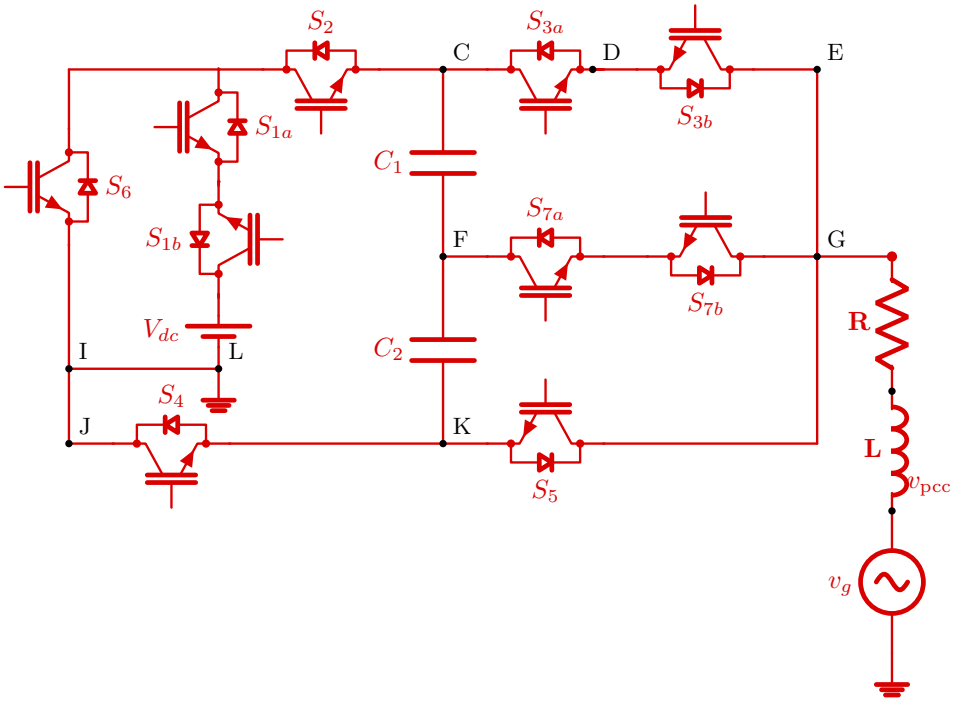


Fig. 2 Circuit diagram of topology with grid

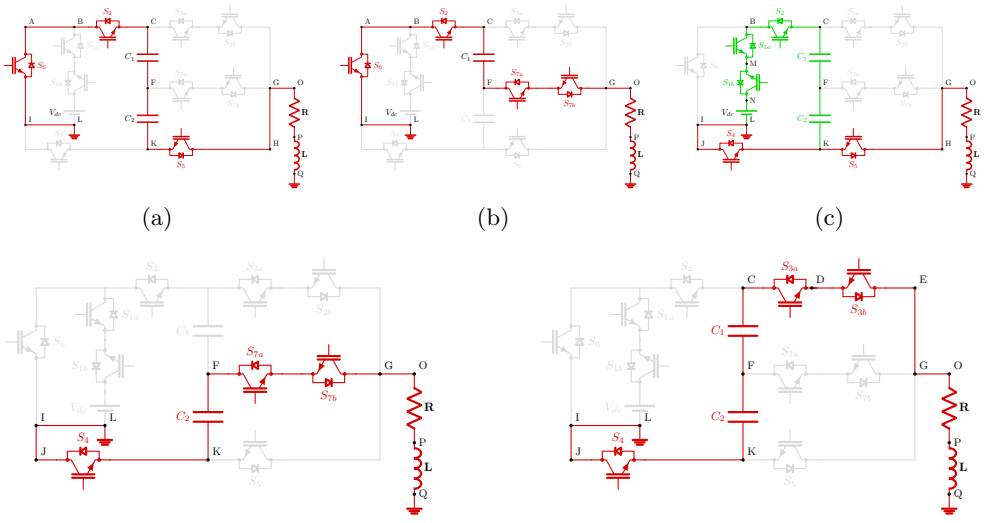


Fig. 3 Voltage Levels Generation by the 5-Level MLI: (a) $-V_{dc}$, (b) $-V_{dc}/2$, (c) 0, (d) $+V_{dc}/2$, (e) $+V_{dc}$.

4 Proposed FCS-MPC control for grid tied MLI

The flowchart of the proposed algorithm is proposed in Fig. 4

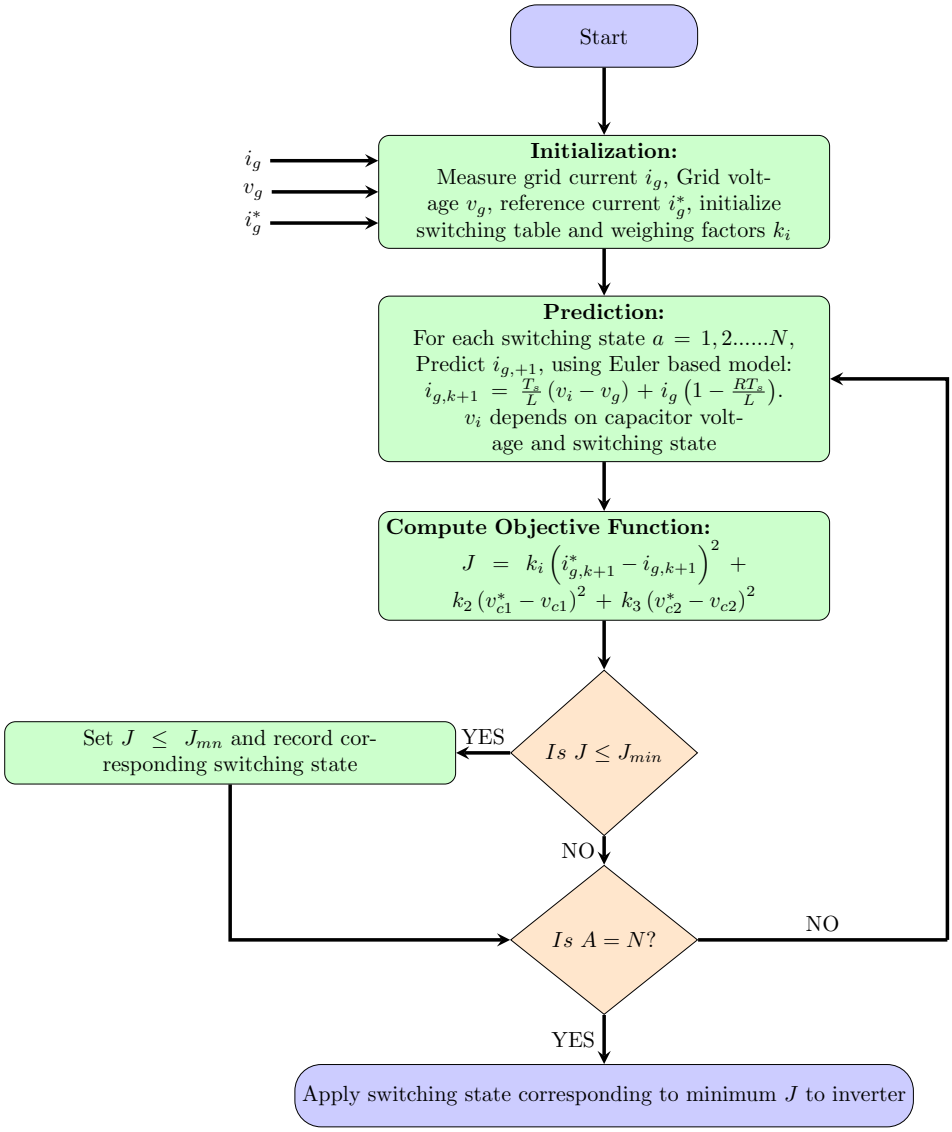


Fig. 4 Algorithm Flowchart.

4.1 State - wise FCS - MPC Predictions and Capacitor Voltage Prediction

Let the capacitor voltages at time k be $v_{c1,k}$ and $v_{c2,k}$. Based on the capacitor participation implied by the table, the inverter output voltage candidates are modeled as:

$$v_i^{(1)} = -(v_{c1,k} + v_{c2,k}), \qquad \text{for } -V_{dc}, \tag{6}$$

$$v_i^{(2)} = -v_{c1,k}, \qquad \text{for } -V_{dc}/2, \tag{7}$$

$$v_i^{(3)} = 0, \qquad \text{for } 0, \tag{8}$$

$$v_i^{(4)} = +v_{c2,k}, \qquad \text{for } +V_{dc}/2, \tag{9}$$

$$v_i^{(5)} = +(v_{c1,k} + v_{c2,k}), \qquad \text{for } +V_{dc}. \tag{10}$$

The capacitor voltage update is determined by the charge/discharge logic. Using the magnitude of grid current $|i_{g,k}|$ for the update:

$$\text{Discharge (D):} \quad v_{c,k+1} = v_{c,k} - \frac{T_s}{C}\,|i_{g,k}|, \tag{11}$$

$$\text{Charge (C):} \quad v_{c,k+1} = v_{c,k} + \frac{T_s}{C}\,|i_{g,k}|, \tag{12}$$

$$\text{No change (N):} \quad v_{c,k+1} = v_{c,k}. \tag{13}$$

For each candidate state $a \in \{1, 2, 3, 4, 5\}$, compute:

$$i_{g,k+1}^{(a)} \text{ from (5) using } v_i^{(a)}, \quad v_{c1,k+1}^{(a)},\, v_{c2,k+1}^{(a)} \text{ from (11)}.$$

The state-wise predictive equations for grid current and the capacitor voltages are written below.

State 1: $-V_{dc}$ (C1=D, C2=D)

$$v_i^{(1)} = -(v_{c1,k} + v_{c2,k}), \tag{14}$$

$$i_{g,k+1}^{(1)} = i_{g,k}\left(1 - \frac{RT_s}{L}\right) + \frac{T_s}{L}\left(v_i^{(1)} - v_{pcc,k}\right), \tag{15}$$

$$v_{c1,k+1}^{(1)} = v_{c1,k} - \frac{T_s}{C_1}|i_{g,k}|, \tag{16}$$

$$v_{c2,k+1}^{(1)} = v_{c2,k} - \frac{T_s}{C_2}|i_{g,k}|. \tag{17}$$

State 2: $-V_{dc}/2$ (C1=D, C2=N)

$$v_i^{(2)} = -v_{c1,k}, \tag{18}$$

$$i_{g,k+1}^{(2)} = i_{g,k}\left(1 - \frac{RT_s}{L}\right) + \frac{T_s}{L}\left(v_i^{(2)} - v_{pcc,k}\right), \tag{19}$$

$$v_{c1,k+1}^{(2)} = v_{c1,k} - \frac{T_s}{C_1}|i_{g,k}|, \tag{20}$$

$$v_{c2,k+1}^{(2)} = v_{c2,k}. \tag{21}$$

State 3: 0 (C1=C, C2=C)

$$v_i^{(3)} = 0, \tag{22}$$

$$i_{g,k+1}^{(3)} = i_{g,k}\left(1 - \frac{RT_s}{L}\right) + \frac{T_s}{L}\left(0 - v_{pcc,k}\right), \tag{23}$$

$$v_{c1,k+1}^{(3)} = v_{c1,k} + \frac{T_s}{C_1}|i_{g,k}|, \tag{24}$$

$$v_{c2,k+1}^{(3)} = v_{c2,k} + \frac{T_s}{C_2}|i_{g,k}|. \tag{25}$$

State 4: $+V_{dc}/2$ (C1=N, C2=D)

$$v_i^{(4)} = +v_{c2,k}, \tag{26}$$

$$i_{g,k+1}^{(4)} = i_{g,k}\left(1 - \frac{RT_s}{L}\right) + \frac{T_s}{L}\left(v_i^{(4)} - v_{pcc,k}\right), \tag{27}$$

$$v_{c1,k+1}^{(4)} = v_{c1,k}, \tag{28}$$

$$v_{c2,k+1}^{(4)} = v_{c2,k} - \frac{T_s}{C_2}|i_{g,k}|. \tag{29}$$

State 5: $+V_{dc}$ (C1=D, C2=D)

$$v_i^{(5)} = +(v_{c1,k} + v_{c2,k}), \tag{30}$$

$$i_{g,k+1}^{(5)} = i_{g,k}\left(1 - \frac{RT_s}{L}\right) + \frac{T_s}{L}\left(v_i^{(5)} - v_{pcc,k}\right), \tag{31}$$

$$v_{c1,k+1}^{(5)} = v_{c1,k} - \frac{T_s}{C_1}|i_{g,k}|, \tag{32}$$

$$v_{c2,k+1}^{(5)} = v_{c2,k} - \frac{T_s}{C_2}|i_{g,k}|. \tag{33}$$

4.2 Objective (Cost) Function and Optimal Switching

The cost function is defined to track the reference grid current i_g^* while regulating the capacitor voltages to their references v_{c1}^* and v_{c2}^*:

$$\begin{aligned} G^{(a)} = \lambda_i \left(i_{g,k+1}^* - i_{g,k+1}^{(a)} \right)^2 \\ + \lambda_{c1} \left(v_{c1}^* - v_{c1,k+1}^{(a)} \right)^2 \\ + \lambda_{c2} \left(v_{c2}^* - v_{c2,k+1}^{(a)} \right)^2 \\ + \lambda_{sw} \alpha \end{aligned} \tag{34}$$

where λ_{sw} is the weighting factor associated with switch transitions, and α represents the number of switch transitions.

The optimal switching state is selected as

$$a^* = \arg \min_{a \in \{1,2,3,4,5\}} G^{(a)}. \tag{35}$$

The corresponding switch vector $(S_1, \ldots, S_7)$ of state a^* is applied for the next sampling interval.

4.3 Algorithm Summary (FCS–MPC)

At each sampling instant k:

1. Measure $i_{g,k}$ and $v_{pcc,k}$, and read $v_{c1,k}$, $v_{c2,k}$.
2. For each candidate switching state $a = 1, \ldots, 5$:
   (a) Compute $v_i^{(a)}$ using (6),(7), (8), (9), (10).
   (b) Predict $i_{g,k+1}^{(a)}$ using (5).
   (c) Predict $v_{c1,k+1}^{(a)}$, $v_{c2,k+1}^{(a)}$ using (11), (12), (13) and the C/D/N logic.
   (d) Compute cost $G^{(a)}$ using (34).
3. Choose a^* using (35) and apply its switch vector.

5 Comparison

In addition to performance validation, a comparative analysis is shown to assess the relative merits of the proposed strategy compared with conventional control strategies. The comparison is based on important parameters that include computational burden, switching frequency, dynamic response, steady-state error, robustness, THD, implementation, and overall suitability as summarised in Table 2. These parameters directly influence the overall complexity, control effort, cost, and scalability of inverter systems. From Table 2, it is evident that the selected control strategy provides a modular structure and addresses multiple objectives simultaneously, such as accurate current tracking, voltage balancing, and optimal switching for lower failure rates, making it a

strong candidate for reliable grid-tied MLI operations. The proposed strategy delivers stable performance with reduced complexity, making it a practical and effective solution for medium and high-power applications.

Table 2 Comparison of Selected Control Strategy With Conventional Control Techniques

Parameters	PI	PR	Hysteresis	Deadbeat	SMC	Proposed
Computational Burden	Low	Low	Low	Medium	Medium	**High**
Switching Frequency	Fixed	Fixed	Variable	Fixed	Variable	**Variable**
Requires Modulator (PWM)	Yes	Yes	No	Yes	No	**No**
Dynamic Response	Slow	Moderate	Fast	Fast	Fast	**Fast**
Steady-State Error	Present	Eliminated	Present	Low	Low	**Very Low**
Robustness to Parameter Variation	Low	Low	Moderate	Low	High	**High**
Constraint / Multi-objective Handling	No	No	No	No	No	**Yes**
Output THD	Moderate	Low	High	Low	Moderate	**Low**
Tuning Complexity	Simple	Simple	Simple	Model dependent	Complex	**Model dependent**
DSP Implementation	Easy	Easy	Easy	Moderate	Moderate	**Feasible**
Overall Suitability for MLI Control	Medium	Medium	Low	Medium	Medium	**High**

6 Reliability Analysis

Reliability analysis is an important part of this study where the switch failure rates are calculated for open-loop operation as well as closed-loop operation (grid-tied as well as standalone mode) to demonstrate the effectiveness of the proposed algorithm in improving the reliability of the multilevel inverter.

Reliability in multilevel inverter systems is a multi-faceted concern, as several constituent components — including DC sources, capacitors, PCB assemblies, cooling mechanisms, and semiconductor switching devices — are each susceptible to failure under operational stress. Among these, semiconductor devices consistently emerge as the most vulnerability-prone elements, owing to the complex and time-varying physical stresses they endure during normal operation. Without a thorough characterization of these stresses, any reliability assessment of an MLI design remains fundamentally incomplete.

In this work, the reliability analysis is focused on the switching devices, specifically considering all switches S_1 through S_7 to share an identical device specification. The selected component is the Infineon Trenchstop series IKWK75T60NT IGBT, equipped with an anti-parallel diode, which is representative of practical MLI implementations at this power level. To extract accurate thermal stress profiles for each device, the PLECS simulation platform was employed in conjunction with the manufacturer-provided thermal models derived from the official datasheet. This approach allows device-level junction temperature variations and power loss distributions to be captured under realistic switching conditions.

Once the thermal stress data were obtained, the individual failure rates of all IGBTs were evaluated using the FIDES Guide on Reliability Methodology for Electronic Systems [20] — a well-established industry framework for component-level

reliability quantification. This methodology accounts for both thermal and non-thermal stress contributors, enabling a physics-informed estimation of each switch's failure behavior across the inverter's expected operating profile.

6.1 FIDES Failure Rate Model

The FIDES methodology expresses the total failure rate λ of a component as

$$\lambda = \lambda_{\text{physical}} \times \Pi_{\text{PM}} \times \Pi_{\text{Process}}, \tag{13}$$

where Π_{PM} is the project management factor and Π_{Process} accounts for manufacturing and process quality. The physical failure rate $\lambda_{\text{physical}}$ is computed by summing contributions over all operating phases:

$$\begin{aligned}\lambda_{\text{physical}} = \sum_{i}^{\text{Phases}} \left(\frac{t_{\text{annual}}}{8760}\right)_i \times \Big(&\lambda_{0\text{TH}} \cdot \Pi_{\text{Thermal}} \\ &+ \lambda_{0\text{TCyCase}} \cdot \Pi_{\text{TCyCase}} \\ &+ \lambda_{0\text{TCySolderjoints}} \cdot \Pi_{\text{TCySolderjoints}} \\ &+ \lambda_{0\text{RH}} \cdot \Pi_{\text{RH}} \\ &+ \lambda_{0\text{Mech}} \cdot \Pi_{\text{Mech}}\Big)\end{aligned} \tag{14}$$

6.2 Parameter Values for Failure Rate Calculation

The MPC of the multilevel inverter has been modified to enhance switch reliability, and this has been validated through PLECS simulation and FIDES guideline-based reliability analysis. Table 3 lists the numerical values of all FIDES model parameters used in the failure rate calculations, extracted from the device datasheet and the FIDES standard [20].

Table 3 Parameter Values Used in Failure Rate Calculations Using Datasheet and FIDES Data

Parameter	**Value**	**Parameter**	**Value**
$\lambda_{0\text{TH}}$	0.3021	$\lambda_{0\text{RH}}$	0.0589
$\lambda_{0\text{TCyCase}}$	0.00303	$\lambda_{0\text{Mech}}$	0.0589
$\lambda_{0\text{TCySolderjoints}}$	0.01515	$C_{\text{sensitivity}}$	5.20
Π_{PM}	1.7	Π_{Process}	4
Π_{Induced}	3.3837		

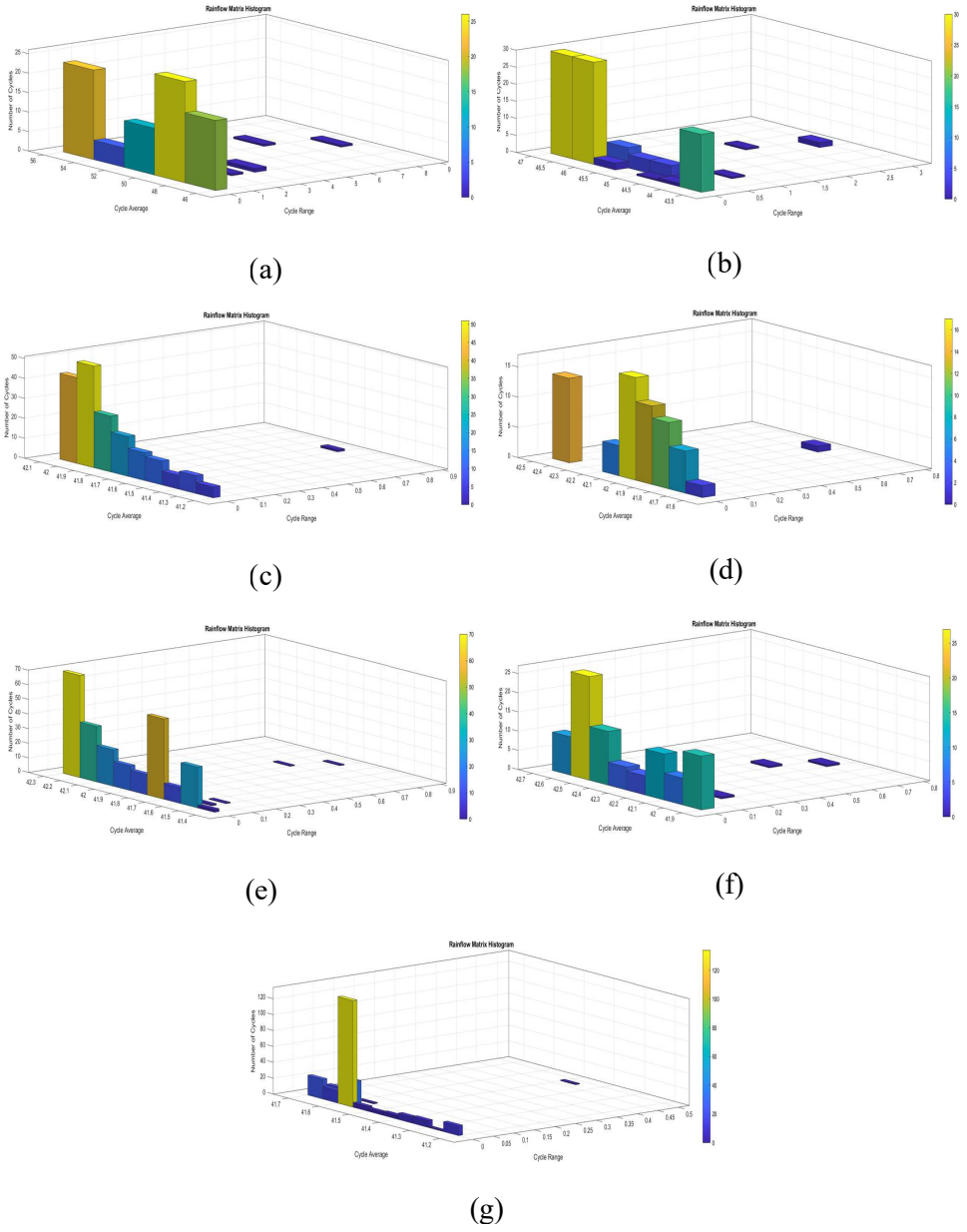


Fig. 5 Histogram Charts of Rain flow Counting of Switches (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, (f) S_6, (g) S_7

7 Results and Discussion

In order to validate the proposed system, both simulation and hardware studies were carried out. Firstly, open-loop results are presented, followed by the closed-loop MPC results (standalone and grid-tied).

7.1 Simulation Results

Simulation was carried out in MATLAB (Simulink). Fig. 6 shows the open-loop output (inverter output voltage v_{inv}, i_{inv}, v_{C1}, and v_{C2}) for a constant R load ($R = 50\ \Omega$), and Fig. 7 shows results for the load resistance step from R_1 to R_2 ($R = 50\ \Omega$ to $R = 50\ \Omega$). The output voltage waveform remains nearly constant despite the load variation. Fig. 8 shows the open-loop response with a fixed RL load ($R = 50\ \Omega, L = 25mH$). The capacitor voltages are observed to remain balanced during the entire period, with only small ripple, which confirms effective self-balancing of the capacitors even with an inductive load. Fig. 9 demonstrates the results for a step change in RL load ($R = 100\ \Omega, L = 50mH$ to $R = 50\ \Omega, L = 25mH$). When the load is reduced, the inductor current increases as expected, but it remains smooth and sinusoidal, with no major distortion or oscillation. Fig. 10 shows the results for the RL-to-R transition ($R = 50\ \Omega, L = 25mH$ to $R = 50\ \Omega$). After the transition, the current waveform quickly adjusts to the new resistive condition and becomes more in phase with the voltage, as expected, without large transients or oscillations. The capacitor voltages also remain balanced with only a small ripple, indicating proper charge distribution even during the load shift. In all of the open-loop results discussed above, the MLI operates satisfactorily as expected.

Next, the closed-loop results are presented to compare the open-loop response with the proposed control algorithm. Fig. 11 (standalone) and Fig. 12 (grid-tied) highlight the improvement in dynamic response and current tracking compared to open-loop operation. In Fig. 6, load current is tracked as a reference (i^*_{ref}) for a load resistance of $R = 50\ \Omega$ with a step change in i^*_{ref}) at $t = 0.1sec$. The multilevel inverter produces a clean and stable five-level output waveform during steady state as well as dynamic conditions. The stepped voltage and corresponding current waveforms clearly show all five levels without noticeable distortion, indicating proper switching operation. Under this load condition, the output current remains well regulated. The controller can track the reference current accurately, with negligible steady-state error and very small phase differences. The zoomed-in view of a single cycle further highlights the smooth tracking performance, even during dynamic conditions. The capacitor voltages remain balanced throughout operation, with small ripple. However, as seen, the ripple increases slightly with the load current.

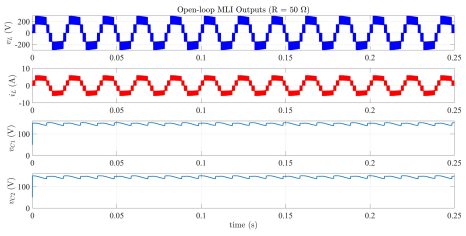


Fig. 6 Output waveform with constant R load

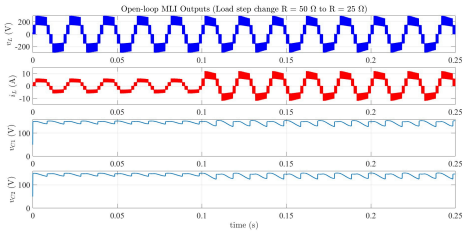


Fig. 7 Output waveform with variable R load

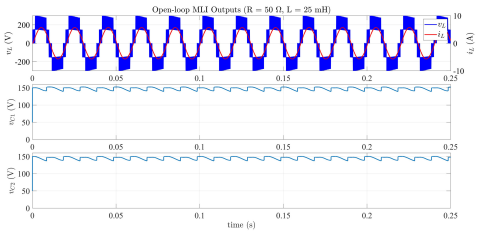


Fig. 8 Output waveform with RL load.

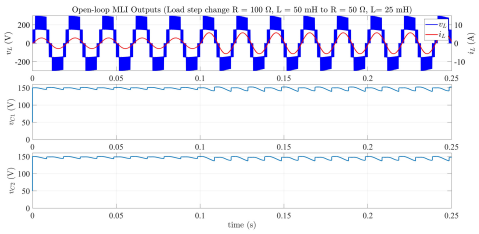


Fig. 9 Output waveform with variable RL load

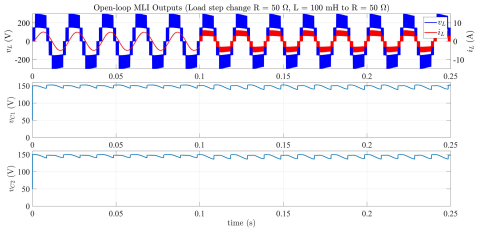


Fig. 10 Output waveform with RL to R load transition

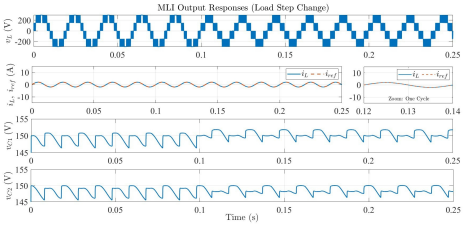


Fig. 11 Output waveform with MPC in standalone mode.

In Fig. 12, the output waveform with the proposed MPC is demonstrated in grid-tied mode. The inverter's output voltage forms a clean, stepped staircase shape. The reference current i^*_{ref} is changed at $t = 0.1sec$ in a single step to see how the controller reacts to a sudden disturbance. The zoomed-in inset shows the current settling back into its smooth sinusoidal shape and almost immediately overlaps i^*_{ref}, which demonstrates a fast controller response and excellent tracking.

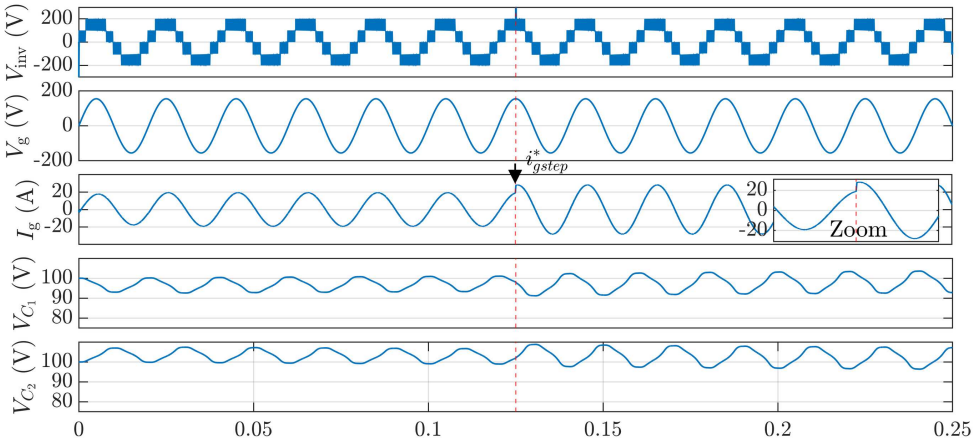


Fig. 12 Output waveform with MPC in grid tied mode.

7.2 Hardware Results

The experimental hardware setup comprises a DC power supply, a variable resistive-inductive (RL) load, an oscilloscope, a multilevel inverter (MLI) with Texas Instruments TMS320F28379D C2000 LaunchXL control card, and measurement probes. The complete setup is illustrated in Fig. 13 . The overall system is designed for 1 kW power. Software findings are validated through hardware implementation. Fig. 14 gives the steady-state output under a constant R load. Fig. 15 and Fig. 16 show how the system responds to a load resistance step and an RL-to-R transition. The switching frequency is varied for R and RL_1 loads in Fig. 17 and Fig. 18 and the modulation index in Fig. 19 and Fig. 20. Fig. 21 shows the inverter's start-up behaviour, and Fig. 22 shows the closed-loop hardware response to a step change in the reference grid current. Overall, the hardware results align closely with the simulation, confirming that the proposed control approach holds up in practice.

In Fig. 14, under steady-state operation, the inverter produces stable voltage and current waveforms across all tested conditions. Across different load types, modulation levels, and frequencies, the inverter operation in open-loop conditions is satisfactory. However, the reliability is lower for the open-loop system as discussed in the previous sections and need the closed loop control as proposed.

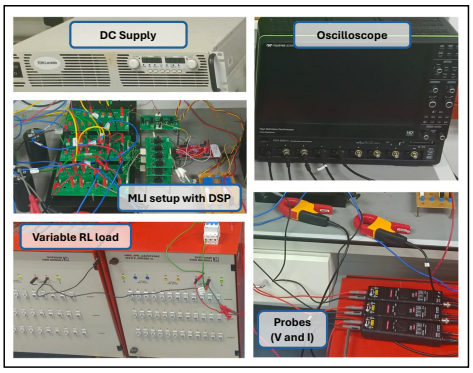


Fig. 13 Hardware Setup

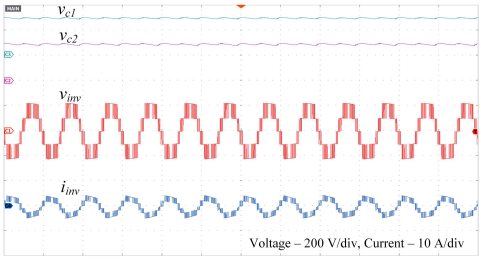


Fig. 14 Output waveform in steady state

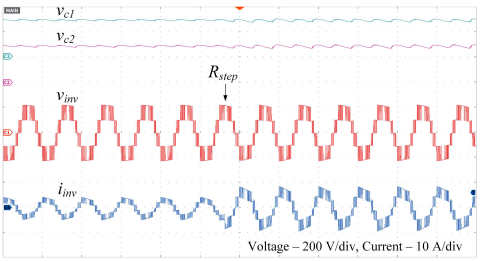


Fig. 15 Output waveform with changing R_1 to R_2 load

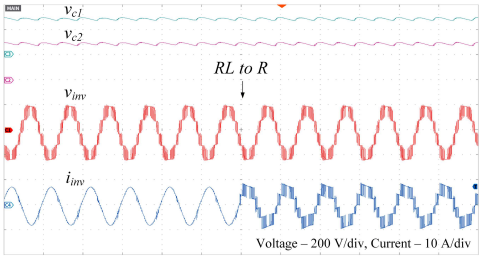


Fig. 16 Output waveform with changing RL to R load

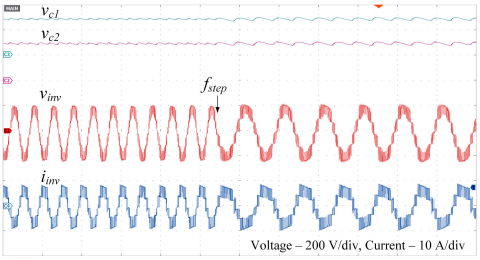


Fig. 17 Output waveform with R load under changing frequency

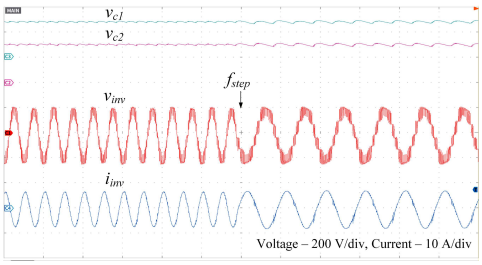


Fig. 18 Output waveform with RL_1 load under changing frequency

Secondly, Fig. 15 reflects the output waveforms of the multilevel inverter under dynamic load conditions, transitioning from $R_1 = 50\,\Omega$ to $R_2 = 25\,\Omega$. The voltage

output maintains a stable multilevel stepped waveform characteristic. In Fig. 16 , the load is changed from $R = 50\,\Omega$ and L = 100 mH to a purely resistive $R = 50\,\Omega$ load. During this transition, the output voltage remains stable, while the output current adapts according to the new load characteristics. No significant oscillations or distortions are observed during the load change. In Fig. 17 and Fig. 18, the frequency is varied while operating with R and RL_1 load to assess the dynamic response of the system. The value of R is 100Ω and L_1 is 50 mH. In case of R load, The output waveforms successfully tracks the new frequency. While, in case of RL_1 load, the output voltage and current waveforms successfully track the new frequency, maintaining their sinusoidal nature and stable amplitude. This demonstrates the converter's ability to handle frequency variations while preserving proper current under inductive loading conditions.

Further tests are carried out by changing the modulation index with R and RL load condition in Fig. 19 and Fig. 20. The value of R is 50Ω, L is 100 mH. The output voltage magnitude follows the modulation change smoothly, while the output current maintains a stable waveform. This confirms that the inverter operates reliably under modulation variation. In Fig. 21, at the start-up, the output voltage and current rise gradually in a stable manner, without transients or oscillations, and show a smooth and undisturbed start-up response.

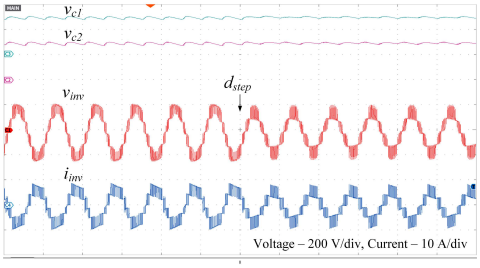


Fig. 19 Output waveform with R load under changing Modulation

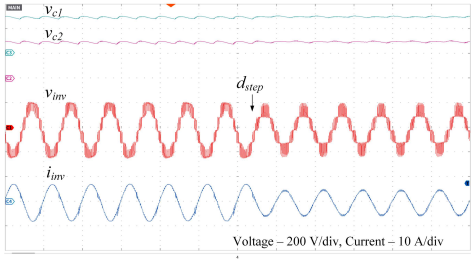


Fig. 20 Output waveform with RL load under changing Modulation

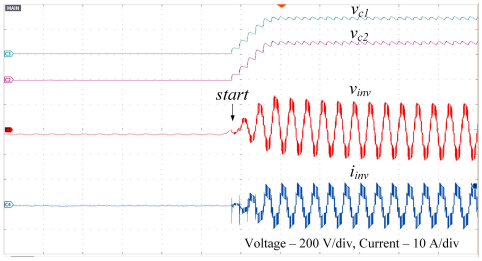


Fig. 21 Output waveform at start-up of inverter

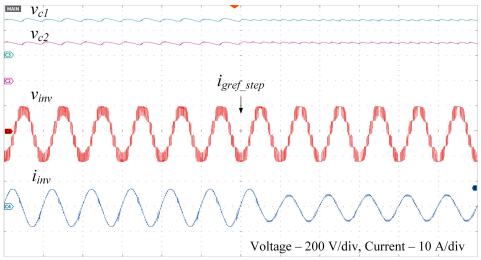


Fig. 22 Output waveform in closed loop operation

Fig. 22 shows the closed-loop response of the system in grid-tied operation. When the grid current reference is reduced, the inverter's modulation current changes in response, causing the actual grid current to reduce as well. This behaviour confirms that the MPC controller can track the reference current effectively; as the reference decreases in step, the actual grid current also decreases to track the reference. As demonstrated in the figure the closed-loop control is also modulating the voltage waveform to maintain the desired reference current. The capacitor voltage ripple remains low, as seen from the figure. The change in the ripple magnitude can be observed as a result of the change in the grid current. However, the capacitor voltages remain balanced throughout the inverter operation. Overall, the hardware results closely match the simulation outcomes and confirm that the proposed control approach ensures stable operation while maintaining higher system reliability. As seen from Table 4, the reliability is expected to be higher for closed-loop operation in standalone mode as compared to the open-loop operation and enhanced further with closed-loop operation in grid-tied mode. Using the FIDES model parameters listed in Table 3 along with the thermal stress data obtained from PLECS simulations, the individual failure rates for all seven switches (S_1–S_7) of the topology were calculated. The observations are presented in Table 4 in units of FIT (Failures in Time, i.e., failures per 10^9 operating hours). The proposed MPC demonstrates improved predictive control performance compared to open-loop operation.

In Table 4, It can be seen that the multilevel inverter topology exhibits significantly higher failure rates when operated without MPC compared to the same topology with the proposed strategy. This demonstrates the effectiveness of the proposed algorithm in enhancing the system reliability.

Table 4 Switch Failure Rates (FIT) in Open and Closed Loop Operation

Switch	**Open Loop Operation**	**Closed Loop Operation (Standalone)**	**Closed Loop Operation (Grid-Tied)**
S_1	884962.2	644610.0	613786.0
S_2	880536.1	842333.7	800427.0
S_3	852123.5	644632.3	614057.8
S_4	854509.4	709635.4	674420.6
S_5	852653.3	703500.3	668841.3
S_6	854608.2	717550.1	682238.9
S_7	848441.6	685416.6	652330.9

8 Conclusion

In this work, a proposed model predictive control-based strategy to enhance system reliability and reduce the switch failure rate is proposed. The proposed technique

is implemented on an existing five-level multilevel inverter topology reported in the literature.

Various parameters such as switching frequency, modulation conditions, and load variations were modified during simulation. The output voltage and current waveforms were observed to remain nearly unchanged and stable throughout the variations. The open-loop results indicate that with level shifted PWM based open loop control the chosen topology itself is capable of maintaining consistent performance, which makes it suitable for practical implementation and further study of the proposed closed-loop control. Even after integrating the proposed enhanced reliability MPC and operating the system in standalone as well as grid-tied mode, the output response remained stable and well regulated. The simulation results were then validated through hardware implementation, where similar output characteristics were obtained. The reliability analysis shows the effectiveness of MPC control compared to open-loop operation. This also indicates that the proposed control strategy is generic and can work effectively with any stable topology without introducing significant performance deviation or instability.

References

[1] L. Malesani and P. Tenti, "PWM current control techniques of voltage source converters—a survey," *IEEE Trans. Ind. Electron.*, vol. 40, no. 6, pp. 631–640, Dec. 1993.

[2] M. H. Mondol, M. A. Rahman, S. P. Biswas, M. R. Islam, M. F. Kibria, and K. M. Muttaqi, "A new integrated multilevel inverter topology for renewable energy transformation," *IEEE Trans. Ind. Appl.*, vol. 59, no. 3, pp. 3031–3043, May–Jun. 2023, doi: 10.1109/TIA.2023.3246461.

[3] K. Deepak *et al.*, "Performance comparisons of multilevel inverter topologies," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 14567–14578, Dec. 2023.

[4] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[5] I. Harbi, S. Bayhan, S. Kouro, and J. Rodríguez, "Model predictive control of multilevel inverters: Challenges and recent advances," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3456–3472, Mar. 2024.

[6] P. K. Pal, K. C. Jana, Y. P. Siwakoti, J. S. M. Ali, and F. Blaabjerg, "A switched-capacitor multilevel inverter with modified pulsewidth modulation and active DC-link capacitor voltage balancing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1215–1229, Apr. 2024, doi: 10.1109/JESTPE.2023.3285690.

[7] A. Tiwari, V. Kumar, R. Agarwal, M. Amir, M. A. Alharbi, and S. M. Muyeen, "Five-level MLI-based grid-connected photovoltaic systems: A review on control

methodologies, modulation strategies and recent developments," *IEEE Open J. Power Electron.*, vol. 6, pp. 78–108, 2025, doi: 10.1109/OJPEL.2024.3515288.

[8] H. Le, A. Dekka, and D. Ronanki, "Model predictive control of a new five-level inverter for medium voltage applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Nashville, TN, USA, 2023, pp. 2597–2602, doi: 10.1109/ECCE53617.2023.10362188.

[9] D. Dwivedi, A. Hussein, and K. A. Chinmaya, "Design of a novel five-level stacked dual-output converter for EV application," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 6, no. 3, pp. 920–930, Jul. 2025, doi: 10.1109/JESTIE.2025.3547789.

[10] S. P. Gautam *et al.*, "Investigating the effectiveness of H-bridge in mitigating switch faults of a single-phase five-level inverter," *IEEE Access*, vol. 13, pp. 27729–27742, 2025, doi: 10.1109/ACCESS.2025.3537896.

[11] D. Saha and T. Roy, "Implementation of model predictive control for conventional switched capacitor multilevel inverter to reduce input current peak and capacitor voltage ripple," in *Proc. 3rd Int. Conf. Convergence Technol. (I2CT)*, Pune, India, 2018, pp. 1–6, doi: 10.1109/I2CT.2018.8529682.

[12] A. Al Shaheer, S. M. Hammad, A. Sarwar, M. Zaid, S. Ahmad, and H.-D. Liu, "A single phase five level switched capacitor inverter with common ground configuration," *IEEE Access*, vol. 12, pp. 101814–101828, 2024, doi: 10.1109/ACCESS.2024.3430538.

[13] M. A. Anees, M. D. Siddique, S. Mekhilef, M. B. Mubin, M. Seyedmahmoudian, and A. Stojcevski, "A new configurable SC-based dual source inverter topology with improved reliability," in *Proc. IEEE Int. Conf. Energy Technol. Future Grids (ETFG)*, Wollongong, Australia, 2023, pp. 1–6, doi: 10.1109/ETFG55873.2023.10407837.

[14] A. Iqbal, M. D. Siddique, B. P. Reddy, and P. K. Maroti, "Quadruple boost multilevel inverter (QB-MLI) topology with reduced switch count," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7372–7377, Jul. 2021, doi: 10.1109/TPEL.2020.3044628.

[15] S. Mondal, S. P. Biswas, M. S. B. Islam, M. R. Islam, and A. Fekih, "A 3-phase switched-capacitor single-source MLI with self-voltage balancing and boosting ability," *IEEE Trans. Appl. Supercond.*, vol. 34, no. 8, pp. 1–5, Nov. 2024.

[16] S. Majumdar, B. Mahato, and K. C. Jana, "Implementation of an optimum reduced components multicell multilevel inverter (MC-MLI) for lower standing voltage," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2765–2775, Apr. 2020.

[17] N. Kumar, T. K. Saha, and J. Dey, "Multilevel inverter (MLI)-based stand-alone photovoltaic system: Modeling, analysis, and control," *IEEE Syst. J.*, vol. 14, no.

1, pp. 909–915, Mar. 2020.

[18] S. K. Annam, R. K. Pongiannan, and N. Yadaiah, "A hysteresis space vector PWM for PV tied Z-source NPC-MLI with DC-link neutral point balancing," *IEEE Access*, vol. 9, pp. 54420–54434, 2021.

[19] K. Molli, P. A. D. V. Raj, and N. P. Subramaniam, "Transformer based 25-level T-type MLI for renewable energy integration," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 4, pp. 1127–1136, Oct. 2022.

[20] S. Munawar, M. S. Iqbal, M. Adnan, M. A. Akbar, and A. Bermak, "Multilevel inverters design, topologies, and applications: Research issues, current, and future directions," *IEEE Access*, vol. 12, pp. 149320–149350, 2024.

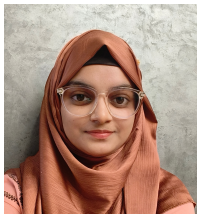
[21] S. B. Mohanty and S. Mohanty, "Modified asymmetrical H-bridge MLI with minimum switching loss and harmonic distortion using JAYA algorithm," *IEEE Access*, vol. 12, pp. 78854–78864, 2024.

[22] K. Molli and P. A. D. V. Raj, "SST-based 25-level T-type MLI for integration of microgrids," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 5, no. 4, pp. 1519–1528, Oct. 2024.

[23] C. Bharatiraja, S. Jeevananthan, and J. L. Munda, "A timing correction algorithm-based extended SVM for three-level neutral-point-clamped MLI in over modulation zone," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 233–245, Mar. 2018.

[24] V. S. Prasadarao K, S. Peddapati, and S. Naresh, "A new fault-tolerant MLI—investigating its skipped level performance," *IEEE Trans. Ind. Electron.*, vol. 69, no. 2, pp. 1432–1442, Feb. 2022.

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