

Monolithic Vertically Stacked Carbon Nanotube Transistor with Emergent Negative Transconductance for Ternary Logic

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Abstract

Vertical integration offers an opportunity to engineer transistor responses as well as device placement. Here, we demonstrate negative transconductance (NTC) using two carbon nanotube (CNT) network channels monolithically integrated on opposite sides of a common gate. The vertically stacked NTC transistor connects the channels internally through a via and retains three external terminals. Sequential processing yields a lower channel that is electron-dominant ambipolar under top-gate operation after HfO_2 deposition, while the subsequently deposited upper channel remains p-type. Their contrasting gate responses shift the current bottleneck between layers, producing a local current peak. Channel geometry and upper-layer CNT density tune this response, yielding an extracted peak-to-valley current ratio above 10^4 at a drain-voltage magnitude of 0.1 V. Paired with an n-type CNT pull-down transistor, the device enables a ternary inverter at a 3 V supply, with three output states and two voltage-gain peaks exceeding maximum 6. Comparisons across fabricated variants link the NTC profile to intermediate-state formation and reveal a trade-off between static noise margins. These results establish vertical stacking as a route to single-semiconductor transfer-function engineering for ternary logic.

Introduction

Monolithic three-dimensional integration and complementary field-effect transistor (CFET) architectures exploit the vertical dimension to increase transistor density. To date, however, vertical integration has primarily served as a geometric strategy: stacked devices generally preserve the monotonic transfer characteristics and binary operation of their constituent transistors [1–10]. If the vertical stack itself could generate an electrical response absent from the individual layers, vertical integration could extend from geometric compaction to functional device engineering. This possibility is particularly relevant to multi-valued logic (MVL), which encodes more than two logic states at a node and requires stable intermediate output levels. Existing ternary and higher-radix devices, however, often create these intermediate states using additional semiconductor materials, laterally distributed active elements, or auxiliary optical and electrical controls, introducing material, area, or control overhead [11].

A ternary inverter requires two distinct output transitions and a finite input-voltage range over which the pull-up and pull-down paths have comparable conductance, thereby establishing an intermediate output state. Negative transconductance (NTC), defined as $(g_m = \partial I_D / \partial V_G < 0)$, offers a compact device-level route to this behavior. Here, g_m , I_D and V_G denote the transconductance, drain current and gate voltage, respectively. When the current peak of an NTC device is appropriately aligned with the opposing inverter branch, it can create two conductance-matching boundaries and open a finite intermediate-state window [12, 13]. NTC-based MVL devices have been realized using dissimilar-semiconductor heterojunctions [12–21], laterally segmented or series-connected channel elements [22–24], and auxiliary optical or electrical controls [23, 25–28]. Vertically integrated [29–32] and single-semiconductor ternary devices [33–35] have also been reported, but their functional elements often remain laterally separated or depend on additional gates, resistive loads, or discrete circuit components. A key opportunity is

therefore to generate NTC within the vertically integrated active stack itself, so that vertical integration contributes directly to the transfer function required for higher-radix operation.

Carbon nanotube (CNT) networks are particularly suited to this approach because they combine low-temperature processability with strong sensitivity of carrier transport to their interfacial environment. Semiconducting CNT networks can be deposited from solution near room temperature, enabling an upper semiconductor channel to be formed after completion of the underlying device stack without another high-temperature channel-growth step [2, 36]. At the same time, CNT charge injection and carrier polarity are highly sensitive to metal contacts [37–40] and the dielectric environment [41–44], allowing sequential processing to create contrasting gate responses within the same semiconductor. Leveraging these complementary attributes, we use vertical integration as a means of transfer-function engineering by positioning two CNT network channels on opposite sides of a common gate and connecting them internally in series through an interlayer via. Following HfO_2 processing, the lower channel develops electron-dominant ambipolar transport, whereas the upper channel, deposited after completion of the dielectric process, remains p-type. During a common-gate sweep, these contrasting responses cause the current-limiting role to shift from one layer to the other, generating a local current peak and an associated valley-to-peak NTC interval in the combined transfer characteristic. The stack thus converts process-defined polarity asymmetry into an emergent nonmonotonic transfer function within a single-semiconductor, common-gate, three-terminal transistor.

We further show that the relative alignment between the transfer characteristics of the two stacked channels can be engineered using channel geometry and layer-specific CNT network density as representative, experimentally accessible design parameters. This control produces a peak-to-valley current ratio above 10^4 at $|V_D| = 0.1$ V. When the vertically stacked NTC transistor is used as the pull-up element of an inverter and appropriately matched to an n-type CNT field-effect transistor (FET) serving as the pull-down, the circuit exhibits three output states and two voltage-gain peaks with a maximum above 6, at $V_{DD} = 3$ V. Across fabricated device variants, the shape and alignment of the engineered NTC profile – not PVR alone – determine whether the same circuit topology exhibits binary-like switching or a well-resolved ternary response, and set the operating window of the intermediate state. These results establish monolithic vertical CNT stacking as an architecture that unites sequential vertical channel integration with transfer-function engineering for ternary logic.

Results

Device architecture and emergence of stack-generated negative transconductance

The vertically stacked NTC transistor exhibits a local current peak that is absent from the transfer characteristics of its constituent channels. This response is obtained by combining the two channels in a common-gate series architecture (Fig. 1a). The lower and upper carbon nanotube (CNT) networks lie on

opposite sides of a Ti/Pd gate, which functions as a top gate for the lower channel and a bottom gate for the upper channel. The external source contacts the lower channel, whereas the external drain contacts the upper channel. An interlayer via joins their remaining terminals, completing the series conduction path without introducing an additional external terminal. The vertically stacked NTC transistor therefore retains three external terminals, with one gate voltage modulating both channels along the source-drain path. Cross-sectional transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS) mapping resolve the common gate between the lower and upper HfO₂ dielectrics, supporting the intended vertical gate-stack configuration (**Supplementary Fig. 1**).

Sequential fabrication gives the two channels different process histories despite their common semiconductor material. The lower CNT network is formed before HfO₂ deposition, whereas the upper network is deposited after formation of the common gate, upper dielectric stack and via opening (**Supplementary Fig. 2**). The top-view scanning electron microscopy (SEM) image in Fig. 1a identifies the terminal arrangement, and the multiscale images in **Supplementary Fig. 3** trace this layout from the device array to the active channel region. Both the upper and lower channels contain interconnected nanotubes with numerous CNT–CNT junctions, providing the morphological basis for percolative transport through each network (**Supplementary Fig. 4a**). Complementary Raman characterization assesses the structural quality of the deposited CNT material. Measured after formation of the lower-channel network, the spectrum exhibits a weak D band and a G/D intensity ratio of approximately 230, consistent with a low defect level in the probed CNT material (**Supplementary Fig. 4b**). Also, the radial breathing mode (RBM) peak at approximately 175 cm⁻¹ in **Supplementary Fig. 4c** corresponds to an estimated CNT diameter of approximately 1.4 nm [45, 46].

Independent characterization reveals the different electrical responses combined within the vertically stacked NTC transistor (Fig. 1b). The representative lower and upper channels both have channel width $W_{\text{ch}} = 20 \mu\text{m}$, channel length $L_{\text{ch}} = 4 \mu\text{m}$ and a CNT network density ρ_{CNT} of 11–13 tubes/ μm . In the isolated measurements, the shared-gate bias is labelled $V_{\text{Top-gate}}$ for the lower-layer transistor and $V_{\text{Bottom-gate}}$ for the upper-layer transistor, reflecting the position of the same gate electrode relative to the channel being probed. At $V_{\text{D}} = +0.1 \text{ V}$, the lower-layer transistor exhibits a U-shaped ambipolar transfer characteristic with a larger electron current than hole current. By contrast, the upper-layer transistor measured at $V_{\text{D}} = -0.1 \text{ V}$ exhibits p-type transport, with its hole-current magnitude decreasing as $V_{\text{Bottom-gate}}$ becomes more positive. Thus, the same CNT semiconductor supports two different gate responses: the rising electron branch of the lower channel overlaps the declining hole branch of the upper channel. This overlap allows a common-gate sweep to change the relative conductances of the two channels, rather than simply increasing or decreasing their conduction together.

The transfer characteristic of the vertically stacked NTC transistor connects this electrical asymmetry to the observed current peak (Fig. 1c). Here, $V_{\text{Common-gate}}$ denotes the voltage applied to the shared gate during series operation. The measured current broadly follows the lower-current envelope of the isolated transfer characteristics, consistent with the less conductive channel limiting the series current. This

comparison is qualitative because the isolated measurements apply the drain bias to each transistor separately, whereas the applied voltage is divided internally between the channels in the vertically stacked NTC transistor. The conductance-state schematics in Fig. 1d illustrate the corresponding interpretation. In Region I, the upper p-type channel remains relatively conductive while the lower ambipolar channel limits transport. Increasing $V_{\text{Common-gate}}$ initially suppresses lower-channel hole conduction, bringing the current to I_{valley} . Further increasing the gate voltage restores electron conduction in the lower channel while the upper channel still supports hole conduction, relieving the lower-layer bottleneck and raising the current toward I_{peak} in Region II. Near this peak-forming condition, the two channels have comparable current-supporting capabilities. At higher gate bias, continued suppression of upper-channel hole conduction makes the upper layer the principal bottleneck in Region III, and the current decreases despite stronger electron conduction in the lower layer. The local peak therefore arises from the competing gate dependences of the series-connected channels rather than from a peak already present in either isolated transfer characteristic. For the vertically stacked NTC transistor measured at $V_D = -0.1$ V, the plotted current magnitude $|I_D|$ equals $-I_D$. Its increase from I_{valley} to I_{peak} corresponds to the signed I_D becoming more negative as $V_{\text{Common-gate}}$ increases, giving $g_m = \partial I_D / \partial V_{\text{Common-gate}} < 0$ over the valley-to-peak interval. The associated current contrast is quantified by the peak-to-valley current ratio, $\text{PVR} = I_{\text{peak}}/I_{\text{valley}}$, with both currents extracted from $|I_D|$ as described in Methods. The transfer measurement therefore identifies both the gate-voltage interval of NTC and the prominence of the local peak relative to the preceding valley. The gate leakage current remains well below the drain-current magnitude around I_{peak} , supporting a source-drain transport origin of the peak rather than a response dominated by direct gate leakage.

The output characteristics provide a complementary comparison of isolated-channel conduction and common-gate series operation (Fig. 1e). The upper-layer hole current and lower-layer electron current reach magnitudes of approximately 10–15 μA under their respective on-state conditions. The vertically stacked NTC transistor carries substantially less current, consistent with the constraints imposed by passing the terminal current through both channels under a shared gate. More importantly, its output curves are not ordered monotonically with $V_{\text{Common-gate}}$: at a fixed V_D , the current magnitude changes nonmonotonically with gate bias, as observed in the transfer characteristic. This behavior is consistent with the gate-dependent change in the current-limiting channel.

Process engineering of ambipolar transport for vertically stacked NTC operation

High- κ dielectric processing is known to modify carrier polarity in CNT transistors, with initially p-type devices evolving toward ambipolar or n-type operation after HfO_2 and related high- κ atomic layer deposition (ALD) processes. Previous studies have attributed this evolution to oxygen desorption during elevated-temperature ALD processing and suppression of oxygen re-adsorption through dielectric encapsulation, together with electrostatic n-doping by positive fixed charge. Positive-charge-induced

field-effect doping can reduce the width of the electron Schottky barriers at the metal/CNT contacts, thereby increasing electron tunnelling. The magnitude of the polarity change depends on the oxide properties, deposition conditions and contact metal [41–44]. For the transfer characteristic targeted here, however, the lower channel must retain hole conduction at negative gate bias while providing an accessible electron branch, rather than undergoing complete conversion to unipolar n-type transport. We therefore formed the lower CNT network with Ti/Pd source and drain contacts before HfO₂ ALD so that the high-work-function Pd contacts would continue to support hole conduction after ALD, while the dielectric-induced effects of HfO₂ enabled electron injection [44]. Figure 2a presents a qualitative, literature-based interpretation of this combined contact and process design. The process schematic and A–A' cross section show HfO₂ covering the Ti/Pd-contacted CNT network on Si/SiO₂ and illustrate oxygen desorption induced by the ALD thermal cycle and positive fixed charge associated with the deposited dielectric. Before ALD, the Pd/CNT alignment favors hole injection, whereas the electron Schottky barriers at the source and drain are sufficiently large to block appreciable electron injection within the relevant gate-voltage range. After ALD, the downward shift of the CNT bands lowers the effective barrier for electron injection while the Pd contacts continue to support hole injection. The right-hand diagrams illustrate the resulting bias-selective transport, in which hole conduction is favored at V_G , $V_D < 0$ and electron conduction is favored at V_G , $V_D > 0$, giving rise to ambipolar rather than complete unipolar n-type transport.

The electrical change produced by this lower-channel process step was resolved by measuring the same lower-layer transistor, with $W_{ch} = 20 \mu\text{m}$, $L_{ch} = 4 \mu\text{m}$ and $\rho_{CNT} = 11\text{--}13 \text{ tubes}/\mu\text{m}$, through the Si/SiO₂ back gate before and after HfO₂ deposition (Fig. 2b). Both states were measured at $V_D = -0.1 \text{ V}$, retaining the CNT network, Ti/Pd contacts, back-gate configuration and drain-bias polarity. Before deposition, denoted w/o ALD, the plotted $-I_D$ decreases monotonically as $V_{Back\text{-}gate}$ becomes more positive, with no discernible electron branch between -3 and 3 V . This response is consistent with inefficient electron injection within the measured gate-voltage range. After deposition, denoted w/ ALD, the transfer characteristic becomes U-shaped, with a hole branch at negative $V_{Back\text{-}gate}$ and an electron branch at positive $V_{Back\text{-}gate}$. The decrease in the hole branch and appearance of the electron branch are consistent with the energy-band diagram (EBD) interpretation, in which ALD weakens the initial adsorbate-induced p-type tendency while lowering the effective barrier for electron injection.

Obtaining ambipolar transport alone is not sufficient for the vertically stacked NTC transistor because the electron branch must also be positioned within the gate-voltage range required for the complete device. The top-gate measurement in Fig. 2c therefore examines how the final gate configuration satisfies this requirement. The top-gate characteristic was measured at $V_D = +0.1 \text{ V}$ following the conventional polarity for n-type operation (the transfer shape and electron-dominant response were qualitatively unchanged at $V_D = -0.1 \text{ V}$). In the back-gate configuration, the lower channel is modulated through 50 nm SiO_2 , whereas top-gate operation uses 30 nm HfO_2 . Compared with back-gate operation, the measured top-gate response exhibits a reduction in the electron-side subthreshold swing from

approximately 0.74 to 0.23 V/dec, together with a lower electron-branch threshold voltage (V_T), consistent with stronger gate coupling through the smaller equivalent oxide thickness [47]. This electron dominance does not indicate carrier-selective gate coupling. Rather, the lower electron-branch V_T places electron conduction at a larger effective overdrive within the measured $V_{\text{Top-gate}}$ range, whereas the hole branch remains farther from its turn-on condition. The electron current therefore exceeds the hole-current magnitude, producing electron-dominant ambipolar transport.

More importantly, this top-gate response is not an isolated electrostatic improvement but an intended consequence of the vertical fabrication sequence. The two CNT networks occupy the same lateral footprint, yet their vertical ordering allows them to acquire different process histories while retaining the same semiconductor material. The lower CNT network is deposited first and subsequently undergoes HfO_2 ALD. The common gate then operates as its top gate, decreasing the electron-branch V_T and bringing the rising electron branch into the $V_{\text{Common-gate}}$ range relevant to the current peak. By contrast, the upper CNT network is deposited only after formation of the common gate and upper dielectric stack. Although the upper CNT network is formed on an $\text{HfO}_2/\text{SiO}_2$ dielectric stack, it is introduced only after completion of the elevated-temperature dielectric process. It therefore does not experience the HfO_2 ALD thermal history after CNT deposition and retains its p-type response, as independently observed in Fig. 1b. This contrast is consistent with the different processing and dielectric environments of the two CNT layers, although the present measurements do not separate the contributions of adsorbate removal, encapsulation and dielectric-associated charge. Because the common gate lies between the two vertically aligned channels, a single $V_{\text{Common-gate}}$ sweep simultaneously drives the lower channel into electron conduction while suppressing hole conduction in the upper channel. The lower electron-branch turn-on voltage favors overlap with upper-layer hole conduction within the common-gate operating range, supporting the formation of the current peak. Vertical stacking therefore converts fabrication chronology into layer-selective transfer characteristics within the same lateral footprint. This deliberately designed process-history asymmetry, rather than ALD-induced polarity conversion alone, allows the current-limiting role to shift between the series-connected channels and generates a local current peak that neither constituent transfer characteristic exhibits alone.

Tuning the NTC response through channel length and CNT network density

Because PVR represents the current contrast between I_{peak} and I_{valley} available for conductance matching in NTC-based ternary circuits [12, 13, 27], controlling the current levels of the constituent channels is required to tune the NTC response. As illustrated schematically in Fig. 3a, changing the current levels and branch positions of the lower and upper channels is expected to modify their conductance overlap and, consequently, PVR. Because channel length directly influences current magnitude, varying L_{ch} provides a straightforward geometric means of tuning the constituent-channel currents without requiring an additional bias or control terminal. We therefore independently measured

the lower- and upper-layer transistors within the completed vertically stacked devices while varying L_{ch} from 30 to 3 μm at $W_{\text{ch}} = 20 \mu\text{m}$ (Fig. 3b). The lower- and upper-layer CNT network densities were 5–7 and 11–13 tubes/ μm , respectively. The lower absolute current of the lower-layer transistor is expected to arise, at least in part, from its lower CNT network density, and the comparison therefore focuses on the systematic L_{ch} dependence within each layer rather than on the current difference between the two layers. As L_{ch} decreases, the current levels of both constituent channels increase. At the same time, the lower-layer electron branch shifts toward lower $V_{\text{Top-gate}}$, whereas the upper-layer p-type transition shifts toward higher $V_{\text{Bottom-gate}}$. These complementary changes extend the gate-voltage range over which lower-layer electron conduction and upper-layer hole conduction coexist, showing that L_{ch} provides direct geometric control over both the constituent-channel currents and their conductance overlap. The branch shifts were quantified using the constant-current method (CCM), with the extracted V_{T} values summarized in **Supplementary Fig. 5**. Because this comparison concerns the absolute branch-current levels relevant to current matching in the series-connected stack, the measured I_{D} was used without $W_{\text{ch}}/L_{\text{ch}}$ normalization. Between $L_{\text{ch}} = 30$ and 3 μm , the lower-layer V_{T} changes from 0.43 to -0.23 V , whereas the upper-layer V_{T} changes from -1.50 to -0.76 V . These length-dependent changes are consistent with the influence of network connectivity and CNT–CNT junctions on transport [48]. Because V_{T} is extracted at a fixed absolute current, its variation also includes the effect of changes in branch-current magnitude and should not be interpreted as an isolated measure of electrostatic gate control. The extracted values therefore describe the gate voltages required to sustain the selected branch-current levels. The complete vertically stacked devices, in which the lower- and upper-layer transistors characterized independently in Fig. 3b are connected in series and controlled by the common gate, were then measured to determine whether the constituent-channel changes translate into the NTC response (Fig. 3c). At $L_{\text{ch}} = 30$ and 20 μm , the transfer characteristics remain largely p-type-like, without a clearly distinguishable central current peak. A valley-to-peak rise first appears at $L_{\text{ch}} = 10 \mu\text{m}$ and becomes progressively more pronounced at 5, 4 and 3 μm , followed by a post-peak decrease at higher $V_{\text{Common-gate}}$. This progression shows that the L_{ch} -dependent current and branch-position changes observed in the constituent channels are translated into a tunable nonmonotonic response in the complete device. The corresponding g_{m} traces quantify the differential strength of this emerging NTC response. Because the plotted $-I_{\text{D}}$ represents $|I_{\text{D}}|$ at $V_{\text{D}} = -0.1 \text{ V}$, the increase in $-I_{\text{D}}$ from I_{valley} to I_{peak} corresponds to the signed I_{D} becoming more negative as $V_{\text{Common-gate}}$ increases, giving $g_{\text{m}} = \partial I_{\text{D}} / \partial V_{\text{Common-gate}} < 0$. No resolvable negative- g_{m} response is observed at $L_{\text{ch}} = 30$ and 20 μm . By contrast, a distinct negative- g_{m} response appears at $L_{\text{ch}} = 10 \mu\text{m}$, and its magnitude increases as L_{ch} is reduced further. The g_{m} analysis therefore provides a direct differential measure of how strongly channel-length scaling enhances the NTC response, complementing the current profile observed in the transfer characteristics.

Figure 3d quantifies the resulting valley-to-peak current contrast using PVR. For $L_{\text{ch}} = 30$ and 20 μm , no distinct valley–peak pair is resolved, and PVR is therefore assigned a value of 1 according to the

convention described in Methods. PVR increases to approximately 67 at $L_{\text{ch}} = 10 \mu\text{m}$, exceeds 100 at 5 and $4 \mu\text{m}$, and reaches approximately 770 at $3 \mu\text{m}$. The separate changes in I_{valley} and I_{peak} identify which current primarily governs this increase. Between $L_{\text{ch}} = 10$ and $3 \mu\text{m}$, I_{valley} increases from 3.90×10^{-14} to 8.14×10^{-14} A, corresponding to an approximately 2.1-fold change, whereas I_{peak} increases from 2.60×10^{-12} to 6.27×10^{-11} A, corresponding to an approximately 24-fold change (I_{valley} , I_{peak} and PVR were extracted as described in Methods). The valley region is consistent with lower-channel-limited transport, whereas the peak depends on the relative electron and hole conduction of both layers. The stronger increase in I_{peak} is consistent with the length-dependent changes in these constituent responses. Because the extracted I_{valley} values remain close to the measurement floor, their approximately twofold variation is not interpreted as a resolved change in intrinsic valley conduction. Under the extraction procedure described in Methods, the increase in the measured PVR is predominantly associated with the enhancement of I_{peak} . These results show that channel-length scaling provides direct geometric control over the NTC strength, current peak and PVR of the vertically stacked NTC transistor. Meanwhile, channel width provides another geometric parameter for adjusting the NTC response alongside L_{ch} scaling. Width-dependent modulation of the NTC response has previously been reported in a CNT-based mixed-dimensional ternary transistor [21]. **Supplementary Fig. 6** compares devices with $L_{\text{ch}} = 4 \mu\text{m}$ and $W_{\text{ch}} = 10, 20$ and $60 \mu\text{m}$, measured at $V_{\text{D}} = -0.1$ V. As W_{ch} increases, PVR increases in the same qualitative manner as observed when L_{ch} is reduced, consistent with the previously reported width dependence.

Layer-selective control of a single constituent response provides a second route to tune the NTC profile without simultaneously changing both channels. In the vertical fabrication sequence, the lower-layer transistor is completed and can be electrically characterized before deposition of the upper CNT network. This sequence makes the upper layer a practical later-stage parameter for adjusting the balance between the two constituent currents. Selective tuning of the lower channel could also modify the current balance, but upper-layer tuning was adopted here because it can be implemented after the lower-layer transistor has already been completed and characterized. The schematic in Fig. 4a therefore illustrates a layer-selective tuning strategy in which the lower-layer response is retained while the current level and p-type transition of the upper channel are adjusted. These changes are expected to modify the conductance overlap with the rising lower-layer electron branch and thereby control the current peak and PVR. CNT network density was used to control the upper-layer current while retaining the device geometry and lower-layer condition. CNT network density can be readily adjusted through fabrication parameters, making ρ_{CNT} a practical process variable for controlling channel current. W_{ch} and L_{ch} were fixed at 20 and $4 \mu\text{m}$, respectively, and the lower-layer ρ_{CNT} was maintained at 11–13 tubes/ μm . The upper-layer ρ_{CNT} was varied among low density (LD), medium density (MD) and high density (HD), corresponding to 5–7, 11–13 and 18–20 tubes/ μm , respectively. Atomic force microscopy (AFM) images of the three upper-layer CNT networks are provided in **Supplementary Fig. 7**.

In the independently measured transfer characteristics in Fig. 4b, the lower-layer response remains nearly unchanged because its ρ_{CNT} is fixed, whereas increasing upper-layer ρ_{CNT} raises the hole current and shifts the p-type transition toward higher $V_{\text{Bottom-gate}}$. A higher ρ_{CNT} increases the number of parallel percolation paths and therefore raises the upper-layer hole current at a given gate bias [49]. For the denser networks, a more positive $V_{\text{Bottom-gate}}$ is needed to suppress the larger hole current to the same CCM criterion, so the extracted V_T shift includes a contribution from the increased current magnitude. The upper-layer V_T extracted at $|I_D| = 10^{-9}$ A using CCM shifts from -1.00 V for LD to 0.29 V for HD, as summarized in **Supplementary Fig. 8**. These results show that upper-layer ρ_{CNT} provides layer-selective control over the upper-channel current level and branch position while retaining the lower-channel response.

These upper-layer changes produce a selective enhancement of the current peak in the vertically stacked NTC transistor (Fig. 4c). At $V_D = -0.1$ V, I_{valley} changes little as upper-layer ρ_{CNT} increases from LD to MD and HD, whereas I_{peak} increases markedly and shifts toward higher $V_{\text{Common-gate}}$. Around I_{valley} , the series current remains primarily limited by the fixed lower channel, so increasing upper-layer conduction has only a small effect. Around I_{peak} , however, the denser upper-layer network sustains hole conduction to a higher $V_{\text{Common-gate}}$ while the lower-layer electron current continues to increase. The upper channel therefore becomes the current-limiting layer at a higher gate voltage, allowing a larger current peak to develop before the post-peak decrease. Thus, the increase in the measured PVR is predominantly associated with the enhancement of I_{peak} . Because the extracted I_{valley} values remain close to the measurement floor, their small variation does not establish that the intrinsic valley current is unchanged. The corresponding g_m traces quantify the differential strength of the NTC response. The LD condition exhibits only a weak negative- g_m response. By contrast, MD and HD exhibit progressively larger negative- g_m magnitudes as upper-layer ρ_{CNT} increases. The g_m analysis therefore provides a direct differential measure of how strongly upper-layer density modifies the NTC response, complementing the valley-to-peak current evolution observed in the transfer characteristics. Consistent with this strengthening, the extracted PVR increases successively from LD to MD and HD, reaching approximately 1.6×10^4 for the representative HD device shown in Fig. 4c.

Additional measurements assess how this representative result relates to the device population. Thirty HD and thirty MD transfer records were analysed at each of two integration settings, 1 and 5 power-line cycles (PLC), using the same extraction procedure and $V_D = -0.1$ V. The median PVR values are 6.42×10^3 and 5.95×10^3 for HD, compared with 4.16×10^2 and 4.94×10^2 for MD, respectively (**Supplementary Fig. 9**). The representative value of approximately 1.6×10^4 therefore lies in the upper range rather than describing the typical population response. Open-contact and fixed-bias current–time measurements provide complementary low-current checks (**Supplementary Fig. 10**). At PLC = 1, the median operational pre-rise currents of 660 fA for HD and 260 fA for MD exceed the observed open-contact drain-current magnitude range of 0–55 fA. These comparisons support reproducible measured current contrast while distinguishing it from a fully calibrated intrinsic valley-current determination.

Because PVR quantifies the gate-controlled current contrast that can be exploited in ternary logic and other nonmonotonic device functions, it provides a basis for comparing the present response with previously reported NTC devices. Such a comparison must also account for $|V_D|$, since the reported PVR values were obtained under different drain-bias conditions. The benchmark in Fig. 4d therefore compares PVR together with $|V_D|$ [14–20, 34, 35], distinguishing single-semiconductor devices with red symbols from devices incorporating two semiconductor materials with blue symbols. The semiconductor materials, PVR values and drain-bias conditions are summarized in **Supplementary Table 1**. The HD result shows that a large current contrast between I_{peak} and the preceding I_{valley} can be achieved using a single semiconductor channel material without requiring a large drain bias.

The experimental results establish L_{ch} and upper-layer ρ_{CNT} as practical parameters for tuning the NTC profile. Beyond these structural and process parameters, different circuit requirements may call for more selective control. For example, the operating-voltage window may need to be shifted while preserving PVR, or the peak-to-valley current contrast may need to be adjusted without changing the CNT network density and its associated switching characteristics. We therefore used calibrated HSPICE Level 3 compact models to examine whether collective and layer-selective electrostatic parameters could provide these complementary tuning functions. The lower-layer electron and hole branches and the upper-layer p-type response were fitted separately using HSPICE Level 3 compact models, with the parameters summarized in **Supplementary Table 2**. Connecting the fitted constituent-channel models in series under a common gate produces a current valley followed by a local peak, consistent with the principal features of the measured response (**Supplementary Fig. 11a**). Common-gate work-function offsets were represented by coordinated shifts in the threshold-voltage parameters of the constituent models, while changes in upper-layer gate capacitance associated with the relative permittivity of the upper-layer gate dielectric, κ_{UL} , were approximated by varying the upper-layer current-strength parameter at fixed mobility. Within this parameterization, coordinated shifts in the model thresholds translate the operating-voltage window with little change in PVR, whereas increasing the upper-layer current strength raises I_{peak} and the simulated PVR (**Supplementary Figs. 11b and 11c**). These results identify complementary phenomenological tuning trends rather than full material-specific predictions for replacement gate metals or dielectrics.

Experimental ternary inverter operation

Pairing the vertically stacked NTC transistor with an n-type CNT FET converts the engineered nonmonotonic response into a ternary inverter with three output states (Fig. 5). To construct the inverter, we used the vertically stacked NTC transistor as the pull-up element because it conducts under a strongly negative gate-to-source bias and becomes suppressed as the gate bias shifts in the positive direction, giving a p-type-like terminal response. An electron-dominant top-gated CNT FET, fabricated using the same lower-layer top-gate process employed in the vertically stacked NTC transistor, was used as the pull-down element. Because only its electron branch is accessed over the inverter operating range, it functions as an n-type device in the circuit. Figure 5a shows the resulting circuit, in which the vertically

stacked NTC transistor connects the supply voltage V_{DD} to V_{out} and the n-type CNT FET connects V_{out} to ground (GND), with V_{out} defined as the voltage at the shared node between the pull-up and pull-down elements and both gates driven by input voltage V_{in} . The corresponding operating sequence is illustrated in Fig. 5b. At low V_{in} , the pull-down remains off while the pull-up is conductive, placing V_{out} near V_{DD} as logic '2'. At intermediate V_{in} , the two paths have comparable conductances, and the resulting voltage division produces logic '1' near $V_{DD}/2$. At high V_{in} , the pull-up enters its suppressed post-peak response while the pull-down remains conductive, driving V_{out} toward GND as logic '0' [12, 13]. The two conductance-matching boundaries between the pull-up and pull-down responses therefore define a finite V_{in} range for logic '1', giving the ternary mapping of input states '0', '1' and '2' to output states '2', '1' and '0', respectively.

The measured inverter realizes this operating sequence at $V_{DD} = 3$ V (Fig. 5c). The pull-up element is a vertically stacked NTC transistor with $W_{ch} = 20$ μm , $L_{ch} = 4$ μm and MD CNT networks in both layers, whereas the pull-down is an n-type CNT FET with $W_{ch} = 6$ μm , $L_{ch} = 20$ μm and an MD CNT network. The pull-down dimensions were selected to provide conductance matching with the nonmonotonic pull-up response over the intermediate V_{in} range. The voltage transfer characteristic (VTC) resolves output levels near V_{DD} , $V_{DD}/2$ and GND, separated by two distinct transitions. Overlaying the measured VTC with its mirrored curve forms the butterfly plot, and each static noise margin (SNM) is extracted from the diagonal length of the largest square inscribed in the corresponding region [50]. The two outer regions correspond to the complementary state pairs (2,0) and (0,2), whereas the two inner regions surround the intermediate state pair (1,1). Both outer-state margins, $\text{SNM}_{2' \leftrightarrow 0'}$, are 0.68 V, and both intermediate-state margins, $\text{SNM}_{1' \leftrightarrow 1'}$, are 0.66 V. The finite inner margins show that logic '1' occupies a nonzero static tolerance region near $V_{in} \approx V_{out} \approx V_{DD}/2$ rather than appearing only as a shoulder in the VTC. Together, the three resolved output levels and finite noise margins provide direct evidence that the measured inverter supports ternary logic operation with a statically distinct intermediate state.

The absolute voltage gain plotted alongside the VTC provides a differential measure of the two switching boundaries. Two separated gain peaks correspond to the logic '2' $\rightarrow$ '1' and logic '1' $\rightarrow$ '0' transitions, with $|dV_{out}/dV_{in}|$ exceeding 3 at both boundaries and reaching a maximum above 6. However, within part of the intermediate-state window corresponding to V_{out} near $V_{DD}/2$, the gain does not remain close to zero, indicating that V_{out} does not form a perfectly flat plateau. **Supplementary Fig. 12** provides a qualitative comparison of the independently measured pull-up and pull-down transfer characteristics. Their different gate-voltage dependences are consistent with a varying ratio of the effective branch conductances, which can produce a finite slope within the intermediate-state window. These fixed-drain-bias measurements are not a quantitative reconstruction of the inverter VTC, because the voltage across each device depends on V_{out} during circuit operation. Adjusting the pull-down V_T through gate-work-function engineering may help align its turn-on with the NTC window, although a flatter intermediate level also requires the effective pull-up/pull-down conductance ratio to remain nearly constant across that window. Nevertheless, the finite inner SNM shows that the present inverter already supports a statically

resolved intermediate state. Finally, the time-domain measurement in Fig. 5d tests whether the three output states are reproduced under repeated input operation. As V_{in} is cycled through the voltage levels assigned to logic '0', '1' and '2', V_{out} repeatedly returns to logic '2', '1' and '0', respectively, over four cycles. The finite static margins, separated gain peaks and repeatable time-domain response therefore show that the engineered NTC profile is translated into ternary inverter operation through a finite conductance-matching window.

The vertical arrangement also provides a layout-level integration benefit for this inverter architecture. Using the fabricated inverter as the vertical reference and a hypothetical lateral counterpart with the same constituent-channel dimensions and separate pull-down, the assessed cell footprints are 1.08 and 1.44 mm², respectively, corresponding to a 25% reduction under the matched contact and spacing conventions (**Supplementary Fig. 13**). Four- and eight-stage repeated-cell estimates retain this reduction before additional routing-space allowances. These are layout-derived comparisons rather than measurements of newly fabricated multistage circuits. Behavioural chains based on the measured single-inverter VTC illustrate nominal three-level propagation under the model (**Supplementary Fig. 14**). The footprint comparison thus identifies an integration benefit accompanying the process-defined transfer-function engineering, while preserving the distinction between measured circuit operation and projected multistage implementations.

Discussion

This work shows how monolithic vertical integration can shape a transistor transfer characteristic rather than merely determine the placement of its constituent channels. Near-room-temperature deposition enables sequential integration of CNT networks, while their different processing and dielectric environments provide contrasting transport responses within the same semiconductor. The lower channel exhibits electron-dominant ambipolar transport under top-gate operation after HfO₂ processing, whereas the subsequently deposited upper channel remains p-type. A common gate and an internal series interconnect combine these responses in the vertically stacked NTC transistor, producing a local current peak absent from either constituent transfer characteristic.

Channel geometry and upper-layer CNT network density provide complementary design parameters for adjusting the constituent responses and the resulting NTC profile. Additional measurements under the high-density upper-layer condition give a median extracted PVR near 6×10^3 at $|V_D| = 0.1$ V, with upper-range values above 10^4 . The inverter measurements establish the circuit significance of this control: at $V_{DD} = 3$ V, appropriately balancing the nonmonotonic pull-up response with an n-type CNT pull-down produces three output states and finite static noise margins. Across fabricated variants, however, a larger PVR does not ensure more balanced logic-state margins. Intermediate-state formation and noise tolerance also depend on the shape and alignment of the pull-up response relative to the pull-down. The resulting design principle is therefore to engineer the complete transfer characteristic for the intended

circuit, rather than maximize current contrast alone. This single-semiconductor, common-gate architecture connects sequential vertical integration with transfer-function engineering for ternary logic.

The layout comparison further links this functional integration to a reduction in inverter footprint under the stated design conventions. The 25% estimate is not an architectural scaling limit. Near-room-temperature CNT deposition, together with established examples of monolithic CNT integration [51, 52], motivates further exploration of compact contacts and interconnects and additional CNT tiers. Such extensions could reduce the cell area further, provided that the process-defined transport contrast and reliable electrical connections are preserved. Their benefits are prospective and are not included in the present footprint estimate.

Methods

Device fabrication

Highly doped p-type Si wafers with 50 nm SiO₂ formed by wet oxidation were used as substrates. The wafer surface was treated with O₂ plasma at 30 W for 60 s, followed by the application of a 0.1% aqueous poly-L-lysine solution for 20 min. A semiconducting CNT dispersion (IsoNanotubes-S, NanoIntegris, 99.9% semiconducting purity) was then dispensed onto the substrate maintained at 30°C. CNT deposition times of 3, 7, and 11 min were used for the low-, medium-, and high-density conditions, respectively. The samples were subsequently rinsed with isopropyl alcohol and deionized water for 1 min each. All patterns were defined by i-line photolithography. Ti/Pd electrodes with thicknesses of 2 and 20 nm, respectively, were deposited by electron beam evaporation at a base pressure of approximately 1.0×10^{-6} Torr. The CNT channels were patterned using O₂ plasma at 3 W for 60 s. A 30 nm HfO₂ gate dielectric was deposited at 250°C by ALD using TEMAH and H₂O. Each cycle consisted of a 0.5 s TEMAH pulse, a 15 s purge, a 0.5 s H₂O pulse, and a second 15 s purge. A total of 280 cycles was used. After formation of the Ti/Pd common gate, an additional 30 nm HfO₂ layer was deposited under the same conditions. A 5 nm SiO₂ layer was then deposited by electron beam evaporation at approximately 1.0×10^{-6} Torr to facilitate adsorption of the upper CNT network. The via opening was formed by reactive ion etching at 150 W for 4 min using SF₆, CHF₃, and Ar flow rates of 20, 30, and 4 sccm, respectively. The upper-layer CNT network was formed using the same surface treatment and deposition procedure as the lower-layer CNT network, followed by formation of the upper-layer Ti/Pd electrodes and O₂ plasma channel patterning. For the CNT density split, only the deposition time of the upper-layer CNT network was varied, while all lower-layer fabrication conditions were maintained.

Electrical measurements

The electrical characteristics of the individual CNT transistors, vertically stacked NTC transistors and inverter circuits were measured using a Keysight B1500A semiconductor device analyzer at room temperature in ambient air. For the additional reproducibility analysis, 30 HD and 30 MD device records were acquired at each integration setting of 1 and 5 power-line cycles (PLC). The common-gate voltage

was swept from -3 to $+3$ V in 50 mV steps at $V_D = -0.1$ V and $V_S = 0$ V, with a 3 s hold before the sweep. Signed drain, source and gate currents were retained. Open-contact measurements were performed at PLC = 1 with all probe contacts disconnected and the same programmed voltage sweep. Fixed-bias current–time measurements were recorded for approximately 120 s at $V_D = -0.1$ V, using $V_{\text{Common-gate}} = 0$ V and -1.3 V for HD and -0.65 V and -1.3 V for MD. Descriptive time-domain statistics were calculated from signed currents over 60–120 s. The reported temporal standard deviations describe within-trace fluctuations, and no background subtraction was applied.

PVR extraction

The peak-to-valley current ratio (PVR) was evaluated from the drain-current magnitude, $|I_D|$, in the common-gate transfer characteristics of the vertically stacked devices. The NTC interval was identified by $g_m = \partial I_D / \partial V_{\text{Common-gate}} < 0$ using the signed drain current I_D . For curves exhibiting a resolvable NTC response, an operational I_{valley} was extracted from a curve-relative pre-rise window to reduce sensitivity to isolated low-current fluctuations, including those near the measurement floor in the original transfer measurements. For each transfer curve, a five-point moving average of $\log_{10}|I_D|$ was used only to identify the onset of the sustained current increase toward the central peak. The onset was defined as the first point, in the sweep direction toward the peak, from which the smoothed current increased monotonically over the subsequent three $V_{\text{Common-gate}}$ steps, with a cumulative increase of at least 0.3 decades. I_{valley} was then calculated as the arithmetic mean of five consecutive raw $|I_D|$ values ending at the identified onset. I_{peak} was determined as the median of three consecutive raw $|I_D|$ values centered on the subsequent local maximum, and PVR was calculated as $I_{\text{peak}}/I_{\text{valley}}$. Isolated single-point fluctuations near the measurement floor were not accepted as the onset or peak. For curves exhibiting neither a resolvable NTC interval nor a distinct central current peak, no valley–peak pair was defined. In such cases, PVR was assigned a value of 1 by convention to denote the absence of a resolved NTC response. This assigned value does not represent a ratio calculated from an extracted current pair. The same extraction criteria were applied to all device conditions. In the additional HD and MD datasets, the five-point moving average was centred, and the central peak was identified within $-1.1 \leq V_{\text{Common-gate}} \leq 0.8$ V using the same search range for all records. Population statistics were calculated separately for each density and PLC setting; records from different settings were not pooled as additional independent devices.

Structural and material characterization

The device structures and CNT network morphologies were characterized by field-emission scanning electron microscopy using an SU8700 system (Hitachi) and atomic force microscopy using an NX10 system (Park Systems). Cross-sectional transmission electron microscopy and high-angle annular dark-field scanning transmission electron microscopy images were obtained using a JEM-ARM200F system (JEOL) equipped with a Schottky thermal field-emission gun and a spherical-aberration corrector. Raman spectra were acquired using a DXR3xi Raman imaging microscope (Thermo Fisher Scientific). CNT

network density was estimated by manually counting individually distinguishable CNT strands in the AFM images and normalizing the count to the corresponding lateral length.

Compact-model simulation

The measured transfer characteristics were fitted using HSPICE Level 3 compact models. The p-type response of the upper-layer transistor and the electron and hole branches of the lower-layer transistor were parameterized separately. The two lower-layer branch models were combined to reproduce the measured ambipolar characteristic, and the resulting lower-layer model was connected in series with the upper-layer model to reproduce the NTC transistor response. The model parameters are listed in Supplementary Table 2. DC simulations were performed using the same gate-voltage range and drain bias as the measurements. The calibrated model was subsequently used for parametric analyses of the common gate work-function offset and the relative permittivity of the upper-layer gate dielectric. These simulations were used as phenomenological compact-model analyses of the measured transfer characteristics rather than as microscopic transport calculations.

Layout-based footprint analysis

Inverter footprints were calculated from the documented vertical-inverter layout and a hypothetical lateral reference using the same channel dimensions, contact convention and spacing assumptions. Four- and eight-stage footprints were estimated by repeating the unit cells with a 50 μm inter-cell gap. Additional in-plane routing-height allowances were treated as explicit sensitivity scenarios rather than extracted interconnect dimensions. The layout assumptions and calculation procedure are provided in **Supplementary Fig. 13** and **Supplementary Table 5**.

Behavioural inverter-chain simulation

Four- and eight-stage feed-forward chains were simulated in HSPICE using identical behavioural inverter stages based on the measured VTC at $V_{\text{DD}} = 3\text{ V}$. A first-order RC response with a time constant of approximately 0.06 s was imposed to represent transient settling. The simulations describe nominal level propagation and are distinct from the constituent-transistor Level 3 analysis and from parasitic-extracted circuit simulation. Further details are provided in **Supplementary Fig. 14**.

Declarations

Data availability

The authors declare that the data supporting the findings of this study are available within the article and its Supplementary Information files. All other relevant data are available from the corresponding author upon request.

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S.J. and S.-J.C. conceived the project and led all aspects of the study. S.J. fabricated the devices, performed the electrical measurements, analyzed the data, and drafted the manuscript. J.Y.I. contributed to device fabrication and structural characterization. H.L. and J.W.P. contributed to electrical measurements. Y.K. and M.C. contributed to the HSPICE simulations. D.H.K., Y.J.L., and J.L. contributed to the interpretation and discussion of the results. M.-H.K. co-supervised the study and contributed to the interpretation of the results and revision of the manuscript. S.-J.C. supervised and coordinated the project and revised the manuscript. All authors reviewed and approved the final manuscript.

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Competing interests

The authors declare no competing interests.

References

1. Radosavljevic M et al (2023) IEEE,. Demonstration of a stacked CMOS inverter at 60 nm gate pitch with power via and direct backside device contacts. In *Proc. 2023 IEEE Int. Electron Devices Meeting (IEDM)* 1–4
2. Luo X et al (2026) Monolithic integration of carbon nanotube-based complementary field-effect transistors with 3D-stacked photodiodes for unified sensing and computing. *ACS Nano* 20:18406–18418

3. Liao S et al (2023) IEEE,. Complementary field-effect transistor (CFET) demonstration at 48 nm gate pitch for future logic technology scaling. In *Proc. 2023 IEEE Int. Electron Devices Meeting (IEDM)* 1–4
4. Demuynck S et al (2024) IEEE,. Monolithic complementary field-effect transistors (CFETs) demonstrated using middle dielectric isolation and stacked contacts. In *Proc. 2024 IEEE Symp. VLSI Technol. Circuits* 1–2
5. Pendurthi R et al (2024) Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors. *Nat Nanotechnol* 19:970–977
6. Liao S et al (2024) IEEE,. First demonstration of monolithic CFET inverter at 48 nm gate pitch toward future logic technology scaling. In *Proc. 2024 IEEE Int. Electron Devices Meeting (IEDM)* 1–4
7. Lim H et al (2025) Heterogeneous 3-D sequential CFET with strain-engineered Ge (100) top-channel pMOSFET on bulk Si (100) nMOSFET. *IEEE Trans Electron Devices* 72:3422–3428
8. Liu M et al (2023) Large-scale ultrathin channel nanosheet-stacked CFET based on CVD 1L MoS₂/WSe₂. *Adv Electron Mater* 9:2200722
9. Jung SG, Jang D, Min SJ, Park E, Yu HY (2022) Device design guidelines of 3-nm node complementary FET (CFET) in perspective of electrothermal characteristics. *IEEE Access* 10:41112–41118
10. Mertens H et al (2023) IEEE,. Nanosheet-based complementary field-effect transistors (CFETs) at 48 nm gate pitch, and middle dielectric isolation to enable CFET inner spacer formation and multi-V_t patterning. In *Proc. 2023 IEEE Symp. VLSI Technol. Circuits* 1–2
11. Andreev M, Seo S, Jung K-S, Park J-H (2022) Looking beyond 0 and 1: principles and technology of multi-valued logic devices. *Adv Mater* 34:2108830
12. Yoo H, On S, Lee SB, Cho K, Kim JJ (2019) Negative transconductance heterojunction organic transistors and their application to full-swing ternary circuits. *Adv Mater* 31:1808265
13. Lee C et al (2021) Systematic control of negative transconductance in organic heterojunction transistor for high-performance, low-power flexible ternary logic circuits. *Small* 17:2103365
14. Lee Y et al (2022) Demonstration of anti-ambipolar switch and its applications for extremely low power ternary logic circuits. *ACS Nano* 16:10994–11003
15. Jung C et al (2025) Scalable ternary logic device based on TeO_x/IGTO heterojunction transistor. *Adv Funct Mater* 35:2501834
16. Kim JY et al (2020) Distinctive field-effect transistors and ternary inverters using cross-type WSe₂/MoS₂ heterojunctions treated with polymer acid. *ACS Appl Mater Interfaces* 12:36530–36539
17. Kim S, Jeon Y, Cho HR, Kim CH, Yoo H (2024) Organic ternary logic inverter using negative transconductance pull-down switching transistor. *IEEE Electron Device Lett* 45:590–592
18. Shin JC et al (2024) Oxide semiconductor heterojunction transistor with negative differential transconductance for multivalued logic circuits. *ACS Nano* 18:1543–1554
19. Duong NT et al (2019) Modulating the functions of MoS₂/MoTe₂ van der Waals heterostructure via thickness variation. *ACS Nano* 13:4478–4485

20. Long Y et al (2026) Composition-modulated anti-ambipolar behavior enabled by two-dimensional $\text{GeS}_x\text{Se}_{1-x}/\text{SnS}_2$ van der Waals heterostructures for high-performance logic inverters. *Nanoscale Horiz* 11:572–584
21. Lee HY et al (2025) Mixed-dimensional semiconductors-based ternary circuits with tunable negative transconductance characteristics. *ACS Appl Mater Interfaces* 17:6774–6782
22. Panigrahi D, Hayakawa R, Wakayama Y (2023) Antiambipolar transistor with double negative differential transconductances for organic quaternary logic circuits. *Adv Funct Mater* 33:2213899
23. Seo S et al (2021) Controllable potential barrier for multiple negative-differential-transconductance and its application to multi-valued logic computing. *npj 2D Mater Appl* 5:32
24. Zhao G et al (2025) A universal implementation approach for multivalued logic gates based on negative transconductance in series-connected two-dimensional transistors. *ACS Nano* 19:24961–24971
25. Panigrahi D, Hayakawa R, Wakayama Y (2022) High-performance multivalued logic circuits based on optically tunable antiambipolar transistors. *J Mater Chem C* 10:5559–5566
26. Shin JC et al (2025) Photonic modulation of negative differential transconductance for tunable multivalued logic in heterojunction transistors. *Small* 21:2501543
27. Lee C et al (2023) A reconfigurable binary/ternary logic conversion-in-memory based on drain-aligned floating-gate heterojunction transistors. *Nat Commun* 14:3757
28. Lee C et al (2026) A light-driven multi-state heterojunction transistor for optoelectronic ternary logic circuits. *Nat Commun* 17:7736
29. Li Z et al (2023) 2D van der Waals vertical heterojunction transistors for ternary neural networks. *Nano Lett* 23:11710–11718
30. Park S et al (2022) Quaternary NAND logic and complementary ternary inverter with p-MoTe₂/n-MoS₂ heterostack channel transistors. *Adv Funct Mater* 32:2108737
31. Choi J et al (2022) Vertically stacked, low-voltage organic ternary logic circuits including nonvolatile floating-gate memory transistors. *Nat Commun* 13:2305
32. Lee C et al (2026) Electrically binary and ternary convertible CMOS inverter and logic gate using complementary field-effect transistors based on vertically stacked MoS₂/WSe₂ n-/p-field-effect transistors. *Adv Funct Mater* 36:e10164
33. Kwon YA et al (2025) Reconfigurable binary and ternary logic devices enabling logic state modulation. *Nat Commun* 16:6740
34. Zhu X et al (2025) High-performance ternary logic circuits and neural networks based on carbon nanotube source-gating transistors. *Sci Adv* 11:eadt1909
35. Zhang Z et al (2025) Near-perfect standard ternary inverter based on MoTe₂ homojunction anti-ambipolar transistor. *Adv Funct Mater* 35:2424728
36. Kim B, Geier ML, Hersam MC, Dodabalapur A (2017) Inkjet printed circuits based on ambipolar and p-type carbon nanotube thin-film transistors. *Sci Rep* 7:39627

37. Wang C, Ryu K, Badmaev A, Zhang J, Zhou C (2011) Metal contact engineering and registration-free fabrication of complementary metal-oxide semiconductor integrated circuits using aligned carbon nanotubes. *ACS Nano* 5:1147–1153
38. Chen Z, Appenzeller J, Knoch J, Lin YM, Avouris P (2005) The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. *Nano Lett* 5:1497–1502
39. Cui X, Freitag M, Martel R, Brus L, Avouris P (2003) Controlling energy-level alignments at carbon nanotube/Au contacts. *Nano Lett* 3:783–787
40. Heinze S et al (2002) Carbon nanotubes as Schottky barrier transistors. *Phys Rev Lett* 89:106801
41. Ha TJ et al (2015) Highly uniform and stable n-type carbon nanotube transistors by using positively charged silicon nitride thin films. *Nano Lett* 15:392–397
42. Lau C, Srimani T, Bishop MD, Hills G, Shulaker MM (2018) Tunable n-type doping of carbon nanotubes through engineered atomic layer deposition HfO_x films. *ACS Nano* 12:10924–10931
43. Moriyama N, Ohno Y, Kitamura T, Kishimoto S, Mizutani T (2010) Change in carrier type in high-k gate carbon nanotube field-effect transistors by interface fixed charges. *Nanotechnology* 21:165201
44. Zhang J, Wang C, Fu Y, Che Y, Zhou C (2011) Air-stable conversion of separated carbon nanotube thin-film transistors from p-type to n-type using atomic layer deposition of high-k oxide and its application in CMOS logic circuits. *ACS Nano* 5:3284–3292
45. Jorio A et al (2001) Structural (n,m) determination of isolated single-wall carbon nanotubes by resonant Raman scattering. *Phys Rev Lett* 86:1118–1121
46. Tseng Y-C, Phoa K, Carlton D, Bokor J (2006) Effect of diameter variation in a large set of carbon nanotube transistors. *Nano Lett* 6:1364–1368
47. An Y et al (2024) Gate capacitance coupling of double-gate carbon nanotube network transistors. *ACS Appl Mater Interfaces* 16:6221–6227
48. Liu H-Y et al (2025) Long-channel effects in randomly oriented carbon nanotube thin film transistors. *Adv Electron Mater* 11:2400660
49. Yang HI et al (2024) Simulation of a randomly percolated CNT network for an improved analog physical unclonable function. *Sci Rep* 14:8811
50. Lee L et al (2019) ZnO composite nanolayer with mobility edge quantization for multi-value logic transistors. *Nat Commun* 10:1998
51. Shulaker MM et al (2017) Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. *Nature* 547:74–78
52. Liu Y, Wang S, Liu H, Peng L-M (2017) Carbon nanotube-based three-dimensional monolithic optoelectronic integrated system. *Nat Commun* 8:15649

Figures

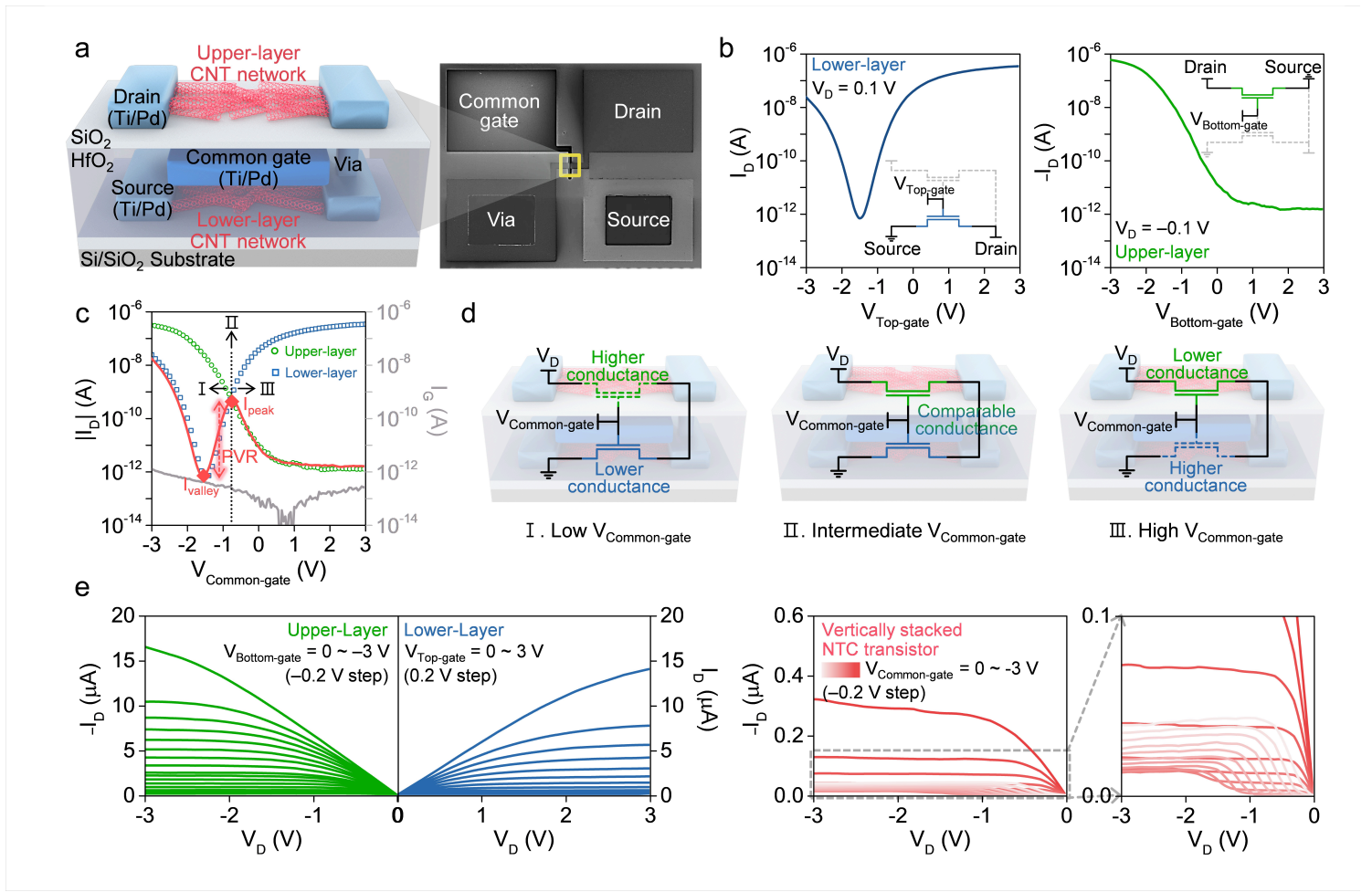


Figure 1

Monolithic vertical device architecture and emergence of stack-generated negative transconductance.

a Schematic of the vertically stacked NTC transistor, in which the lower- and upper-layer CNT network channels are positioned on opposite sides of a common gate and connected in series through an interlayer via. The top-view scanning electron microscopy (SEM) image shows the lateral registration of the common gate, drain, source and interlayer via. The yellow box indicates the channel region. **b** Transfer characteristics of the isolated lower- and upper-layer transistors measured by sweeping $V_{\text{Top-gate}}$ at $V_D = +0.1$ V and $V_{\text{Bottom-gate}}$ at $V_D = -0.1$ V, respectively. The inset schematics show the selective measurement configurations for the lower- and upper-layer transistors within the vertically stacked device. **c** Transfer characteristics plotted as drain-current magnitudes $|I_D|$ for the isolated upper- and lower-layer transistors and the vertically stacked NTC transistor, showing I_{valley} , I_{peak} , the valley-to-peak interval and PVR. The lower-layer transistor was measured at $V_D = +0.1$ V, whereas the upper-layer transistor and the vertically stacked NTC transistor were measured at $V_D = -0.1$ V. The grey curve represents the gate leakage current. **d** Schematics of the relative conductance states of the upper and lower channels in Regions I–III during a common-gate sweep. **e** Output characteristics of the upper-layer transistor for $V_{\text{Bottom-gate}} = 0$ to -3 V in -0.2 V steps, the lower-layer transistor for $V_{\text{Top-gate}} = 0$ to 3 V in

0.2 V steps and the vertically stacked NTC transistor for $V_{\text{Common-gate}} = 0$ to -3 V in -0.2 V steps. A magnified view of the low-current region is also included for the vertically stacked NTC transistor.

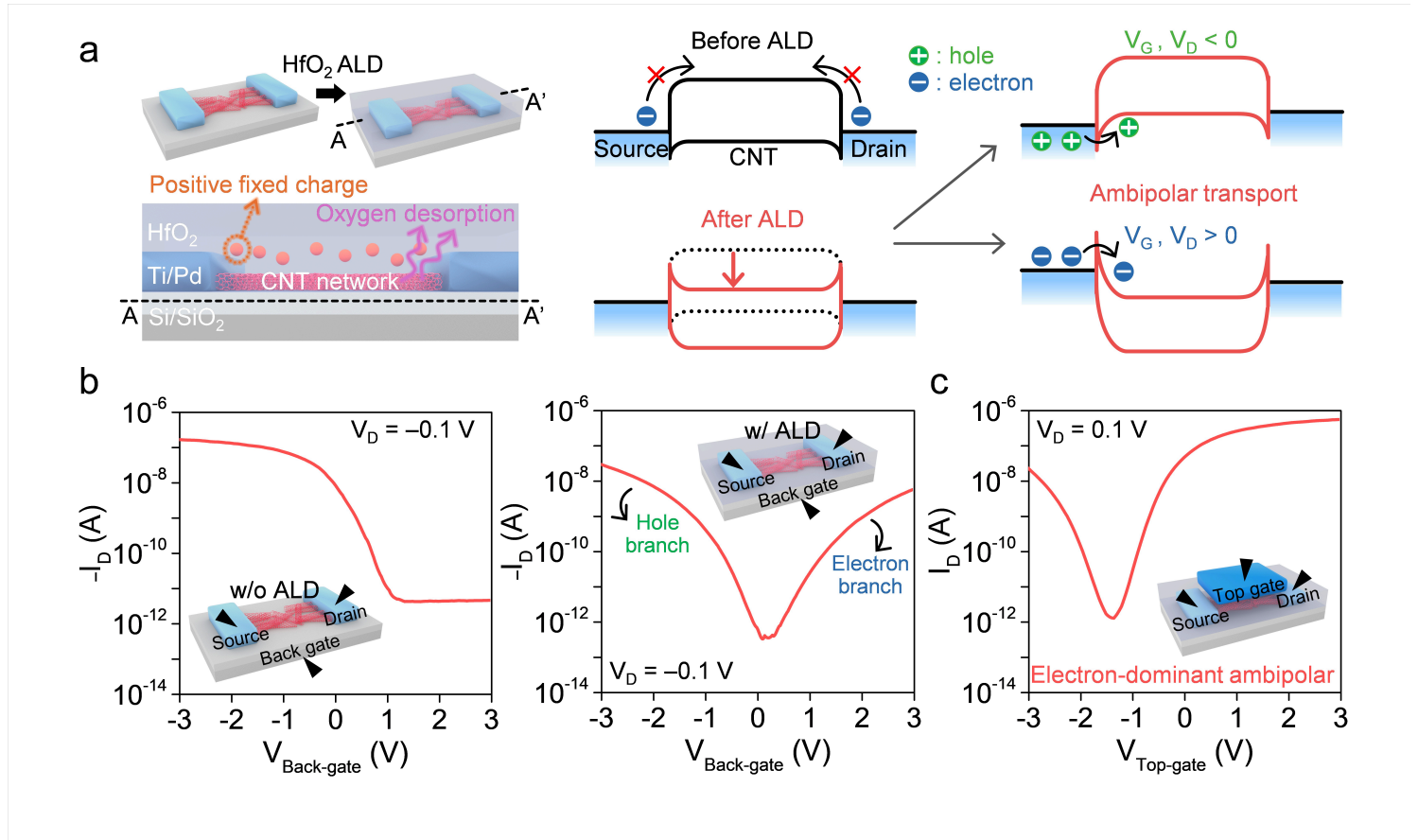


Figure 2

HfO₂-induced layer-selective polarity control in the lower-layer transistor.

a Schematics of the lower-layer CNT network transistor in the back-gate configuration before and after HfO₂ atomic layer deposition (ALD). The A–A' cross-sectional view illustrates proposed contributions from oxygen desorption during the ALD thermal cycle and dielectric-associated positive charge to the transport evolution of the Ti/Pd-contacted CNT network on Si/SiO₂. The lateral energy-band diagrams along the source–CNT–drain direction before and after ALD illustrate bias-selective carrier injection after HfO₂ processing. Negative gate and drain biases favour hole injection, whereas positive gate and drain biases favour electron injection, giving rise to ambipolar transport. **b** Transfer characteristics of the lower-layer transistor before and after HfO₂ ALD, measured through the Si/SiO₂ back gate at $V_D = -0.1$ V. The w/o ALD state exhibits a monotonic p-type response, whereas the w/ ALD state exhibits ambipolar transport with hole and electron branches at negative and positive $V_{\text{Back-gate}}$, respectively. The inset schematics indicate the corresponding fabrication stages and probing configurations. **c** Top-gate transfer characteristic of the lower-layer transistor after formation of the top gate, measured by sweeping $V_{\text{Top-gate}}$ at $V_D = +0.1$ V.

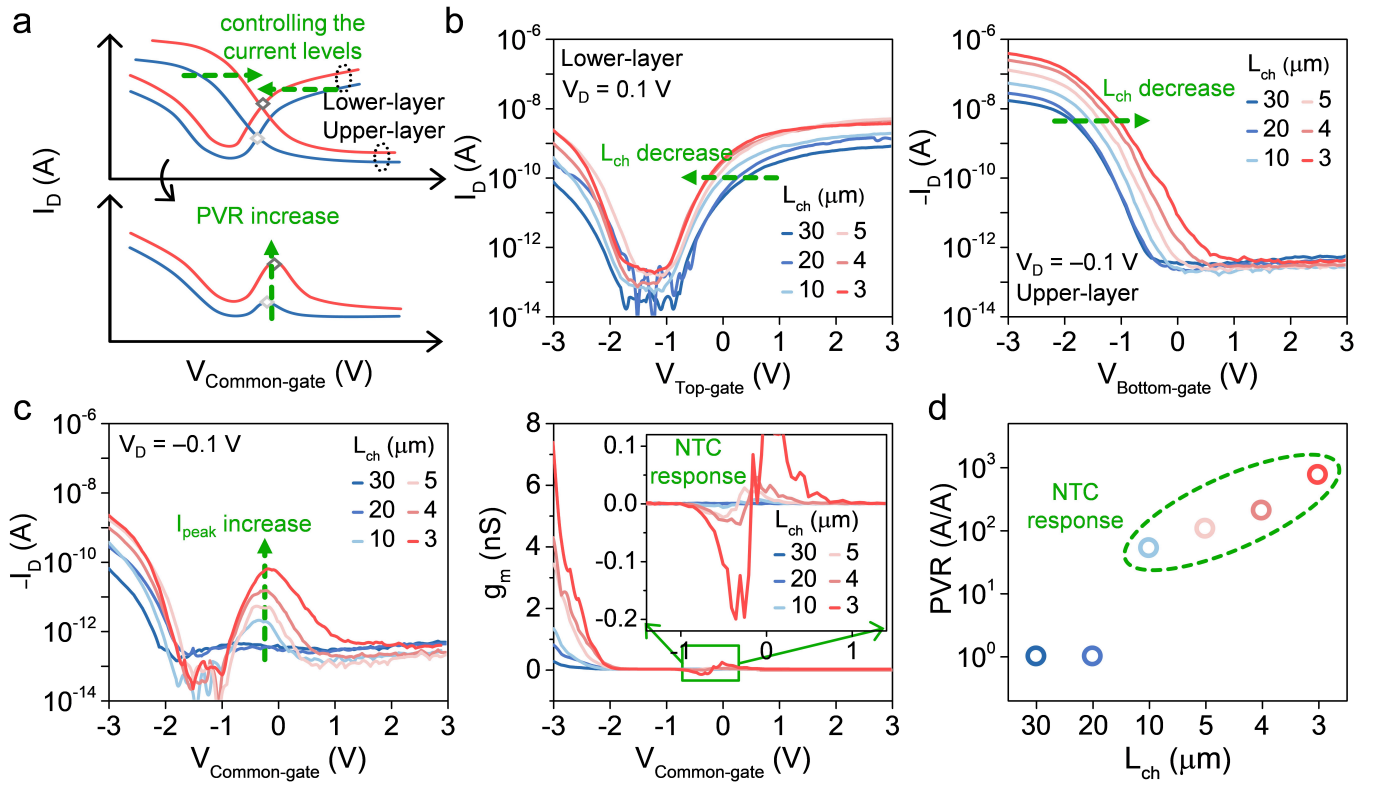


Figure 3

Channel-length-dependent control of the NTC response in the vertically stacked NTC transistor.

a Schematic illustration of controlling the current levels and transfer-characteristic alignment of the constituent channels (top) and the resulting modulation of the current peak and PVR in the vertically stacked NTC transistor (bottom). **b** Transfer characteristics of the independently measured lower-layer transistor (left), obtained by sweeping $V_{\text{Top-gate}}$ at $V_D = +0.1$ V, and upper-layer transistor (right), obtained by sweeping $V_{\text{Bottom-gate}}$ at $V_D = -0.1$ V, for $L_{\text{ch}} = 30, 20, 10, 5, 4$ and 3 μm. As L_{ch} decreases, the lower-layer electron branch shifts toward lower $V_{\text{Top-gate}}$, whereas the upper-layer p-type transition shifts toward higher $V_{\text{Bottom-gate}}$. **c** Transfer characteristics of the complete vertically stacked NTC transistor measured by sweeping $V_{\text{Common-gate}}$ at $V_D = -0.1$ V for the same L_{ch} values (left), showing the progressive emergence and enhancement of the valley-to-peak response as L_{ch} decreases. Corresponding transconductance, $g_m = \partial I_D / \partial V_{\text{Common-gate}}$ (right). The inset magnifies the region in which g_m becomes negative. **d** PVR values extracted for $L_{\text{ch}} = 30, 20, 10, 5, 4$ and 3 μm.

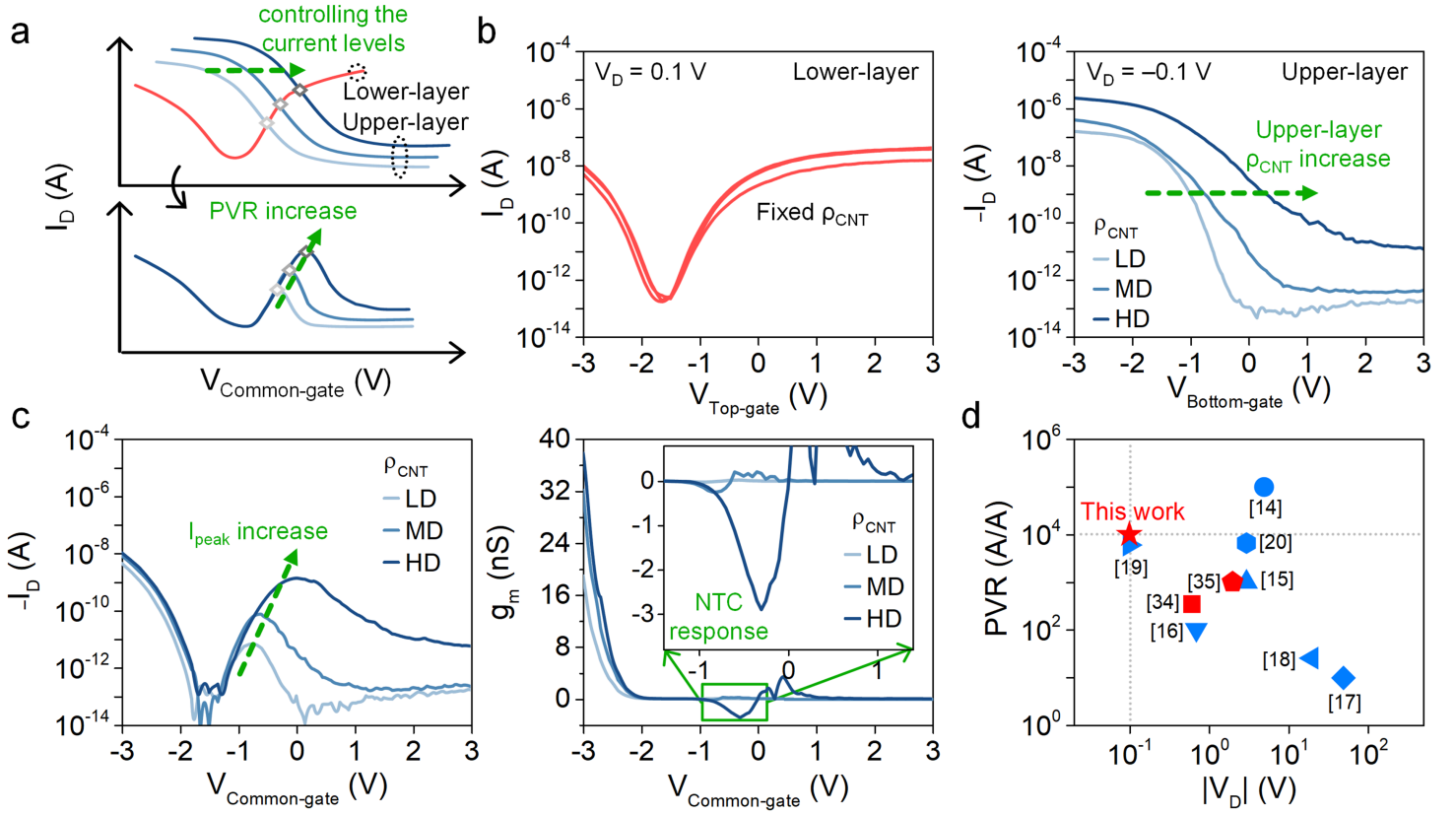


Figure 4

Layer-specific tuning of the NTC response using upper-layer CNT network density.

a Schematic illustration of layer-selective control of the constituent-channel current levels and transfer-characteristic alignment (top), and the resulting modulation of the current peak and PVR in the vertically stacked NTC transistor (bottom). **b** Transfer characteristics of the independently measured lower-layer transistor with fixed $\rho_{\text{CNT}} = 11\text{--}13$ tubes/ μm , obtained by sweeping $V_{\text{Top-gate}}$ at $V_D = +0.1$ V (left), and upper-layer transistors with different ρ_{CNT} , obtained by sweeping $V_{\text{Bottom-gate}}$ at $V_D = -0.1$ V (right). Low-density (LD), medium-density (MD) and high-density (HD) conditions correspond to upper-layer CNT network densities of 5–7, 11–13 and 18–20 tubes/ μm , respectively. Increasing upper-layer ρ_{CNT} raises the hole current and shifts the p-type transition toward higher $V_{\text{Bottom-gate}}$, while the lower-layer response remains nearly unchanged. **c** Transfer characteristics of the complete vertically stacked NTC transistor measured by sweeping $V_{\text{Common-gate}}$ at $V_D = -0.1$ V for the LD, MD and HD upper-layer conditions (left). Increasing upper-layer ρ_{CNT} selectively increases I_{peak} and shifts it toward higher $V_{\text{Common-gate}}$ with little change in I_{valley} . Corresponding transconductance, $g_m = \partial I_D / \partial V_{\text{Common-gate}}$ (right). The inset magnifies the region in which g_m becomes negative. **d** Benchmark of PVR and $|V_D|$ for this work and previously reported NTC devices. The red symbols denote single-semiconductor devices, whereas the blue symbols denote devices incorporating two semiconductor materials. The red star denotes the original representative HD-device result rather than a population average. Additional device statistics and low-current controls are provided in **Supplementary Figs. 9 and 10**.

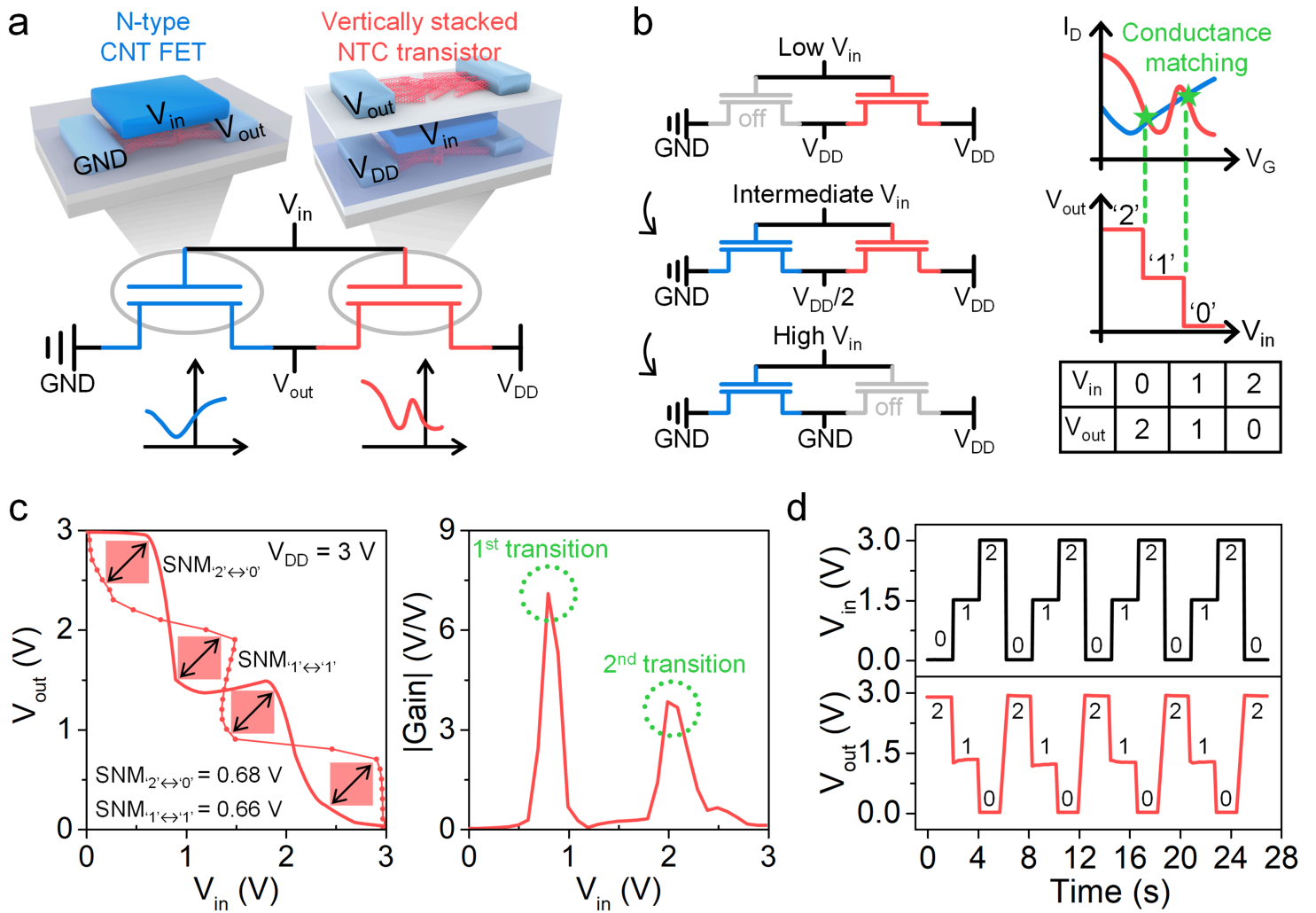


Figure 5

Experimental ternary inverter operation using the vertically stacked NTC transistor.

a Schematic of the ternary inverter, in which the vertically stacked NTC transistor is used as the pull-up element and an n-type CNT FET serves as the pull-down. Both gates are connected to V_{in} , and the shared node defines V_{out} . **b** Operating states at low, intermediate and high V_{in} . The right panels illustrate the two conductance-matching boundaries formed between the pull-up and pull-down paths, the resulting three output states and the ternary inverter truth table. **c** Voltage transfer characteristic (VTC) measured at $V_{DD} = 3$ V and the corresponding butterfly plot (left). The solid and dotted curves denote the measured and mirrored VTCs, respectively, and the inscribed squares indicate static noise margins, $SNM_{2' \leftrightarrow 0'}$ and $SNM_{1' \leftrightarrow 1'}$. Corresponding absolute voltage gain, $|dV_{out}/dV_{in}|$, showing two voltage-gain peaks associated with the logic $2' \rightarrow 1'$ and logic $1' \rightarrow 0'$ transitions (right). **d** Time-domain response under repeated input levels corresponding to logic '0', '1' and '2', showing the inverted output states '2', '1' and '0', respectively.

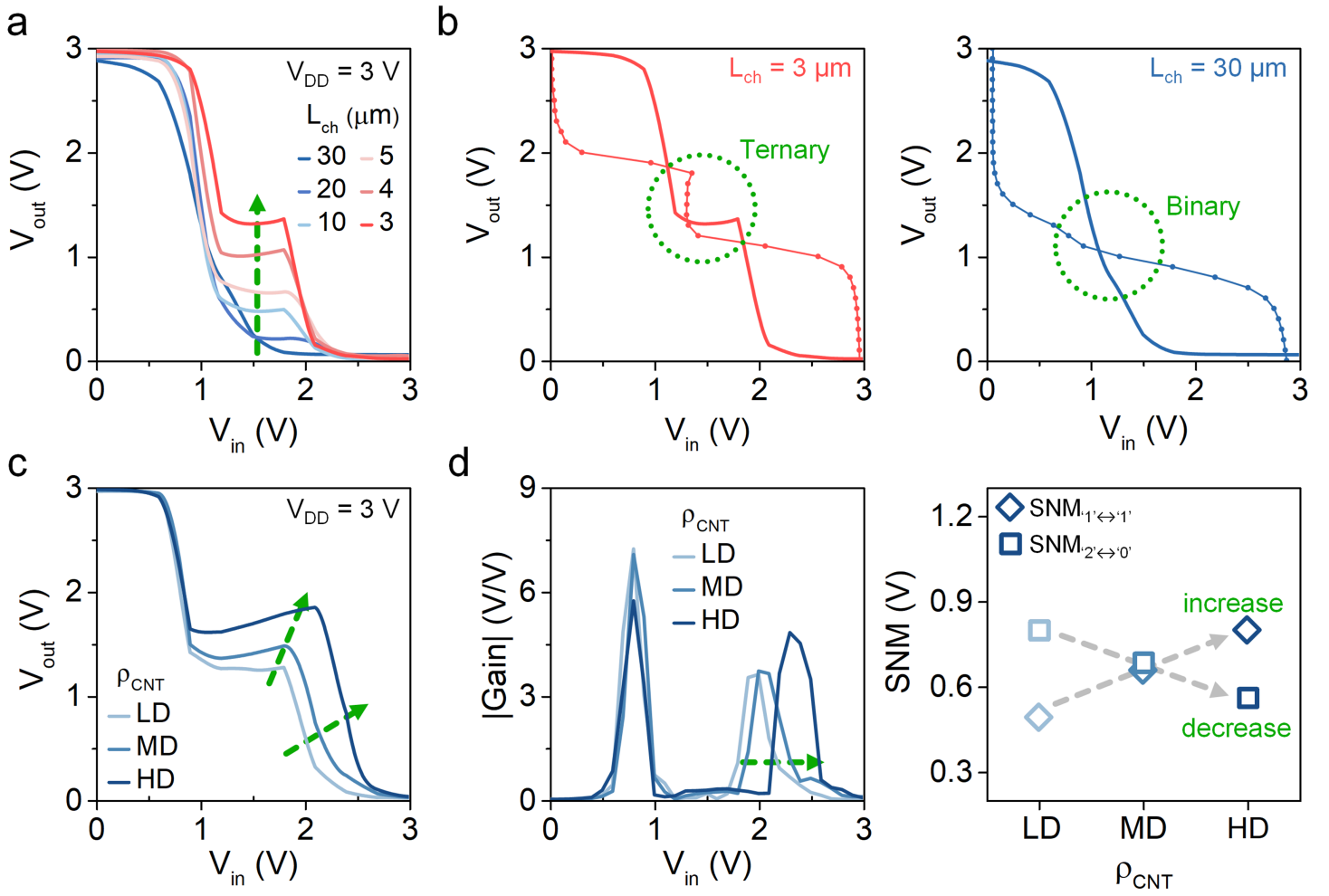


Figure 6

Logic-state control through channel length and upper-layer CNT network density.

a Voltage transfer characteristics (VTCs) measured at $V_{DD} = 3$ V using vertically stacked NTC transistors with L_{ch} values of 30, 20, 10, 5, 4 and 3 μm as the pull-up elements. The n-type CNT FET serving as the pull-down and the remaining circuit conditions were unchanged. **b** Butterfly plots constructed from the measured and mirrored VTCs at $L_{ch} = 3$ μm (left) and 30 μm (right), showing ternary operation with a finite intermediate-state region and binary operation without an intermediate-state region, respectively. **c** VTCs measured at $V_{DD} = 3$ V while varying only the upper-layer ρ_{CNT} of the pull-up element. **d** Corresponding absolute voltage gain, $|dV_{out}/dV_{in}|$, for the LD, MD and HD conditions (left). Increasing upper-layer ρ_{CNT} decreases the first voltage-gain peak and increases the second voltage-gain peak while shifting it toward higher V_{in} . Measured $\text{SNM}_{1' \leftrightarrow 1'}$ and $\text{SNM}_{2' \leftrightarrow 0'}$ values for the three upper-layer ρ_{CNT} conditions (right). $\text{SNM}_{1' \leftrightarrow 1'}$ increases from LD to HD, whereas $\text{SNM}_{2' \leftrightarrow 0'}$ decreases.

Supplementary Files

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