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Article

Keywords:

Posted Date: October 23rd, 2026

DOI: <https://doi.org/10.21203/rs.3.rs-11326561/v1>

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Additional Declarations: There is **NO** Competing Interest.

Wafer-scale integration of atomically thin metal oxide in memtransistor arrays for artificial neural networks

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Abstract

Liquid metal printed (LMP) two-dimensional (2D) metal oxides offer unprecedented opportunities toward next-generation information storage and neuromorphic computing. However, the scalable manufacturing of LMP metal oxides based integrated electronic circuits for the complex neuromorphic applications remains challenging, due to low device yield and high device-to-device variability. Here we report the 2-inch wafer-scale synthesis of the ultrathin 2D stannous oxide (SnO) film with high crystallinity and uniformity by using the electrostatic-assisted LMP stripping technique at low temperature of 225 °C. The integrated 32×32 vector-matrix SnO memtransistors in 48 independent blocks are achieved with a high yield of 96.9%. The memtransistor arrays are employed to emulate diverse synaptic plasticity, exhibiting low device-to-device variability (1.66%) and cycle-to-cycle variability (1.59%). By leveraging the synaptic characteristics of the memtransistor arrays in multiply-to-accumulate operation, we construct the convolution neural networks (CNNs) and Hopfield neural networks (HNNs) to implement the image processing and restoration tasks, respectively. The hardware convolution image processing is performed using the programmable kernels, where the extracted features are comparable to those processed by software. Additionally, the HNNs demonstrate robust multi-pattern associative memory capability, in which the structural similarity index (SSIM) approaches 100% and maintains above the 50% threshold in restoring three and four image patterns at various noise amplitudes, respectively. Our findings promise LMP metal oxides as potential building blocks to support scalable and compact neuromorphic system for the application of back-end-of-line compatible artificial intelligent agents.

Introduction

With the scaling of artificial intelligence (AI) workloads, the energy and latency costs induced by the frequent data movement between memories and processors increasingly dominate system performance¹. This fundamental bottleneck in conventional von Neumann architecture drives the exploration of alternative computing paradigms to reduce or eliminate the repeated memory–compute shuttling. Artificial synapses are promising candidates for time- and energy-efficient AI hardware by embedding memory and computation in a single device²⁻⁴. Moreover, the synaptic devices in crossbar array are particularly suitable for vector–matrix multiplication and weight updates in neural networks, enabling their wide applications in diverse AI tasks such as pattern recognition, computer vision, and natural language processing⁵⁻⁷. To promote the progress of neural networks at hardware level, analogue non-volatile memories (NVMs) mimicking the synaptic plasticity have been extensively investigated in different devices, such as resistive random-access memories, phase-change memories, flash memories, and ferroelectric memories⁸⁻¹⁰. Two-dimensional metal oxides (2DMOs), as part of the two-dimensional material family, have been identified as potential candidates for these artificial synaptic architectures, owing to their extraordinary physical properties, such as strong electrostatic gate controllability, low power switching, and flexible heterostructure integration¹¹⁻¹³. Compared to the van der Waals transition metal dichalcogenides (TMDCs), 2DMOs possess abundant defect states (e.g., oxygen vacancies), which is favorable for controllable charge trapping and ion migration. This enables the stable and gradual conductance modulation at the ultrathin limit, which is essential for analog weight updates and tunable synaptic plasticity^{14,15}. Moreover, metal oxides are highly compatible with the established CMOS processing technologies such as low thermal budget deposition of high- κ dielectrics and diverse interface engineering strategies, facilitating wafer-scale fabrication of high-

density neuromorphic devices¹⁶.

Despite these advantages, integration of metal oxides in high-performance neuromorphic systems at large scale remains challenging. Oxide thin films are typically prepared by conventional solution-based synthesis^{17,18}, physical vapor deposition (PVD)¹⁹, or chemical vapor deposition (CVD)²⁰, which however often suffer from poor stability and uniformity. For example, solution-processed approaches have been demonstrated to achieve large-area oxides at low cost, whereas the as-synthesized films are susceptible to inhomogeneous thickness, local compositional fluctuations, and high density of pinholes, significantly degrading device yield and increasing device-to-device variation²¹⁻²³. Although PVD and CVD techniques can produce compact oxide films with high chemical purity and thickness uniformity, pronounced device-to-device and cycle-to-cycle variations still exist in the oxide crossbar arrays, owing to the stochastic defect/ion migration and unstable conductive pathways²⁴⁻²⁶. Moreover, the growth temperature of CVD is generally above 400 °C²⁰, restricting its application in CMOS processing platform. Therefore, the development of low-temperature oxide synthesis techniques with high stability and conformity is essential for enabling scalable integration of uniform and complementary metal-oxide-semiconductor (CMOS) compatible neuromorphic devices.

Liquid metal printing (LMP) is a rapidly emerging technique for synthesizing ultrathin metal oxides under low temperature and ambient conditions, offering a promising alternative to conventional solution- and vacuum-based approaches^{27,28}. The low-melting-point liquid metals such as gallium (Ga), indium (In), and tin (Sn) could spontaneously form a thin oxide layer at the metal-air interface when heated in ambient below 300 °C. The growth of the atomically layered interfacial oxides is dominated by the Cabrera–Mott mechanism in the ultrathin regime, in which field-assisted ion transport induces rapid oxidation that becomes self-limited as the oxide thickens^{27,29}. This oxide layer with thickness of

~1–6 nm adheres more strongly to the target substrate than to the parent liquid metal, enabling its mechanical exfoliation and transfer onto the substrate. Recently, various ultrathin oxide layers including gallium oxide, tin oxide, and indium tin oxide, have been synthesized by the LMP techniques such as van der Waals touch-printing, squeeze-printing, or lateral smearing across a target substrate, which demonstrates great potential for the implementation of artificial synaptic devices^{12,28,30}. However, most 2DMOs synthesized by manual LMP are typically in the centimeter scale, whereas wafer-scale fabrication and reproducible transfer remain rarely achieved. Moreover, the manufacturing of LMP-based 2DMO synaptic devices has largely been restricted to single units or small proof-of-concept arrays, with limited investigation of the large-scale integration and functionalization.

In this work, we develop an electrostatic-assisted LMP stripping strategy that enables the clean and uniform synthesis of 2D stannous oxide (SnO) film on 2-inch SiO₂/Si wafer. The integrated three-terminal memtransistors in 32×32 vector-matrix are fabricated by using the as-synthesized SnO film with 48 independent blocks, giving rise to a high yield of 96.9%. The memtransistor arrays demonstrate consistent transport behavior, as reflected by the uniform distributions of the on/off ratio, hysteresis window, and subthreshold swing. The synaptic measurements further reveal the sufficiently high analogue on/off ratio and linear weight update, together with low device-to-device variability (1.66%) and cycle-to-cycle variability (1.59%), which are essential for neuromorphic hardware implementation. We then constructed the convolution neural networks and Hopfield neural networks using the memtransistor arrays in multiply-to-accumulate operation to perform the image processing and restoration tasks, respectively. The images processed using the six different convolution kernels exhibit extracted features comparable to the software counterparts, while the robust image restoration capability is identified in the Hopfield neural networks, illustrating the potential of LMP metal oxides

for scalable neuromorphic hardware.

Results and Discussion

Synthesis and characterization of wafer-scale SnO film

Figure 1a schematically demonstrates the synthesis process of ultrathin SnO film on 2-inch wafer-scale SiO₂/Si substrate using liquid-metal printing technique under ambient conditions. Firstly, liquid Sn was prepared on a glass plate heated at ~235 °C and then cooled to ~225 °C to prevent SnO₂ formation. The pre-existing oxide layer with air-borne contaminants on the liquid Sn surface was subsequently removed by a glass rod. After the preconditioning step, the freshly formed tin oxide skins were exfoliated and transferred onto a 2-inch SiO₂/Si substrate by gently touching the surface (see detailed fabrication process in Methods section). It is worth noting that pre-wiping the SiO₂/Si substrate using clean cloth before exfoliation is favorable for improving the continuity of the SnO film at wafer scale, which is due to the enhanced interfacial interactions (e.g., electrostatic forces) between the substrate and the surface oxide. Figure 1b shows the photograph of the SnO film covering almost the entire 2-inch SiO₂/Si wafer with negligible empty region. The enlarged optical image is shown in Figure 1c, in which the SnO sample exhibits smooth surface free of wrinkles and metal residues. Such atomically flat surface is further validated by atomic force microscopy (AFM) characterization shown in Supplementary Fig. 1, where a low surface roughness ranging from 0.5 to 0.77 nm is observed at the different positions of the 2-inch wafer. The thickness of the as-synthesized film is also revealed by the AFM measurement, which is around 5.0 nm, corresponding to 10 layers of SnO (Figure 1d). To verify the crystallographic quality of the SnO film, we conducted the high-resolution transmission electron microscopy (HRTEM) and X-ray diffraction (XRD) measurements, as shown in Figure 1e and Supplementary Fig. 2, respectively. The SnO film shows a periodic atomic ordering structure with

lattice spacing of 0.27 nm, which can be assigned to the (110) crystal plane. The corresponding selected-area electron diffraction (SAED) pattern depicts the diffraction spots from the (110) and (200) crystal planes along with the central diffraction rings, indicating the polycrystalline nature of the printed SnO sample. Figure 1f exhibits the TEM image and the corresponding energy-dispersive X-ray spectroscopy (EDS) elemental mapping of the SnO film, illustrating the homogeneous distribution of Sn and O constituents with approximately 1:1 stoichiometric ratio. The EDS results are consistent with the XPS spectra shown in Supplementary Fig. 3, confirming that the exfoliated SnO is dominated by stannous oxide (Sn^{2+}) rather than stannic oxide (Sn^{4+}), without significant presence of elemental tin (Sn^0). These results suggest the high quality of the ultrathin SnO film in large area, which is essential for achieving the integrated 2D memtransistor arrays with high yield.

We further investigate the quality and uniformity of the wafer-scale SnO film by using the Raman characterization in a statistical manner. To fabricate the SnO transistors in crossbar arrays, the wafer-scale film is patterned into 48 isolated blocks by using RIE technique, with each block containing 1024 channels (shown in Supplementary Fig. 4). Figure 1g shows the Raman spectra of the 1024 SnO channels selected from a single block circled in the photograph (Supplementary Fig. 4). Only one single characteristic peak (A_{1g}) located at 213.5 cm^{-1} is observed in all the spectra, indicating the absence of the mixed-valence oxides (e.g., $145/171\text{ cm}^{-1}$ for $\text{Sn}_2\text{O}_3/\text{Sn}_3\text{O}_4$) in the sample³¹, further validating the high purity of the as-synthesized SnO. The A_{1g} peak positions of all the channels are then extracted and mapped onto the 32×32 array (Figure 1h), revealing no significant outliers and a small wavenumber deviation within 3.0 cm^{-1} . The corresponding statistical analysis is presented as a histogram in Figure 1i, where a typical Gaussian distribution is identified. The intensities and full widths at half maximum (FWHMs) of the characteristic peaks are also examined, which are consistent

with the peak-position distribution, as shown in Supplementary Fig. 5. To further confirm the phase homogeneity of SnO, Raman mapping of A_{1g} mode was performed on selected SnO channels at multiple locations across the wafer, as shown in Figure 1j and Supplementary Fig. 6. The Raman signal demonstrates strong intensity and uniform color contrast, validating the high purity and quality of the SnO sample at wafer scale. Based on the patterned SnO channels, we then fabricated the 2D memtransistors in a three-dimensional matrix configuration which is schematically shown in Figure 1k. A 5 nm/15 nm layer of Cr/Au is firstly deposited on the SnO channels to create the drain-source contact regions through electron beam evaporation, followed by the growth of 30 nm gate dielectric (Al_2O_3) using ALD. The dielectric layer is then etched via holes to connect the bottom and top metal layers required for routing the source and drain signals without overlap. Subsequently, a second Cr/Au layer (5 nm/50 nm) is deposited on top to form the gate electrode and drain wire (see detailed manufacturing process in Methods section and Supplementary Fig. 7). Figure 1l displays the optical image of a single matrix consisting of 32 rows and 32 columns for a total of 1024 top-gated memtransistors, with the corresponding diagrammatic representation shown in Figure 1m. The scanning electron microscopy (SEM) characterization provides a detailed visualization of the SnO memtransistors with a channel length of 12 μm , which are successfully integrated at large scale via the different functional metal lines (Figure 1n). The source lines are vertically connected at the top and bottom, while the gate and drain lines are connected at the right and left, respectively, demonstrating submicron alignment accuracy. This crossbar matrix features a compact topological layout, which is intrinsically suitable for vector–array multiplication operations, allowing for the parallel computation achieved through precise conductance modulation.

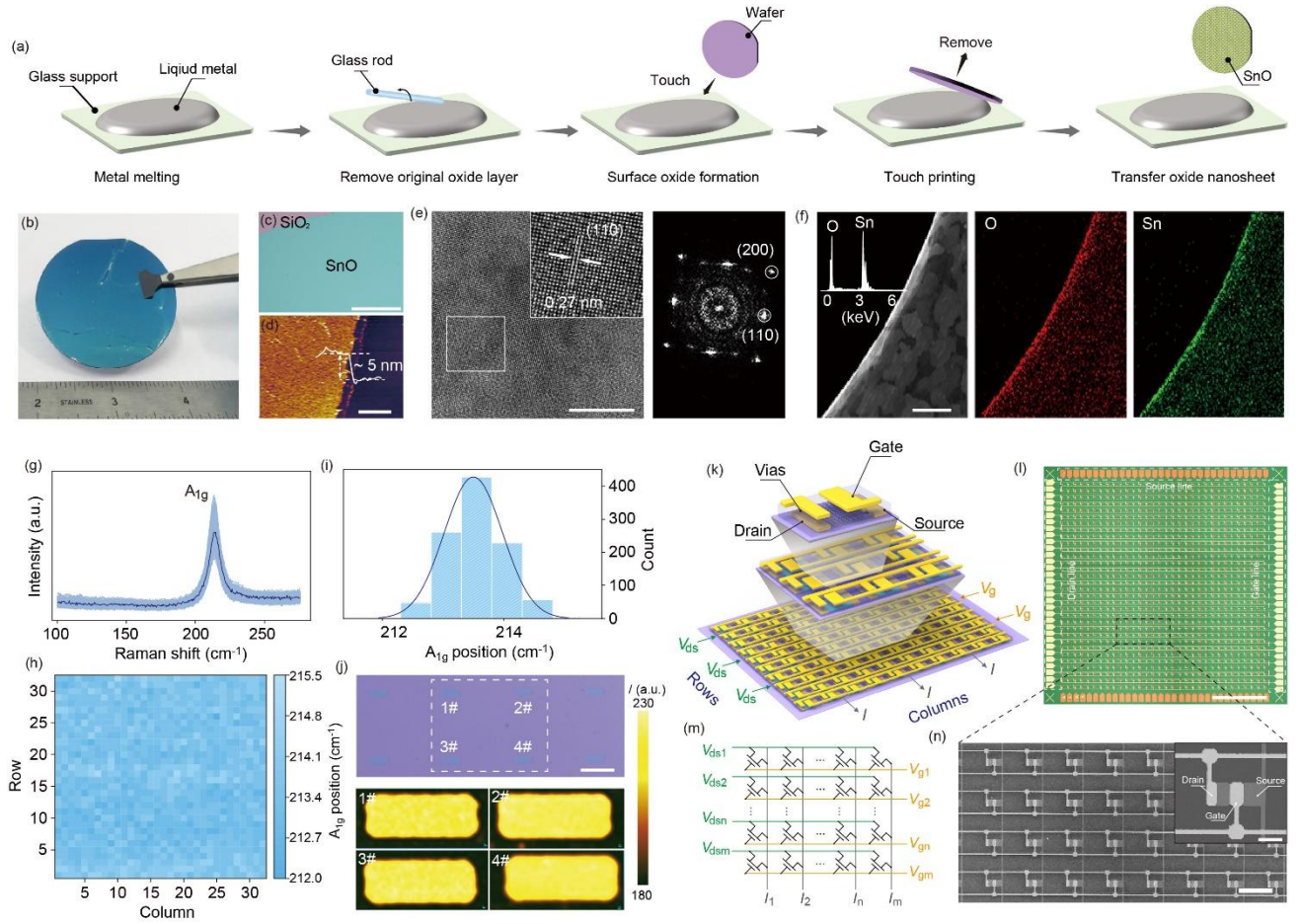


Figure 1. Synthesis and characterization of wafer-scale SnO film. (a) Schematic illustration of the preparation process of ultrathin SnO film under ambient conditions. (b) Photograph of the SnO film in 2-inch wafer scale. (c) Enlarged optical image of SnO sample. The scale bar is 200 μm . (d) AFM image of the SnO film with a step height of ~ 5 nm. The scale bar is 3 μm . (e) HRTEM image and the corresponding SAED pattern obtained by fast Fourier transform (FFT). The scale bar is 10 nm. The inset shows an enlarged view of the lattice fringes from the white rectangular region. (f) EDS mappings of the Sn and O elements. The inset shows the stoichiometric ratio of Sn and O approximating 1:1. The scale bar is 200 nm. (g) Raman spectra of the 1024 SnO channels. (h) Spatial distribution mapping of A_{1g} peak positions for the 32×32 channel array. (i) Histogram of the statistical analysis of the A_{1g} peak positions. (j) Raman mapping of the selected SnO channels. The scale bar is 50 μm . (k) Three-dimensional configuration of the top-gated SnO FETs connected in matrix array. (l) Optical image of the 32×32 SnO arrays. The scale bar is 1 mm. (m) Schematic illustration of the crossbar matrix for vector-array multiplication. (n) Enlarged SEM images of the SnO array at different magnifications. The scale bars are 100 μm and 20 μm for the low- and high-magnification images, respectively.

Statistical performance of the SnO memtransistor matrix

We then conducted the electrical transport measurements on the SnO memtransistor matrix to evaluate its yield and uniformity. Figure 2a displays the bidirectional transfer characteristics of all the 1024

devices fabricated in the 32×32 crossbar array, which exhibit hole-dominated transport property, in good agreement with the previous reports³². Typical hysteresis and memory behavior are identified in the transfer curves due to charge trapping at the SnO/amorphous (am-) Al₂O₃ interface, a mechanism which will be discussed later. After excluding 32 non-conductive devices, the yield of the vector–matrix is determined to be 96.9%. This yield not only exceeds that of most ultra-thin device arrays³³⁻⁴³, but also surpasses the International Technology Roadmap for Semiconductors (ITRS) requirement of 89.5% for flash memory⁴⁴ (Figure 2b). It is worth noting that the wafer-scale SnO film is grown at 250 °C within 5 minutes, which is much more energy- and time-efficient than conventional CVD synthesis of 2D semiconductors, generally demanding high temperatures beyond 400 °C and growth durations over 1 hour⁴⁵. These characteristics promise the liquid-metal-exfoliated 2D SnO as a potential material platform for the applications of large scale back-end-of-line (BEOL)-compatible memories and artificial synapses. We further investigated the uniformity of the vector–matrix by extracting the characteristic parameters of the memtransistors, including on- and off-state current distributions, memory window (ΔV), on/off ratio ($I_{\text{on}}/I_{\text{off}}$), and subthreshold swing (SS), as shown in Figure 2c–e and Supplementary Fig. 8. The on- and off-state currents are distributed uniformly without significant outliers, forming two distinct planes over the entire array in Figure 2c. Figures 2d and 2e show the spatial mapping (left) and statistical histograms (right) of the memory window and on/off ratio, respectively. It is noted that the memory window is defined as the V_g difference between the forward and backward sweeping at a channel current (I_{ds}) of 1 nA. After excluding the non-functional units represented by the white squares, consistent color contrast is observed in both the ΔV and $I_{\text{on}}/I_{\text{off}}$ ratio mappings, suggesting high device-to-device uniformity across the array. The histograms in the right side illustrate the highly concentrated Gaussian distributions of the ΔV and $I_{\text{on}}/I_{\text{off}}$ ratio, where

the variabilities are determined to be 4.17% and 2.51%, respectively. These statistical results suggest that the improved liquid metal self-oxidation peeling process possesses excellent controllability and repeatability, thereby laying a solid material foundation for constructing the large-scale memtransistors and neuromorphic devices with high uniformity and reliability.

The memory characteristic of the SnO memtransistor is further investigated by performing the cyclic writing/erasing operations (Figure 2f), in which the positive and negative gates generate the low resistance state (LRS) and high resistance state (HRS), respectively. We propose that the memory behavior can be mainly attributed to the Sn-diffusion induced interfacial charge trapping states during the ALD deposition of the am-Al₂O₃ dielectric at high temperature of 150 °C. Figure 2g shows the elemental depth distribution of the SnO/am-Al₂O₃ interface characterized by using the Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS). Through monitoring the Sn-related elements, including Sn⁺, Sn₂O⁺, and SnO₂⁻, the Sn ions are observed to diffuse approximately 4 nm into the am-Al₂O₃ dielectric, which is essential to produce significant amounts of trapping states located at or near the SnO/am-Al₂O₃ interface. Density functional theory calculations were further performed to investigate the thermodynamic stability and electronic structure of the Sn-diffused am-Al₂O₃ layer. The structural parameters of the tetragonal SnO and pristine am-Al₂O₃ employed in the calculations are presented in Supplementary Table 1. The band structures and total density of states (TDOS) of the SnO and am-Al₂O₃ are shown in Figures 2h, 2i, and Supplementary Fig. 9. The calculations reveal a direct bandgap of approximately 2.1 eV for tetragonal SnO, with the valence-band maximum and conduction-band minimum occurring at the same k-point, while am-Al₂O₃ exhibits a bandgap of approximately 4.25 eV. The corresponding TDOS profiles exhibit state-free energy intervals between the valence- and conduction-band edges, consistent with the calculated band structures (Supplementary

Fig. 9). We then investigated the incorporation of Sn atoms into the am- Al_2O_3 network via substitution at the Al sites with distinct local oxygen-coordination environments. The formation energies were calculated for Sn substitution at the fourfold-, fivefold-, and sixfold-coordinated Al sites, respectively (Supplementary Fig. 10), in which the fivefold-coordinated configuration exhibits the lowest formation energy of -7.65 eV. The discrete occupied gap states located near the Fermi level of am- Al_2O_3 are clearly identified under this energetically preferred condition (Figure 2j), indicating that the incorporated Sn atoms significantly perturb the electronic structure of the Al-O network. These gap states near the SnO/am- Al_2O_3 interface could act as the energetically accessible sites for the capture and storage of carriers in the SnO channel, which is essential for realizing the memory effect in the device. Figure 2k schematically illustrates the electrically driven memory behavior in the am- Al_2O_3 gated SnO transistors. The negative and positive gate voltages are employed to drive the holes to be trapped and released in the gap states near the SnO/am- Al_2O_3 interface, generating the HRS and LRS storage states.

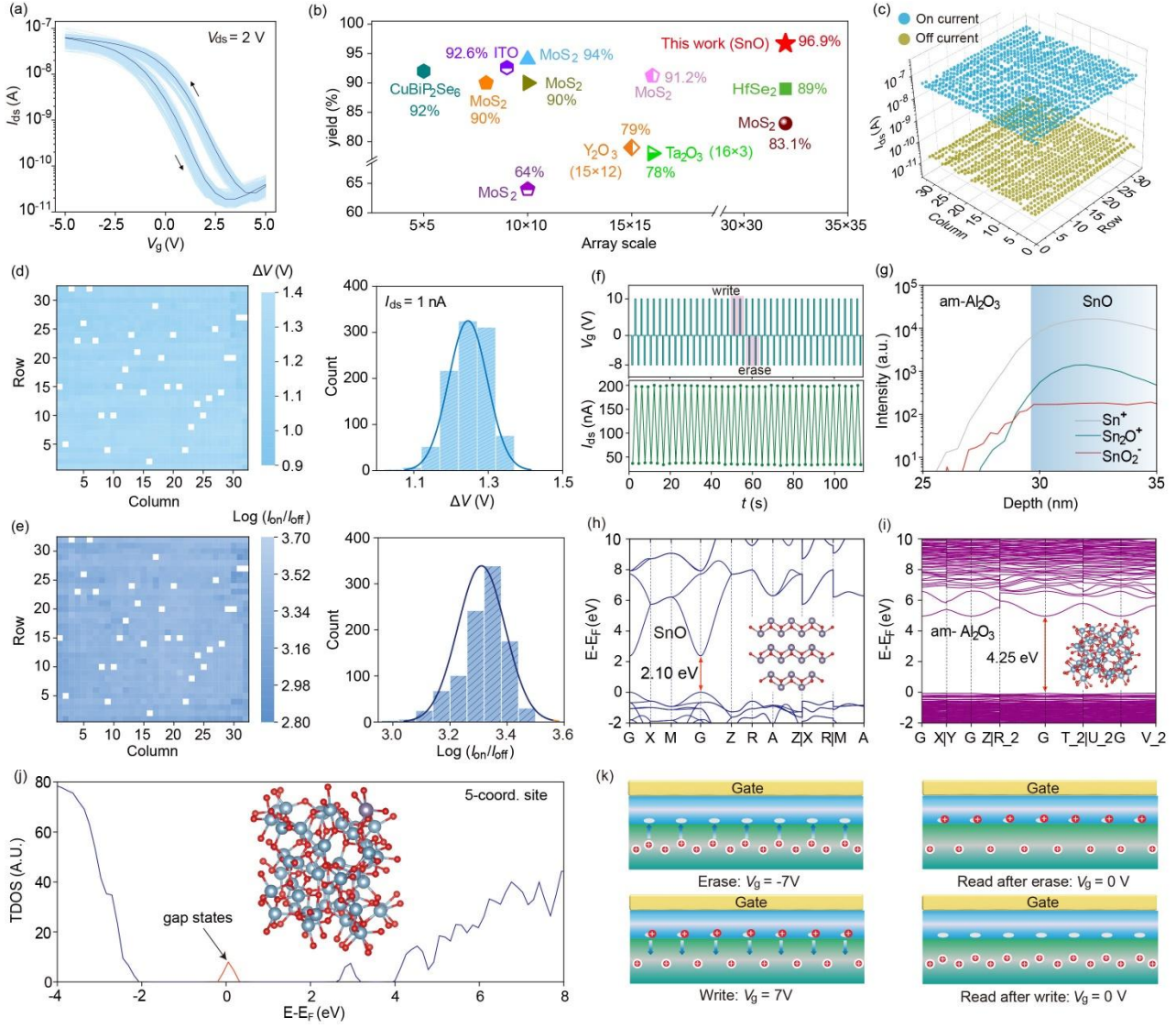


Figure 2. Statistical performance of the SnO memtransistor matrix. (a) Bidirectional transfer characteristics of the functional 992 devices in the 32×32 memtransistor array. (b) Yield benchmark of the SnO memtransistor with the reported crossbar arrays using other channel materials. (c) Three-dimensional mapping of the on and off currents for the 32×32 SnO memtransistor matrix. Spatial mapping (left) and statistical histograms (right) of the (d) memory window and (e) on/off current ratio, respectively. (f) Cyclic writing/erasing operations on the SnO memory. The writing and erasing gate pulses are set as 10 V and −8 V, respectively. (g) TOF-SIMS depth profiles of the Sn element at the SnO/am-Al₂O₃ layer interface. Band structures of (h) SnO and (i) am-Al₂O₃ calculated using the HSE06 functional. (j) Density of states of the Sn-diffused am-Al₂O₃ layer. (k) Schematic illustration for clarifying the memory effect of the SnO/am-Al₂O₃ device. The rectangles in the blue and green colors represent the am-Al₂O₃ and SnO, respectively. The ellipses in the am-Al₂O₃ denote the trapping states. The circles represent the holes that move between the am-Al₂O₃ and the p-type SnO driven by the gates with different polarities.

Synaptic plasticity of the SnO memtransistor matrix

Based on the memory properties, we explore the essential synaptic plasticity of the 2D SnO memtransistors to evaluate their applications in neuromorphic computing. Figure 3a shows a schematic of a biological synapse, which can be analogized to the V_g -modulated SnO artificial synaptic device. The pre- and post-synaptic spikes are applied via the top gate terminal and the drain terminal, respectively; the input spike V_g triggers the postsynaptic output current (PSC) in the SnO memtransistor, and the corresponding conductance represents the synaptic weight⁴⁶. The synaptic behavior of the device under various V_g pulses with different magnitudes is shown in Figure 3b and Supplementary Fig. 11. The gradual increase and decrease of the PSC in the positive and negative V_g regimes correspond to the excitatory and inhibitory behaviors (EPSC and IPSC), respectively. The PSC can also be effectively tuned by the pulse width (Supplementary Fig. 12), where the EPSC and IPSC demonstrate a rapid rise and decline followed by a gradual saturation with increasing the pulse width, respectively. The PSC modulation is further revealed by employing the successive V_g pulses to train the device under the excitatory and inhibitory states (Supplementary Fig. 13). Each subsequent V_g stimulus arrives before complete relaxation of the preceding PSC, giving rise to the cumulative excitation and inhibition, which is analogous to the postsynaptic membrane summation in a biological system. To illustrate the dependence of synaptic plasticity on the relative timing of two adjacent action potentials, we investigated the indirect spike-timing-dependent plasticity (STDP) of the SnO synaptic device by changing the time interval (Δt) in two paired V_g pulses, as shown in Figure 3c. Through fitting the experimental curves using exponential function, the time constants are extracted to be ~ 5 ms and ~ 9 ms for the EPSC and IPSC, respectively, which are comparable to the typical response time of biological synapses⁴⁷.

The uniformity and reliability of the SnO synaptic devices are further evaluated through conducting the long-term potentiation and depression (LTP–LTD) measurements. To ensure a linear conductance weight response, the successive V_g pulses with amplitudes varying from 0.1 V to 5 V (0.1 V step) and from -0.1 V to -3.2 V (-0.1 V step) are applied on the devices in the LTP and LTD processes, respectively, generating a sufficiently high on/off ratio ranging from 28.0 to 31.3. Figure 3d summarizes the P–D curves of 150 devices randomly selected from the SnO matrix array, in which the dots represent the conductance of one typical device. The individual P–D curve of each device is demonstrated in Supplementary Fig. 14. All the tested devices exhibit consistent weight updating behavior in the potentiation and depression processes under the stimulation of continuous V_g pulses, confirming their excellent uniformity for synaptic application. Supplementary Fig. 15 further validates the performance consistency by analyzing the stochastic fluctuations of the tested devices across all the conductance states, in which clustered distribution of each state with low dispersion is identified. To quantitatively evaluate the device-to-device variation, the statistical distribution of the maximum conductance is depicted among all the devices, as shown in Figure 3e. The variability (σ/μ) is determined to be 1.66% through fitting the distribution using Gaussian function, further indicating the high uniformity of the synaptic array for weight updating. To quantify the deviations from ideal linear weight updating in the SnO devices, we introduced a parameter A to characterize the linearity in the LTP and LTD processes (Supplementary Fig. 16). The parameter A is extracted as $A_P = 2.2897$ and $A_D = 2.4225$ using the median conductance based on the behavioral device model for multilayer perception algorithm, indicating the good linearity of the weight response tuned by V_g pulses. The A_P and A_D of all the tested devices are summarized in Supplementary Fig. 17. In addition to device uniformity, we also investigated the cyclic endurance of the synaptic array to evaluate their reliability. Figure 3f shows

the 150 consecutive P–D operation cycles of the SnO device, in which the enlarged cycles are presented in the right panel. The device exhibits stable switching characteristics without performance degradation throughout all testing cycles, indicating robust cyclic endurance. The stochastic fluctuation of each conductance level is also investigated to qualitatively visualize the cycle-to-cycle variation in both the potentiation and depression processes, as shown in Figure 3g. The concentrated distribution of conductance with a small variation across all the states directly illustrates the excellent cycle-to-cycle stability. The statistical distribution of the maximum conductance among all 150 operation cycles is also plotted in the histogram (Figure 3h), giving rise to a variability of 1.59% based on the Gaussian function fitting.

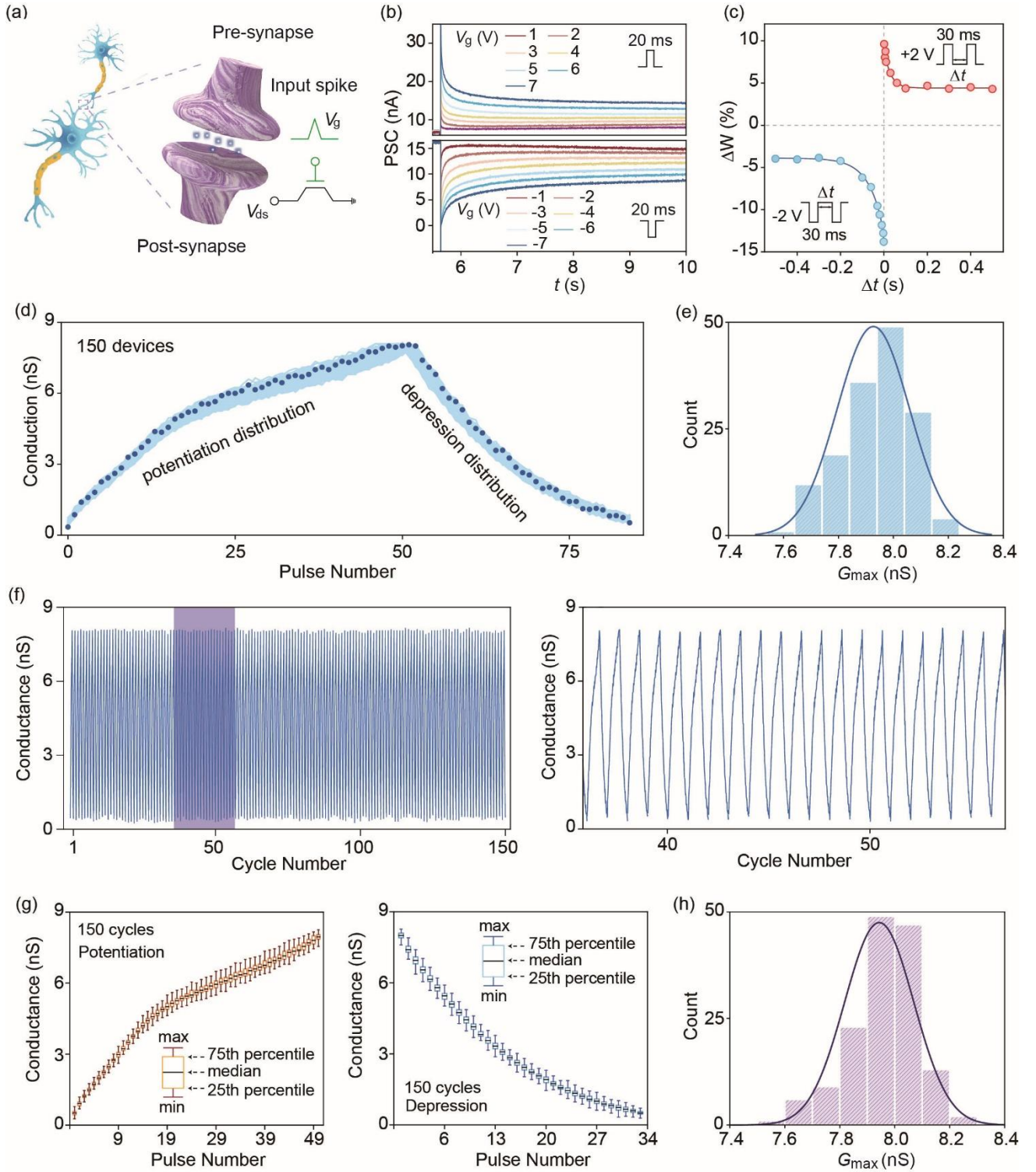


Figure 3. Synaptic plasticity of the SnO memtransistor matrix. (a) Schematic illustration of a biological synapse and the SnO memtransistor based artificial synaptic device. (b) The EPSC and IPSC modulated under the positive and negative V_g pulses, respectively. (c) Dependence of synaptic weight change (Δw) on the time interval (Δt) between the paired gate pulses. The solid curves are the exponential fitting of the Δw . (d) The LTP-LTD test for 150 randomly selected SnO synaptic devices. (e) Histogram of the G_{max} distribution extracted from the P-D curves for the 150 devices. (f) Endurance test of the synaptic device measured for 150 LTP-LTD cycles. The right panel shows the enlarged

view of the shaded area in the left panel. (g) Cycle-to-cycle variation of the LTP (left) and LTD (right) in the 150 testing cycles. (h) Histogram of the $G_{\max}$ distribution in the 150 cycles.

Convolutional image processing based on SnO crossbar array

Convolutional neural networks (CNNs) have been widely used to implement different types of image processing tasks, such as image classification, detection, and segmentation. Convolution kernels consist of small trainable weight matrix that acts as a local feature extractor. The kernels slide across the input feature map and perform multiply-accumulate (MAC) operation between the kernel weights and each local input patch, generating an output feature map. With the capability of achieving continuously tunable non-volatile weight states, the SnO synaptic array demonstrates significant potential to construct various convolution kernels by adjusting the conductance of individual device to desired values. Thus, we randomly selected a 7×7 SnO sub-array from the 1024 devices to implement the CNN based image processing tasks. Specifically, two memtransistors are used as a differential pair to represent both positive and negative weights. The weights of $-1/+1$ were mapped by using the high resistance state (HRS) and low resistance state (LRS), such that $G^{\text{HRS}} - G^{\text{LRS1/2/3/4}} \sim -1$ and $G^{\text{LRS1/2/3/4}} - G^{\text{HRS}} \sim +1$. Figure 4a shows the contour distribution of the five resistance states including HRS, LRS1, LRS2, LRS3, and LRS4 in the 7×7 array precisely modulated by the gate terminal, while the corresponding cumulative probability plot is demonstrated in Figure 4b. The five resistance states can not only be reliably distinguished from each other, but also show excellent spatial uniformity across different devices, enabling integer weights mapping from -4 to 4 . Accordingly, two 3×3 crossbar arrays were employed to construct the target G convolution kernel, with the kernel values derived from the conductance matrix based on the spatial positions and resistance states of the memtransistors, as shown in Supplementary Fig. 18. In our work, we used the Fudan Library as the input image, in which

the intensity of the image is converted into voltage applying across the rows of the SnO synaptic array (Figure 4c). In the processed image, each pixel is generated by performing a convolution operation between the input voltage (V_{ij}) vector mapped from the 3×3 input sub-image and the G convolution kernel (G_{ij}), i.e., $I_{out} = \sum V_{ij} \times G_{ij}$. Here, the I_{out} is the summation of the differential currents which can be expressed as $I_{out} = \sum (I_j^+ - I_{j+3}^-)$ according to the Ohm's law and Kirchhoff's law. It is noted that the G convolution kernel is mapped from the conductivities of the memtransistor array as mentioned above, while the convolution operation is simulated using software code. After completing the convolution operation over the entire image, the full extraction result can be achieved.

Figures 4d–f compare the software- and hardware-processed images for vertical edges, horizontal edges, and embossed edges, respectively. It is noted that the kernel values are arranged precisely without considering device variation in the software implementation, whereas such variation is inherently included in the hardware platform. Nevertheless, both the software- and hardware-processed images demonstrate similar extracted features in implementing different edge detection tasks, indicating the robust device-variation tolerance of the SnO memtransistor array for convolution operation. Moreover, arising from the uniform and consistent resistance states in the memtransistor array tuned by the gate terminal, the integer weights from -4 to 4 can be mapped to construct complex Gaussian kernels (Supplementary Fig. 18). Therefore, we successfully achieved a range of image processing results including Gaussian, sharpen, and average, which are comparable to the images processed by software (Figure 4g). The Learned Perceptual Image Patch Similarity (LPIPS) metric is employed to further quantitatively evaluate the consistency between the hardware and software processed results (Supplementary Fig. 19). It is noted that the six different convolution kernels demonstrate significant perceptual differences from each other (0.07 – 0.28), validating their capability

to extract the distinct differentiated features. In contrast, the LPIPS under the same convolution kernel remains below 0.05, suggesting the high perceptual consistency of the two different processing images (Supplementary Table 1). Moreover, nearly identical pixel distributions are observed for the same convolution kernels in the hardware and software (Supplementary Fig. 20), in good agreement with the LPIPS results. This verifies that the SnO memtransistor matrix can implement convolution kernels for different image processing tasks, which is promising to be used as the building block for CNNs.

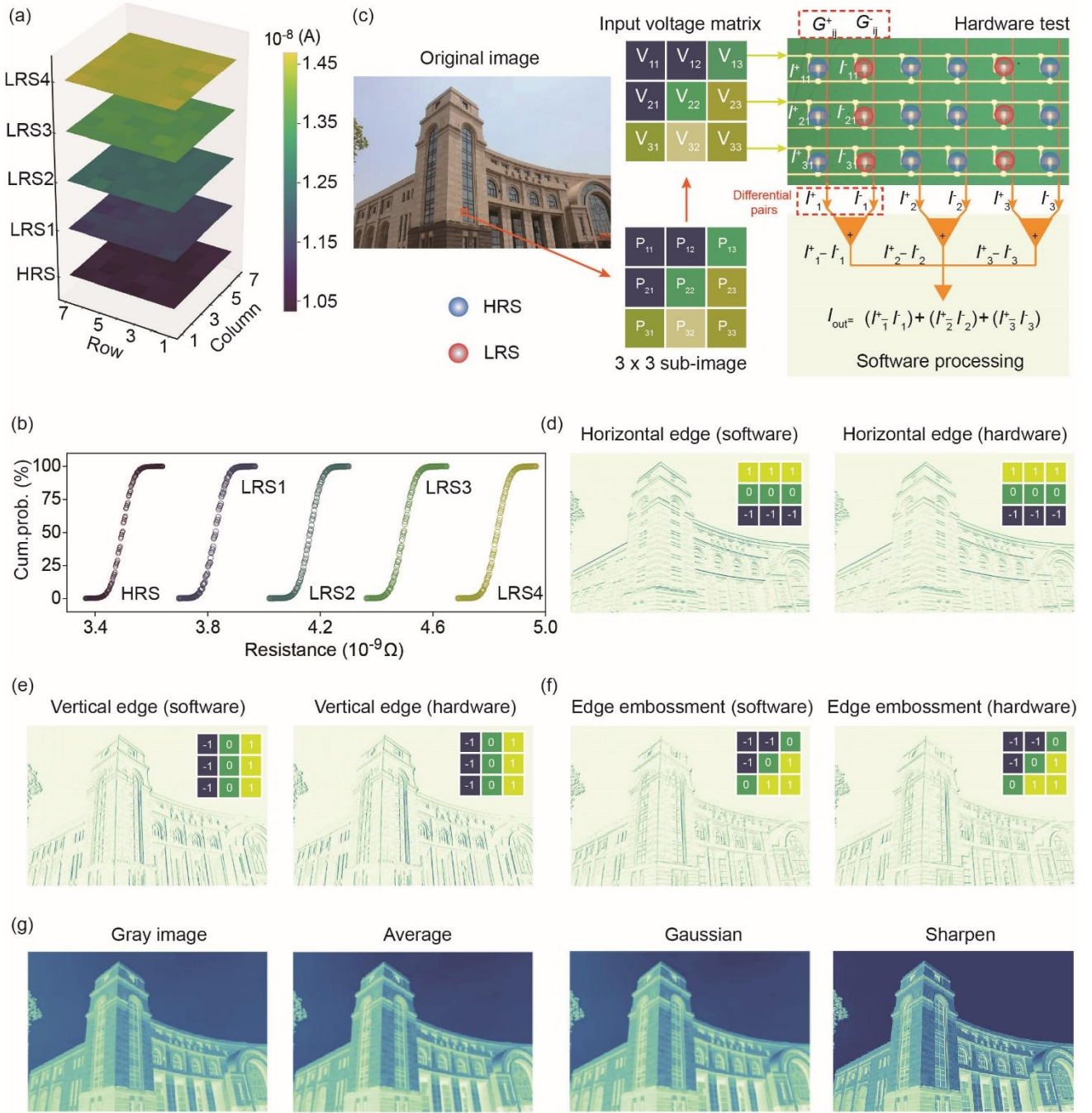


Figure 4. Convolutional image processing based on the SnO crossbar array. (a) Current distribution of five different resistance states (HRS, LRS1, LRS2, LRS3, and LRS4) by applying different operation voltages on a 7×7 SnO memtransistor array ranging from 2 V to 6 V. (b) Cumulative probability plots of the HRS, LRS1, LRS2, LRS3, and LRS4. (c) The convolutional image processing flow based on the SnO crossbar array. Hardware- and software-processed edge extractions using the (d) horizontal, (e) vertical, and (f) embossment kernels. The inset shows the different kernel designs. (g) Convolutional image processing results including Gaussian, sharpen and average by using the SnO hardware devices.

Hopfield neural networks for image restoration

In human brain, information is not encoded as discrete entities but rather distributed across an interconnected web of neural association. Upon encountering a particular stimulus, the brain concurrently activates multiple related memory traces, facilitating multidimensional association and retrieval. Hopfield neural network (HNN) simulates human brain's associative memory by storing information in distributed recurrent connections and retrieving complete patterns from partial or noisy inputs through attractor dynamics^{48,49}. The SnO memtransistor array is promising to be used in HNNs, because it provides non-volatile and tunable conductance weights that support parallel weighted summation. Figure 5a illustrates the HNN architecture along with the image restoration process via multiple associative memories. The network pre-stores multiple image patterns, with each pixel in the image encoded from its decimal value ξ_i^u (i : the position of the pixel; u : the u -th image pattern) into binary and bipolar codes. This process generates the input data for the HNN, which is denoted as $s_{i,k}^u$ ($k = 1, 2, \dots, 8$). The same bit data from different images is transmitted to the same HNN network layer Net_k , and the theoretical weights of the Net_k are defined as:

$$w_{ij,k} = \begin{cases} \frac{1}{P} \sum_{u=1}^P s_{i,k}^u s_{j,k}^u, & i \neq j \\ 0, & i = j \end{cases}$$

Where $s_{j,k}^u$ denotes the transpose matrix of $s_{i,k}^u$. Theoretically, when $s_{i,k}^u$ and $s_{j,k}^u$ are both 1 in each pattern, $w_{ij,k}$ reaches its theoretical maximum value of +1, and similarly, the theoretical minimum value can be -1. The precise mapping of these idealized weights onto the stable and programmable resistance states of physical devices is essential to realize the neural network hardware. Figure 5b shows the current distribution of the five different resistance states (HRS, LRS1, LRS2, LRS3, and LRS4) in 1000 reading cycles, and the corresponding Gaussian fits are depicted in Figure 5c. Although slight fluctuations are observed, the currents are consistently clustered within a narrow range without

significant outliers, confirming the robust cyclic endurance of the SnO memtransistor. Therefore, the weights of the Net_k layer mapped to the parameter W (mapping weights) are defined as follows. When the theoretical weight $\omega_{ij,k} \geq 0$, the $W_{ij,k}$ (positive) can be expressed as $\omega_{ij,k} \times (\text{LRS4} - \text{HRS}) + \text{HRS}$, indicating the linear relationship between the mapped weights and the operating range of $[\text{HRS}, \text{LRS4}]$. In contrast, the negative $\omega_{ij,k}$ suppresses the positive weight branch, in which the $W_{ij,k}$ (positive) is assigned to zero. Correspondingly, the $W_{ij,k}$ (negative) is defined as $\omega_{ij,k} \times (\text{LRS4} - \text{HRS}) + \text{HRS}$ in the negative weight branch, otherwise it is set to zero. The continuous modulation of channel conductance via V_g in the SnO vector-matrix enables the physical implementation of the HNN weight mapping $W_{ij,k} = W_{ij,k} \text{ (positive)} - W_{ij,k} \text{ (negative)}$, which determines the image restoration process described by $s_i(t+1) = \text{sign}(\sum_j^n W_{ij,k} s_{j,k}(t))$ (Figure 5a). It is noted that the network dynamics are determined by the Hopfield energy $E(s,k) = -\frac{1}{2} \sum_{i,j} W_{ij,k} s_{i,k} s_{j,k}$, in which the monotonic non-increase characteristic is guaranteed by the Lyapunov theory. When the HNN converges to the energy minimum, the steady-state output is processed through inverse bipolar mapping followed by binary decoding, which eventually generates the restored image result $\zeta_i(t+1)$.

The restoration performance of the HNN is quantified by using the Structural Similarity Index (SSIM) that better aligns with human visual perception than the conventional parameters such as Mean Squared Error (MSE) and Mean Absolute Error (MAE), thereby providing a more accurate and reliable evaluation of visual fidelity⁵⁰. We firstly tested the restoration capability of the network by implementing a fundamental three-pattern task using the Fashion-MNIST dataset, as shown in Supplementary Fig. 21. The network successfully restores all the three image patterns despite varying degrees of random noise interference, demonstrating robust multi-pattern associative memory functionality. To evaluate the influence of memory load on network performance, we increased the

number of stored image patterns to four (Figures 5d, 5e, and Supplementary Fig. 22). The SSIM gradually declines with increasing the noise level, suggesting the weakened image restoration performance. This is a typical characteristic of the HNN networks operating near their storage capacity, in which the inter-pattern interference degrades reconstruction fidelity, as further confirmed in Supplementary Fig. 23. Nevertheless, the SSIM remains above the 50% threshold even at a high noise intensity of 35 % for all the four image patterns, indicating the robustness of the SnO based HNN under increased memory load. The similar trend is maintained even when the storage load is extended to five image patterns, as shown in Supplementary Fig. 24. Additionally, we compared the restoration performance of the constructed HNN networks based on the three different types of devices including SnO memtransistor, resistive random-access memory (RRAM), and phase-change memory (PCM) by using the T-shirt image pattern (Figures 5f-g and Supplementary Fig. 25). The detailed parameters of the networks are discussed in Supplementary Fig. 26. The T-shirt images are fully restored across the noise levels ranging from 0 to 35% in the SnO memtransistor based HNN, achieving a high SSIM of 100%. In contrast, the RRAM and PCM based networks either generate blurred reconstructions with reduced SSIM or degrade significantly under elevated noise conditions. The improved performance can be attributed to the enhanced stability of the SnO memtransistor compared to RRAM and PCM, with long-term weight accuracy retention and energy convergence characteristics.

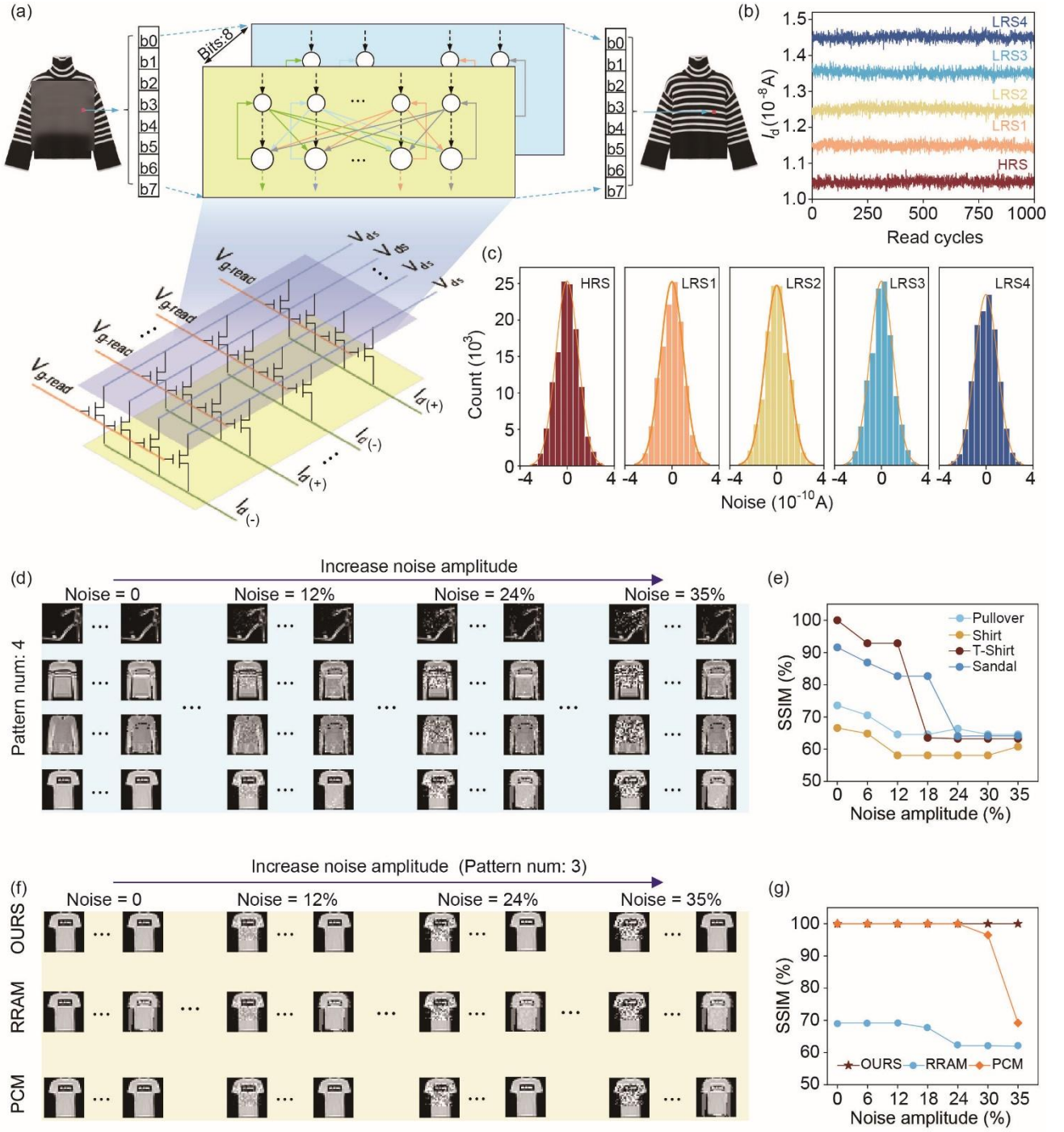


Figure 5. Hopfield neural networks for image restoration. (a) Schematic illustration of the Hopfield neural network via multi-associative memory for image restoration based on the SnO synaptic array. (b) Five resistance states including HRS, LRS1, LRS2, LRS3, and LRS4 in 1000 reading cycles of the SnO memtransistors. (c) Gaussian distributions of the current noise for all the resistance states. (d) Visualization of the restoration results for four different image patterns using the SnO-based Hopfield neural network. Four different random noise intensities including 0, 12%, 24%, and 35% are selected for the task implementation. Each column presents the noisy input image at the left and the corresponding restoration output image at the right. (e) Evolution of SSIM as a function of noise intensity for different image patterns. (f) Comparison of the image restoration results based on the

HNNs constructed by using the SnO, RRAM, and PCM devices. (g) SSIM versus noise intensity for the HNNs using different devices.

Conclusions

In summary, we have demonstrated the wafer-scale synthesis of ultrathin 2D SnO film at low temperature of 225 °C via electrostatic-assisted LMP stripping method. The SnO film possesses high crystallinity and uniformity, as characterized by the TEM and Raman statistics, which is essential for achieving the integrated 2D memtransistor arrays. The 32×32 memtransistor vector-matrix was fabricated in 48 independent blocks with a yield of 96.9%, demonstrating consistent transport characteristics. The observed nonvolatile memory behavior originates from the Sn-diffusion induced interfacial charge trapping states, which is verified by the TOF-SIMS and DFT calculations. The diverse synaptic plasticity is further characterized in the memtransistor arrays with minimal device-to-device variability (1.66%) and cycle-to-cycle variability (1.59%). The CNNs and HNNs are then constructed based on the memtransistor arrays to implement the image processing and restoration tasks, respectively. The output feature images processed by the hardware convolution kernels closely match those of the software counterparts. Moreover, the HNNs demonstrate robust restoration capability for the Fashion-MNIST dataset with increasing the noise amplitudes and memory loads, which is more superior to the networks based on the representative RRAM and PCM devices. Our work envisions LMP 2D metal oxides as promising candidates to craft memtransistor vector-matrix in high uniformity and reliability, paving the way to achieve scalable and compact neuromorphic system in CMOS compatible manner.

Experimental Methods

Growth of high-quality SnO films at wafer scale. 2D SnO thin films were prepared on a SiO₂/Si substrate using the liquid metal-printing method. Elemental tin (99.99% purity, Shot Metals) was initially melted on a glass substrate at approximately 235 °C under ambient conditions. After cooling to 225 °C, the original top oxide layer formed on the molten metal was removed to expose a clean metal surface by scraping. After 10 seconds, the freshly generated surface oxide layer was transferred from the liquid metal to the 2-inch SiO₂/Si wafer by direct contact. The surface of the SiO₂/Si substrate was wiped by a velvet cloth for 30 seconds and preheated to ~225 °C.

Material characterization. The Raman characterization is conducted by using a HORIBA Odyssey system with a laser wavelength of 532 nm at room temperature. The thickness and surface morphology of the SnO film surface are measured by using atomic force microscopy (Cypher S AFM). The film structures were examined by HRTEM (FEI Talos F200S) with an acceleration voltage of 200 kV. The TEM samples were prepared through directly transferring the SnO film to a carbon-coated grid with 200-mesh using the same liquid printing method described above. The XPS measurements were carried out in an analysis chamber using Al K α ($h\nu = 1486.6$ eV) as the excitation source. The samples were measured without extra surface cleaning, and the spectra were corrected by the C 1s core levels. XRD measurements were conducted using a Cu K α cathode target (Voltage = 40 kV, Current = 40 mA). TOF-SIMS was used to analyze element diffusion in both positive and negative ion modes equipped with a Bi primary ion source, a TRIFT analyzer (Triple Ion Focusing Time-of-Flight Analyzer), and a DMCP detector. The chamber pressure for the measurement is around 2.0×10^{-7} Pa.

Fabrication of SnO array. After printing the SnO thin film onto the 2-inch SiO₂/Si substrate, the sample was then patterned by photolithography with AZ5214 used as the photoresist. The exposed SnO was etched by reactive ion etching (RIE) technique in mixed BCl₃/Ar atmosphere. The photoresist

residue is removed by N-Methylpyrrolidone (NMP), which produces the patterned SnO channels. The photolithographic pattern for the first metal layer was defined using an MA/BA Gen8 mask aligner with a 1.4- μm -thick 1500 photoresist layer. The Cr/Au (5 nm/20 nm) is deposited as metal contact by electron-beam evaporator under a high vacuum (10^{-7} Torr). After lift-off in acetone solution, deionized water and isopropanol were used to further clean the sample. 30 nm Al_2O_3 isolating layer was then deposited on the wafer by atomic layer deposition (ALD) at 150 °C. The photolithography was then employed to pattern via on the Al_2O_3 isolation layer followed by RIE etching in BCl_3/Ar atmosphere. After removing the photoresist, the drain and gate electrodes were defined by photolithography, in which the channel width and length are arranged as 12 μm and 10 μm , respectively. The Cr/Au (5 nm/50 nm) metal contacts were then deposited by electron-beam evaporation followed by lift-off. To improve the adhesion of metal contacts, the fabricated crossbar array was annealed in N_2 atmosphere at 150 °C for 30 seconds. All the electrical measurements were carried out in a vacuum probe station (CGO-4) at a base pressure of 10^{-6} Torr with a four-channel source measurement unit.

HNN simulation. The Hopfield neural network (HNN) was constructed as a single-layer recurrent network with 28×28 neurons, where each neuron corresponds to one pixel in a Fashion-MNIST image. To represent grayscale pixel values, an 8-bit binary encoding scheme was adopted, such that each image pattern was stored and reconstructed using eight parallel HNN layers based on the Hebbian learning rule. In the simulation, non-ideal factors, including the limited conductance-state range as well as device-to-device and cycle-to-cycle variations, were taken into account. The simulation code was implemented in Python. Ten sample images, corresponding to the ten Fashion MNIST categories, were selected for reconstruction, and their HNN mapping weights were obtained using the above method together with the weight-mapping procedure described in the section

“Hopfield neural networks for image restoration”. During reconstruction, Gaussian noise was first added independently to each pixel within a fixed range of the original images, with noise intensity (i.e., $n(x, y)$) controlled by the standard deviation σ ($\sigma = 0, 15, 30, 45, 60, 75, 90$), that is, $n(x, y) \sim N(0, \sigma^2)$. The noisy images were then sequentially fed into the network for reconstruction. The iterative update process was terminated according to the monotonic decrease of the energy function. Finally, the steady-state outputs of the eight HNN layers were decoded from binary form into decimal pixel values to obtain the reconstructed images.

DFT calculations Methods. For the DFT calculations, the Vienna Ab Initio Simulation Package (VASP)^{51,52} and the projector-augmented wave (PAW)^{53,54} method were used. The generalized gradient approximation (GGA) parameterized by Perdew, Burke, and Ernzerhof (PBE)⁵⁵ and the hybrid functional proposed by Heyd, Scuseria, and Ernzerhof (HSE06)⁵⁶ were used for the exchange-correlation functionals, with the plane-wave basis function within 500 eV cutoff energy. The 3s and 3p orbitals of Al, the 4d, 5s, and 5p orbitals of Sn, and the 2s and 2p orbitals of O were treated as valence electrons. At first, unit cell calculations were conducted for the experimentally found phases: tetra-SnO, am-Al₂O₃. The electronic self-consistency energy convergence criterion and force convergence criterion for ionic relaxation were set to 10^{-7} eV and 0.01 eV Å⁻¹ for SnO, and 10^{-5} eV and 0.001 eV Å⁻¹ for am-Al₂O₃, respectively. The details of the generation of amorphous and atomic structures are presented in Supplementary Table 2.

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Data availability

All data are presented in the manuscript or Supplementary Information or available upon reasonable request to the corresponding author.

Code availability

The codes used for the simulation are available from the corresponding author upon reasonable request.

Acknowledgements

This work was supported by the National Key Research and Development program of China (No. 2024YFA1410700 and 2023YFA1407800), and the National Natural Science Foundation of China (62374038 and 62204051), and Fundamental and Interdisciplinary Disciplines Breakthrough Plan of the Ministry of Education of China (JYB2025XD XM701).

Author contributions

D. X., Z. W., T. L., and Y. Z. conceived and designed the project. H. L., Y. C., and T. L. contributed equally to this paper. H. L., T. L., and Y. N. prepared the LMP SnO thin films and fabricated the memtransistor arrays. H. L. and T. L. performed the material characterizations and device measurements. Y. C. and T. L. constructed the CNN and HNN neural networks and performed all the simulations with the assistance of Z. X. Y. Z. performed the theoretical calculations. D. X., H. L., Z. W., T. L., Y. C., and Y. Z. prepared all the figures. D. X., H. L., Z. W., T. L., Y. C., and Y. Z. co-wrote the manuscript and supplementary materials. All authors reviewed and commented on the manuscript and supplementary materials.

Competing interests

The authors declare no competing interests.

Additional information**Supplementary information**

The online version contains supplementary material available at <https://doi.org/xxx/xxxxxx>.

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