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Development and Experimental Validation of a Dual-Input Dual-Output DC-DC Converter for PV–Battery Hybrid Energy Systems

Saber Zare
Shiraz University of Technology
Amirhossein Rajaei
a.rajaei@sutech.ac.ir

Shiraz University of Technology
Mohammad Karimianfard
Shiraz University of Technology

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Development and Experimental Validation of a Dual-Input Dual-Output DC-DC Converter for PV–Battery Hybrid Energy Systems

Saber Zare, Amirhossein Rajaei, Mohammad Karimianfard

***Abstract*— Due to the inherently fluctuating nature of renewable energy sources, their output current and voltage exhibit significant intermittency, rendering them insufficient for standalone sustainable power delivery. To address this, hybrid systems combining renewables with auxiliary storage or generation units are commonly deployed. This study introduces an innovative dual-input dual-output (DIDO) DC-DC converter configuration utilizing a T-source impedance network. In the proposed setup, a photovoltaic (PV) array and a battery storage unit serve as the dual input ports. The converter is controlled such that the battery compensates for any power deficits when the PV output falls short of the load requirements, whereas excess PV generation is directed to charge the battery during surplus periods. The mathematical model and operational modes of the converter are thoroughly analyzed. Additionally, the Hill Climbing algorithm is implemented to realize Maximum Power Point Tracking (MPPT) for the PV system. The feasibility of the design is assessed through MATLAB/Simulink simulations and verified experimentally using a hardware prototype under diverse operating scenarios.**

***Index Terms*— Renewable Energy Resources, T-Source Converter, Hill Climbing Algorithm, Maximum Power Point Tracking, Dual-Input Dual-Output Converters.**

I. Introduction

Due to their dependence on environmental conditions, photovoltaic (PV) systems exhibit high volatility, making them unable to satisfy load requirements during night hours, early mornings, or cloudy periods [1,2]. To mitigate these reliability issues, PV units are frequently coupled with energy storage systems (ESS) or auxiliary power generator [3] to form hybrid energy systems. These configurations combine multiple energy sources—not necessarily restricted to renewables—and typically feature units capable of bidirectional power flow [4]. Consequently, PV-battery hybrid systems have received significant research attention [5-9]. Utilizing multi-input converters (MICs) [10] as the grid/load interface in such hybrid setups offers a pathway to enhance overall system efficiency and operating performance [11].

Historically, MICs are divided into two primary architectures. The first approach, shown in Fig. 1(a), employs dedicated DC-DC (buck or boost) stages for each input source, which are subsequently connected to a shared DC bus. The main drawbacks of this decoupled layout are the elevated capital costs due to the redundant power stages and the increased complexity of managing multiple independent control loops. To address these shortcomings, integrated MIC topologies have been developed. As shown in Fig. 1(b), this paradigm replaces individual converters with a single, unified power stage. By sharing core components among the input ports, this integrated design reduces system cost, optimizes component utilization, and yields a more compact and lightweight system. Hence, integrated MICs have become highly attractive for modern applications owing to their reduced component count and high-power density [12,13].

S. Zare, A. Rajaei, M. Karimianfard, are with the Department of Electrical Engineering, Shiraz University of Technology, Shiraz, 13876-71557, I.R. Iran (e-mails: s.zare@sutech.ac.ir, a.rajaei@sutech.ac.ir, m. karimianfard@sutech.ac.ir).

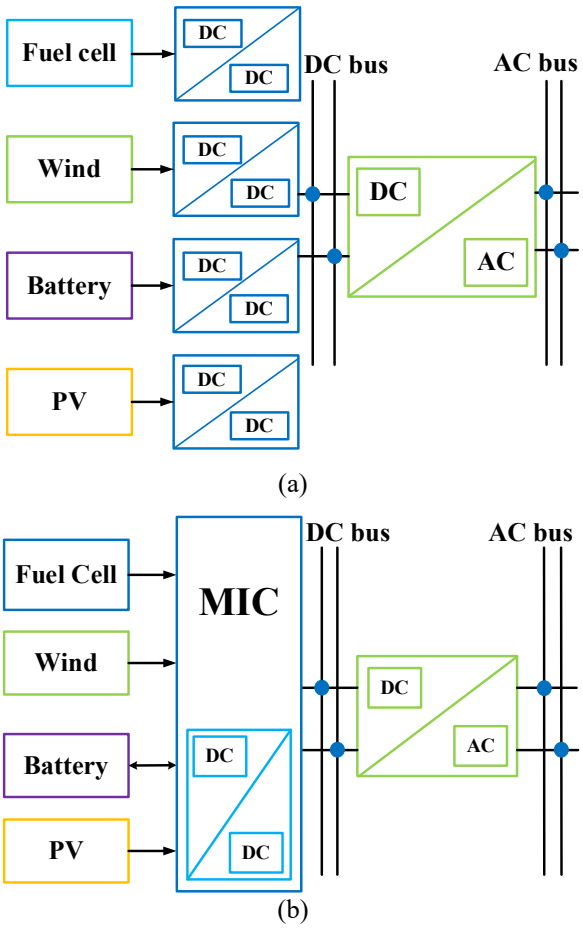


Fig. 1. Multi-input converters; (a) Unified converter for each input (b) Single unified converter for inputs

Compared to using multiple discrete converters, the key benefits of multi-input converters (MICs) include:

- Lower component count
- Streamlined control implementation
- Improved system stability
- Minimized power losses
- Reduced physical volume and mass

Physically, MICs are categorized into three main structural types: magnetically coupled configurations [14], electrically coupled topologies [15,16], and isolated architectures employing a single primary winding [17], as detailed below.

Magnetically Coupled Multi-Input Converters: Under this architecture, the magnetic flux generated by different input sources is merged via multi-winding transformers [14]. According to Ampere's law, the excitation currents in the primary windings induce a magnetic flux in the shared core, which subsequently induces a voltage across the secondary winding. The multi-input full-bridge topology is a classic example of this category. The main benefits of these magnetically coupled systems include:

- Adaptability to highly diverse input DC voltage levels.
- Capability for concurrent or independent power transfer from the sources to the load.
- Integration of soft-switching techniques (ZVS and ZCS).
- Electrical/galvanic isolation.

Electrically Coupled Multi-Input Converters [18]: These configurations do not utilize a high-frequency transformer. The six basic non-isolated topologies—buck, boost, buck-boost, Cuk, Zeta, and Sepic—form the foundation of this class [15, 16]. As shown in Fig. 2, these structures are partitioned into three primary functional blocks: the Input Port (IP), the Output Port (OP), and the Energy Buffer Port (EBP).

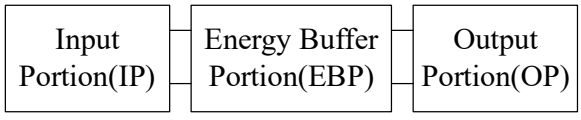


Fig. 2. Main functional stages of a PWM converter.

Based on the electrical nature of the output port, these converters are subdivided into:

- *Pulsating Voltage Source Converters (PVSCs):* When the output stage is interfaced through an inductor, the load behaves as a dependent current source. A freewheeling diode is placed in parallel with this dependent current source. The buck, Cuk, and Zeta configurations fall into this category.
- *Pulsating Current Source Converters (PCSCs):* When the output stage features a capacitive filter, the load is represented as a dependent voltage source. Here, a diode is placed in series with the dependent voltage source, resulting in a pulsating output current.

Designing MICs involves integrating these PVSC and PCSC concepts within standard PWM converter topologies.

Multi-Input Converters Featuring a Single Primary Winding: In traditional magnetically coupled MICs, each input source requires its own dedicated primary winding, which shares a common secondary. However, scaling up the number of input sources adds physical complexity to the transformer [19]. This increase in primary windings raises the leakage inductance, leading to higher power dissipation and severe voltage spikes across the active switches [20]. To overcome these limitations, modern isolated MICs employ a single primary winding (SPW) configuration [17]. The SPW approach reduces switch voltage stress and leakage flux, making the system highly scalable for multiple input sources.

II. Proposed Dual-Input Dual-Output Converter Topology and its Steady-State Analysis

The derivation methodology for the proposed converter topology is detailed in this section. Figure 3 illustrates the baseline structure of a conventional T-source converter [21,22]. The design objective centers on embedding an electrically coupled DC-DC stage within this T-source framework. This integration is feasible through two primary methods: either by interfacing a PVSC-based circuit (such as a Buck, Zeta, or Cuk topology) with the coupled inductor, or by incorporating a PCSC-based configuration (such as a Boost, Buck-Boost, or Sepic circuit) across the capacitor. In this study, a boost converter—categorized as a PCSC—is chosen to be integrated with the T-source capacitor to form the proposed architecture.

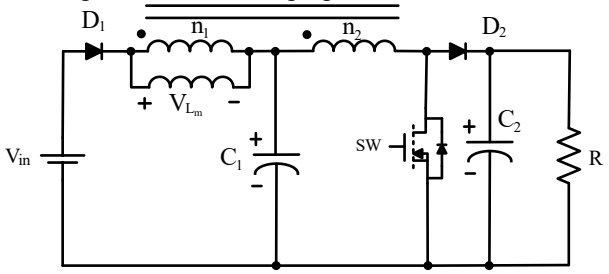
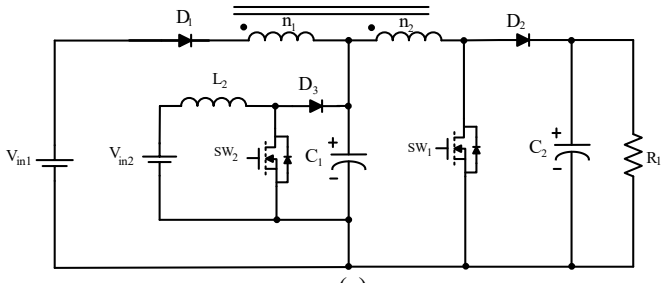


Fig. 3. Schematic of the conventional single input-single output T-source Converter [21].

As illustrated in Fig. 4, a boost-based parallel-capacitor switching cells (PCSC) stage is connected across the capacitor of the T-source network, following standard PCSC design rules. To facilitate bidirectional energy exchange for the battery port during both charge and discharge states, a controllable active switch replaces the traditional boost diode.

Furthermore, an isolated auxiliary output is established by integrating a tertiary winding into the high-frequency magnetic core of the T-source coupled inductor. As shown in Fig. 4, this winding configuration, coupled with two diodes and two capacitors, powers an auxiliary load to form a dual-input dual-output (DIDO) topology. While the primary output voltage is directly stabilized by the closed-loop controller, the auxiliary output voltage is naturally dependent on the primary port. If independent regulation of this auxiliary port is required, an auxiliary switching stage can be integrated as depicted in Fig. 4. Lastly, continuous battery current during charge/discharge modes is ensured by placing an active switch and an interface inductor in series with the battery terminal. The complete schematic of the proposed converter is detailed in Fig. 4(c).



(a)

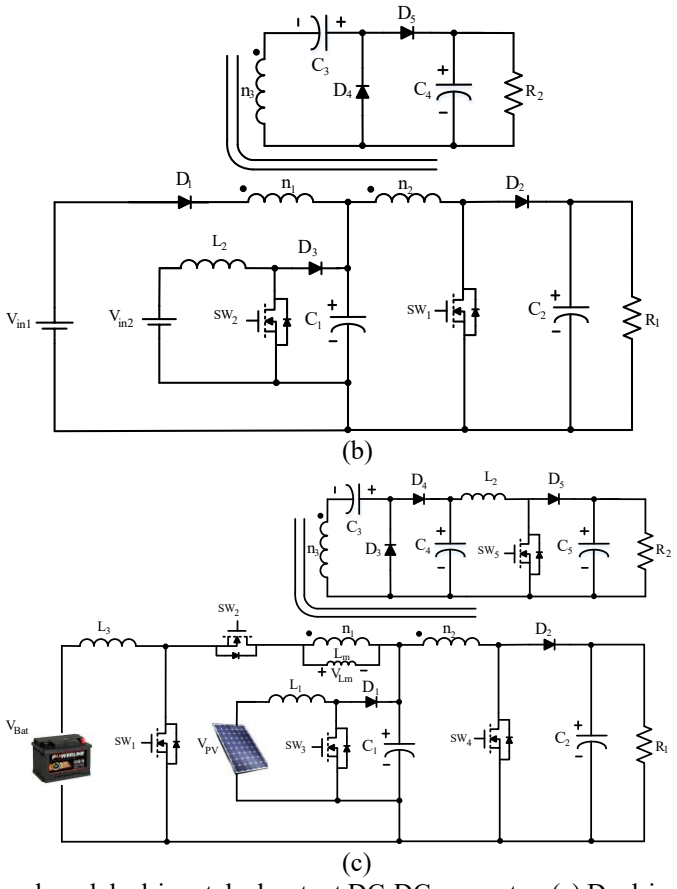
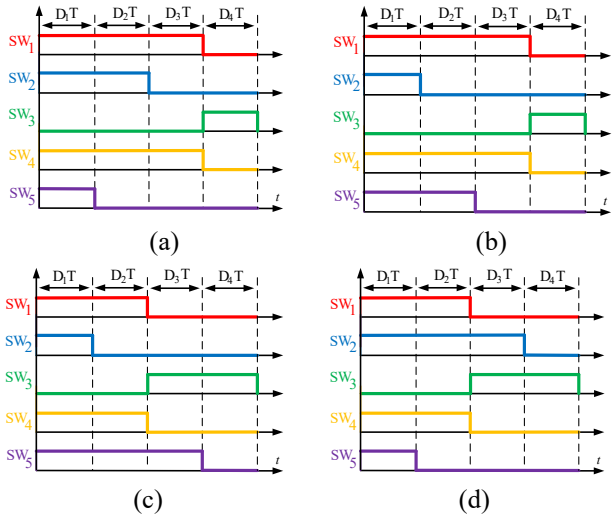
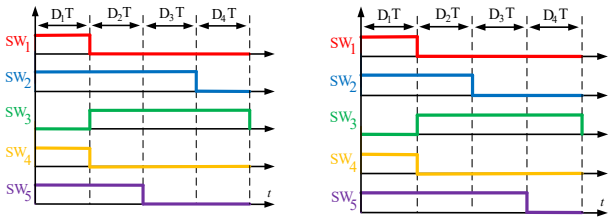


Fig. 4. Proposed topology T-source-based dual-input dual-output DC-DC converter; (a) Dual-input T-source network with a boost converter integrated across the capacitor C_1, (b) Dual-input dual-output structure with an unregulated output (c) Dual-input dual-output structure with regulated outputs and featuring continuous current and independent control of both outputs.

The proposed converter is developed around a T-source impedance network, which imposes a fixed assignment for the PV and battery ports. These two input connections cannot be exchanged because the PV voltage may fall to nearly zero at night or under heavily overcast conditions. Such a connection reversal would disturb the intended energy-transfer mechanism and could prevent the converter from operating properly.

As shown in Fig. 5, the converter has six possible switching modes. The corresponding switching intervals are represented by the duty ratios D_1, D_2, D_3, and D_4, which satisfy $D_4 = 1 - (D_1 + D_2 + D_3)$. In each mode, switches $SW_1$and $SW_4$are operated synchronously, whereas SW_3 is driven complementarily. The gating signals of SW_2 and SW_5 are determined according to the operating condition. Differences in their conduction intervals consequently produce the six distinct switching states shown in Fig. 5.

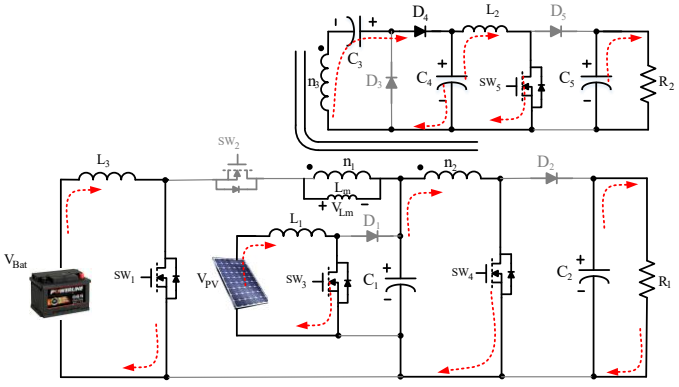




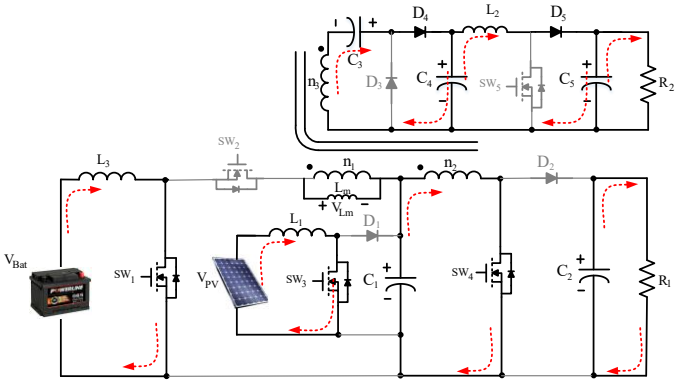
(e) (f)

Fig. 5. Different switching modes of operation for the proposed DIDO converter.

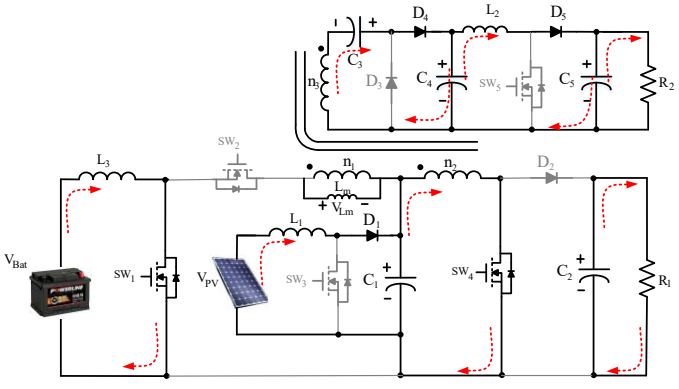
The mathematical formulations describing the circuit behavior in the first operational interval (State I) are formulated herein. Additionally, the equivalent circuit topology and the corresponding current flow routes during this specific interval are depicted in Fig. 6.



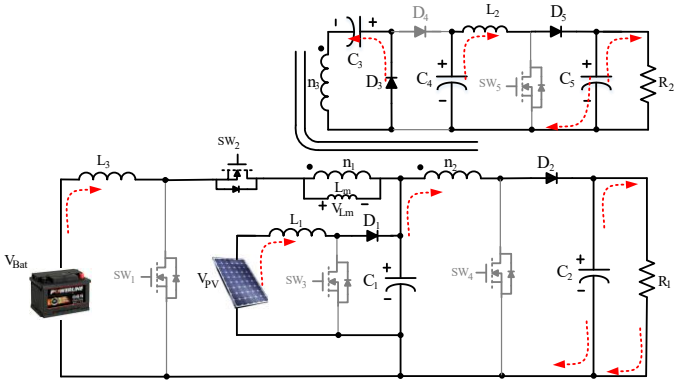
(a)



(b)



(c)



(d)

Fig. 6. Circuit diagram and the current paths during different switching states; a) state I, b) state II, c) state III, d) state IV.

State I: The circuit relations for the first switching interval are obtained from the equivalent topology shown in Fig. 6(a). During this interval, SW_3 remains in the OFF state, whereas SW_1, SW_2, SW_4, and SW_5 are simultaneously gated ON.

$$v_{L_1} = V_{bat} \tag{1}$$

$$v_{L_2} = V_{pv} \tag{2}$$

$$v_{L_3} = v_{C_4} \tag{3}$$

$$v_{L_m} = \frac{n_1}{n_2} v_{C_1} \tag{4}$$

$$i_{C_1} = -i_X \tag{5}$$

$$i_{C_2} = -\frac{v_{C_2}}{R_1} \tag{6}$$

$$i_{C_3} = \frac{1}{n_3}\left(n_1 I_{L_m} - n_2 I_X\right) \tag{7}$$

$$i_{C_4} = -i_{L_3} - \frac{1}{n_3}\left(n_1 I_{L_m} - n_2 I_X\right) \tag{8}$$

$$i_{C_5} = -\frac{v_{C_5}}{R_2} \tag{9}$$

By applying Kirchhoff's Voltage Law (KVL) to the third winding stage, the following auxiliary equation is obtained:

$$-V_{C_4} + V_{C_3} + \frac{n_3}{n_2} V_{C_1} = 0 \tag{10}$$

State II: The governing equations of the circuit during the second switching state, depicted in Fig. 6(b), are analyzed. In this operational mode, the power switches SW_1, SW_2, and SW_4 are turned on, whereas the switches SW_3 and SW_5 are turned off.

$$v_{L_1} = V_{bat} \tag{11}$$

$$v_{L_2} = V_{pv} \tag{12}$$

$$v_{L_3} = v_{C_4} - v_{C_5} \tag{13}$$

$$v_{L_m} = \frac{n_1}{n_2} v_{C_1} \tag{14}$$

$$i_{C_1} = -i_X \tag{15}$$

$$i_{C_2} = -\frac{v_{C_2}}{R_1} \tag{16}$$

$$i_{C_3} = \frac{n_1}{n_3} i_{L_m} - \frac{n_2}{n_3} I_X \tag{17}$$

$$i_{C_4} = -i_{L_3} - \frac{n_1}{n_3} i_{L_m} + \frac{n_2}{n_3} i_X \tag{18}$$

$$i_{C_5} = i_{L_3} - \frac{v_{C_5}}{R_2} \tag{19}$$

State III: The circuit equations for the second switching interval are derived from the equivalent configuration shown in Fig. 6(b). In this mode, SW_1, SW_2, and SW_4 are ON, while SW_3 and SW_5 are OFF.

$$v_{L_1} = V_{bat} \tag{20}$$

$$v_{L_2} = V_{pv} - V_{C_1} \tag{21}$$

$$v_{L_3} = V_{C_4} - V_{C_5} \tag{22}$$

$$v_{L_m} = \frac{n_1}{n_2} V_{C_1} \tag{23}$$

$$i_{C_1} = i_{L_2} - I_X \tag{24}$$

$$i_{C_2} = -\frac{v_{C_2}}{R_1} \tag{25}$$

$$i_{C_3} = \frac{n_1}{n_3} i_{L_m} - \frac{n_2}{n_3} I_X \tag{26}$$

$$i_{C_4} = -i_{L_3} - \frac{n_1}{n_3} i_{L_m} + \frac{n_2}{n_3} I_X \tag{27}$$

$$i_{C_5} = i_{L_3} - \frac{v_{C_5}}{R_2} \tag{28}$$

$$i_{bat} = i_{L_3} \tag{29}$$

State IV: The converter dynamics in the fourth switching interval are obtained using the equivalent circuit shown in Fig. 6(d). In this state, SW_3 is gated ON, while SW_1, SW_2, SW_4, and SW_5 remain OFF.

$$v_{L_1} = V_{bat} - v_{C_1} - v_{L_m} \quad = V_{bat} - V_{C_1} - \frac{n_1}{n_2}\left(v_{C_1} - v_{C_2}\right) \tag{30}$$

$$v_{L_2} = -r_{PV} i_{in2} + v_{in2} - v_{C_1} \tag{31}$$

$$v_{L_3} = v_{C_4} - v_{C_5} \tag{32}$$

$$v_{L_m} = \frac{n_1}{n_2}\left(v_{C_1} - v_{C_2}\right) \tag{33}$$

$$i_{C_1} = i_{L_1} + i_{L_2} - i_Y \tag{34}$$

$$i_{C_2} = I_Y - \frac{V_{C_2}}{R_1} \tag{35}$$

$$i_{C_3} = -\frac{n_1}{n_3}\left(i_{L_1} - i_{L_m}\right) - \frac{n_2}{n_3} I_Y \tag{36}$$

$$i_{C_4} = -i_{L_3} \tag{37}$$

$$i_{C_5} = -\frac{v_{C_5}}{R_2} \tag{38}$$

Under steady-state conditions, the average inductor currents and capacitor voltages are obtained by applying the inductor volt–second balance (IVSB) and capacitor charge balance (CCB) principles, as expressed below:

$$V_{C_1} = \frac{n_2 V_{bat}}{n_2 D_4 - n_1(1 - D_4)} \tag{39}$$

$$V_{C_2} = V_{o1} = \frac{V_{C_1}}{D_4} \tag{40}$$

$$V_{C_3} = \frac{n_3}{n_2}\left(V_{C_2} - V_{C_1}\right) \tag{41}$$

$$V_{C_4} = \frac{n_3}{n_2} V_{C_1} + V_{C_3} \tag{42}$$

$$V_{C_5} = V_{o2} = \frac{V_{C_4}}{1 - D_1} \tag{43}$$

$$I_Y = \frac{V_{C_2}}{R_1 D_4} \tag{44}$$

$$I_{L_3} = \frac{V_{C_5}}{R_2(1-D_1)} \tag{45}$$

$$I_X = \frac{\frac{n_3 I_{L_3}}{(1-D_4)} + (n_1+n_2) I_Y D_4 - n_1 I_{L_2}(D_3+D_4)}{n_2 - (n_1+n_2)(1-D_4)} \tag{46}$$

$$I_{L_1} = \frac{I_X(1-D_4) + I_Y D_4 - I_{L_2}(D_3+D_4)}{D_4} \tag{47}$$

$$I_{L_m} = \frac{n_2 I_X(1-D_4) - n_3 I_{L_3}}{n_1(1-D_4)} \tag{48}$$

III. Converter Design, Capacitor and Inductance Selection

A. Design of passive elements

The boundary conditions for the converter inductance and capacitance values are defined by their respective peak-to-peak current and voltage ripple requirements. Based on these design criteria, the minimum parameters for L and C are computed as follows:

$$L_1 = \frac{V_{Bat} D_{onSW1(\max)}}{2\Delta I_{L1} f} \tag{49}$$

$$L_2 = \frac{V_{in2} D_{onSW2(\max)}}{2\Delta I_{L2} f} \tag{50}$$

$$L_m = \frac{V_{Lm} D_{onSW1(\max)}}{2\Delta I_{Lm} f} \tag{51}$$

$$C_1 = \frac{-I_X D_{onsw2} + \left(I_{L_2} - I_X\right)\left(D_{onsw1} - D_{onsw2}\right)}{2\Delta V_{C_1} f} \tag{52}$$

$$C_2 = \frac{V_{C_2} D_{onsw1}}{2\Delta V_{C_2} f R_1} = \frac{I_{o_1} D_{onsw1}}{2\Delta V_{C_2} f} \tag{53}$$

$$C_3 = \frac{-\left(\frac{n_1}{n_3} I_{L_m} - \frac{n_2}{n_3} I_X\right) D_{onsw1}}{2\Delta V_{C_3} f} \tag{54}$$

$$C_4 = \frac{\left(-\frac{V_{C_4}}{R_2} - \frac{n_1}{n_3} I_{L_m} + \frac{n_2}{n_3} I_X\right) D_{onsw1}}{2\Delta V_{C_4} f} \tag{55}$$

B. Controller design

As illustrated by the V-I and P-V profiles of the photovoltaic source in Fig. 7, a maximum power point tracking (MPPT) algorithm is indispensable for maximizing the conversion efficiency of the PV system. This necessity arises because the maximum power point (MPP) fluctuates continuously under the influence of environmental factors, including solar irradiance, operating temperature, and the solar incidence angle defined by the Kelly cosine relation [23-25].

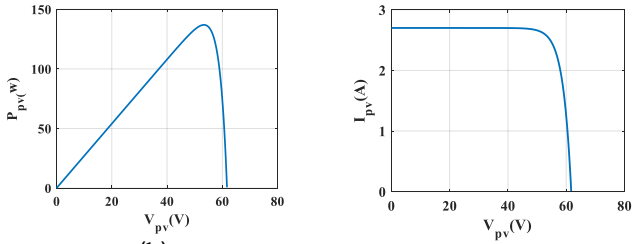


Fig. 7. Characteristics of the modeled PV panel ;(a) I-V characteristic, b) P-V characteristic.

The Hill Climbing technique is adopted in this study for maximum power point tracking, with the corresponding algorithmic steps outlined in Fig. 8. This method operates by directly adjusting the converter duty cycle. Specifically, the PV voltage and current are sampled to compute the instantaneous PV power. By evaluating the changes in power and voltage relative to their prior values, the algorithm determines the direction of the duty-cycle step according to the decision path in Fig. 8. For example, a simultaneous power increase and voltage decrease dictates a reduction in the duty-cycle increment. The simulation parameters are configured with a starting duty cycle of 48%, a step change (ΔD) of 0.5%, and an update frequency of 10 Hz.

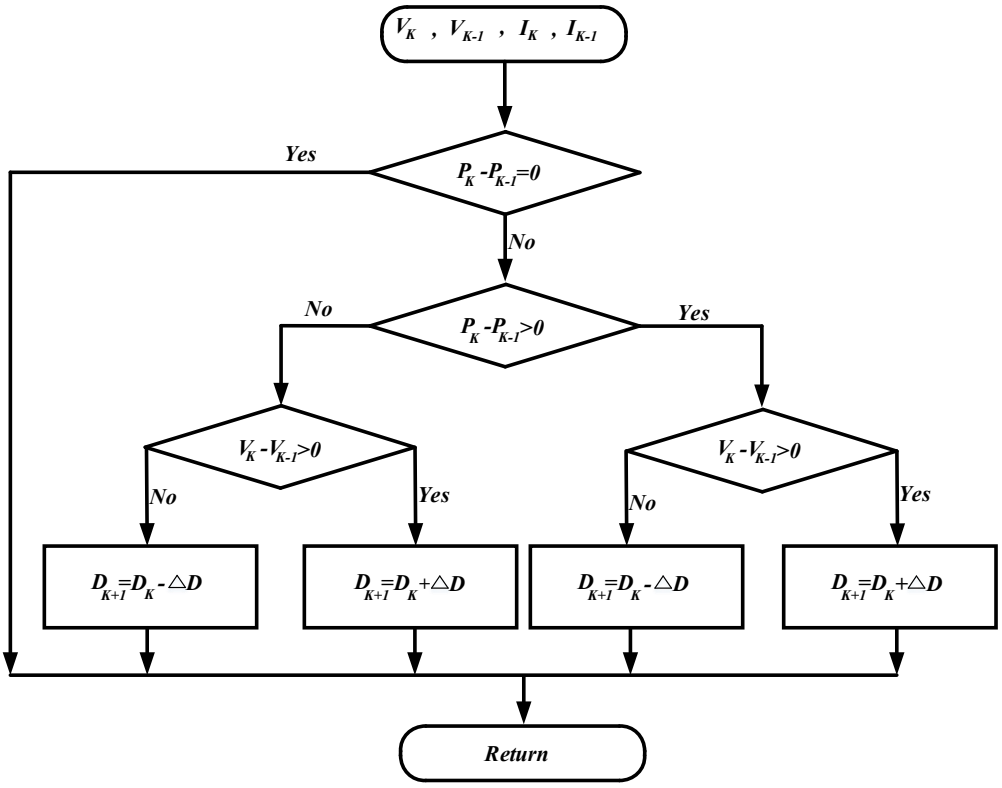


Fig. 8. The flowchart for the MPPT Hill Climbing method [26].

A sliding-mode controller (SMC) is employed as the inner control loop to regulate the output voltage. Its design follows a systematic procedure. In accordance with the control objective of this study, the main output voltage, V_{O1}, is regulated through the switching action of S_1. The design and implementation procedure of the proposed SMC are described in the following.

First, a sliding manifold must be constructed such that the output-voltage tracking error converges to zero. For the second-order system considered here, whose state variables include the output voltage and inductor current, the sliding surface $S(t)$ is defined as:

$$S = k_1(v_{o1} - v_{o1}^*) + k_2 \int (v_{o1} - v_{o1}^*)dt + \frac{d(v_{o1} - v_{o1}^*)}{dt} \tag{56}$$

v_{o1}^* is the reference value of the output voltage. $k_1$and k_2 are the design coefficients adjusted for corresponding response time and the stability purpose.

The next step is deriving the state-space equations. To implement the SMC, the system dynamics are required for each switching interval. Since the converter operates across six distinct switching states, the state-space model is derived using the average technique upon all the switching states and expressed as follows:

$$\dot{x} = A_k x + B_k u \tag{57}$$

where, x is the state vector (comprising the inductor currents and capacitor voltages), and u represents the control signal (the duty cycle of switch S_1).

Control Law: The control law comprises in two components: the equivalent control (to maintain the system trajectories on the sliding surface) and the switching control (to guarantee robustness and disturbance rejection):

$$u = u_{eq} + u_n \tag{58}$$

where u_{eq} is the equivalent Control Component obtained by setting $\dot{S}(t) = 0$ in the state-averaged model. This component calculates the nominal duty cycle required for voltage regulation. Nonlinear Control Component (u_n) is added to mitigate modeling uncertainties and external disturbances (such as load variations or fluctuations in PV voltage).

$$u_n = K \cdot sat\left(\frac{S}{\phi}\right) \tag{59}$$

where, K is the switching gain and sat $\left(\frac{S}{\phi}\right)$ is the saturation function implemented to eliminate the chattering phenomenon (high-frequency oscillations) in the control output.

The schematic of the controller system employing MPPT as inner-loop control and SMC as outer-loop controller is shown in Fig. 9.

V. Simulation And Experimental Results

To evaluate the performance and verify the viability of the proposed converter, a laboratory prototype was constructed (as shown in Fig. 10) and subjected to diverse experimental scenarios. This section presents the experimental outcomes and compares them with both the theoretical predictions and simulation results. The electrical specifications of the converter, which are identical for both the simulation model and the physical prototype, are summarized in Table I.

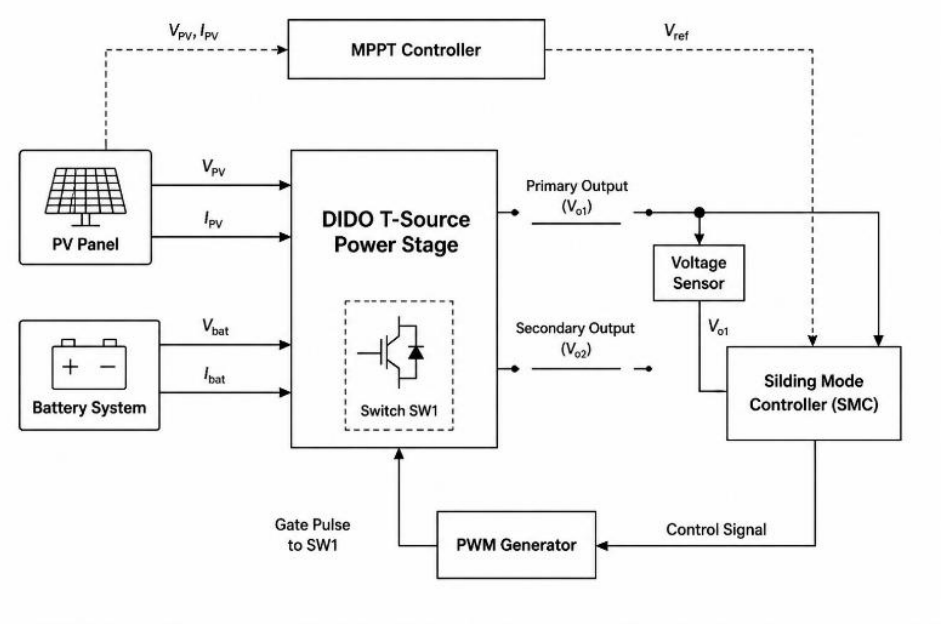
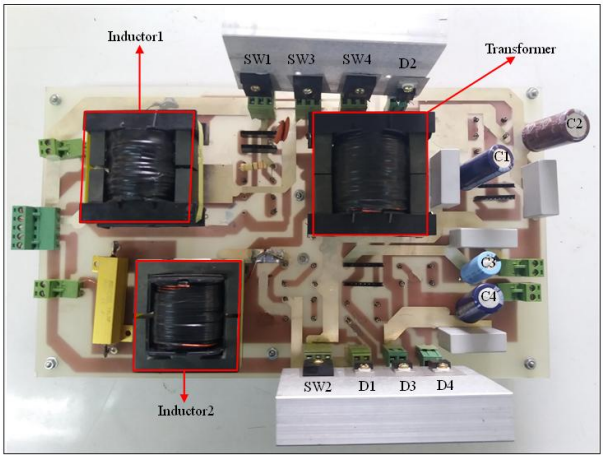
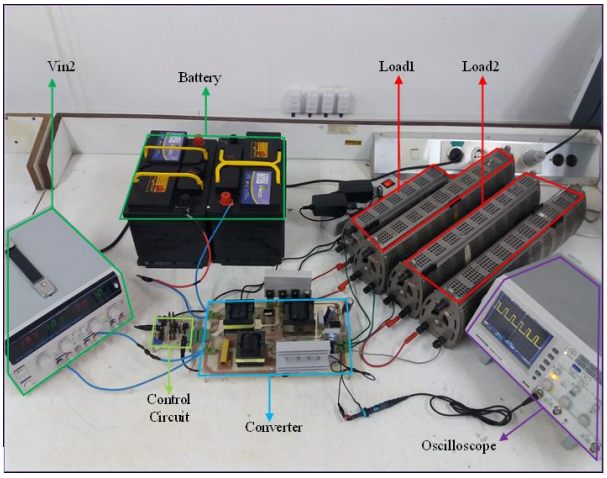


Fig. 9. The schematic of the controller system for the proposed converter.



(a)



(b)

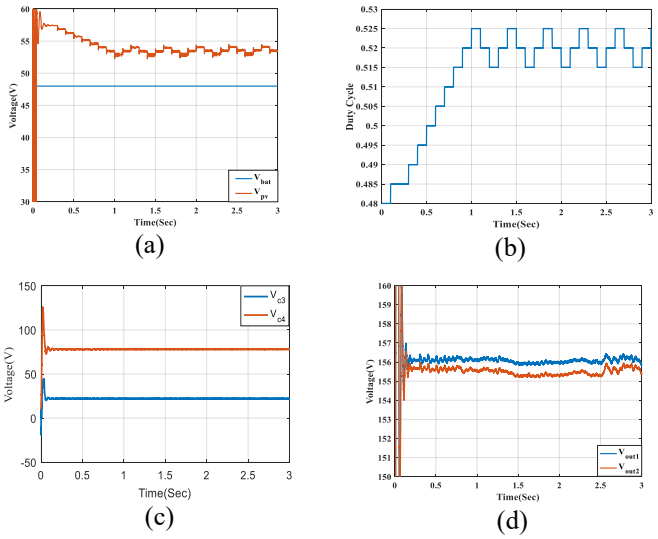
Fig. 10. The experimental set up for the proposed converter. a) The converter prototype, b) test set up.

Table I

SPECIFICATIONS OF THE LABORATORY PROTOTYPE USED FOR EXPERIMENTAL TESTS AND SIMULATIONS.

Parameters	Symbol	Value
Battery voltage	V_{bat}	24V
PV voltage	V_{PV}	36.5V
PV current	I_{PV}	3.5A
Turns ratio-first winding	n_1	1
Turns ratio-second winding	n_2	1
Turns ratio-third winding	n_3	1.3
First load resistance	R_1	160 Ω
Second load resistance	R_2	240 Ω
Switching frequency	f_s	20 kHz
Capacitance	$C_i, i = 1, \ldots, 5$	220μF
Magnetizing inductance	L_m	100 μH
inductance	$L_i, i = 1, \ldots, 3$	200 μH

MPPT algorithm is implemented in the simulations, which the results are shown in Fig. 11. The results show that the algorithm effectively tracks the MPP using the proposed converter.



(a) (b)

(c) (d)

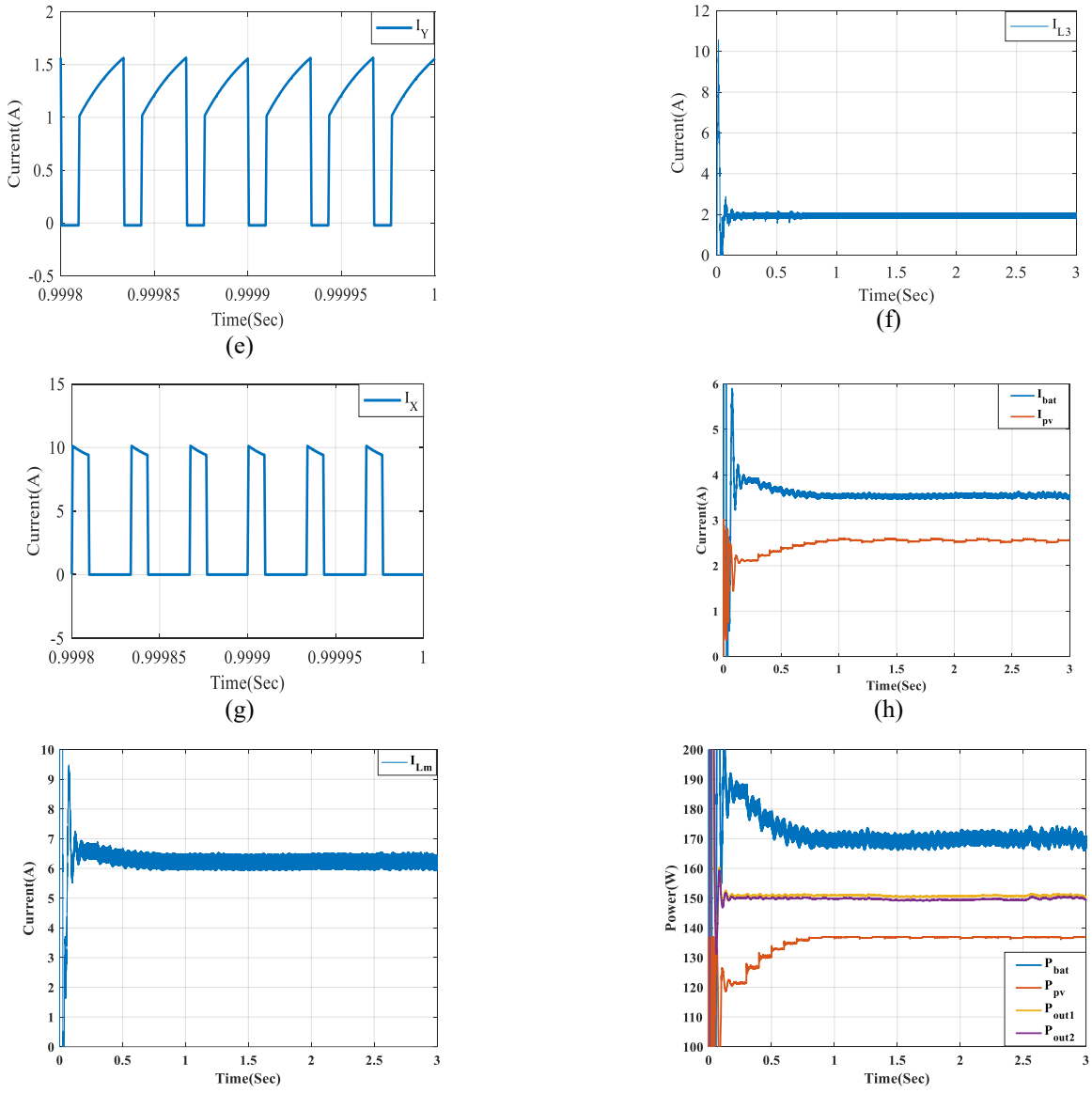
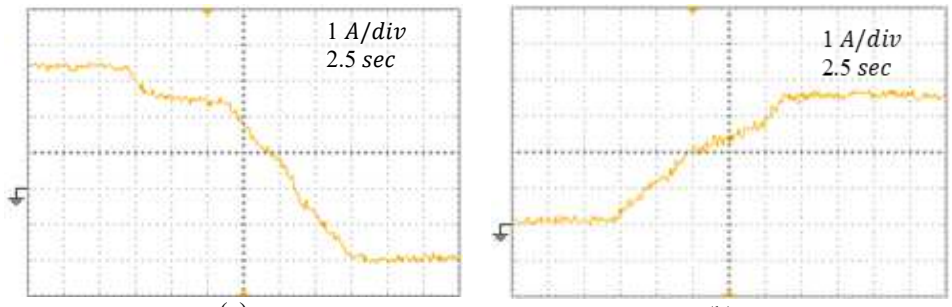


Fig. 11. Simulation results: (a) battery voltage and PV panel voltage, (b) duty cycle variation of switch S_1 for MPP tracking, (c) voltages across capacitors C_1 and C_2, (d) output load voltages, (e) switch S_1 current, (f) inductor L_1 current, (g) diode D_1 current, (h) battery current and PV panel current, (i) magnetizing current I_m, and (j) output load powers, battery power, and PV panel power.

Test Scenario I: In this test, the battery initially supplies the entire load demand, while the power contribution of the PV source is gradually increased by raising the duty ratio of SW_2. The transient response of the battery current is shown in Fig. 12(a). At the beginning of the test, the battery delivers approximately 3.4 A. As the PV array starts contributing power, the battery current decreases and reaches -1.9 A, thereby confirming a transition from the discharge mode to the charging mode.

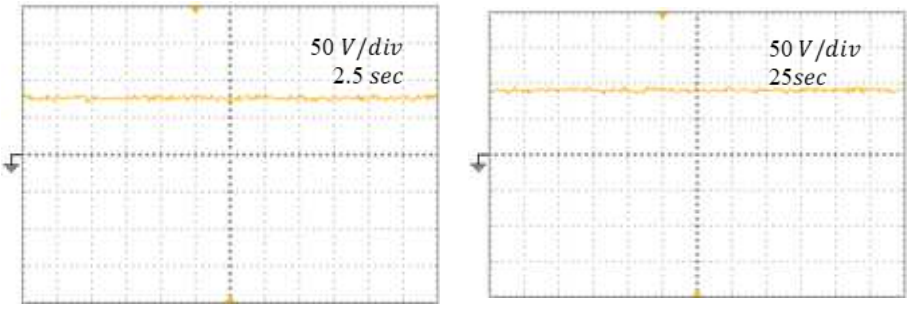
The associated PV current waveform is provided in Fig. 12(b). Initially, the PV current is zero; however, it progressively increases to 3.6 Aas the duty cycle of SW_2 is increased. Meanwhile, a closed-loop controller acting on SW_1 maintains the regulated output voltages despite the changes in input power sharing. Figure 13 depicts the output-capacitor voltages during the SW_2duty-cycle ramp. Their nearly constant values demonstrate the effectiveness and robustness of the proposed feedback controller.

At the end of this scenario, the duty ratio of SW_2 becomes greater than that of SW_1. A magnified time-scale comparison between the simulated and experimental PV currents is presented in Fig. 14, where the switching-frequency ripple is observable.



(a) (b)

Fig. 12. The Simulation and experimental results in the first test scenario for (a) battery current variation, (b) PV panel current variation



(a) (b)

Fig. 13. The experimental results in the first test scenario for the output voltages, a) C_2 Voltage, b) C4 Voltage.

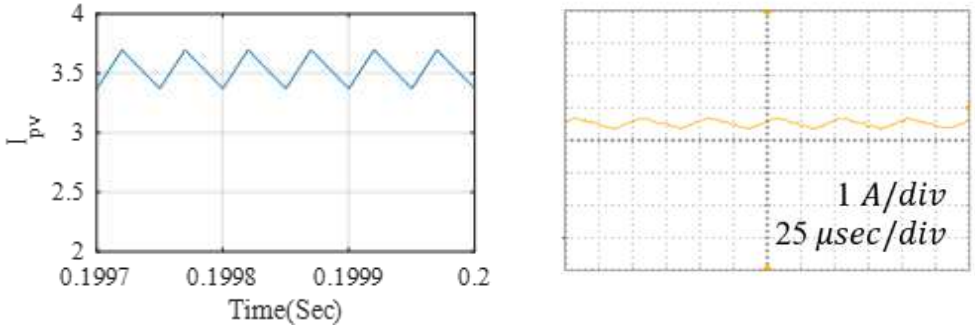


Fig. 14. The Simulation and experimental results in the first test scenario for PV current.

The finalized quantitative results are summarized below. By employing the steady-state formulations developed in Section II, the voltage levels across capacitors C_1, C_2, C_3, and C_4 are calculated. A comparison of these calculated values with the corresponding simulation and experimental waveforms is presented in Fig. 15.

$$V_{C_1} = \frac{1 \times 24}{1 \times 0.74 - 1 \times 0.26} = 50V$$

$$V_{C_2} = \frac{V_{C_1}}{D_{offsw1}} = \frac{50}{0.74} = 67.56\,V$$

$$V_{C_3} = \frac{n_3}{n_2}\left(V_{C_2} - V_{C_1}\right) = \frac{1.3}{1}(67.56 - 50) = 22.8\,V$$

$$V_{C_4} = \frac{n_3}{n_2}V_{C_1} + V_{C_3} = \frac{1.3}{1} \times 50 + 22.8 = 87.8V$$

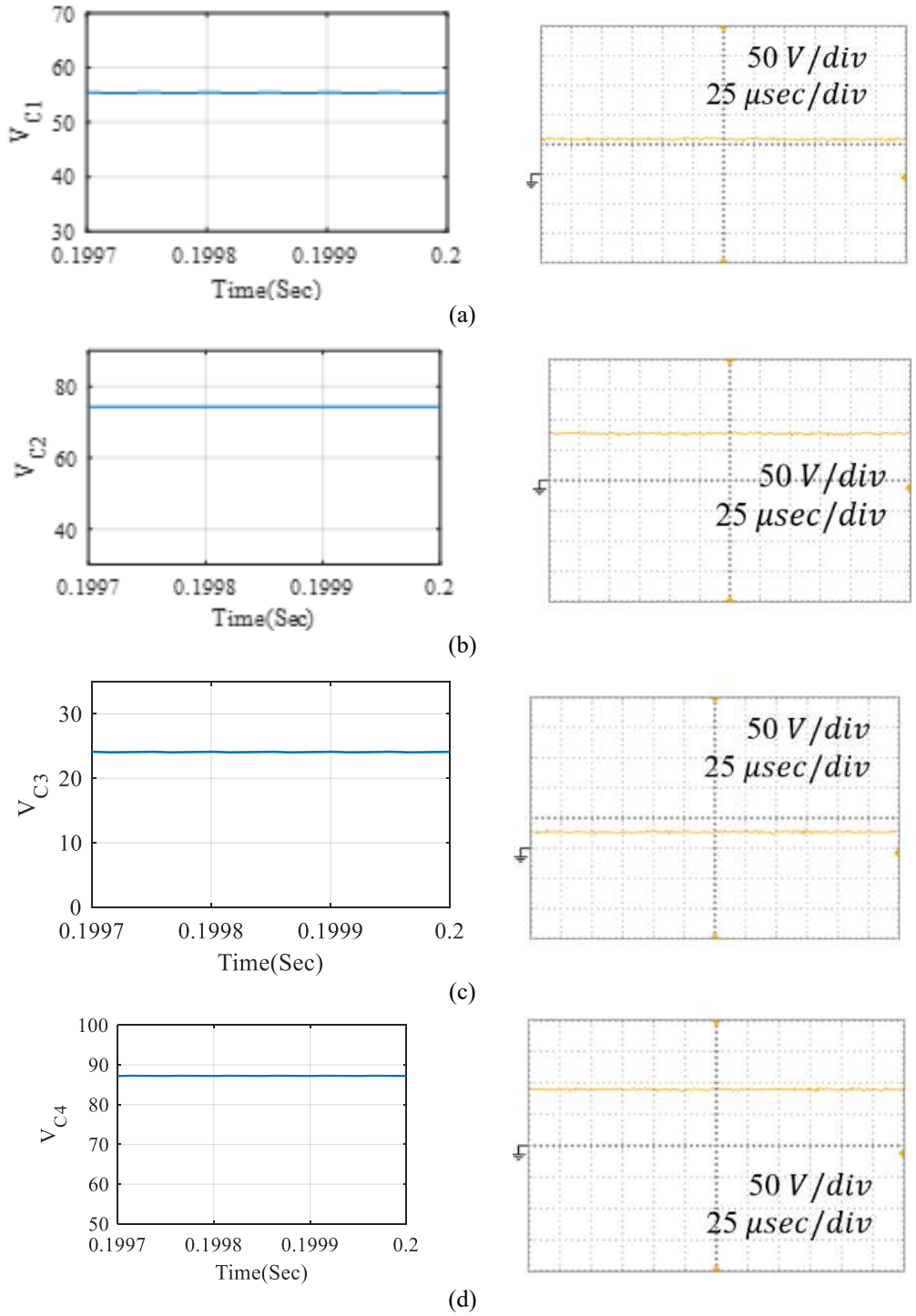


Fig. 15. The Simulation and experimental results in the first test scenario for capacitor voltage; (a) V_{C1} (b) V_{C2} , (c) V_{C3} , (c) V_{C4}

Using the theoretical analysis, the currents are calculated as follows:

$$I_Y = \frac{V_{C_2}}{R_1 D_{offsw4}} = \frac{67.56}{160 \times 0.74} = 0.57 \ A$$

$$I_X = \frac{\frac{n_3 V_{C_4}}{R_2 D_{onsw1}} + (n_1 + n_2) I_Y D_{offsw1} - n_1 I_{L_2} D_{offsw2}}{n_2 - (n_1 + n_2) D_{onsw1}} = \frac{\frac{1.3 \times 87.8}{240 \times .026} + (1+1)0.57 \times 0.74 - 1 \times 3.5 \times 0.6}{1 - (1+1) \times 0.26} = 1.19 \ A$$

$$I_{L_m} = \frac{1 \times 1.19 \times 0.26 - \frac{1.3 \times 87.8}{240}}{1 \times 0.26} = -0.64A$$

$$I_{L_1} = \frac{1.19 \times 0.26 + 0.57 \times 0.74 - 3.5 \times 0.6}{0.74} = -1.85A$$

The voltage across L_1 is also given by:

$V_{L_1} = V_{bat} = 24V$ (positive half cycle)

$V_{L_1} = -\frac{1}{1} \times (50 - 67.56) - 50 + 24 = -8.5V$ (negative half cycle)

The simulation and experimental results for i_{L1} and v_{L1} are shown in Fig. 16(a) and Fig. 16(b) respectively which match the theoretical results.

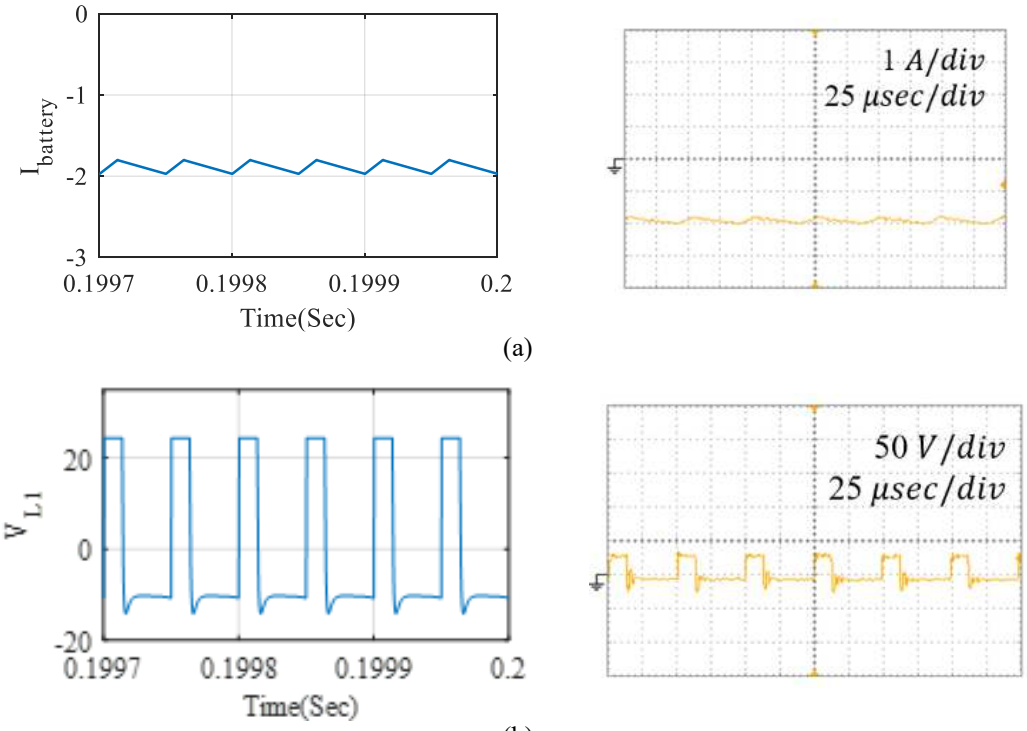


Fig. 16. The simulation and experimental results for a) i_{L1} (equals to the battery current), b) v_{L1} .

The voltage across inductor L_2 during different switching cycles are calculated as follows, which the results for simulation and experiments are shown in Fig. 17. The experimental results validate the theoretical and simulation findings, showing good agreement.

$V_{L2} = V_{PV} = 36.5$ (positive half cycle)

$V_{L_2} = -24.33V$ (negative half cycle)

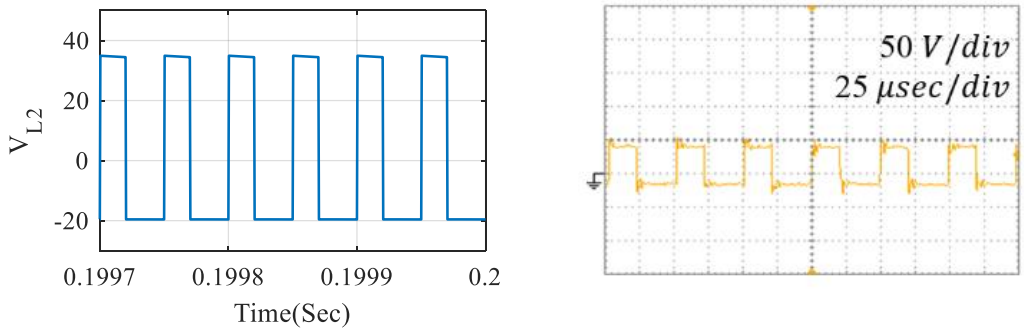


Fig. 17. The simulation and experimental results for L_2 voltage.

The values of voltage stress on the power semiconductor devices are expressed as:

$$V_{SW1} = \frac{1}{1}(50 - 67.56) + 50 = 32.44V$$

$$V_{SW2} = V_{C_1} = 50V$$

$$V_{SW3} = \frac{n_1}{n_2}(V_{C_1}) + V_{C_1} = \frac{1}{1}(50) + 50 = 100V$$

$$V_{SW4} = V_{C_2} = 67.56V$$

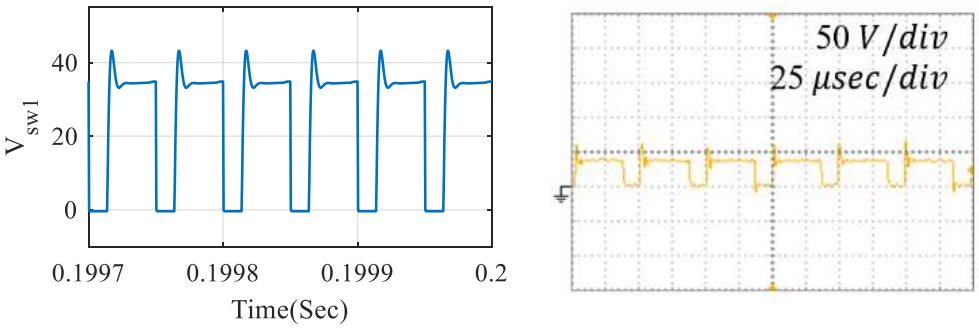
$$V_{D_1} = V_{C_1} = 50V$$

$$V_{D_2} = V_{C_2} = 67.56V$$

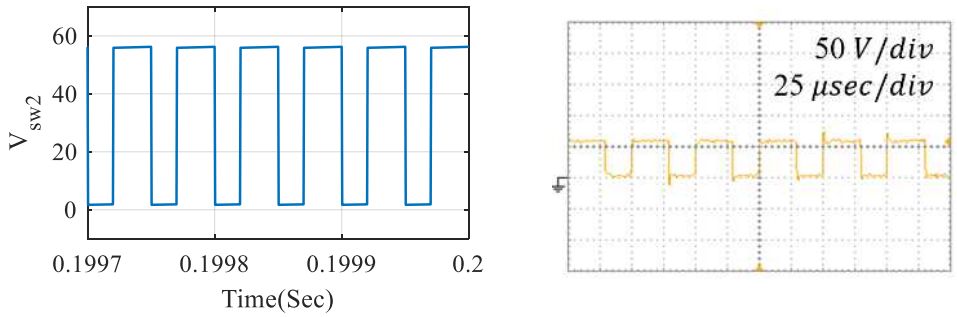
$$V_{D_3} = V_{C_4} = 87.8V$$

$$V_{D_4} = V_{C_4} = 87.8V$$

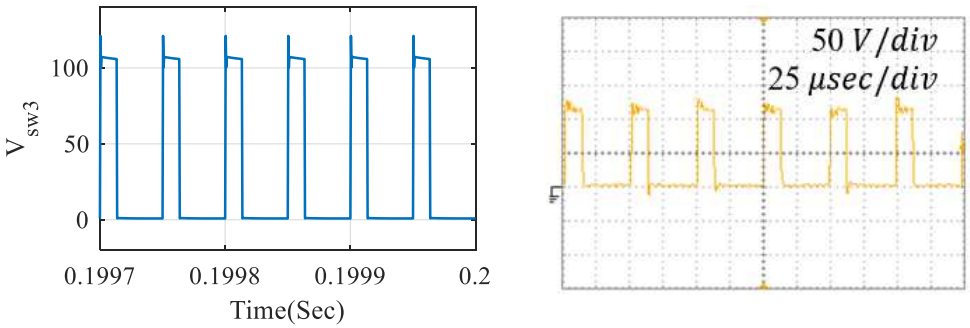
Comparing these values with the simulation and experimental results (Fig. 18) shows good consistency and validate the theoretical analysis.



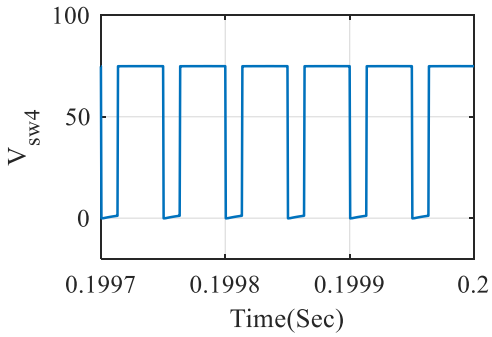
(a)

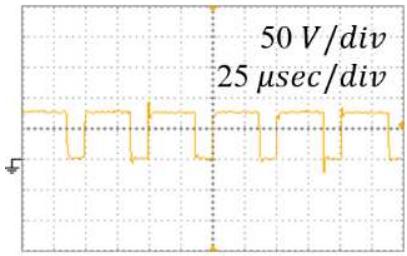


(b)

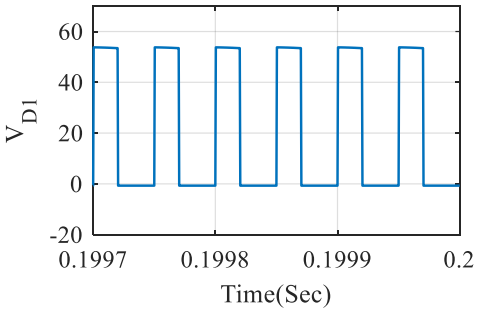


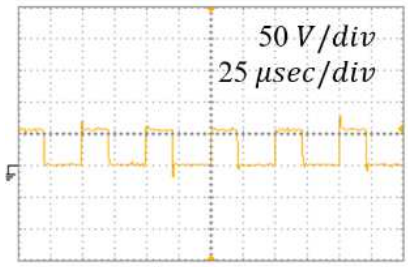
(c)


100
50
0
V_{sw4}
0.1997
0.1998
0.1999
0.2
Time(Sec)

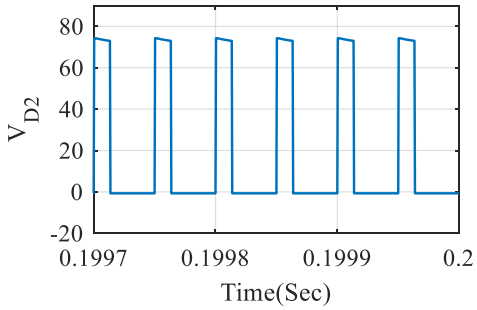

50 V/div
25 μsec/div

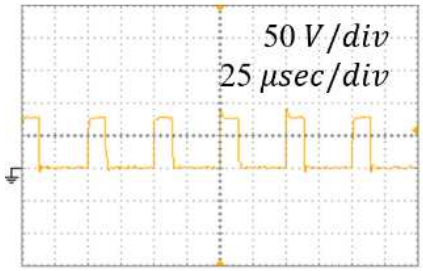
(d)


60
40
20
0
-20
V_{D1}
0.1997
0.1998
0.1999
0.2
Time(Sec)

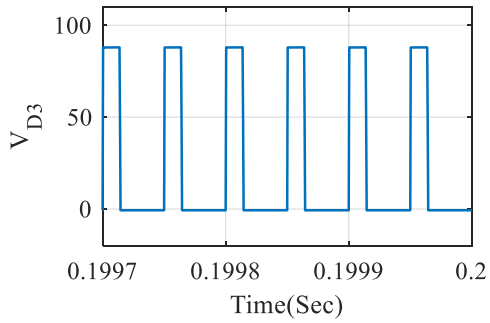

50 V/div
25 μsec/div

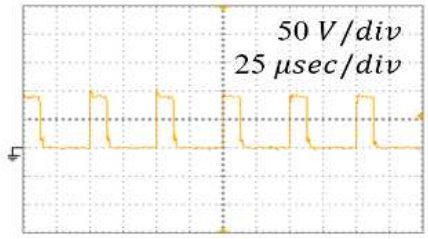
(e)


80
60
40
20
0
-20
V_{D2}
0.1997
0.1998
0.1999
0.2
Time(Sec)

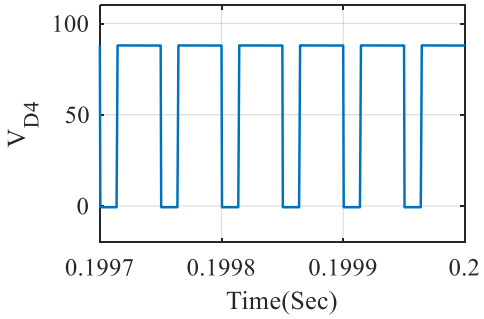

50 V/div
25 μsec/div

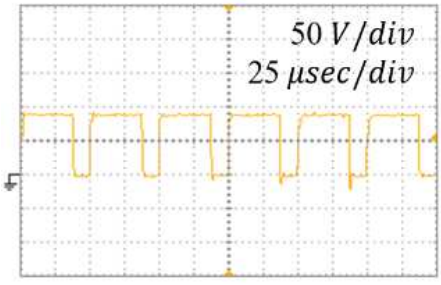
(f)


100
50
0
V_{D3}
0.1997
0.1998
0.1999
0.2
Time(Sec)


50 V/div
25 μsec/div

(g)


100
50
0
V_{D4}
0.1997
0.1998
0.1999
0.2
Time(Sec)


50 V/div
25 μsec/div

(h)

Fig. 18. The simulation and experimental results for the voltage across switches and diodes, a) SW_1, b) SW_2, c) SW_3, d) SW_4, e) D_1, f) D_2, g) D_3, h) D_4.

The similar comparison is conducted for the three windings of the high frequency transformer. The voltage across the primary, secondary and tertiary windings which are consistent with simulations and experiments (Fig. 19) are given by:

$V_{n_1} = \frac{n_1}{n_2} V_{C_1} = \frac{1}{1} \times 50 = 50V$ (positive half cycle)

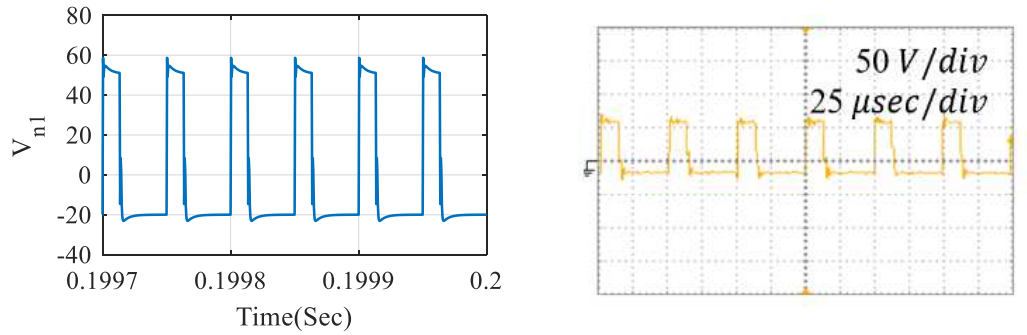
$V_{n_1} = \frac{1}{1} \times (50 - 67.56) = -17.56V$ (negative half cycle)

$V_{n_2} = V_{C_1} = 50V$ (positive half cycle)

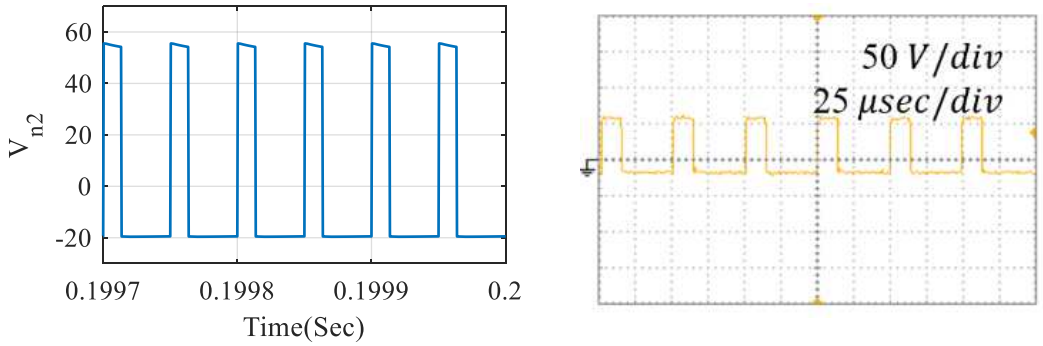
$V_{n_2} = V_{C_1} - V_{C_2} = 50 - 67.56 = -17.56V$ (negative half cycle)

$V_{n_3} = \frac{n_3}{n_2} V_{C_1} = \frac{1.3}{1} \times 50 = 65V$ (positive half cycle)

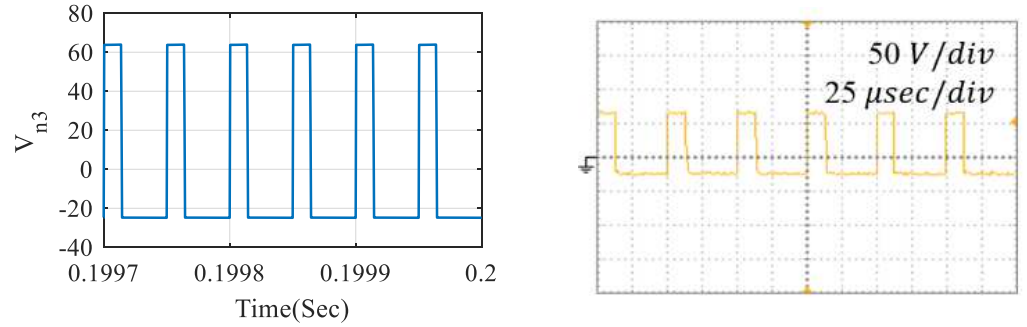
$V_{n_3} = \frac{n_1}{n_2}(V_{C_1} - V_{C_2}) = \frac{1.3}{1} \times (50 - 67.56) = -22.8V$ (negative half cycle)



(a)



(b)



©

Fig. 19. The simulation and experimental results for the winding voltages, a) Primary winding, b) secondary winding, c) tertiary winding.

The efficiency of the proposed converter in the first scenario is calculated as follows:

$$\eta = \frac{P_{out1} + P_{out2} - P_{Bat}}{P_{PV}} = \frac{\frac{74^2}{160} + \frac{88^2}{240} - 24 \times (-1.9)}{36.5 \times 3.4} = 94\%$$

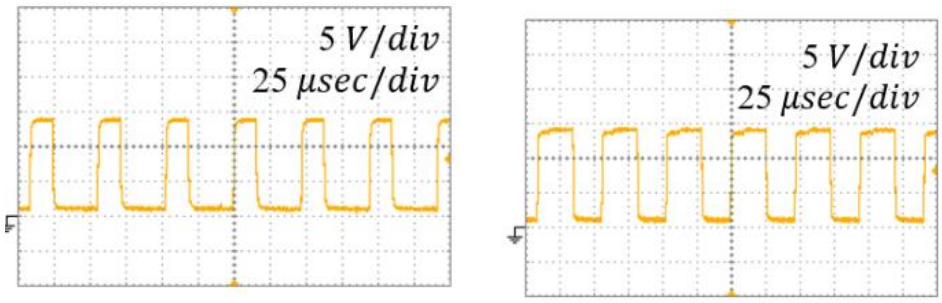
Test Scenario II: During this test scenario, the power generated by the PV panel exceeds the total demand of the loads; Consequently, the surplus energy is effectively stored in the battery (battery is charging). Throughout this operational condition, the duty cycle of SW_2 remains greater than that of SW_1. The quantitative experimental data for this test scenario are declared in Table II.

Table II

Specifications of the third test Scenario

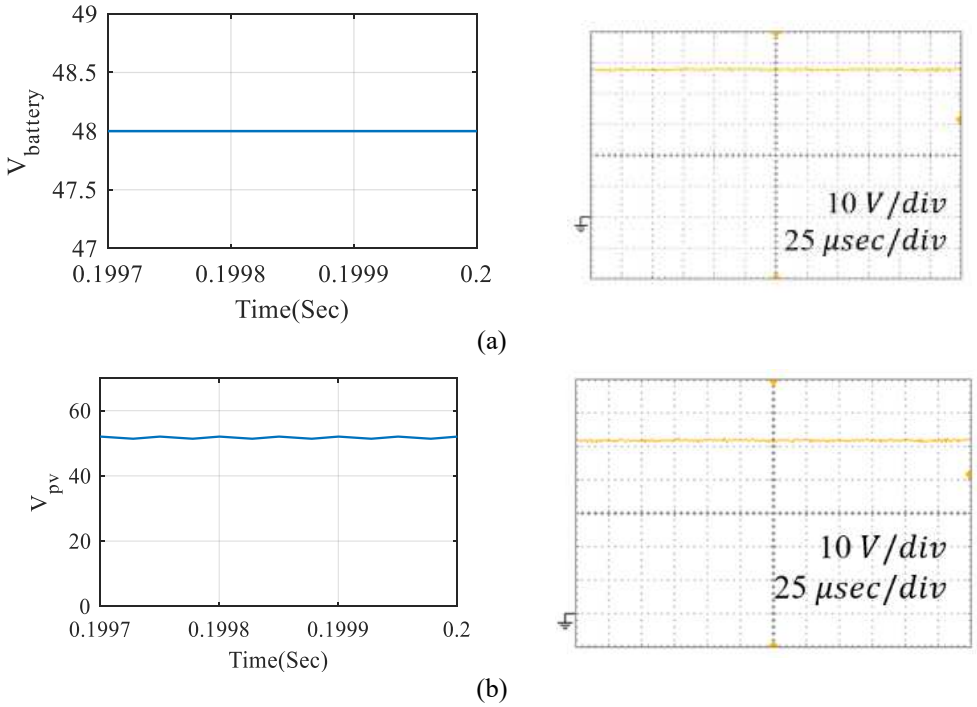
Parameters	Symbol	Value
Battery voltage	V_{bat}	24V
PV voltage	V_{PV}	51.7V
PV current	I_{PV}	3.3A
Duty cycle for first time interval	D_1	0.32
Duty cycle for second time interval	D_2	0.23
Duty cycle for third time interval	D_3	0.45

The switching commands of SW_1 and SW_2 during the second test scenario are shown in Fig. 20. The simulation and experimental results for the two input source voltages and the PV current are shown in Fig. 21 and Fig. 22 respectively.



(a) (b)

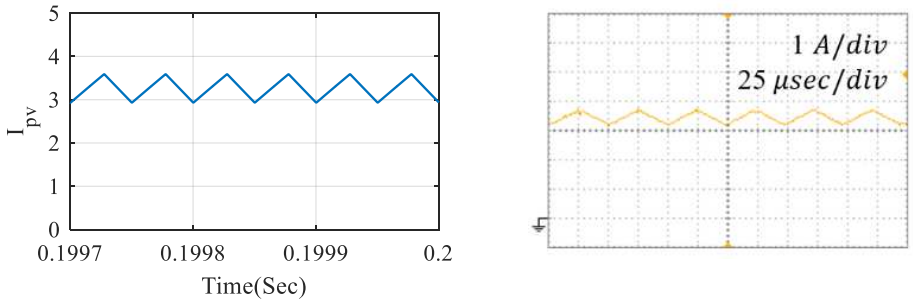
Fig. 20. The switching commands of a) SW_1, b) SW_2 for the second test scenario.



(a)

(b)

Fig. 21. The simulation and experimental results for the two input source voltages (second scenario).



(a) (b)

Fig. 22. PV current (a) Simulation (b) Experimental case

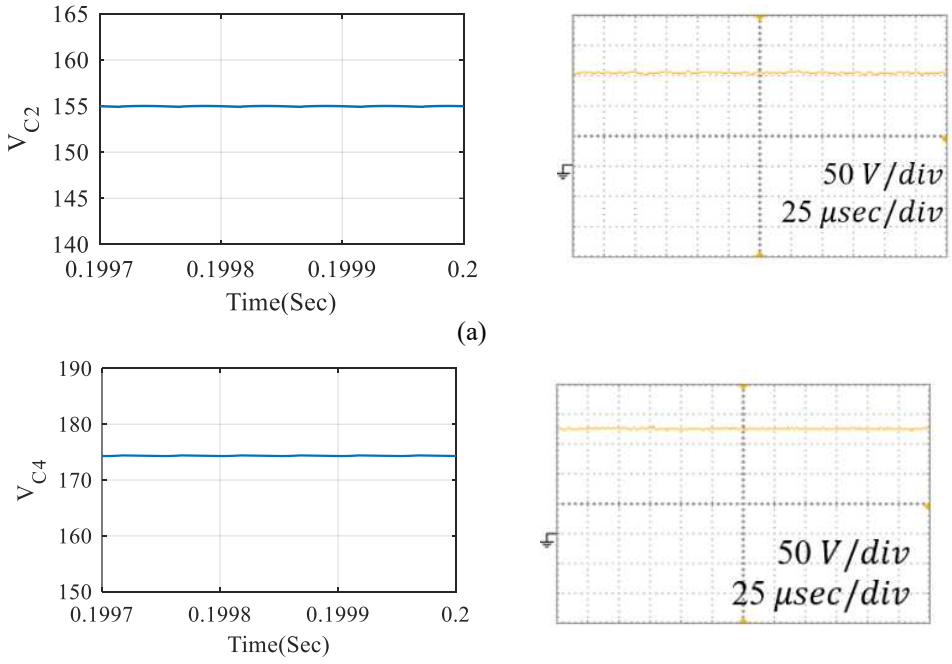
The theoretical values of voltage across the capacitors are expressed as follows which are in good agreements with the simulation and experimental results shown in Fig 23.

$$V_{C_1} = \frac{n_2 V_{bat}}{n_2 D_{offsw1} - n_1 D_{onsw1}} = \frac{1 \times 48}{1 \times 0.68 - 1 \times 0.32} = 133V$$

$$V_{C_2} = \frac{V_{C_1}}{D_{offsw1}} = \frac{133}{0.68} = 195V$$

$$V_{C_3} = \frac{n_3}{n_2}\left(V_{C_2} - V_{C_1}\right) = \frac{1.3}{1}(195 - 133) = 80.6V$$

$$V_{C_4} = \frac{n_3}{n_2} V_{C_1} + V_{C_3} = \frac{1.3}{1} \times 133 + 80.6 = 253V$$



(a)

(b)

Fig. 23. The simulation and experimental results for the voltage across a) C_2, b) C_4.

The battery current values of the inductors is calculated as follows and shown in Fig. 24.

$$I_{L_1} = \frac{I_X D_{onsw1} + I_Y D_{offsw1} - I_{L_2} D_{offsw2}}{D_{offsw1}} = \frac{14.53 \times 0.32 + 2.32 \times 0.68 - 3.3 \times 0.45}{0.68} = 6.9A$$

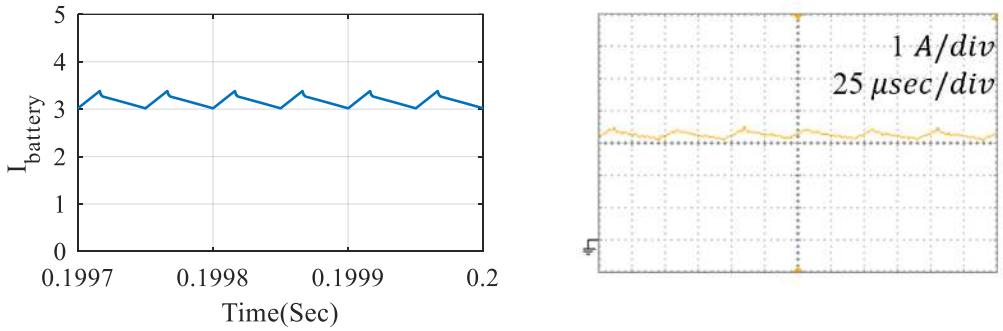


Fig. 24. The simulation and experimental results for the Battery current. (second test scenario)

The converter efficiency in the second test scenario is calculated as:

$$\eta = \frac{P_{out1} + P_{out2}}{P_{bat} + P_{PV}} = \frac{\frac{155^2}{160} + \frac{174^2}{240}}{48 \times 3.2 + 51.7 \times 3.3} = 92\%$$

V. Conclusion

This paper proposed and experimentally validated a novel dual-input dual-output (DIDO) T-source DC-DC converter for photovoltaic–battery hybrid systems. The proposed topology integrates a PV source and a battery into a single converter structure, enabling efficient power sharing, battery charging and discharging, and regulated output voltage under different operating conditions. By using a T-source impedance network, a coupled inductor, and an auxiliary winding, the converter achieves reduced component count, lower control complexity, and improved system compactness compared with conventional multi-converter solutions. A Hill Climbing MPPT algorithm was implemented to ensure that the PV array operates near its maximum power point, while the closed-loop feedback control maintained stable output voltages during variations in input power and load demand. The theoretical analysis, simulation results, and experimental measurements showed good agreement, confirming the validity of the proposed model and control strategy. The results demonstrated that the converter can successfully supply the load when PV power is insufficient and can charge the battery when excess PV power is available. Overall, the proposed converter represents a promising solution for renewable-energy-based hybrid power systems, particularly in applications where high efficiency, flexible power management, and compact structure are required. Future work may focus on independent regulation of the secondary output, efficiency optimization, and performance evaluation under wider operating conditions.

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Author contributions statement

S. Zare has developed main idea, conducted simulations and extracted relations. A. Rajaei and M. Karimianfard contributed to the analysis, supervision, verifications, and worked on paper writing.
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