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Inverse-designed subwavelength metamaterial 3×3 reconfigurable power distributor for high-density programmable photonic computing

Lei Deng

denglei_hust@mail.hust.edu.cn

Huazhong University of Science and Technology https://orcid.org/0000-0003-2647-4610

Hangming Fan

Huazhong University of Science and Technology

Zhenyu Hu

Huazhong University of Science and Technology

Chengying Yu

Huazhong University of Science and Technology

Xiaoyang Liu

Huazhong University of Science and Technology

Xiao Ren

Huazhong University of Science and Technology

Mengfan Cheng

Huazhong University of Science & Technology

Qi Yang

Huazhong University of Science and Technology

Tang Ming

Huazhong University of Science and Technology

Deming Liu

Huazhong University of Science and Technology

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Inverse-designed subwavelength metamaterial 3×3 reconfigurable power distributor for high-density programmable photonic computing

Hangming Fan,[1, †] Zhenyu Hu,[1,†] Chengying Yu,[1] Xiaoyang Liu,[1] Xiao Ren,[1] Mengfan Cheng,[1,2] Qi Yang,[1] Ming Tang,[1] Deming Liu,[1] and Lei Deng[1,2,*]

[1] *Huazhong University of Science and Technology, Wuhan National Laboratory for Optoelectronics and School of Optical and Electronic Information, Wuhan 430074, China*

[2] *Shenzhen Huazhong University of Science and Technology Research Institute, Shenzhen 518000, China*

† These authors contributed equally: Hangming Fan, Zhenyu Hu

[*] *Corresponding author E-mail address: denglei_hust@mail.hust.edu.cn*

Abstract

Silicon photonic integrated circuits underpin high-speed photonic computing and optical communication systems. Conventional on-chip optical switches are inherently limited to two output ports, imposing a fundamental ceiling on computational density and architectural scalability under fixed chip footprints, while bulky weight-tuning units further hinder integration miniaturization. Here we report a synergistic phase and optical field manipulation strategy for dynamic on-chip power redistribution enabled by inverse-designed subwavelength silicon metamaterials. We experimentally realize a 3×3 reconfigurable power distributor with an ultra-compact 4×1.9 μm² footprint, achieving continuous power tuning of 0.3%–78.6%, 0.3%–91.8% and 1.6%–72.1% across three output channels. Serving as a compact optical classifier primitive, it yields 88.67% five-fold accuracy on 150 Iris samples via a calibrated hardware-response model, and on-chip measurements of the fabricated device validate class-selective optical routing on an independent 30-sample test set. Extending the architecture to four ports, direct finite-difference time-domain simulations yield 97.0% accuracy (388/400 images) for four-class handwritten digit recognition. These results establish reconfigurable multi-port silicon photonics as compact building blocks for high-density programmable photonic computing.

Introduction

Photonic integrated circuits (PICs) have emerged as a core platform for modern optical research due to their high integration and multifunctionality (1–4). Benefiting from high-throughput parallel processing capabilities, photonic computing has attracted extensive research attention as a promising alternative to conventional electronic computing (5–7). It implements complex matrix operations via reconfigurable optical weight tuning, where on-chip optical switches act as the fundamental building blocks (8). State-of-the-art solutions mainly rely on Mach-Zehnder modulators (9), directional couplers (10), and microring resonators (11), which have been widely adopted for constructing optical neural network systems.

However, nearly all conventional optical switching units are inherently limited to dual-output ports, forming a structural bottleneck that fundamentally restricts port scalability and computational density improvement. Driven by the rapid iteration of next-generation optical neural networks, the demand for high-computational-density architectures under fixed chip footprints has become increasingly urgent. Current dual-port-based photonic computing architectures have approached their performance ceiling, and further breakthroughs in computational throughput and scalability are fundamentally constrained by two-port weight-tuning units. As verified in Fig. 1(a), the computational density of photonic systems scales positively with the port number of basic functional units when ignoring extra area overhead (12). In this regard, multi-port reconfigurable power distributors are indispensable core devices for breaking current limitations, enabling high-performance optical computing and innovative neural network architecture design within a given footprint as shown in Fig. 1(b).

Metamaterials have been widely used in silicon-based devices such as mode division multiplexing (13), wavelength division multiplexing (14), and power splitting (15), leveraging their advantages of flexible design and precise manipulation of optical fields. At the sub-wavelength scale, metamaterials enable accurate control of the effective refractive index, thereby realizing a variety of complex functions. As an intelligent design method, inverse design, when combined with the structural characteristics of metamaterials, can explore the feasibility of device structures in ultra-small size (16-18). Furthermore, for unconventional functional designs, inverse design allows the acquisition of device structures without the support of empirical structures, making it particularly suitable for designing complex functions. The combination of metamaterial

structures and inverse design methods provides a solution for multi-port reconfigurable power splitters with ultra-high integration and large-range adjustment.

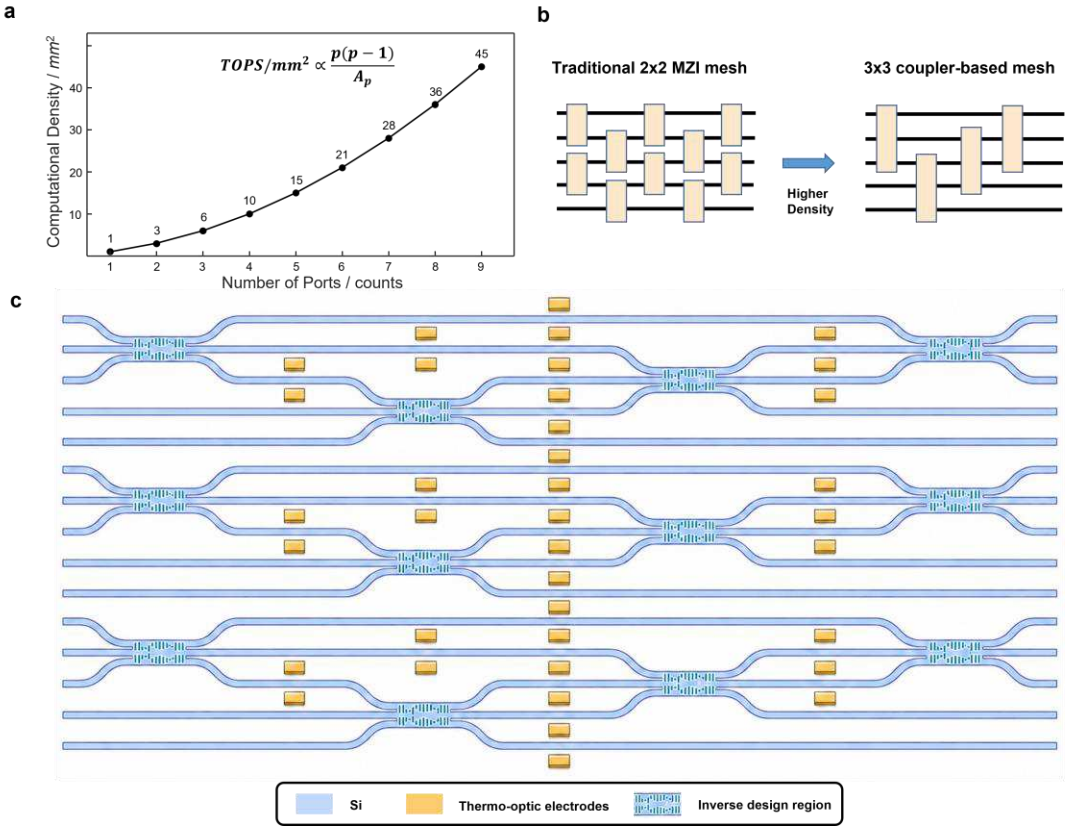

Fig. 1. 3×3 coupler-based photonic mesh for high-density programmable photonic computing. (a) Computational density scaling with port count, (b) Conceptual comparison between traditional 2×2 MZI mesh and 3×3 coupler-based mesh with higher density, (c) high-density programmable photonic computing based on three-port reconfigurable power distributor**.**

Previous inverse-designed photonic devices have realized fixed on-chip optical classification tasks with improved integration density (19,20). Nevertheless, these static devices feature non-reconfigurable light-field mappings after fabrication, which greatly limits their versatility and adaptability for programmable photonic computing. Beyond port count, the physical footprint of individual weight-tuning units is another key factor governing overall computational density: reducing device dimensions directly yields higher integration levels and thus higher computing throughput per unit area. The combination of inverse design and subwavelength metamaterials is particularly suited for this goal, as it enables complex optical functionalities in ultra-compact

footprints, further boosting computational density as shown in Fig. 1(c). However, reconfigurable multi-port power distributors based on this synergistic design strategy remain largely unexplored.

In this work, we propose a novel photonic regulation strategy based on synergistic phase tuning and optical field manipulation, enabling reconfigurable power mapping and on-chip photonic classification. Unlike conventional static inverse-designed photonic devices with fixed input–output light-field mappings, our scheme flexibly reconfigures incident phase combinations via electrodes, eliminating the need for bulky high-precision optical field control modules. At its core is a particle swarm optimization (PSO) inverse-designed metamaterial nanostructure with parametric subwavelength gratings, which expands design freedom and reconstructs distinct output optical fields under varied input phase states. We experimentally demonstrate an ultra-compact 3×3 reconfigurable power distributor with a 4×1.9 μm² footprint, delivering continuous full-range power tuning of 0.3%–78.6%, 0.3%–91.8%, and 1.6%–72.1% across three output channels. Beyond acting as programmable weighting units, the device supports class-selective optical outputs driven by an electronic encoder: for Iris classification, five-fold evaluation with a calibrated hardware-response model yields 88.67% accuracy over 150 samples, and on-chip measurements on an independent 30-sample test set verify class-selective optical routing. This work establishes a scalable and flexible paradigm for reconfigurable photonic hardware design, providing a promising solution for high-density programmable photonic computing and multifunctional integrated optoelectronic systems.

Results

The schematic of the inverse-design workflow is depicted in Fig. 2(a). The metamaterial design region adopts a parametric subwavelength grating architecture. Each grating tooth is bisected by the axis into upper and lower segments, whose lengths serve as two independent geometric design variables, denoted hu (upper) and hd (lower), respectively. With 20 teeth per segment and the structural symmetry constraint, the entire design space yields a total of 40 independent optimization variables. The figure of merit (FOM) of 3×3 reconfigurable power distributor in the inverse design is described by:

$$\mathrm{FOM} = \mathrm{abs}(1 - P_{11}) + \mathrm{abs}(1 - P_{22}) + \mathrm{abs}(1 - P_{33}) \quad (1)$$

where Pin denotes the output power of the n-th port under the i-th phase input. Here, three discrete phase configurations are employed: (π, 0, 0), (0, π, 0), and (0, 0, π), which correspond to

the three target normalized power output states of the three-port device: (1, 0, 0), (0, 1, 0), and (0, 0, 1), respectively. A smaller FOM value indicates a closer match between the achieved power distribution and the target profile.

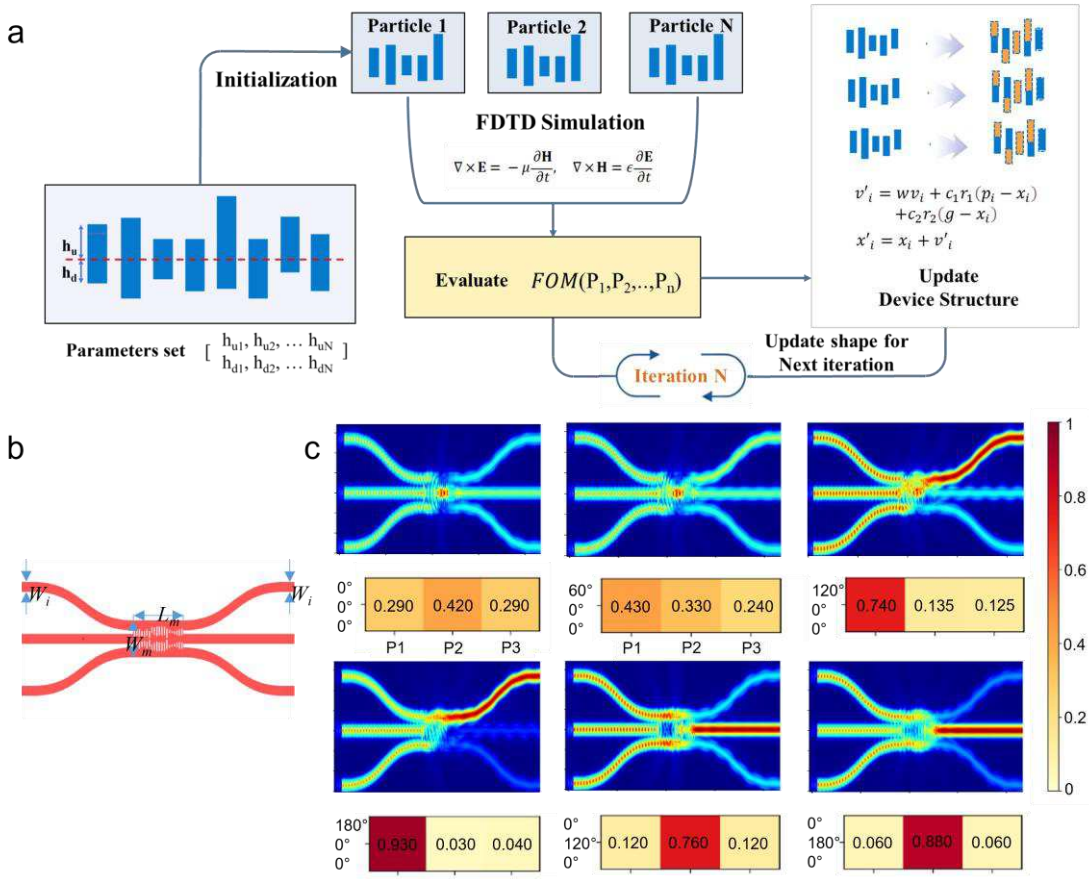

Fig. 2. Inverse design and optical characterization of the 3×3 reconfigurable power distributor. (a) The schematic of the inverse-design workflow, (b) the structure of the proposed 3×3 reconfigurable power distributor, (c) simulation of power distribution under different phase combinations.

3×3 reconfigurable power distributor

A micrograph of the proposed three-port reconfigurable power distributor is presented in Fig. 2(b). Monolithically integrated thermo-optic heating electrodes apply independent, precise phase shifts to the split beams, enabling programmable input phase combinations. The phase-modulated optical fields are then fed into the inverse-designed metamaterial core, which redistributes optical power across the three output waveguides in a phase-dependent manner. By tuning the electrode driving voltages, continuous full-range power allocation with arbitrary ratios is achieved across all three output channels.

Figure 2(c) shows the simulation results of the 3×3 reconfigurable power distributor. Owing to the vertical structural symmetry, the power responses of Port 1 and Port 3 are complementary. We present the output power distributions under several representative input phase configurations. The calculation method for the power ratio of each channel is as follows:

$$Pr_m = P_m/(P_1 + P_2 + \cdots + P_N) \tag{2}$$

where Prm denotes the power ratio of the m-th port and PN is the output power of the n-th port. The normalized power of Port 1 and Port 3 is tuned from 0.06 to 0.93, and Port 2 from 0.03 to 0.88, approaching the ideal 0–1 full-range power tuning. The device insertion loss remains nearly constant across all phase configurations, indicating no additional loss penalty from power reconstruction.

Broadband performance is simulated under six representative phase configurations: (60°,0°,0°), (120°,0°,0°), (180°,0°,0°), (0°,60°,0°), (0°,120°,0°), and (0°,180°,0°), as shown in Fig. 3. The transmission characteristics remain nearly consistent across the 1535–1565 nm wavelength range, verifying the favorable broadband property of the proposed device.

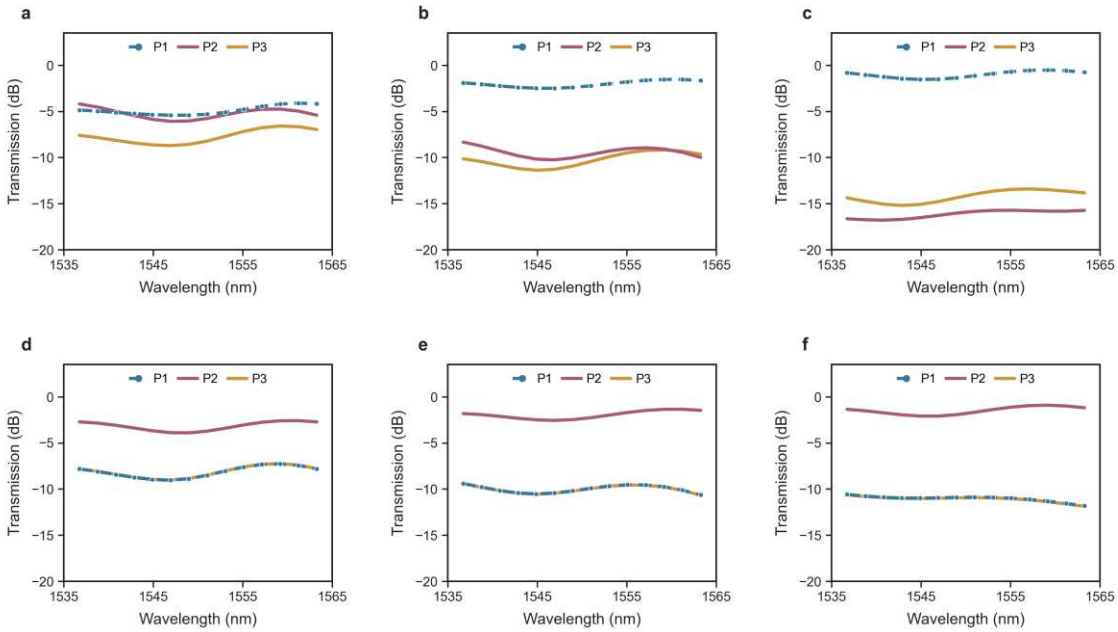

Fig. 3. Transmission spectra of the 3×3 reconfigurable power distributor. (a–f) Simulated spectra under input phase configurations of (60°, 0°, 0°), (120°, 0°, 0°), (180°, 0°, 0°), (0°, 60°, 0°), (0°, 120°, 0°), and (0°, 180°, 0°).

Optical three-classifier

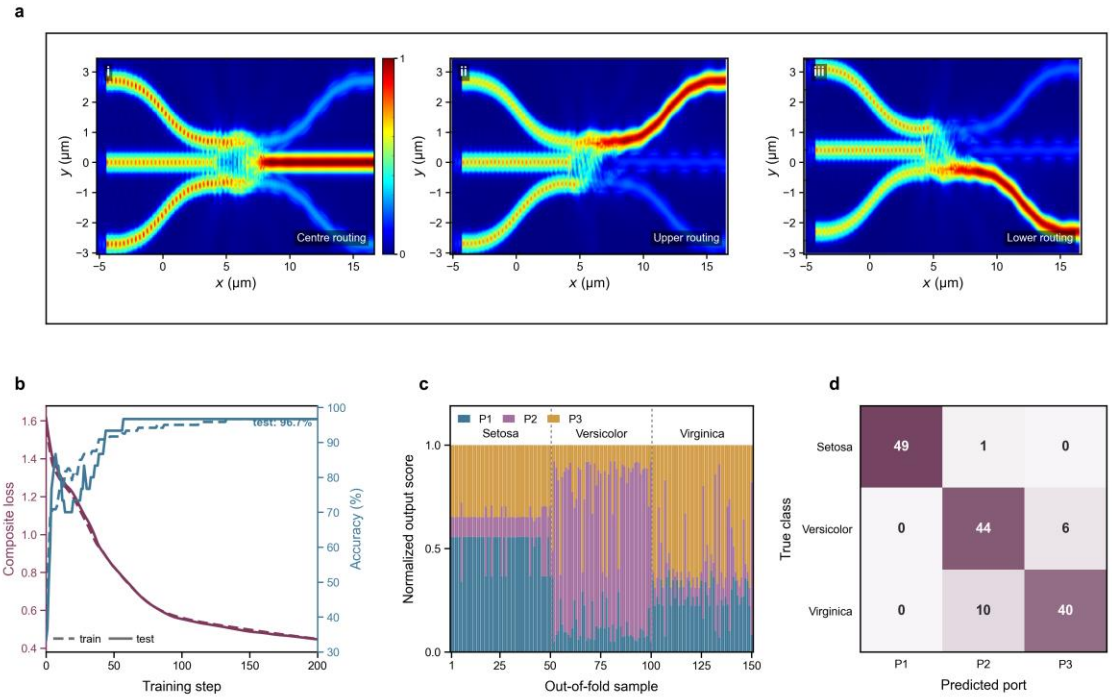

Fig. 4. Three-class inference with a calibrated three-port photonic processor model. (a) Simulated optical-field distributions for (i) centre, (ii) upper, and (iii) lower routing. (b) Composite loss and classification accuracy over 200 training steps in an independent fixed-split run. (c) Normalized output scores from stratified five-fold evaluation of the calibrated hardware-response model for 150 Iris samples, with 50 samples per class. (d) Pooled out-of-fold confusion matrix for the predictions in (c).

To assess the three-port device's programmable phase-to-power response for photonic inference, we demonstrate classification on the Iris dataset. An electronic encoder maps each sample's four morphological features to three control voltages, and the device's corresponding optical response assigns each sample to one of three output ports. To incorporate the fabricated circuit's measured characteristics, the encoder is optimized against a response surface constructed from 1224 calibrated voltage states. Simulated field distributions exemplify how distinct control states route optical signals to the centre, upper and lower output branches, respectively, as shown in Fig. 4(a)(i–iii).

Figure 4(b) displays a representative independent 200-step training run, featuring progressive loss reduction and improving classification accuracy. Stratified five-fold evaluation of the calibrated response model across 150 Iris samples yielded 88.67% accuracy (133 correct

predictions; Fig. 4(c, d)), with 16 of the 17 total errors arising from Versicolor–Virginica confusion. These results correspond to offline inference via the interpolated hardware response; the training curve shown is not the optimization history of the five-fold models.

Experiment characterization of the 3×3 reconfigurable power distributor

Figure 5(a) depicts the experimental setup for on-chip device characterization, on the basis of which we perform both arbitrary power-splitting and optical classification measurements. The Microphotograph of fabricated chip is shown in Fig. 5(b). Scanning electron microscopy (SEM, GeminiSEM 300) images of the fabricated device are shown in Fig. 5(c) and 5(d), confirming high-fidelity pattern transfer under standard fabrication processes and the absence of microscale features that pose manufacturing challenges.

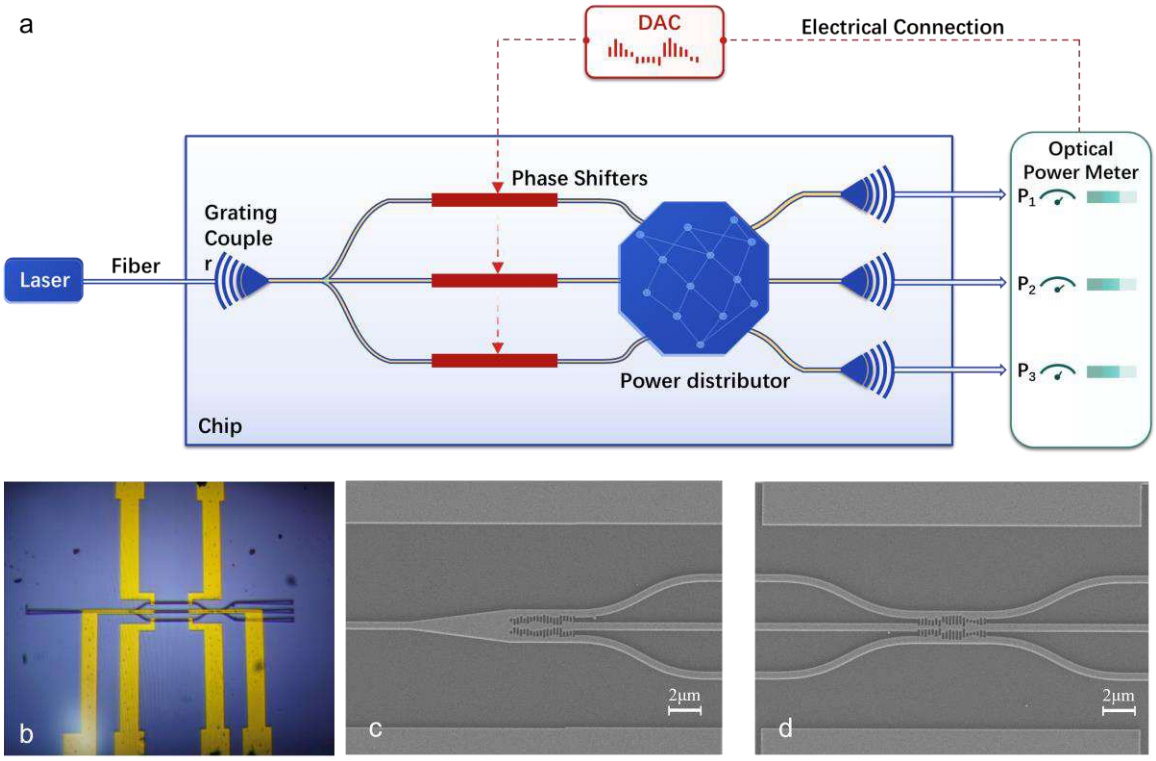

Fig. 5. Experimental setup and fabricated device characterization. (a) Schematic of the experimental system setup, (b) Micrograph of the fabricated chip, (c) Scanning electron micrograph of the 1×3 power splitter, and (d) Scanning electron micrograph of the reconfigurable power distributor.

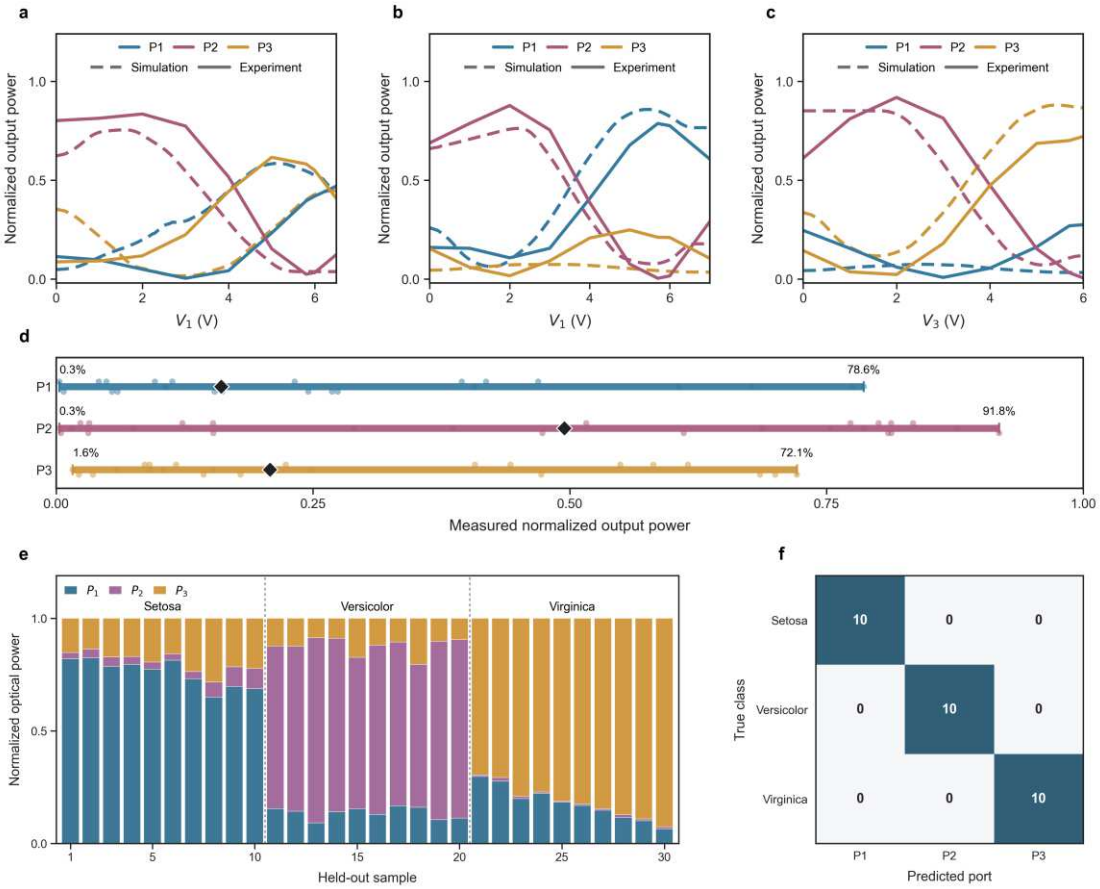

Fig. 6. Power tuning and experimental Iris classification with the three-port photonic processor. (a) Normalized output powers during a V1 sweep with V2 = 0 V and V3 = 0 V. (b) V1 sweep with V2 = 6.9 V and V3 = 0 V. (c) V3 sweep with V2 = 7.1 V and V1 = 0 V. Dashed and solid curves in a–c denote simulation and experiment, respectively. (d) Measured power fractions across the bias scans. (e) Output-power fractions measured at 1550 nm for 30 held-out Iris samples, with ten per class. (f) Confusion matrix for the samples in (e), classified by their highest-power output port.

Figure 6(a-c) compares simulated and measured power distributions under single-channel voltage sweeps, with the other two channels fixed at biases covering each port's full power extrema. Fabrication-induced symmetry breaking disrupts the inherent vertical structural symmetry, so independent voltage-sweep measurements are performed for Port 1 and Port 3. Experimental measurements yield power ratio tuning ranges of 0.3%–78.6% (Port 1), 0.3%–91.8% (Port 2), and 1.6%–72.1% (Port 3) as shown in Fig. 6(d). All three ports support broad continuous power reconfiguration, experimentally validating the proposed design concept. With simulated phase distributions adjusted to match experimental observations, the results show good agreement with

numerical predictions. Primary deviations stem from fabrication-tolerance-induced vertical asymmetry and phase perturbations from thermal crosstalk between adjacent heating electrodes. The voltage axes in Fig. 6(a)-(c) correspond to experimental bias points rather than simulated values. Voltage-to-phase mismatches between simulation and experiment mainly arise from thermal crosstalk across adjacent heaters. Nevertheless, synergistic tuning of the three independent biases achieves wide-range power control closely matching simulated performance, further corroborating the proposed scheme.

We next examine class-selective routing on the fabricated device using voltage commands from a separate fixed-split encoder. The voltage triplets for 30 held-out Iris samples, with ten samples per class, are applied to the three control channels. Optical powers are measured at 1550 nm and normalized across the three output ports for each sample. The resulting port-power distributions exhibit class-selective output patterns as depicted in Fig. 6(e). Averaging the per-sample power fractions in Fig. 6(e) gives target-port fractions of 75.8%, 74.2% and 81.4% for Setosa, Versicolor and Virginica, respectively. Assigning samples to the port with the highest measured power produces the class-resolved outcomes shown in Fig. 6(f). The measured assignments are consistent with the target labels in this test set. These observations support transfer of the encoded voltage states to class-selective optical outputs in this measurement, independent of the five-fold model evaluation.

4×4 reconfigurable power distributor and optical four-classifier

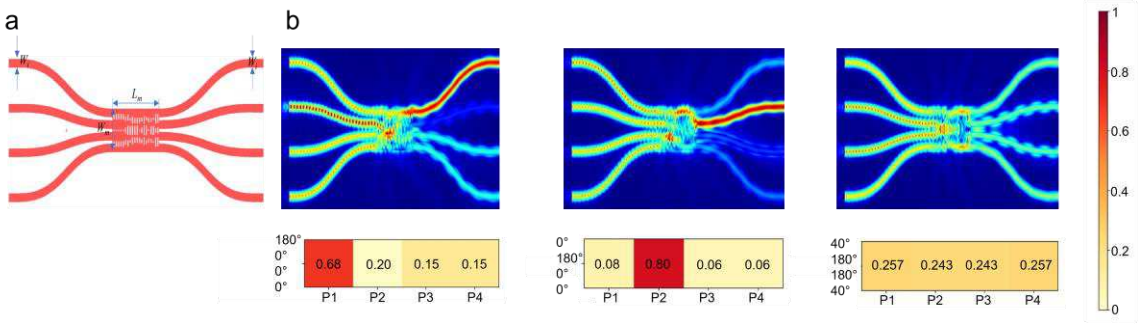

Fig. 7. Design and simulated performance of the 4×4 reconfigurable power distributor. (a) Schematic structure of the 4×4 reconfigurable power distributor, (b) Simulated optical field distributions under different phase configurations.

To further validate the scalability of our proposed design paradigm, we extend the architecture to a 4×4 reconfigurable power distributor. The structure is shown in Fig. 7(a), and the

device footprint is only 4×2.6 μm². Figure 7(b) shows simulation results for three representative power distribution scenarios: single-port output states (1:0:0:0, 0:1:0:0) and uniform multi-port excitation (1:1:1:1). By virtue of vertical structural symmetry, these results generalize to all symmetric port configurations, confirming effective power regulation for both single-port and simultaneous multi-port operation. Figure 8 characterizes the broadband performance of the four-port device. All four ports maintain stable transmission across the 1535–1565 nm wavelength range. Favorable broadband performance is preserved despite the increased port count and structural complexity.

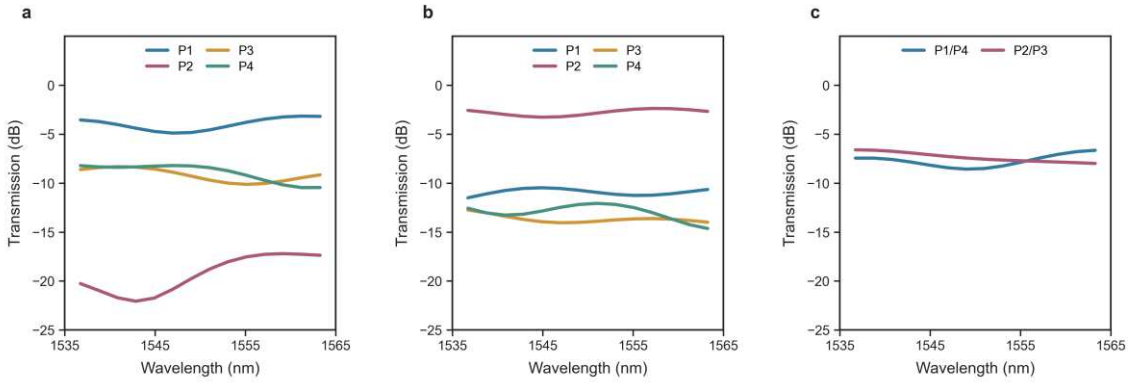

Fig. 8. Transmission spectra of the four-port power distributor. (a–c) Simulated spectra under input phase configurations of (180°, 0°, 0°, 0°), (0°, 180°, 0°, 0°) and (40°, 180°, 180°, 40°), respectively. P1–P4 denote the output ports. Panel c shows the paired responses P1/P4 and P2/P3.

To examine the scalability of the phase-controlled routing approach, we extend the architecture to four input and output ports and consider classification of the handwritten digits 0, 1, 4 and 7. Each image is encoded into four input phases, with the four output ports representing the four classes. A differentiable surrogate trained on 1,000 full-wave responses is used to optimize the encoder, after which the phase states of the independent test images are returned to the finite-difference time-domain (FDTD) solver for evaluation. Validation performance selects the encoder checkpoint at epoch 220 as shown in Fig. 9(a).

Direct FDTD evaluation correctly classifies 388 of 400 test images, corresponding to an accuracy of 97.0% as illustrated in Fig. 9(b). The confusion matrix resolves the outcomes for all four digit classes, with twelve errors distributed among digits 0, 4 and 7. The target-port power margins in Fig. 9(c), defined relative to the largest competing output, have a mean of 0.279 in

arbitrary power units across the 400 test images. Across 1,600 port–image pairs, surrogate and FDTD powers show close agreement, with a mean port-wise coefficient of determination of 0.99978 and a mean absolute error of 0.00203 in arbitrary power units. The winning ports agree for 399 of the 400 test images as shown in Fig. 9(d). This numerical demonstration extends phase-controlled classification from three to four output classes.

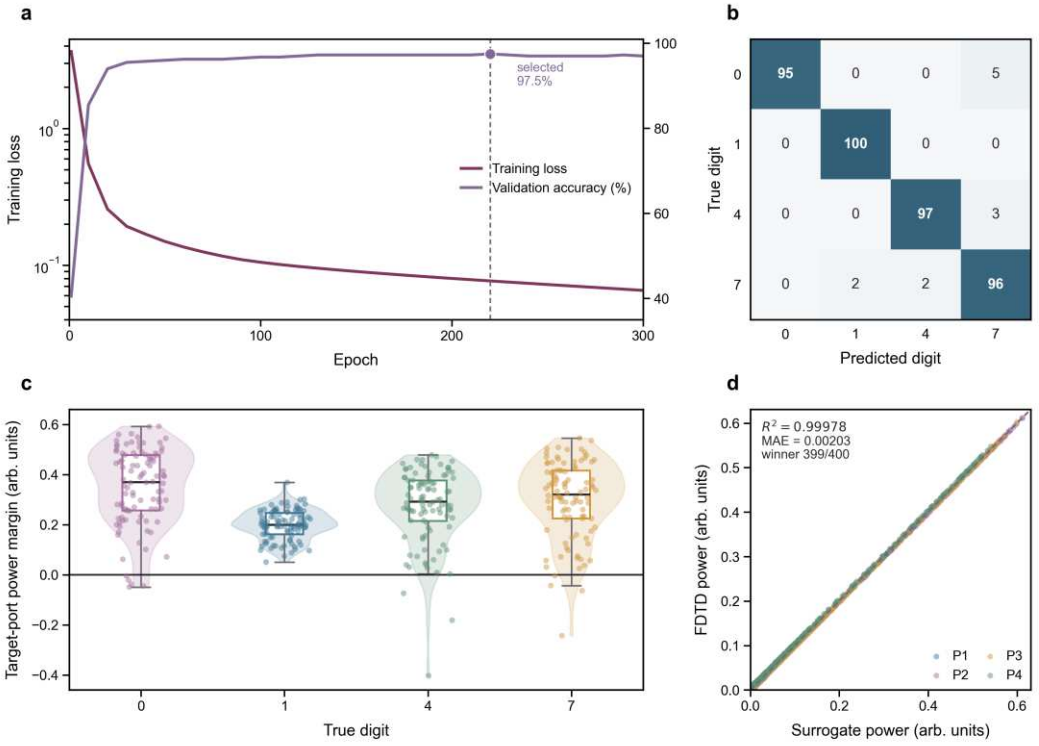

Fig. 9. Four-class handwritten digit recognition by direct FDTD evaluation of the four-port photonic processor. (a) Training loss and validation accuracy during surrogate-assisted encoder optimization. The dashed vertical line marks the checkpoint selected at epoch 220. (b) Confusion matrix for 400 test images, with 100 images each for digits 0, 1, 4 and 7. (c) Target-port power margins, defined as the target-port power minus the largest non-target-port power. Points represent individual test images (n = 100 per digit), and violins show their distributions. (d) Surrogate-predicted and FDTD-calculated powers for 1,600 port–image pairs, coloured by port, with a dashed identity line.

Discussion

In summary, we present a reconfigurable photonic control strategy leveraging synergistic phase tuning and optical field manipulation, and experimentally demonstrate a compact 3×3 reconfigurable power distributor based on particle-swarm-optimized inverse-designed

metamaterials. Unlike conventional static inverse-designed photonic devices with fixed input–output mappings, our device achieves arbitrary output power ratios by reconfiguring incident phase combinations via integrated electrodes, eliminating the need for bulky high-precision optical field control modules. Occupying an ultra-compact footprint of only 4×1.9 μm², the device delivers continuous power tuning across three output channels (0.3%–78.6%, 0.3%–91.8%, 1.6%–72.1%). Fivefold evaluation of the calibrated hardware-response model yielded 88.67% accuracy for Iris classification. Measurements on a separate 30-sample test set supported class-selective optical routing on the fabricated device. Together, these observations support the feasibility of this hardware primitive for programmable photonic classification.

Simulation validation of a 4×4 reconfigurable power distributor and four-class handwritten digit recognition confirms the scheme's scalability: the underlying phase-to-field control principle extends seamlessly to higher port counts without architectural modification. Beyond serving as programmable weighting elements for large-scale optical neural networks, the devices find broad applicability in optical phased arrays, reconfigurable optical interconnects, and other multifunctional integrated photonic systems. This work establishes a scalable, flexible hardware paradigm for reconfigurable silicon photonics, paving the way for high-density programmable photonic computing and integrated optoelectronic platforms. Future efforts will focus on port count expansion, insertion loss optimization, and architecture scaling for complex real-world photonic inference tasks.

Materials and Methods

Chip fabrication

The device is fabricated on a standard 220 nm SOI platform. The fabrication process is performed as follows: first, electron beam lithography (EBL, Vistec EBPG5000+ES) coupled with electron beam evaporation (EBE) is employed to fabricate gold alignment marks. Subsequently, device patterns are defined by overlay lithography using EBL and inductively coupled plasma (ICP, Oxford Plasmalab System 100) etching. A 2-μm-thick silica cladding is then deposited on the device surface. After that, metal electrodes are deposited via EBL and EBE. Upon completion of device fabrication, the chip is diced with a precision dicing saw and wire-bonded to the control circuit board with gold wires.

Experimental details

To test the power tuning capability of the device, a 1550 nm continuous-wave (CW) laser is utilized as the input light source. The light emitted from the laser traverses a PC prior to being coupled into a grating coupler. At the output end, the light is coupled into an optical fiber through another grating coupler and subsequently connected to an optical power meter for optical power measurement.

Acknowledgments

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Author contributions

The concept of this work was conceived by H.F. and L.D. H.F., Z.H., and C.Y. developed the experimental systems, performed the measurements, and analysed the data. X.L. and X.R. helped with the experiments. This project was organized by L.D., and supervised by M.C., Q.Y., M.T., D.L., and L.D. The manuscript was written by H.F. and Z.H. All authors revised the manuscript.

Data availability

The data supporting the findings of this study are available within the Article and its Supplementary Information and from the corresponding authors upon reasonable request.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information is available for this paper.

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