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A Novel Dopingless Circular MOSFET with S/D Schottky Contact

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A Novel Dopingless Circular MOSFET with S/D Schottky Contact

Pooja Shilla, Abhinav Pratap Singh, Arvind Kumar

Abstract

In this paper, a dopingless circular gate metal oxide semiconductor field effect transistor (DL-CG-MOSFET) with source/drain schottky contact has been designed for low power circuit applications. Study of electrical parameters is carried out by changing the oxide material (HfO_2, SiO_2, Al_2O_3), gate oxide thickness and gate length. Device performance also has been observed by employing oxide engineering and work-function engineering. Device parameters like ON current, OFF current, ON/OFF current ratio, sub-threshold slope (SS), drain induced barrier lowering (DIBL) and gate capacitance (Cgg) calculated to analyse device performance. ON current of order 10^{-5}A is obtained and leakage current is reduced up to the order of 10^{-16}A which shows good ON/OFF ratio. Furthermore, this study examined the performance of DL-CG-MOSFET by minimizing the gate length from 40 nm to 10 nm and Si thickness 5 nm–8 nm with oxide thickness variation from 2nm-4nm.

Keywords Circular gate transistor (CGT), Dopingless Circular gate metal oxide semiconductor field effect transistor (DL-CG-MOSFET), Short Channel effect (SCE), Sub-threshold slope, Gate capacitance

1 Introduction

Semiconductor industries enhance device performance in scaling era by following Moore's law. Conventional CMOS technology restricted up to a scaling limits to avoid major difficulties like low ON current, high leakage current, high package density, short channel effects (SCE's) like Hot carrier effect, threshold voltage roll off, DIBL, impact ionisation high Sub-threshold swing (SS) etc. and many multi-gate structures [1][2]with double gate, triple gate and gate all around was designed to enhance electrostatics control on device to improve ON current. FinFETs and TFETs also becomes most attracted structures in highly performed devices[3][4][5][6] and advance structure like nanowire, nanotube also helps in moving further with technology node scaling by enhancing electrostatic control with some high-k materials

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device results in low leakage current due to increased capacitance[7][8]. Some material based solutions like replacement of Si with strained Si, SiO2 is replaced with high-k materials, metal gate replaces Poly-silicon (poly-Si) also improves device performance. To remove abrupt junctions and ultra-shallow regions many work-function engineering based technologies like junctionless (JL), dopingless (DL), dual metal gate has introduced and also oxide engineering[8] helps in improving the device performance[9][10][11]. Junctionless technology requires uniform heavily doping (1×1019 cm-3) throughout the device with high gate metal work-function ($\phi \sim 5.1$eV) to completely depleting the device which results in high leakage current due to heavily doping[12][13]. Instead of this dopingless device requires intrinsic doping with low work-function ($\phi \sim 4.8$ eV) in comparison with Junctionless device[14][15].

Longitudinal corner effects can also reduce with non-standard layout geometries like hexagonal, octagonal, ellipsoidal and circular which helps in lowering leakage currents and short channel effects [16]. The circular MOSFET with circular gate structure helps in boosting reliability of the MOSFET by diminishing down the electric field strength between the source and drain of the MOSFET results in high integration density[17][18][19]. It is investigated that electric fields divergence in drain of MOSFETs tends to reduce injected hot carrier's high energy in drain which makes MOSFET significantly more reliable. The velocity of hot carriers in drain region get

decreased with the reduction of electric fields and this leads to less damage of the oxide layer due to decreased energy with a corresponding improvement in reliability[17]. The ring/ circular/annular gate MOSFET is highly popular layout with circular gate, which provides higher immunity to SCEs than traditional planar MOSFETs due to its non-standard layout design helps in increasing transistor's effective width of provided silicon area with absence of side interface areas causing trap-induced leakages[20][21][22]. The circular gate device design provides minimized side interfaces and simultaneously helps in improving suppressed drain side field for shorter channel lengths as channel of a circular gate transistor (CGT) is encircled by drain/source regions (internally and externally or vice-versa) . Furthermore, the asymmetric layout design (either the source or the drain within the channel) provides an extra tuning parameter for the optimization of desired application[21][23][24]. The Circular MOSFET with double gate (CDGT) provides better electrical characteristics instead of circular single gate (CSGT) at 30 nm gate length[20]. CGT manufacturing is compatible with the traditional planar MOSFET fabrication process[21][23].

In this work, we are presenting a dopingless circular MOSFET with single gate. Study of electrical parameters is carried out by changing the oxide material (HfO_2, SiO_2, Al_2O_3), gate oxide thickness and gate length. Device performance have been analyzed by employing oxide engineering and work-function engineering. Device performance parameters like ON current, OFF current, ON/OFF current ratio, SS, DIBL, gate capacitance also calculated. V-curve of both DL-CG-n MOSFET and DL-CG-p MOSFET in linear and saturation region also shown.

2 Device design

The 3-D structure of the proposed device is shown in Fig. 1 whereas the 2-D cross-section view of the same is depicted in Fig.3.The metal source, gate and drain regions have been formed on an intrinsic Si body with different work-function to establish a dopingless device.

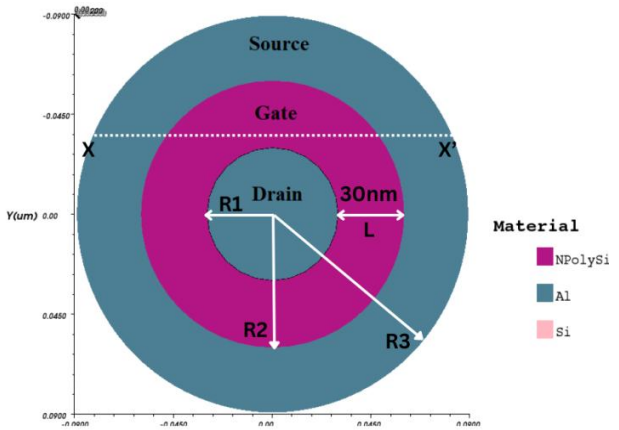


Fig. 1 Circular Gate Transistor (CGT)

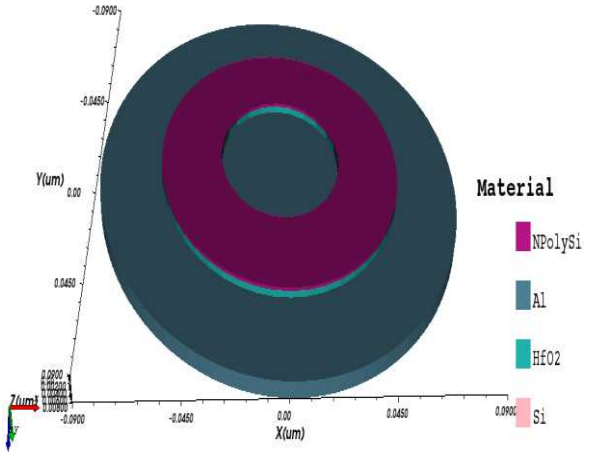


Fig. 2 CGT MOSFET without oxide

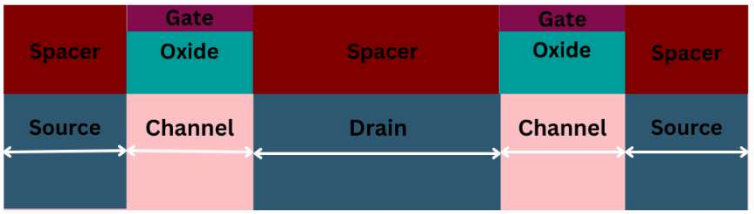


Fig. 3 Cross-sectional view of DL-CGT single gate MOSFET

Fig.2 shows device without oxide and the parameters of proposed device is given in Table 1. Parameters are selected with the reference [3] and [1].

3 Results and Discussion

Firstly, simulated work is calibrated with existing experimental work (dopingless Gate All Around nanowire focuses on S/D Schottky contact) [25] and simulated outcome is very close to experimental result as shown in Fig. 4. Drift-diffusion model and a unified Lombardi mobility model used to acknowledge doping dependent mobility (μ_b), mobility degradation due to surface roughness scattering (μ_{sr}), and acoustic phonon (μ_{ac}). Shockley-Read-Hall (SRH), auger and direct recombination model have also included for considering recombination phenomena. Fermi-Dirac statistics and Boltzmann statistics helps to define carrier concentration in semiconductor[14][25].

Fig.5 shows simulation study of CSGT n-MOS for different gate length. I_{DS}-V_{GS} characteristics shows ON current increases with the gate length due to increase area (effective width)[23] which can be calculated by Eq. (3)[19][20][23][26].

Table I Various parameters used in device design and simulation

Device Parameters	[3]	[1]	Proposed Device Dimensions
Gate Length (L)	30 nm	10 nm	30 nm
Drain Length(R1)	30 nm	10 nm	30 nm
Source Length(R3-R2)	30 nm	10 nm	30 nm
Gate Oxide (T_{ox})	1.5 nm	1 nm	2 nm
Channel Thickness	10 nm	5 nm	5 nm
Channel Doping (cm^{-3})	$1*10^{16}$	$1*10^{15}$	$1*10^{15}$
Source/Drain Doping (cm^{-3})	$1*10^{20}$	$1*10^{20}$	-------
Substrate Doping	$1*10^{15}$	$1*10^{15}$	-------
S/D thickness	10 nm	5 nm	5 nm
Spacer Length	-------	-------	30 nm

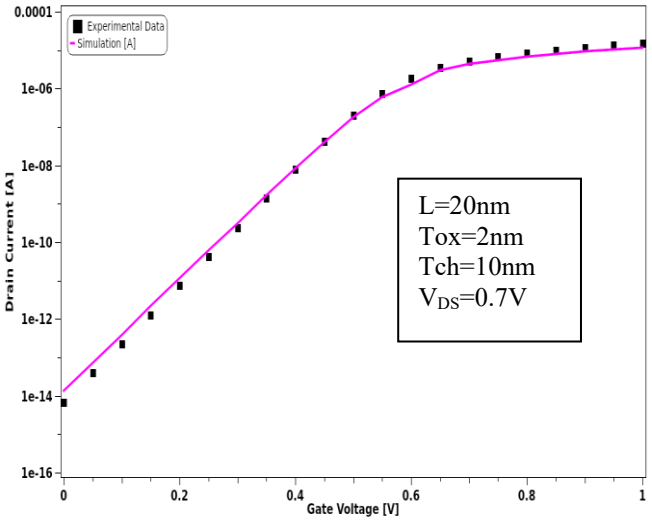


Fig. 4 Calibrated I_{DS}-V_{GS} characteristics of simulated work with existing experimental data results[25]

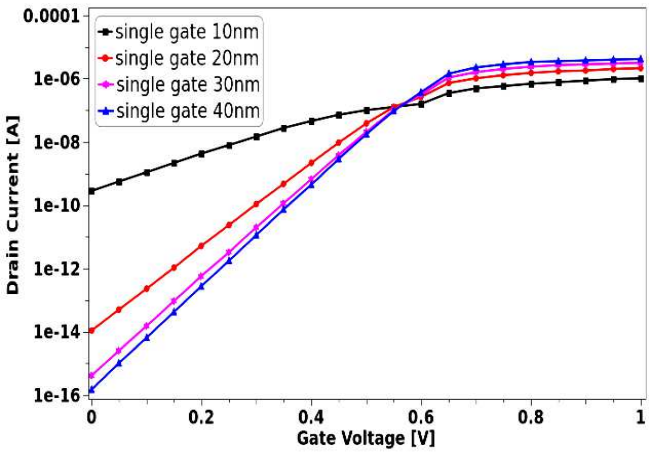


Fig. 5 $I_{DS}V_{GS}$ characteristics for different gate length with T_{ch}=5nm and T_{OX}=2nm at V_{DS}=0.05V.

The Circular MOSFET's device geometrical factor in terms of effective channel width (W_{Rect}) and channel/gate length (L_G) of the conventional rectangular gate transistor is given by Eq.(1).[2]

$$\left[\frac{2\pi}{\ln\left(\frac{R2}{R1}\right)}\right] Circular = \left[\frac{WRect}{LG}\right] Rectangular \quad (1)$$

In the CGT, the effective width of the channel W is defined as,

$$W = 2\pi \times \frac{[R1+R2]}{2} \quad (2)$$

or

$$W = 2\pi \times [R1 + 0.5 \times L_G] \quad (3)$$

Fig.5 depicts that OFF current obtained on increasing gate length follow the trend contributed by short channel effect[14][25][7].OFF current of order $1*10^{-16}$ is obtained on 40 nm gate length which is significantly good.

Fig.6 shows total gate capacitance (Cgg) with applies gate voltage for different gate lengths at V_{DS} = 0 V. Increment in Cgg with increment in gate voltage up to flat-band voltage (V_{FB}) and get constant above it showing accumulation effects[14][15]. A great increment in total gate capacitance is observed on increasing channel length of device.

Fig. 7 shows I_D-V_G characteristics using different gate oxide materials. High-k materials rise capacitance helps in reducing leakage current due to its high dielectric constant value.

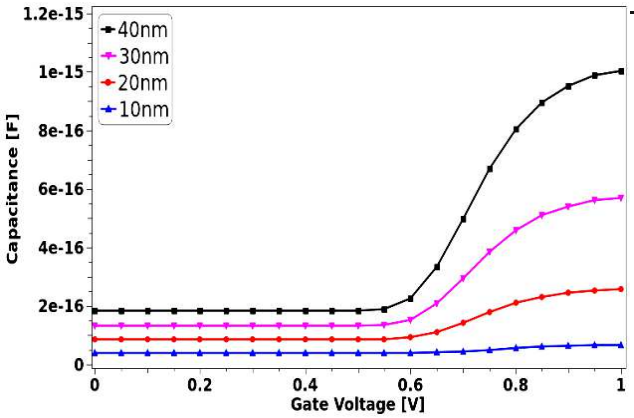


Fig. 6 Total gate capacitance (Cgg) with gate voltage at various channel length

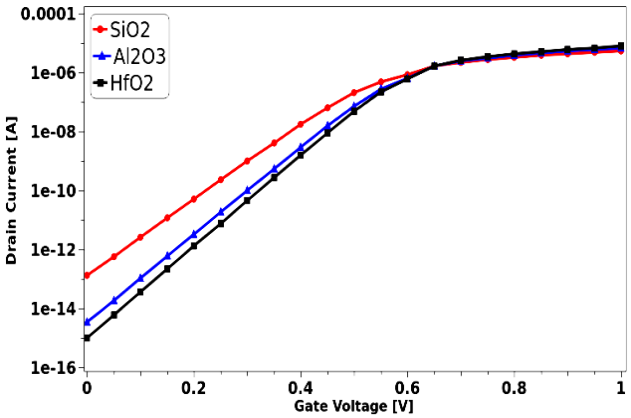


Fig. 7 I_D-V_G characteristics for different gate oxide material with Lg=30nm,T_{OX}=2nm and T_{ch}=5nm at V_{DS}=0.75V

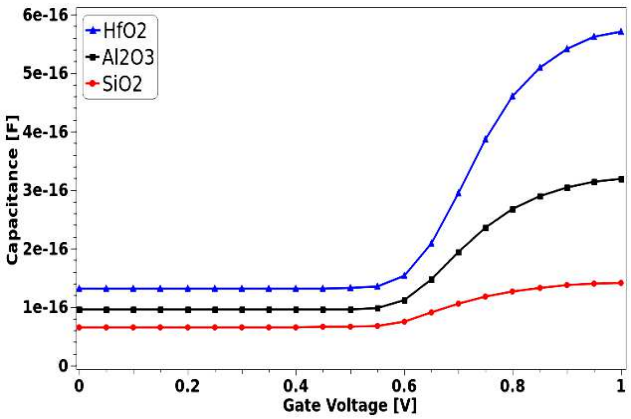


Fig. 8 Total Gate Capacitance variation with applied gate voltage for different oxide material

SiO2 allows tunneling which results in high leakage due to its low capacitance[8][25] as shown in Fig. 8. High-k dielectric increases barrier height and tunneling width which allows reduction in leakage current as well as increases in device total capacitance.

Fig. 9 shows Output characteristics of proposed DL-CG-MOSFET which with conspicuously similar to a regular MOSFET.

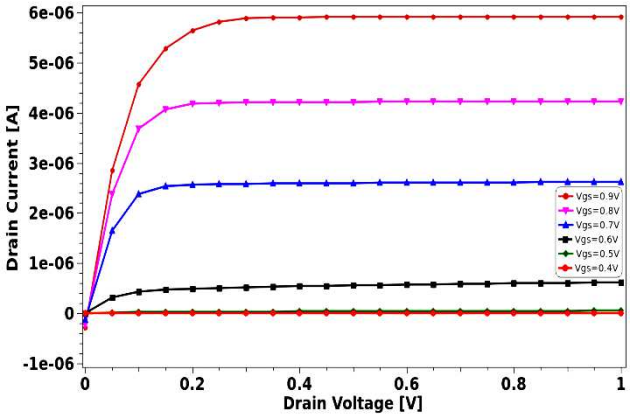


Fig. 9 I_D-V_D characteristics by varying V_{GS}

It is noticed that at lower value of V_{GS} drain current saturates earlier as compared to higher value due to limited space-charge inversion which shows greater control over channel[7][12]. Fig. 10 depicts transfer characteristics curve of proposed DL-CG-MOSFET on the basis of temperature difference. A significant temperature effect can be seen on OFF current of device and instead of ON current, OFF current increases with increase in temperature and show less leakage current at room temperature due to increase in carrier concentration with temperature[21][27]. Here no major increment is seen in ON current above room temperature due to scattering of phonon which limits the mobility in doping-less devices[14]. We further move to see the effect of source and drain size on device performance [Fig.11, 12].

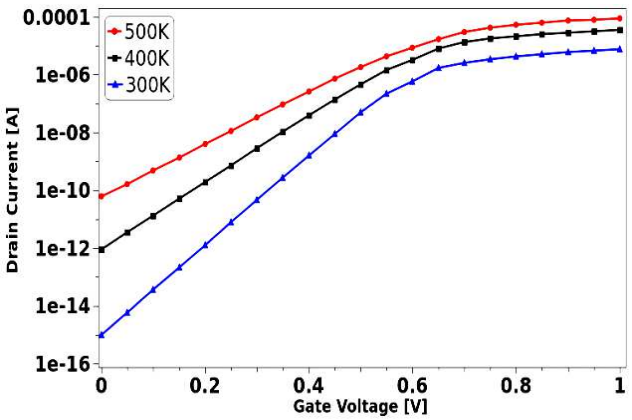


Fig. 10 Temperature effect on DL-CGT-MOSFET with Lg = 30nm, T_{OX} = 2nm and Tch = 5nm at V_{DS} = 0.75V

We compare the DL-CG-MOSFET with drain and source of same length as gate length (R1=R2=R3=40nm) and DL-CG-MOSFET with reduced drain and source (R1=R3=10nm and R2=40nm) [Fig.13]. As DL-CG-MOSFET with R1=R2=R3=40nm show more ON current due to increase in effective channel width and average circumference and DL-CG-MOSFET with R1=R3=10 nm show less OFF current due to smaller drain region[16]. From Fig13 and 14, we can observe that there is no major difference due to reduction length of

source and drain because schottky barrier depends upon metal work function and semiconductor interface[28]. That's why we further go for to see the effects of source and drain length on the device performance and calculate the performance parameter [fig. 13 and 14].

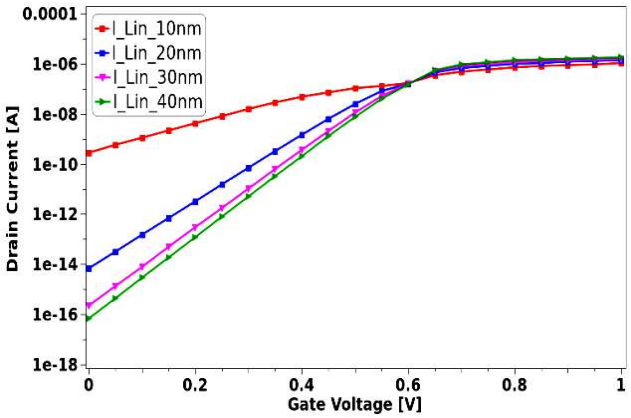


Fig. 11 I_{DS}-V_{GS} characteristics for different gate length with fixed source and drain length (R1 and R3=10nm) in linear region at V_{DS}=0.05V

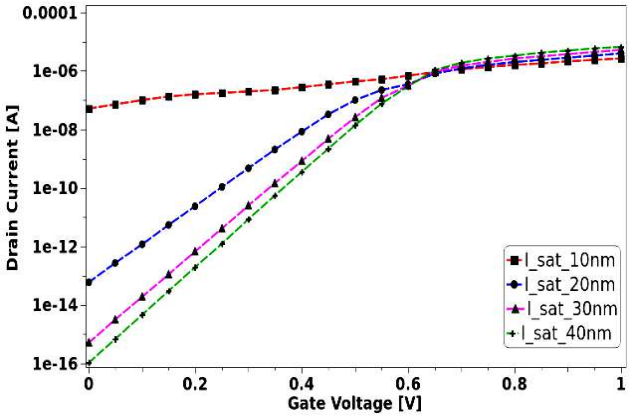


Fig. 12 I_{DS}-V_{GS} characteristics for different gate length with fixed source and drain length (R1 and R3=10nm) in saturation region at V_{DS}=0.75V

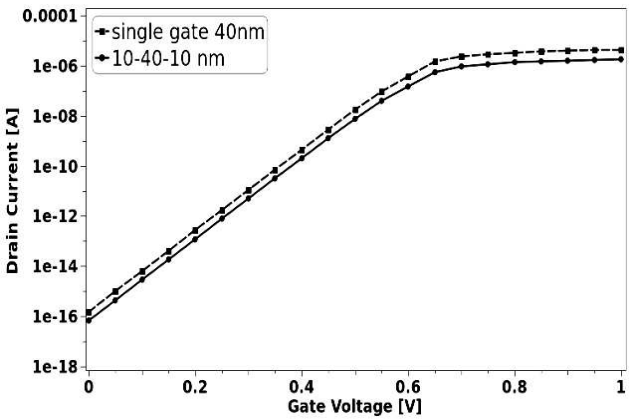


Fig. 13 Comparison of DL-CG-MOSFET with R1+R2+R3=40nm and DL-CG-MOSFET R1=R3=10nm & R2=40nm at VDS=0.05V

Further p type DL-CG-MOSFET also proposed and transfer characteristics for p type DL-CG-MOSFET and n type DL-CG-MOSFET at Vds_Lin=0.05V and Vds_sat=0.75V making V-curve shown in Fig. 15.

Design parameter taken same as proposed n type DL-CG-MOSFET and to match OFF current and ON current work-function engineering has been engaged[14][25]. V_{tsat} and V_{tlin} are nearly obtained 0.4V.

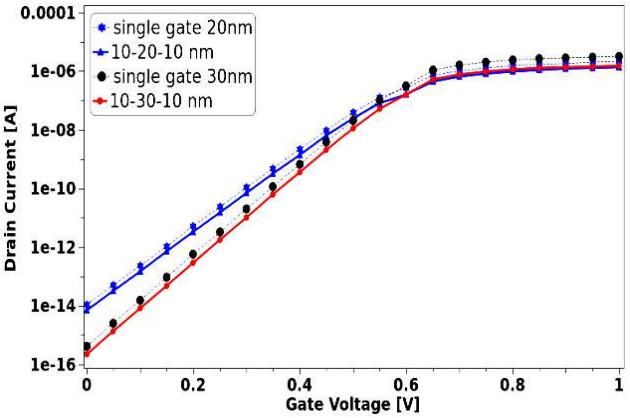


Fig. 14 Comparison of DL-CG-MOSFET keeping source/drain lengths constant with varying channel length at V_{DS}=0.05V

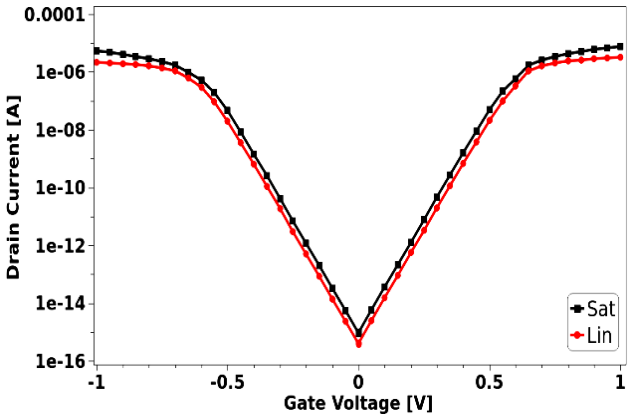


Fig. 15 Transfer characteristics for p type DL-CG-MOSFET and n type DL-CG-MOSFET at V_{DS}_Lin=0.05V and V_{DS}_sat=0.75V

The conventional metal oxide semiconductor devices (MOSFETs) set a sub- threshold slope or theoretical limits or Boltzmann limits up to 60 mV/decade due to its harmonics emission of an electron [5–8]. The extracted parameters for different channel thickness, oxide thickness and gate lengths is shown in tables 2, 3 and 4 which gives good performance.

Table 2 Performance comparison of DL-CG-MOSFET by varying channel thickness

Channel Thickness	SS(mV/dec)	DIBL(mV/V)
5 nm	60.7207	17.514
8 nm	62.2415	26.1174
10 nm	63.9636	34.5717

Table 3 Performance comparison of DL-CG-MOSFET by changing gate oxide thickness

Oxide Thickness	SS(mV/dec)	DIBL(mV/V)
2 nm	60.7207	17.514
3 nm	61.599	22.1052
4 nm	62.6335	28.3901

Table 4 Performance comparison of DL-CG-MOSFET with different gate lengths

Gate Length	V_{tlin}[V]	V_{tsat}[V]	SS(mV/dec)	DIBL(mV/V)	I_{ON}	I_{OFF}
20 nm	0.449411	0.387661	74.913	88.2138	1e-06	1e-14
30 nm	0.476074	0.451468	63.9635	35.1513	1e-06	1e-15
40 nm	0.483322	0.467808	61.5114	22.1624	1e-05	1e-16

4 Conclusions

A dopingless device with source/drain schottky contacts concept based simulations using cogenda visual TCAD have been used to study n-DL-CG-MOSFET with varying dimensions. The completely self-contained channel inside the device eliminates drain-to-source leakage induced by interface charges. An improvement in SS=61.51mV/dec, DIBL=22.16mV/V, I_{ON} and I_{OFF} ratio=1e+11 is obtained on increasing the gate length and opposite effect can be seen on increasing the oxide and channel thickness. Dopingless device helps in reducing SCEs due to avoidance of ultra-sharp abrupt region formed in conventional MOSFETs helps in further scaling the technology node. ON and OFF current both increase with temperature. High-k dielectric materials like HfO_2 shows low leakage current due to its high capacitance and capacitance also increased with increment in gate length. As functioning of dopingless device depends on metal work-function and intrinsic channel material so there is no major effect is shown after the reduction of source/drain length. Fabrication becomes simpler and less cost effective due to avoidance of mask in S/D region during fabrication in dopingless S/D schottky MOSFETs. Further the behaviour of p/n DL-CG-MOSFETs is studied in both linear and saturation region.

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