

Active Current Balancing for the Current-Sensorless Interleaved Boost Converter Under Severe Branch Asymmetries

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Research Article

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Active Current Balancing for the Current-Sensorless Interleaved Boost Converter Under Severe Branch Asymmetries

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Abstract

This paper presents an output-voltage-based active current-balancing method for a two-phase current sensorless interleaved boost converter. The method supplements a previously developed robust output voltage controller with an auxiliary balancing loop that requires neither input-current nor individual phase-current measurements. A first-order filter reconstructs the capacitor-voltage waveform from the measured converter output voltage. Phase-associated voltage peaks are then extracted and their difference is processed by a proportional-integral controller. The resulting correction is added to the nominal duty ratio of one converter phase and subtracted from that of the other, thereby reducing the average phase-current mismatch while preserving the nominal total duty-ratio command. Simulation results for operating conditions below and above a duty ratio of 0.5 demonstrate improved current sharing under unequal phase inductances, winding resistances, and output-capacitor equivalent series resistance. The method also maintains output-voltage regulation during the balancing process. These preliminary results establish the feasibility of output-voltage-only active current balancing and motivate future experimental validation. Furthermore, exact, non-linear transcendental equations modeling sub-period charge delivery for both overlapping and non-overlapping operating regions are developed and detailed for completeness in the appendices.

Index Terms

Interleaved boost converter, current-sensorless control, active current balancing, charge-area evaluation, peak sampling, parameter asymmetry.

I. INTRODUCTION

Interleaved boost converters distribute the input current among parallel converter phases, reducing current ripple and component stresses. In practice, unequal phase inductances, winding resistances, switching-device characteristics, and parasitic elements can produce substantial phase-current imbalance. Persistent imbalance increases conduction losses and thermal stress and may prevent the converter phases from sharing power as intended.

Conventional current-sharing methods generally use individual phase-current measurements to regulate the current of each converter leg. Although effective, this approach increases sensing, conditioning, calibration, and implementation requirements. Current-sensorless voltage controllers avoid some of this hardware, but output-voltage regulation alone does not necessarily ensure balanced phase currents when the converter-leg parameters are unequal.

The present paper extends [1] by introducing an output-voltage-based active current-balancing loop. A first-order filter reconstructs the capacitor-voltage waveform from the measured terminal voltage, and phase-associated voltage peaks are extracted from the reconstructed signal. Their difference is processed by a proportional-integral controller to generate a differential duty-ratio correction. The correction is added to one phase command and subtracted from the other, allowing the phase-current distribution to be adjusted without altering the nominal common duty-ratio command or introducing current sensors. The method is evaluated through switched-circuit simulations for duty ratios below and above 0.5 under converter-leg parameter mismatches and output-capacitor parasitics.

The remainder of the paper presents the balancing principle, simulation results, and conclusions.

II. CONVERTER AND BASELINE CONTROLLER

A. Two-phase interleaved boost converter averaged model

A basic two-phase interleaved boost converter averaged model is shown in Figure 1.

For the derivation of the nominal averaged model, the equivalent series resistance of the output capacitor is neglected. Under this assumption, the load-terminal output voltage v_o and the internal capacitor voltage v_c coincide, such that $v_o = v_c$ in the

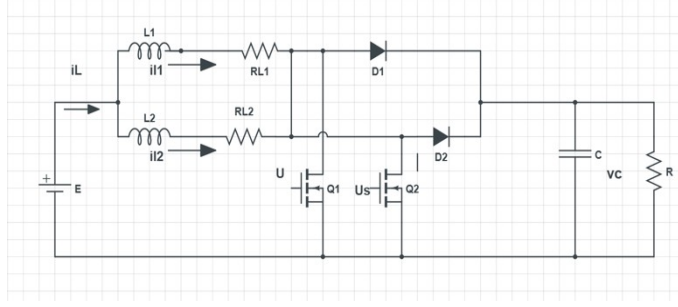


Fig. 1. Circuit diagram of the two-phase interleaved boost converter.

averaged representation. This approximation is adopted only in the nominal model described by (1); the distinction between v_o and v_c is retained in the capacitor-voltage reconstruction and detailed switched-circuit simulation. Under continuous conduction mode, the averaged model is:

$$\begin{aligned}\dot{i}_{L_1} &= -\frac{R_{L_1}}{L_1}i_{L_1} - (1-u)\frac{v_c}{L_1} + \frac{E}{L_1} \\ \dot{i}_{L_2} &= -\frac{R_{L_2}}{L_2}i_{L_2} - (1-u)\frac{v_c}{L_2} + \frac{E}{L_2} \\ \dot{v}_c &= (1-u)\frac{i_{L_1}}{C} + (1-u)\frac{i_{L_2}}{C} - \frac{v_c}{RC}\end{aligned}\quad (1)$$

where i_{L_1} and i_{L_2} denote the average currents through inductors L_1 and L_2 , respectively, and v_c denotes the internal capacitor voltage. Because the capacitor ESR is neglected in (1), the load current is represented by v_c/R , and the load-terminal voltage satisfies $v_o = v_c$ within the nominal averaged model. When the capacitor ESR is included in the detailed switched-circuit model, v_o and v_c are treated as distinct voltages. The unknown parameters E , C and R represent the input voltage, the capacitance and the load resistance, respectively with known nominal values E_o , C_o and R_o . The control input u to the converter is the duty ratio function and u_s is the same duty ratio as u but staggered in phase by an angle of 180° .

The extended estimator of [1], is given by

$$\begin{aligned}\dot{q}_1 &= \frac{u}{L_o C_o} \left[4(e_2 + V_{ref}) - 2E_o \right] \\ &\quad + q_3 + K_3 e_2 - K_1 q_1 - K_1^2 e_2 \\ \dot{q}_2 &= q_1 + K_1 e_2 + K_2 \tilde{q}_2 \\ \dot{q}_3 &= -K_3 q_1 - K_1 K_3 e_2\end{aligned}\quad (2)$$

The trajectories $\hat{e}_1$, $\hat{e}_2$ and $\hat{d}$ denote the reconstructed values of $e_1 = \dot{e}_2$, $e_2 = v_c - V_{ref}$ and the lumped uncertainty d , respectively, and are algebraically generated via:

$$\hat{e}_1 = q_1 + K_1 e_2, \quad \hat{e}_2 = q_2, \quad \hat{d} = q_3 + K_3 e_2 \quad (3)$$

The linear sliding manifold is :

$$\sigma = \hat{e}_1 + \gamma \hat{e}_2 - K_1 e_2 = q_1 + \gamma q_2 \quad (4)$$

and the The tracking control law u is given by:

$$\begin{aligned}u &= \alpha (K_1 - \gamma) q_1 - \alpha q_3 \\ &\quad + \alpha (-K_3 + K_1^2 - \gamma K_1) e_2 - \alpha K_2 \gamma \tilde{q}_2 - \alpha K_4 \sigma\end{aligned}\quad (5)$$

with the auxiliary gain variable α formulated as:

$$\alpha = \frac{L_o C_o}{[4(e_2 + V_{ref}) - 2E_o]} \quad (6)$$

III. OUTPUT-VOLTAGE-BASED CURRENT-SHARING METHOD

By exploiting the discrete, high-frequency voltage ripple dynamics across the output capacitor, a synchronized peak-sampling routine extracts the local boundary points (V_{C_1} and V_{C_2}) at the falling edges of the alternating gate drive signals, please see Fig. 2. A linear proportional-integral (PI) regulator subsequently forces these discrete values to be equal ($V_{C_1} = V_{C_2}$), minimizing the sub-period charge-area delivery mismatch and partially balances the two legs of the converter.

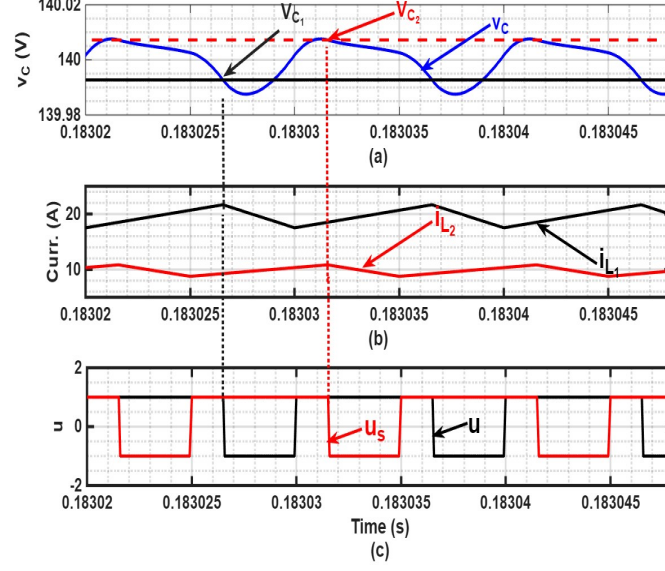


Fig. 2. transient responses: (a) capacitor voltage $v_C(t)$ with the two phase-associated voltage V_{C1} and V_{C2} extracted from v_C , (b) phase currents i_{L1} in (black) and i_{L2} in (red), and (c) duty ratios u in black and u_s in red.

A. Estimating the internal capacitor voltage

The output voltage v_o across the load resistor R is related to the capacitor voltage v_c and current capacitor i_c by

$$v_o = v_c + r_{C_o} i_c = v_C + r_{C_o} C_o \frac{dv_C}{dt} \quad (7)$$

and in the Laplace domain we have

$$V_C(s) = \frac{1}{r_{C_o} C_o s + 1} V_o(s) \quad (8)$$

Let the voltage imbalance

$$e_{v_c} = V_{C1} - V_{C2} \quad (9)$$

with the auxiliary PI controller

$$\Delta u = K_p e_{v_c} + K_i \int_0^t e_{v_c} d\tau \quad (10)$$

and the phase duty ratios are modified according to

$$u_1 = u + \Delta u, \quad u_2 = u - \Delta u \quad (11)$$

with u_2 staggered in phase by an angle of 180° .

The PI controller attempts to drive $V_{C1} \approx V_{C2}$ and therefore $\bar{I}_{L1} \approx \bar{I}_{L2}$ with $\bar{I}_{Lj}, j \in \{1, 2\}$, the average phase current

$$\bar{I}_{Lj} = \frac{1}{T_s} \int_{t_p}^{t_p+T_s} i_{Lj}(\tau) d\tau, \quad j \in \{1, 2\}. \quad (12)$$

The resulting current-sharing error can be defined as

$$\epsilon = \frac{|\bar{I}_{L1} - \bar{I}_{L2}|}{(\bar{I}_{L1} + \bar{I}_{L2})/2} \times 100\% \quad (13)$$

IV. SIMULATION RESULTS

To validate the robustness and map the operational boundaries of the proposed current-sensorless active balancing loop, a structured multi-scenario simulation pipeline was established in Table II. The input voltage is held constant at $E = 12$ V, while the target reference voltage V_{ref} is adjusted to sweep across the requested theoretical duty ratios ($D_o = 0.35, 0.38, 0.4, 0.45, 0.5, 0.55, 0.6$). Severe manufacturing asymmetries ($\pm 20\%$) are applied to the branch inductances (L_1, L_2) and winding resistances (R_{L1}, R_{L2}) to simulate worst-case industrial operating environments. Table I lists the nominal values of the DC converter, the proposed controller/estimator gains with the PI auxiliary controller gains.

Remark 1

To stabilize the current-balancing control loop of the interleaved boost converter at a switching frequency of $f_s = 100$ kHz with a continuous output voltage of $v_o = 24$ V, a high-performance capacitor bank must be selected. The design constraints require a total capacitance of $C_{bank} \approx 300 \mu F$. To provide a safe voltage overhead margin against switching transients, individual capacitors are selected with a rated voltage much greater than 24 V. Conductive hybrid conductive-polymer capacitors are selected due to their exceptionally low native ESR characteristics at high frequencies.

The capacitor selected is a CapXon AA-series 150 microfarad hybrid conductive-polymer capacitor with a rated voltage of 63 V and a maximum equivalent series resistance of 0.0015Ω at a frequency of 100 kHz. When two identical capacitors are arranged in a parallel layout, the equivalent resistance decreases to a maximum of 0.0075Ω at a frequency of 100 kHz. By keeping the bank's combined ESR under $10 m\Omega$, the high-frequency internal voltage drop $r_C \cdot i_C$ becomes negligible. This allows the measured terminal voltage $v_o(t)$ to accurately mirror the true internal capacitor state $v_c(t)$, preventing control loop instabilities in the current-sensorless balancing algorithm.

To evaluate the performance of the proposed current-sensorless active balancing loop under severe hardware asymmetries, comprehensive switched-circuit simulations were executed utilizing the system specifications outlined in Table II. The primary figure of merit chosen to assess the phase current mismatch is the sharing error ϵ , defined mathematically in (13).

A. Discussion of the Simulation Results

Table III demonstrates that the proposed auxiliary controller substantially improves phase-current sharing under severe converter-leg asymmetry. Without auxiliary correction, the current-sharing error remains approximately 40% in all asymmetric cases. With active balancing, the error decreases to 3.42%, 0.81%, 0.72%, and 1.36% for $D_o = 0.45, 0.50, 0.55$, and 0.60 , respectively. At $D_o = 0.40$, the error is reduced from 39.94% to 8.51%, indicating that the balancing accuracy begins to deteriorate near the lower operating boundary. The controller also maintains current-sharing errors below 2.26% under the tested capacitance and ESR variations and below 1% when the converter-leg asymmetry is reversed. In all cases, output-voltage regulation is preserved during the balancing process.

The degradation becomes more pronounced for $D_o < 0.40$. At $D_o = 0.38$ and $D_o = 0.35$, the auxiliary controller reduces the current-sharing error from approximately 40% to 12.23% and 22.89%, respectively, but does not achieve close current sharing. As the duty ratio decreases, the phase-associated capacitive ripple components become smaller, while the ESR-induced voltage discontinuities become increasingly influential in the sampled terminal-voltage peaks. Consequently, the peak-voltage error $e_{v_c} = V_{C1} - V_{C2}$ progressively loses its correlation with the difference between the average phase currents. The results therefore identify $D_o \approx 0.40$ as an empirical lower operating boundary for accurate peak-voltage-based current balancing under the investigated converter parameters, rather than as a universal analytical limit.

TABLE I
NOMINAL SYSTEM SPECIFICATIONS

Parameter Description	Symbol	Nominal Value
Input Voltage	E	12 V
Nominal Capacitance	C	$300 \mu F$
Equivalent Series Resistance	r_C	0.0075Ω
Nominal Load Resistance	R	20Ω
Switching Frequency	f_s	100 kHz
Phase 1 and 2 Inductances	L_1, L_2	$330 \mu H$
Phase 1 and 2 Resistance	R_{L1}, R_{L2}	0.1Ω
<i>Controller & Estimator Gains</i>		
Estimator Gain	K_1	5×10^3
Estimator Gain	K_2	12.50×10^3
Estimator Gain	K_3	6.25×10^6
Sliding Control Gain	K_4	10^3
Sliding Surface Design Parameter	γ	6.25×10^3
<i>Balancing Auxiliary PI Controller gains</i>		
Proportional Gain	K_p	0.01
Integral Gain	K_i	100

B. Nominal Baseline and Steady-State Optimization

Initially, a symmetric baseline control group was established under nominal parameters ($L_1 = L_2 = 330 \mu H$, $R_{L1} = R_{L2} = 0.1 \Omega$) operating at a duty cycle of $D_o = 0.5$ (Sim 1). As seen in Fig. 3, under these ideal conditions, the current-sharing loop converges rapidly, yielding an exceptional residual current-sharing error of $\epsilon \approx 0\%$ and illustrating the perfect ripple-cancellation effect.

TABLE II
SYSTEMATIC SIMULATION MATRIX

Sim.	Test Group	D_o	V_{ref} (V)	L_1 (μH)	R_{L1} (Ω)	L_2 (μH)	R_{L2} (Ω)	C (μF)	r_C (Ω)
1	Symmetric baseline	0.50	24.00	330	0.10	330	0.10	300	0.0075
2	Duty-ratio sweep	0.40	20.00	264	0.08	396	0.12	300	0.0075
3	Duty-ratio sweep	0.45	21.82	264	0.08	396	0.12	300	0.0075
4	Duty-ratio sweep	0.50	24.00	264	0.08	396	0.12	300	0.0075
5	Duty-ratio sweep	0.55	26.67	264	0.08	396	0.12	300	0.0075
6	Duty-ratio sweep	0.60	30.00	264	0.08	396	0.12	300	0.0075
7	Lower-boundary test	0.35	18.46	264	0.08	396	0.12	300	0.0075
8	Lower-boundary test	0.38	19.35	264	0.08	396	0.12	300	0.0075
9	Low-capacitance case	0.50	24.00	264	0.08	396	0.12	240	0.0075
10	High-capacitance case	0.50	24.00	264	0.08	396	0.12	360	0.0075
11	Low-ESR case	0.50	24.00	264	0.08	396	0.12	300	0.00375
12	High-ESR stress case	0.50	24.00	264	0.08	396	0.12	300	0.015
13	Reversed leg asymmetry	0.50	24.00	396	0.12	264	0.08	300	0.0075

The input voltage and switching frequency are fixed at $E = 12$ V and $f_s = 100$ kHz, respectively. The capacitor-voltage reconstruction filter parameters are fixed at $C_o = 300$ μF and $r_{Co} = 0.0075$ Ω for all simulations. Each asymmetric case is evaluated both without auxiliary correction ($\Delta u = 0$) and with the proposed active-balancing correction. Here, D_o denotes the theoretical target duty ratio. The actual steady-state duty ratio obtained from the switched-circuit simulation is reported separately in Table III.

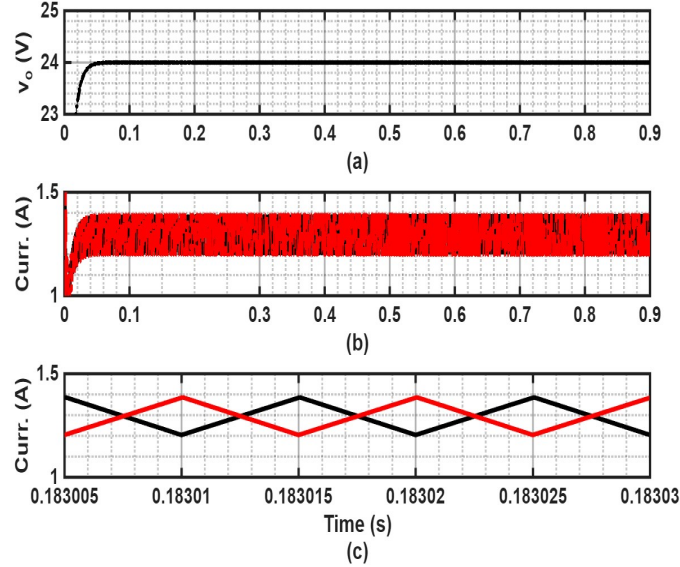


Fig. 3. Simulation 1: Transient responses for $D_o=0.5$ for the symmetric baseline with active-balancing controller enabled at $t=0.3$ s: (a) output-voltage response $v_o(t)$, (b) phase currents i_{L1} (black) and i_{L2} (red), and (c) magnified view illustrating the complete ripple-cancellation effect.

C. Duty Cycle Boundary Trajectory

To map the operational limits of the peak-tracking algorithm, a systemic parametric sweep was conducted across varying voltage references to alter the steady-state operating duty cycles ($D = 0.40, 0.45, 0.50, 0.55, 0.60$).

V. CONCLUSION

This paper presented an output-voltage-based active current-balancing method for a two-phase current-sensorless interleaved boost converter. The method supplements the robust voltage controller developed in [1] with an auxiliary balancing loop that requires neither input-current nor individual phase-current measurements. A first-order filter reconstructs the capacitor-voltage waveform from the measured converter output voltage, while synchronized peak sampling and a PI controller generate a differential duty-ratio correction that is added to one phase command and subtracted from the other.

Switched-circuit simulations under severe converter-leg asymmetry showed that the proposed method substantially improves phase-current sharing while preserving output-voltage regulation. Without auxiliary correction, the current-sharing error was

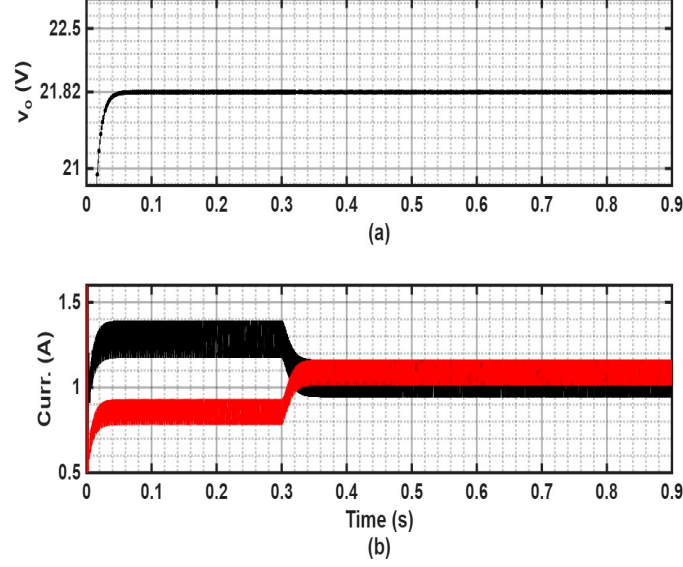


Fig. 4. Simulation 3: Transient responses for $D_o=0.45$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) output-voltage response $v_o(t)$; (b) phase currents i_{L1} (black) and i_{L2} (red).

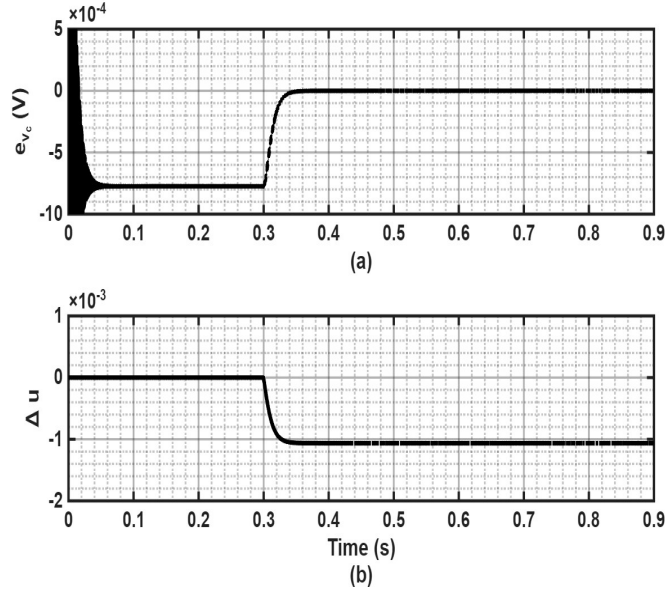


Fig. 5. Simulation 3: Transient responses for $D_o=0.45$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) voltage peak error $e_{v_c} = V_{C1} - V_{C2}$, and (b) duty-ratio differential $\Delta u(t)$.

approximately 40% in all asymmetric cases. With active balancing, the error was reduced to between 0.72% and 3.42% for $0.45 \leq D_o \leq 0.60$, while an error of 8.51% was obtained at $D_o = 0.40$. The method also maintained errors below 2.26% under the investigated capacitance and ESR variations and below 1% when the converter-leg asymmetry was reversed.

For $D_o < 0.40$, the current-sharing error increased as the sampled peak-voltage difference progressively lost its correlation with the average phase-current difference. This degradation results from attenuation of the phase-associated capacitive ripple and the increasing influence of ESR-induced voltage discontinuities. Consequently, $D_o \approx 0.40$ represents an empirical lower operating boundary for accurate peak-voltage-based current balancing under the investigated parameters. Future work will focus on experimental validation, sensitivity to sampling and measurement noise, and extension of the balancing method to converters with more than two interleaved phases.

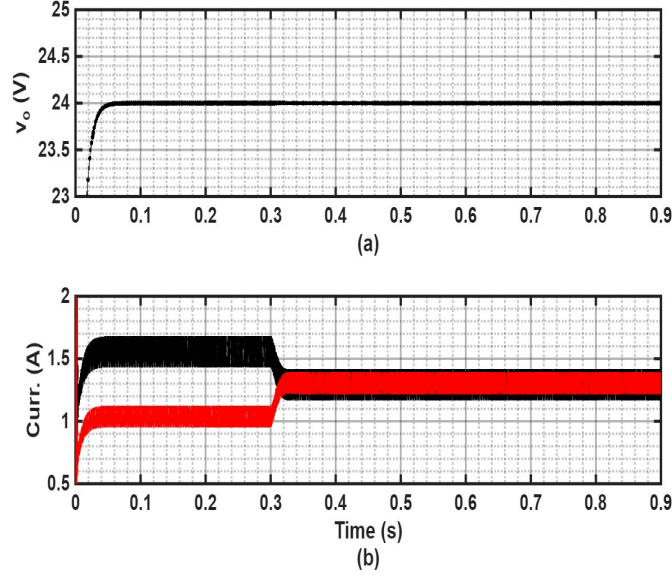


Fig. 6. Simulation 4: Transient responses for $D_o=0.5$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) output-voltage response $v_o(t)$; (b) phase currents i_{L1} (black) and i_{L2} (red).

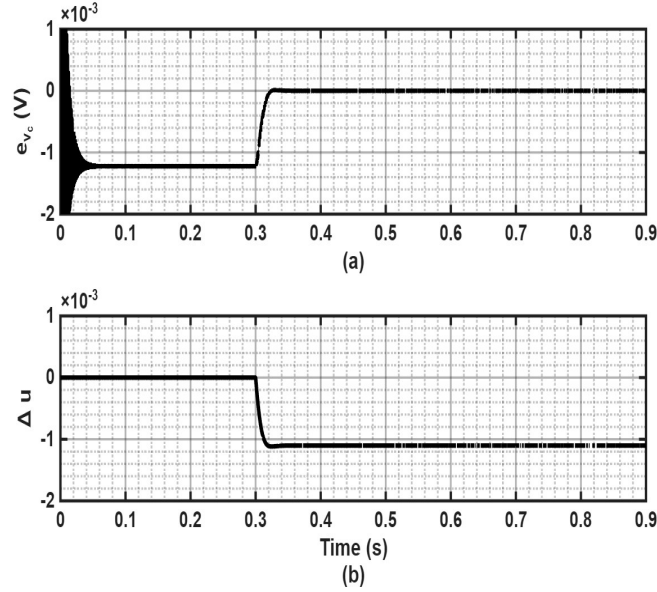


Fig. 7. Simulation 4: Transient responses for $D_o=0.5$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) voltage peak error $e_{v_c} = V_{C1} - V_{C2}$, and (b) duty-ratio differential $\Delta u(t)$.

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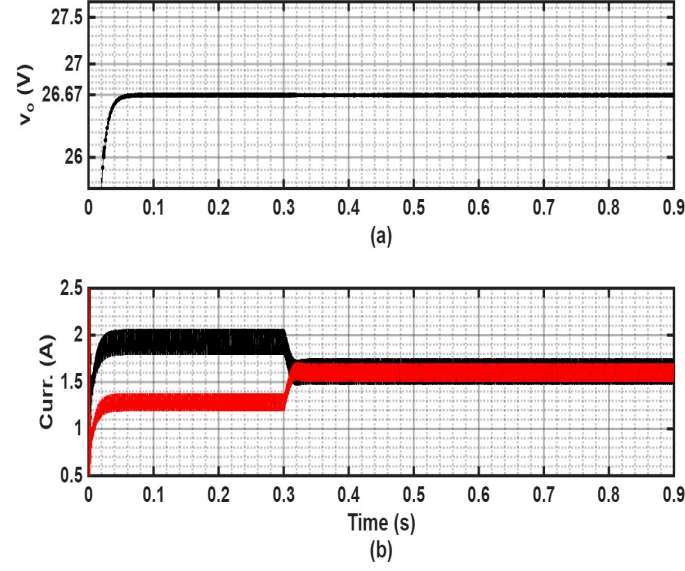


Fig. 8. Simulation 5: Transient responses for $D_o=0.55$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) output-voltage response $v_o(t)$; (b) phase currents i_{L1} (black) and i_{L2} (red).

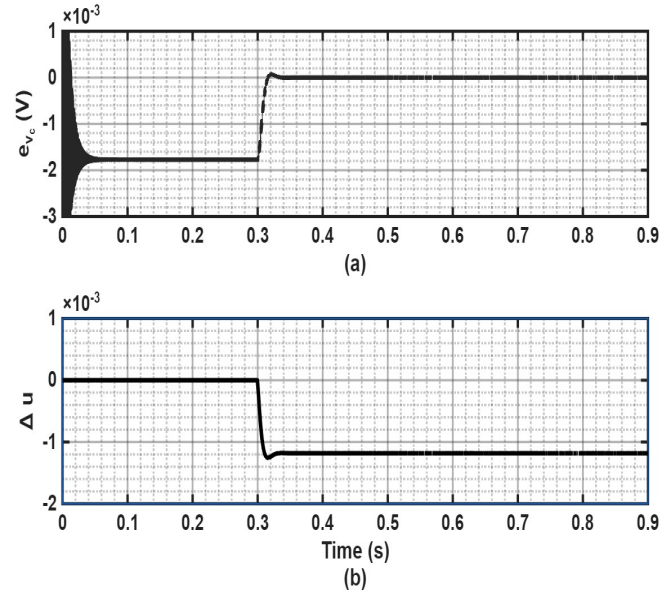


Fig. 9. Simulation 5: Transient responses for $D_o=0.55$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) voltage peak error $e_{v_c} = V_{C1} - V_{C2}$, and (b) duty-ratio differential $\Delta u(t)$.

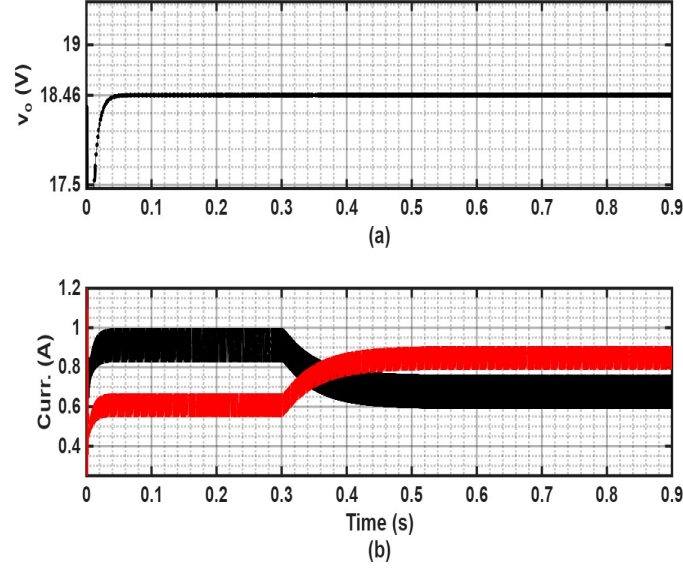


Fig. 10. Simulation 7: Transient responses for $D_o=0.35$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) output-voltage response $v_o(t)$; (b) phase currents i_{L1} (black) and i_{L2} (red).

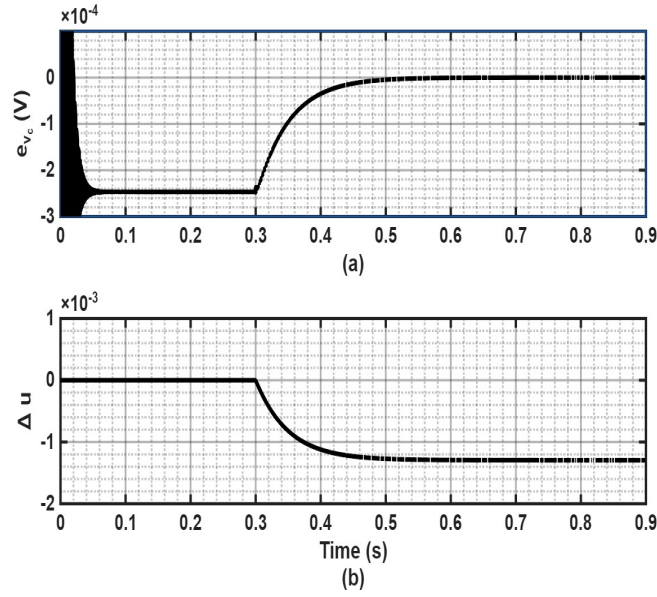


Fig. 11. Simulation 7: Transient responses for $D_o=0.35$ under severe converter-leg asymmetry with active-balancing controller enabled at $t=0.3$ s: (a) voltage peak error $e_{v_c} = V_{C1} - V_{C2}$, and (b) duty-ratio differential $\Delta u(t)$.

TABLE III
COMPARATIVE ANALYSIS OF CURRENT SHARING PERFORMANCE WITH AND WITHOUT AUXILIARY CORRECTION

Sim	$D_o \backslash D$	Test Group	Without Auxiliary Correction ($\Delta u = 0$)			With Active Balancing Correction		
			Error ϵ (%)	Avg. I_{L1} (A)	Avg. I_{L2} (A)	Error ϵ (%)	Avg. I_{L1} (A)	Avg. I_{L2} (A)
1	$D_o = 0.50$, $D = 0.505443$	Symmetric baseline	0	1.295082	1.295082	0.162304	1.296503	1.294400
2	$D_o = 0.40$, $D = 0.405154$	Duty-ratio sweep	39.941236	1.075258	0.717277	8.513846	0.858736	0.935098
3	$D_o = 0.45$, $D = 0.455476$	Duty-ratio sweep	39.948170	1.283902	0.856397	3.421494	1.052586	1.089227
4	$D_o = 0.50$, $D = 0.505851$	Duty-ratio sweep	39.959149	1.557290	1.038635	0.813615	1.293637	1.304205
5	$D_o = 0.55$, $D = 0.556736$	Duty-ratio sweep	39.970637	1.925881	1.284313	0.718432	1.612157	1.600616
6	$D_o = 0.60$, $D = 0.607762$	Duty-ratio sweep	39.980090	2.440690	1.627464	1.364130	2.049836	2.022063
7	$D_o = 0.35$, $D = 0.354832$	Lower-boundary test	39.938839	0.912219	0.608534	22.892159	0.673949	0.848172
8	$D_o = 0.38$, $D = 0.385025$	Lower-boundary test	39.939716	1.005384	0.670677	12.231253	0.787377	0.889956
9	$D_o = 0.50$, $D = 0.505940$	Low-capacitance case	39.948400	1.536527	1.024902	1.377449	1.272774	1.290428
10	$D_o = 0.50$, $D = 0.505815$	High-capacitance case	39.966291	1.578037	1.052394	0.264194	1.314507	1.317985
11	$D_o = 0.50$, $D = 0.505670$	Low-ESR case	39.958204	1.505560	1.004144	2.254644	1.241475	1.269785
12	$D_o = 0.50$, $D = 0.506214$	High-ESR stress case	39.960866	1.660858	1.107690	1.800550	1.398069	1.373120
13	$D_o = 0.50$, $D = 0.505510$	Reversed leg asymmetry	39.959149	1.038635	1.557290	0.970950	1.304866	1.292258

APPENDIX A

EXACT CHARGE-AREA DERIVATIONS FOR NON-OVERLAPPING OPERATION ($D < 0.5$)

To formulate the current-sensorless active-balancing condition when the steady-state duty ratio is below 0.5, the two converter legs must be tracked individually. The auxiliary balancing command is applied differentially as

$$D_1 = D + \Delta D, \quad D_2 = D - \Delta D, \quad (\text{A.1})$$

where the admissible correction must satisfy $0 < D_1 < 0.5$ and $0 < D_2 < 0.5$. For converter leg $j \in \{1, 2\}$, define

$$\gamma_j = \frac{R_{Lj}}{L_j}, \quad A_j = \frac{E}{R_{Lj}}, \quad B_j = \frac{E - V_o}{R_{Lj}}. \quad (\text{A.2})$$

Here, A_j and B_j are the equilibrium-current terms associated with the ON and OFF current equations, respectively. The corresponding exponential factors are

$$a_j = e^{-\gamma_j D_j T_s}, \quad b_j = e^{-\gamma_j (1-D_j) T_s}. \quad (\text{A.3})$$

Under periodic steady-state operation, the maximum current in leg j is

$$I_{Lj,\max} = \frac{A_j(1-a_j) + a_j B_j(1-b_j)}{1-a_j b_j}. \quad (\text{A.4})$$

Equations (A.2)–(A.4) retain the unequal inductances and winding resistances of the two converter legs. For $0 < D < 0.5$, the two switch-ON intervals do not overlap. The gate signals are displaced by $T_s/2$. Let $t = 0$ be the falling edge of the Phase-2 gate signal. The switching boundaries within the following period are

$$t_{b1} = (0.5 - D_2)T_s, \quad (\text{A.5})$$

$$t_{b2} = (0.5 + D_1 - D_2)T_s, \quad (\text{A.6})$$

$$t_{b3} = (1 - D_2)T_s. \quad (\text{A.7})$$

The switching states are therefore

$$\begin{cases} 0 \leq t < t_{b1} : & \text{both switches OFF,} \\ t_{b1} \leq t < t_{b2} : & \text{Switch 1 ON, Switch 2 OFF,} \\ t_{b2} \leq t < t_{b3} : & \text{both switches OFF,} \\ t_{b3} \leq t < T_s : & \text{Switch 1 OFF, Switch 2 ON.} \end{cases} \quad (\text{A.8})$$

A. First Subperiod

At $t = 0$, Switch 2 has just turned OFF and $i_{L2}(0) = I_{L2,\max}$. Hence, for $0 \leq t < t_{b2}$,

$$i_{L2}(t) = B_2 + (I_{L2,\max} - B_2) e^{-\gamma_2 t}. \quad (\text{A.9})$$

During $0 \leq t < t_{b1}$, Phase 1 is also OFF. Its current at $t = 0$ is

$$I_{p1} = B_1 + (I_{L1,\max} - B_1) e^{-\gamma_1 [0.5 + (D_2 - D_1)] T_s}, \quad (\text{A.10})$$

and its OFF-state current over this interval is

$$i_{p1}(t) = B_1 + (I_{p1} - B_1) e^{-\gamma_1 t}. \quad (\text{A.11})$$

The total charge delivered by the converter legs during the first subperiod is

$$\begin{aligned} Q_a &= \int_0^{t_{b2}} i_{L2}(t) dt + \int_0^{t_{b1}} i_{p1}(t) dt \\ &= B_2 t_{b2} + \frac{I_{L2,\max} - B_2}{\gamma_2} (1 - e^{-\gamma_2 t_{b2}}) \\ &\quad + B_1 t_{b1} + \frac{I_{p1} - B_1}{\gamma_1} (1 - e^{-\gamma_1 t_{b1}}). \end{aligned} \quad (\text{A.12})$$

Consequently,

$$C(V_{P2} - V_{P1}) = Q_a - I_o t_{b2}. \quad (\text{A.13})$$

B. Second Subperiod

At $t = t_{b2}$, Switch 1 has just turned OFF and therefore $i_{L1}(t_{b2}) = I_{L1,\max}$. It is important that the exponential decay in this interval be measured from t_{b2} , rather than from $t = 0$. Thus, for $t_{b2} \leq t < T_s$,

$$i_{L1}(t) = B_1 + (I_{L1,\max} - B_1) e^{-\gamma_1(t-t_{b2})}. \quad (\text{A.14})$$

The Phase-2 current at $t = t_{b2}$ is

$$I_{p2} = B_2 + (I_{L2,\max} - B_2) e^{-\gamma_2[0.5+(D_1-D_2)]T_s}. \quad (\text{A.15})$$

During the interval in which Phase 2 remains OFF,

$$i_{p2}(t) = B_2 + (I_{p2} - B_2) e^{-\gamma_2(t-t_{b2})}, \quad t_{b2} \leq t < t_{b3}. \quad (\text{A.16})$$

The total charge delivered by the converter legs during the second subperiod is therefore

$$\begin{aligned} Q_b &= \int_{t_{b2}}^{T_s} i_{L1}(t) dt + \int_{t_{b2}}^{t_{b3}} i_{p2}(t) dt \\ &= B_1(T_s - t_{b2}) + \frac{I_{L1,\max} - B_1}{\gamma_1} [1 - e^{-\gamma_1(T_s - t_{b2})}] \\ &\quad + B_2(t_{b3} - t_{b2}) + \frac{I_{p2} - B_2}{\gamma_2} [1 - e^{-\gamma_2(t_{b3} - t_{b2})}]. \end{aligned} \quad (\text{A.17})$$

The corresponding capacitor-voltage variation is

$$C(V_{P1} - V_{P2}) = Q_b - I_o(T_s - t_{b2}). \quad (\text{A.18})$$

C. Balancing Condition

Periodic steady-state charge balance requires

$$Q_a + Q_b = I_o T_s. \quad (\text{A.19})$$

Subtracting (A.18) from (A.13) gives the scalar nonlinear balancing equation

$$F(\Delta D) = Q_a - Q_b + I_o(T_s - 2t_{b2}) = 0. \quad (\text{A.20})$$

Under (A.19), satisfying (A.20) gives

$$Q_a - I_o t_{b2} = 0, \quad Q_b - I_o(T_s - t_{b2}) = 0, \quad (\text{A.21})$$

and therefore $V_{P1} = V_{P2}$. Equation (A.20) can be solved numerically for ΔD using a bracketed scalar root solver, subject to the duty-ratio constraints on D_1 and D_2 .

The preceding expressions are exact within the assumed piecewise converter model, which retains L_j and R_{Lj} but treats E and V_o as constant over one switching period and neglects semiconductor voltage drops and output-capacitor ESR.

The model was evaluated using $E = 12$ V, $V_{\text{ref}} = 21.82$ V, $C = 300$ μ F, and $T_s = 10^{-5}$ s. Two inverted parameter-asymmetry cases were considered. The analytical correction was obtained by solving (A.20) with the corrected second-subperiod charge expression (A.17).

D. Case 1: $R_{L1} < R_{L2}$

The converter parameters were $L_1 = 264$ μ H, $R_{L1} = 0.08$ Ω , $L_2 = 396$ μ H, and $R_{L2} = 0.12$ Ω . The steady-state common duty command obtained in the switched-circuit simulation was $D = 0.455476$. Without active balancing, the simulated average currents were $\bar{I}_{L1} = 1.284$ A and $\bar{I}_{L2} = 0.856$ A.

Solving (A.20) gives

$$\Delta D_{\text{calc}} = -0.00110838, \quad (\text{A.22})$$

whereas the switched-circuit balancing loop settles at

$$\Delta D_{\text{sim}} = -0.00104706. \quad (\text{A.23})$$

The negative correction decreases D_1 and increases D_2 , as expected for the leg that initially carries the larger average current. The difference between the calculated and simulated corrections, normalized by the simulated magnitude, is approximately 5.9%.

TABLE IV
CALCULATED AND SIMULATED DUTY CORRECTIONS FOR $D < 0.5$

Case	ΔD_{calc}	ΔD_{sim}	Difference
$R_{L1} < R_{L2}$	-0.00110838	-0.00104706	5.9%
$R_{L1} > R_{L2}$	+0.00099389	+0.00092828	7.1%

E. Case 2: $R_{L1} > R_{L2}$

The leg parameters were interchanged: $L_1 = 396 \mu\text{H}$, $R_{L1} = 0.12 \Omega$, $L_2 = 264 \mu\text{H}$, and $R_{L2} = 0.08 \Omega$. The simulated common duty command was $D = 0.45491218$. The analytical model gives

$$\Delta D_{\text{calc}} = +0.00099389, \quad (\text{A.24})$$

and the switched-circuit balancing loop gives

$$\Delta D_{\text{sim}} = +0.00092828. \quad (\text{A.25})$$

The positive correction increases D_1 and decreases D_2 , consistently reversing the balancing action when the parameter asymmetry is reversed. The normalized difference between the calculated and simulated corrections is approximately 7.1%.

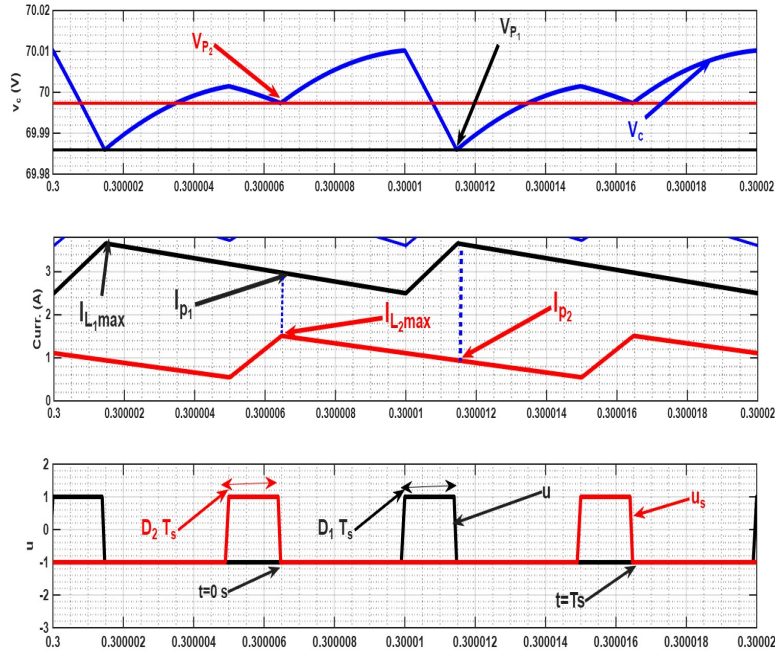


Fig. 12. Representative switched-circuit waveforms for the different operating regions for $D < 0.5$.

APPENDIX B
EXACT CHARGE-AREA DERIVATIONS FOR OVERLAPPING OPERATION ($D > 0.5$)

Consider a two-phase interleaved boost converter operating in continuous-conduction mode with a phase displacement of 180° . The analysis below assumes that the output voltage V_o is approximately constant over one switching period, semiconductor voltage drops are neglected, and the capacitor equivalent series resistance is sufficiently small that the reconstructed capacitor-voltage peaks can be used. The winding resistance of each phase is retained explicitly.

The phase duty ratios are defined as

$$D_1 = D + \Delta D, \quad D_2 = D - \Delta D, \quad (\text{B.1})$$

where D is the common duty-ratio command and ΔD is the differential correction generated by the auxiliary balancing controller. The admissible correction must satisfy

$$0 < D + \Delta D < 1, \quad 0 < D - \Delta D < 1. \quad (\text{B.2})$$

For $D > 0.5$, the two switch-on intervals overlap. Nevertheless, each phase retains an on interval of duration $D_j T_s$ and an off interval of duration

$$t_{bj} = (1 - D_j)T_s, \quad j \in \{1, 2\}. \quad (\text{B.3})$$

During the on interval of phase j , its inductor current satisfies

$$L_j \frac{di_{Lj}}{dt} = E - R_{Lj} i_{Lj}, \quad (\text{B.4})$$

whereas during its off interval,

$$L_j \frac{di_{Lj}}{dt} = E - V_o - R_{Lj} i_{Lj}. \quad (\text{B.5})$$

Define

$$\gamma_j = \frac{R_{Lj}}{L_j}, \quad A_j = \frac{E}{R_{Lj}}, \quad B_j = \frac{E - V_o}{R_{Lj}}, \quad (\text{B.6})$$

and

$$a_j = e^{-\gamma_j D_j T_s}, \quad b_j = e^{-\gamma_j (1-D_j) T_s}. \quad (\text{B.7})$$

Let $I_{Lj,\min}$ denote the phase current at the beginning of the on interval and $I_{Lj,\max}$ the current at the end of that interval. Exact integration of 940 gives

$$I_{Lj,\max} = A_j + (I_{Lj,\min} - A_j) a_j. \quad (\text{B.8})$$

Similarly, exact integration of (5) gives

$$I_{Lj,\min}^+ = B_j + (I_{Lj,\max} - B_j) b_j, \quad (\text{B.9})$$

where $I_{Lj,\min}^+$ is the minimum current at the beginning of the following switching period. Imposing periodic steady state,

$$I_{Lj,\min}^+ = I_{Lj,\min}, \quad (\text{B.10})$$

yields the exact maximum current

$$I_{Lj,\max} = \frac{A_j(1 - a_j) + a_j B_j(1 - b_j)}{1 - a_j b_j}. \quad (\text{B.11})$$

The corresponding minimum current is

$$I_{Lj,\min} = B_j + (I_{Lj,\max} - B_j) b_j. \quad (\text{B.12})$$

The exact off-state current waveform, with the local time origin placed at the beginning of the off interval, is

$$i_{Lj}(t) = B_j + (I_{Lj,\max} - B_j) e^{-\gamma_j t}, \quad 0 \leq t \leq t_{bj}. \quad (\text{B.13})$$

Therefore, the charge delivered to the output by phase j during its off interval is

$$\begin{aligned} Q_j(D_j) &= \int_0^{t_{bj}} i_{Lj}(t) dt \\ &= B_j t_{bj} + \frac{I_{Lj,\max} - B_j}{\gamma_j} (1 - e^{-\gamma_j t_{bj}}). \end{aligned} \quad (\text{B.14})$$

For completeness, the exact switching-period average phase current is

$$\begin{aligned} \bar{I}_{Lj} &= \frac{1}{T_s} \left[A_j D_j T_s + \frac{I_{Lj,\min} - A_j}{\gamma_j} (1 - a_j) \right. \\ &\quad \left. + B_j t_{bj} + \frac{I_{Lj,\max} - B_j}{\gamma_j} (1 - b_j) \right]. \end{aligned} \quad (\text{B.15})$$

Let V_{P1} and V_{P2} denote two successive phase-associated peaks of the reconstructed capacitor voltage. During the half switching period from V_{P1} to V_{P2} , phase 2 delivers the charge Q_2 , while the load removes approximately $I_o T_s / 2$. Hence,

$$C(V_{P2} - V_{P1}) = Q_2(D_2) - \frac{I_o T_s}{2}. \quad (\text{B.16})$$

Over the following half switching period,

$$C(V_{P1}^+ - V_{P2}) = Q_1(D_1) - \frac{I_o T_s}{2}, \quad (\text{B.17})$$

where V_{P1}^+ is the next occurrence of the phase-1-associated peak. At periodic steady state, $V_{P1}^+ = V_{P1}$. Subtracting (B.17) from (B.16) gives

$$2C(V_{P2} - V_{P1}) = Q_2(D_2) - Q_1(D_1). \quad (\text{B.18})$$

The load-current contribution cancels because the two peak intervals have the same duration $T_s/2$.

Using (B.1), the exact steady-state balancing condition is therefore

$$F(\Delta D) = Q_2(D - \Delta D) - Q_1(D + \Delta D) = 0. \quad (\text{B.19})$$

Equation (B.19) is a scalar nonlinear equation and can be solved using bisection or Newton's method while enforcing (B.2).

For a sufficiently small duty correction, a local linear approximation about $\Delta D = 0$ is

$$F(\Delta D) \approx F(0) - [Q'_1(D) + Q'_2(D)] \Delta D. \quad (\text{B.20})$$

Consequently, the approximate equilibrium correction is

$$\Delta D^* \approx \frac{Q_2(D) - Q_1(D)}{Q'_1(D) + Q'_2(D)}. \quad (\text{B.21})$$

This local form explains why the peak-voltage difference supplies a directional balancing signal. It does not imply exact equality of the average phase currents for arbitrary converter-leg parameters. Instead, forcing $V_{P1} \approx V_{P2}$ equalizes the alternating charge areas and, for the investigated parameter range, produces closely matched average phase currents.

The parameters used for the overlapping-conduction test are listed in Table V.

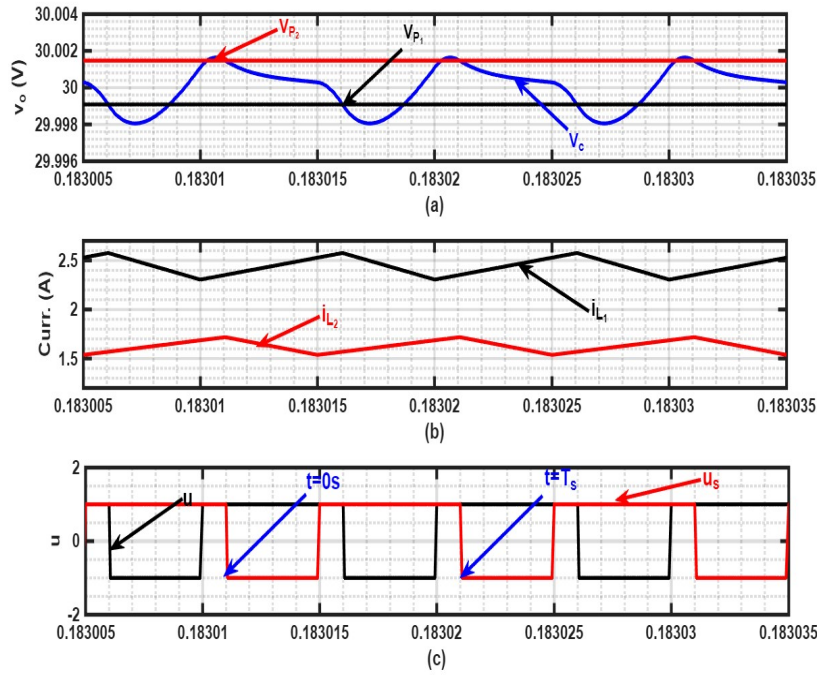


Fig. 13. Representative switched-circuit waveforms for the non-overlapping operating region for $D > 0.5$.

In the first arrangement,

$$R_{L1} = 0.08 \, \Omega, \quad R_{L2} = 0.12 \, \Omega. \quad (\text{B.22})$$

Numerical solution of (B.19) gives

$$\Delta D_{\text{exact}} = -0.00158892. \quad (\text{B.23})$$

The switched-circuit simulation produces

$$\Delta D_{\text{sim}} = -0.00130108. \quad (\text{B.24})$$

Both values have the physically correct negative sign when phase 1 is the more heavily conducting leg.

For the reversed-resistance arrangement,

$$R_{L1} = 0.12 \, \Omega, \quad R_{L2} = 0.08 \, \Omega, \quad (\text{B.25})$$

the exact charge-area model gives

$$\boxed{\Delta D_{\text{exact}} = 0.00158901}, \quad (\text{B.26})$$

whereas the switched-circuit simulation gives

$$\Delta D_{\text{sim}} = 0.00144085. \quad (\text{B.27})$$

The positive sign is consistent with phase 2 being the more heavily conducting leg.

The remaining numerical differences are expected because the analytical model assumes constant output voltage during a switching period, negligible capacitor ESR, idealized semiconductor behavior, and exact periodic steady state. The detailed switched-circuit simulation additionally contains switching transitions, the capacitor-voltage reconstruction filter, the auxiliary PI dynamics, and other circuit nonidealities.

These results show that the phase-associated peak-voltage difference retains the correct directional information in the overlapping-conduction region. Thus, the auxiliary balancing controller remains effective for $D > 0.5$ under the investigated converter parameters. The result is specific to the stated assumptions and operating conditions and should not be interpreted as a universal guarantee for arbitrary converter parameters.

A. Influence of Output-Capacitor ESR

The corrected analytical model predicts both the direction and the magnitude of the balancing correction with reasonable accuracy. Consequently, the larger discrepancy obtained with the unshifted second-subperiod current expressions should not be attributed entirely to capacitor ESR. The remaining difference between the analytical and switched-circuit results may arise from capacitor ESR, output-voltage variation within the switching period, semiconductor voltage drops, the peak-sampling instant, and numerical switching effects.

If the balancing error is formed from the measured terminal voltage $v_o = v_c + r_C i_C$, capacitor ESR can distort the phase-associated voltage peaks because switching transitions produce discontinuous changes in $r_C i_C$. This effect should be quantified by repeating otherwise identical simulations for $r_C = 0$ and for the selected nonzero ESR values. A lower duty-ratio boundary, such as $D \approx 0.40$, should be described as an empirical operating boundary only after it has been established through a duty-ratio sweep and an explicit performance criterion.

TABLE V
CONVERTER PARAMETERS FOR THE $D > 0.5$ TEST

Parameter	Symbol	Value
Input voltage	E	12 V
Output voltage	V_o	30 V
Load current	I_o	1.50 A
Switching period	T_s	1.0×10^{-5} s
Common duty ratio	D	0.60779327
Phase-1 inductance	L_1	264 μ H
Phase-2 inductance	L_2	396 μ H

TABLE VI
EXACT CHARGE-AREA PREDICTION AND SWITCHED-CIRCUIT RESULT

Resistance arrangement	ΔD_{exact}	ΔD_{sim}
$R_{L1} = 0.08 \Omega, R_{L2} = 0.12 \Omega$	-0.00158892	-0.00130108
$R_{L1} = 0.12 \Omega, R_{L2} = 0.08 \Omega$	0.00158901	0.00144085