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Research Article

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Physics-Based Performance Mapping of Ultra-High-Voltage SiC IGBTs and MOSFETs With Machine-Learning Acceleration

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Abstract

Ultra-high-voltage SiC IGBTs, SiC MOSFETs, series-connected Si IGBTs, and series-connected SiC MOSFETs are compared under hard- and soft-switching using a self-consistent electrothermal framework with a machine-learning surrogate to accelerate the generation of comparison maps. Three different analyses are performed: maximum-current capability mapping, deterministic minimum-loss device selection, and machine-learning-assisted generation of optimal-device maps with deterministic correction near transition boundaries. For the 20 kV class, the SiC IGBT provides the highest current capability in the low- and medium-frequency range under the zero-voltage-switching approximation, while hard switching and lower carrier lifetimes reduce this advantage, highlighting the superior performance of the series-connected SiC MOSFET configuration. The hybrid machine-learning approach achieves a $2.1\times$ speed-up in map generation, excluding one-time training. This framework provides an efficient first-stage technology-screening method before detailed compact-model extraction and (experimental) converter-level verification.

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1 Introduction

SiC Insulated-Gate Bipolar Transistor (IGBTs) have been investigated for several decades, evolving from early 6H-SiC UMOS IGBTs and p-channel 4H-SiC IGBTs to later n-channel 4H-SiC devices based on planar, flip-type, free-standing, and waffle-substrate concepts [1–4]. Experimental demonstrations have extended SiC IGBTs and modules into the 10–27 kV voltage range, including 12 kV-class modules, 16 kV flip-type IE-IGBTs, 27 kV n-IGBTs, and 10 kV box-cell or waffle-substrate structures [5, 6]. Despite this progress, SiC IGBTs have not reached widespread commercial adoption, mainly due to challenges in carrier-lifetime engineering, backside processing, p-type contacts, bipolar degradation, edge termination, yield, and cost. The transition from SiC MOSFETs to SiC IGBTs also remains less clearly defined than that from Si MOSFETs to Si IGBTs. The conductivity modulation of a SiC IGBT can reduce conduction losses, but this is counterbalanced by the larger built-in voltage of 4H-SiC bipolar junctions (~ 2.7 V at 300 K) compared with Si (~ 0.7 V), so the voltage class at which a SiC IGBT becomes favorable is expected to be higher than that at which a Si IGBT becomes superior to a Si MOSFET. The comparison is further complicated because ultra-high-voltage converter requirements can also be met using series-connected lower-voltage devices. For example, series-connected SiC MOSFETs may retain low switching losses and avoid bipolar charge storage, while series-connected Si IGBTs benefit from mature silicon processing and commercially available modules 6.5 kV modules; both, however, introduce additional active area, voltage-balancing requirements, increased parasitic inductances, and greater driving and control complexity.

TCAD simulations have been used to optimise SiC IGBT cell designs by balancing on-state voltage, breakdown voltage, and switching loss across different topologies and design parameters [4, 7], but converter-oriented comparisons remain limited across broad switching-frequency, temperature, and current ranges. Physics-based FEM modelling is essential for such comparisons because physical effects such as incomplete ionisation, anisotropic transport, oxide/semiconductor interface scattering, carrier recombination, and carrier-lifetime effects all affect the static and dynamic characteristics of SiC devices [8–14], and are difficult to retain in compact SPICE-type models without extensive calibration. In this context, machine-learning methods have recently been introduced in TCAD and power-electronics workflows to accelerate optimisation, prediction, and calibration, including TCAD-trained models for SiC breakdown-voltage prediction, GaN HEMT current–voltage prediction, FinFET transfer-characteristic prediction, process-profile prediction, IGBT design optimisation from design-of-experiments datasets, and SPICE-augmented parameter extraction [15–18], as well as converter-level efficiency prediction for SiC- and GaN-based converters. However, their efficacy depends strongly on the training data, the underlying physical models, and the range over which the model is used.

In this paper, machine learning is therefore not used to replace the physics-based electrothermal solver, but rather to accelerate generation of the device-selection map, while deterministic re-evaluation is retained in the transition regions where competing devices exhibit comparable performance. A variety of active cells (SiC IGBT, SiC MOSFET, series connected SiC MOSFETs and series connected Si-IGBTs)

under equivalent converter-level constraints, treating hard- and soft-switching operation, thermal limits, maximum-current capability, deterministic loss minimisation, and series-connected alternatives within the same modelling framework. Section 2 describes the device geometries and finite-element simulation setup and training, Section 3 the electrothermal and ML-assisted mapping methods, and Section 4 the current-capability maps, superior-device maps, and comparison with a compact-model-based workflow.

2 TCAD Modelling

Table 1 Drift-region parameters used for the considered device voltage classes (1.2 kV–20 kV) based on the impact ionisation integral of each material with a 20% extra voltage margin.

Device	BV (kV)	Drift thickness (μm)	Doping (cm^{-3})
Silicon IGBT	6.5	500	8.5×10^{12}
4H-SiC MOSFET/IGBT	1.2	10	1.0×10^{16}
4H-SiC MOSFET/IGBT	3.3	30	7.0×10^{15}
4H-SiC MOSFET/IGBT	6.5	60	3.0×10^{15}
4H-SiC MOSFET/IGBT	10	100	1.0×10^{15}
4H-SiC MOSFET/IGBT	15	120	8.0×10^{14}
4H-SiC MOSFET/IGBT	20	150	5.0×10^{14}

2.1 Finite-Element Simulations: Design and Training

Mixed-mode finite-element (FEM) simulations are utilised to obtain the static and dynamic characteristics of the investigated devices. Switching losses were obtained from a double-pulse-test (DPT) circuit, shown with its simulation parameters in Fig. 1; output characteristics used a slow voltage ramp at approximately 1 V/s, representative of quasi-static operation.

The active-cell structures are shown in Fig. 2 and the drift-region parameters in Table 1. The SiC MOSFET and SiC IGBT cells (Fig. 2(a) and (b)) share a 14 μm pitch for a consistent geometrical comparison, with a 2 μm epi-type JFET region doped at $2 \times 10^{16} \text{ cm}^{-3}$. The n-buffer is 1 μm at $1 \times 10^{18} \text{ cm}^{-3}$ for the MOSFET and 2 μm at $1 \times 10^{17} \text{ cm}^{-3}$ for the IGBT, which further includes a 2 μm p-anode at $5 \times 10^{17} \text{ cm}^{-3}$ and a 1 μm p⁺ collector at $1 \times 10^{19} \text{ cm}^{-3}$.

The SiC devices use a 30 nm SiO₂ gate oxide, an n-type polysilicon gate at $1 \times 10^{19} \text{ cm}^{-3}$, and 1 μm lateral n⁺ source and p⁺ body contacts. Doping is uniform except near the front-side p-body and channel, where implanted profiles follow calibrated 4H-SiC process- and device-modelling assumptions [9–13]. The Si IGBT (Fig. 2(c)) uses the same pitch with multiple dummy-emitter trenches representative of recent-generation 6.5 kV trench technologies, a 2 μm enhancement layer at $3 \times 10^{15} \text{ cm}^{-3}$ analogous to the SiC JFET region, a 4 μm trench depth, a 75 nm gate

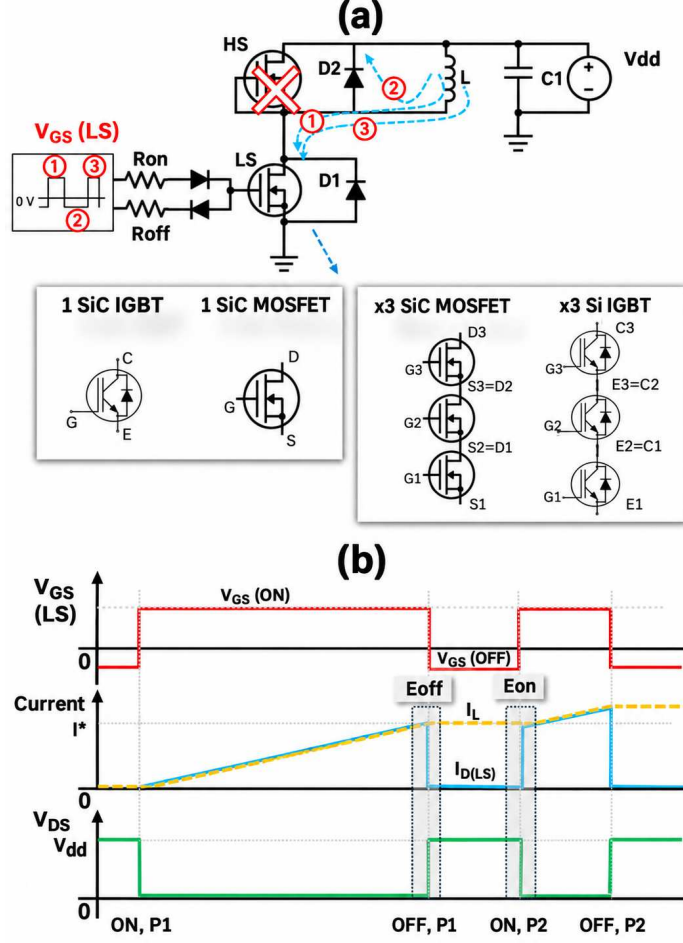


Fig. 1 (a) Double-pulse-test circuit used for the mixed-mode finite-element simulations. The high-side switch is replaced by an ideal diode and the four device configurations analysed in this work are used as the low-side switch. (b) Representative waveforms indicating the time intervals used for the extraction of turn-on and turn-off switching energies. The simulation parameters are $R_{on} = 10 \, \Omega$, $R_{off} = 1 \, \Omega$, $C_1 = 10 \, \text{pF}$, $V_{DD} = BV/1.6$, $V_{GS,on} = 15 \, \text{V}$, and $V_{GS,off} = -5 \, \text{V}$. D1 represents the internal body diode of the MOSFET and is absent in the IGBT case.

oxide, and backside n-buffer and p-anode regions from process simulations. The resulting room temperature output characteristics highlight the voltage-class dependence of the MOSFET–IGBT crossover (Fig. 3) and the 20 kV comparison for all the analysed devices (Fig. 4). It is evident that for the 6.5 kV the crossover voltage is well above 5 V, making SiC IGBTs less compelling than the unipolar (MOSFETs) counterparts.

Incomplete ionisation is included for the 4H-SiC devices through a generalised trap-based model that also captures the corresponding recombination level [9, 10]. Carrier lifetime combines Auger, radiative, and Shockley–Read–Hall (SRH) recombination [13, 14]; the peak SRH lifetime τ is a variable parameter, identical for electrons and

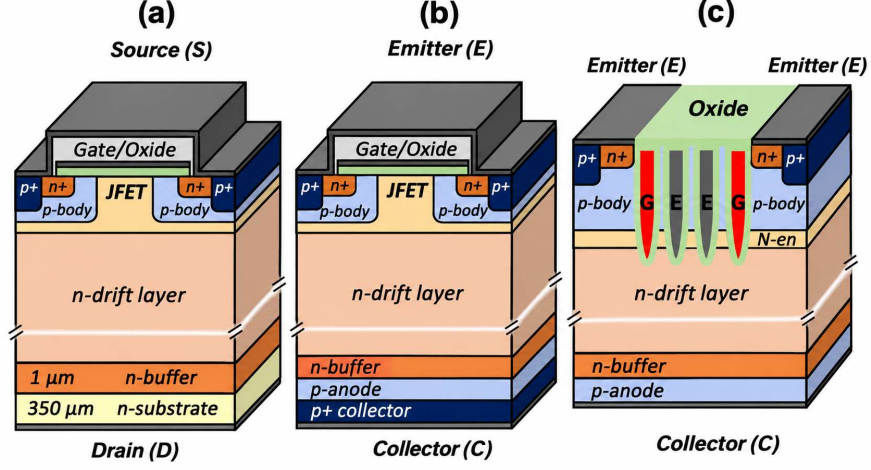


Fig. 2 (a) Schematic active-cell view of the SiC MOSFET, (b) SiC IGBT, and (c) Si IGBT used in this work.

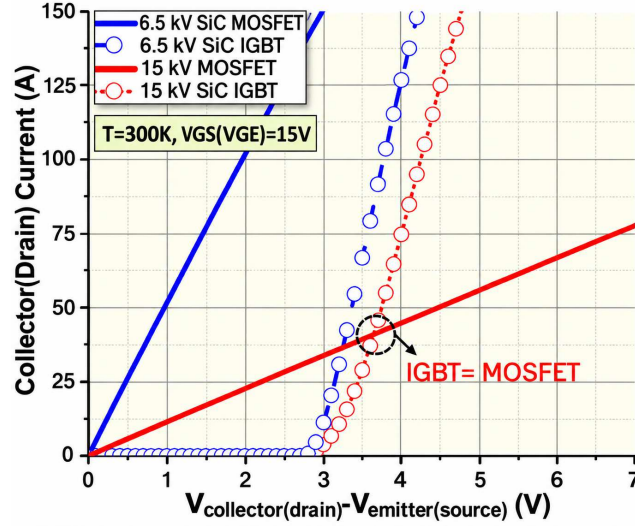


Fig. 3 Output characteristics at $T = 300$ K for the SiC IGBT and SiC MOSFET, highlighting the shift of the crossover point towards lower current at higher voltage classes. τ_0 for SiC IGBT is $1 \mu s$

holes, with $\tau_m(T) = \tau_{0,m}(T/300 \text{ K})^{\alpha_{\tau,m}}$, where $\alpha_{\tau,4H-SiC} = 1.7$ [14] and $\alpha_{\tau,Si} = 1.5$; in the Si IGBT $\tau_{0,n} = 30 \mu s$ and $\tau_{0,p} = 10 \mu s$, with benchmark 6.5 kV Si IGBT parameters [19]. The SiC channel mobility model [11] combines Coulomb, surface acoustic phonon, surface roughness, and bulk contributions; remaining 4H-SiC parameters follow established references [9, 10, 13]. Drift thickness and doping are scaled assuming avalanche impact ionisation as the dominant breakdown mechanism, with anisotropic

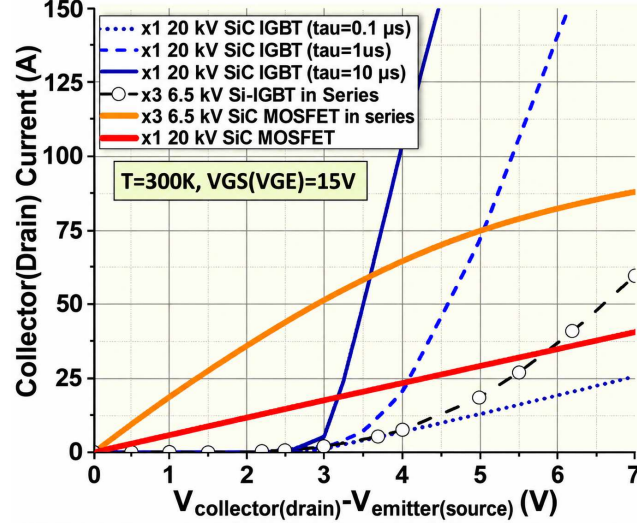


Fig. 4 Comparison of output characteristics at $T = 300$ K for the 20 kV voltage class.

parameters for 4H-SiC. Edge termination and gate pads are excluded, devices' currents are normalised to 1 cm^2 , and the 20 kV series-connected cases use three 6.5 kV devices, giving three times the active area of the single device case (SiC IGBT and SiC MOSFET). More than 2000 mixed-mode simulations generated the training dataset, extracting V_{on} , E_{on} , and E_{off} over the current range for junction temperatures from 300 K to 448 K. Switching energies integrate the instantaneous switching power over the 10–90% voltage and current transition, following the JEDEC convention and recent wide-bandgap methodologies [20].

3 Physics-Based and ML-Surrogate Loss Modelling

Three complementary calculations are used for the device comparison: a maximum-current capability surface I^* , a deterministic self-consistent electrothermal comparison, and a bagged decision-tree classifier trained on deterministic solutions to accelerate superior-device mapping over dense grids. The candidate device set is $\mathcal{K} = \{k_1, \dots, k_N\}$, where each candidate k is one device architecture, such as a single SiC MOSFET, a SiC IGBT with a given carrier lifetime (for SiC IGBT), a series connection of SiC MOSFETs, or a series connection of Si IGBTs. Each is described by tabulated electrical data $V_{\text{on},k}(I, T)$, $E_{\text{on},k}(I, T)$, and $E_{\text{off},k}(I, T)$, where I is the device current and T the evaluation temperature. The operating variables are I , the switching frequency f_{sw} , duty cycle D , heatsink temperature T_{sink} , ambient temperature T_{amb} , voltage class, and thermal resistance $R_{\text{th},k}$. The total device loss is the sum of a conduction term $P_{\text{cond},k} = D V_{\text{on},k}(I, T) I$ from the on-state output characteristics and a switching term $P_{\text{sw},k} = f_{\text{sw}} E_{\text{tot},k}(I, T)$ from the switching energy per pulse, as shown in (1).

$$P_{\text{tot},k} = D V_{\text{on},k}(I, T) I + f_{\text{sw}} E_{\text{tot},k}(I, T), \quad (1)$$

$E_{\text{tot},k}^{\text{hard}} = E_{\text{on},k} + E_{\text{off},k}$ for hard switching and, for the soft-switching case considered here (zero voltage switching, ZVS), the turn-on energy assumed strongly reduced so that $E_{\text{tot},k}^{\text{soft}} = E_{\text{off},k}$.

3.1 Thermal Resistance and Device Stack

Each device candidate is assigned a steady-state thermal resistance from a simplified multilayer package model with lateral heat spreading, assuming bottom side cooling (through the drain/collector contacts) [21]. The total $R_{\text{th},k}$ is the series sum over semiconductor, die attach, DBC copper, AlN isolation, baseplate, and external cooling, with each conductive layer being evaluated with a 45° heat-spreading approximation (2).

$$R_i = \frac{t_i}{k_i A_i}, \quad A_i = \frac{A_{\text{in}} + (\sqrt{A_{\text{in}}} + 2t_i)^2}{2}, \quad (2)$$

t_i and k_i are the thickness and thermal conductivity of layer i , and A_{in} is the active-device area for the first layer and the expanded output footprint of the previous layer thereafter. The external boundary is modelled with a convective term as $R_{\text{conv}} = 1/(hA_{\text{plate}})$. The semiconductor thickness is device dependent: drift region plus substrate for the SiC MOSFET, only the voltage-supporting region for the SiC IGBT (assuming n+ substrate backgrinding), and the full die thickness for the series-connected Si IGBT. The AlN thickness is scaled with blocking voltage as $t_{\text{AlN}} = S_{\text{F}} BV / E_{\text{AlN}}$. All parameters are listed in Table 2; they define a consistent reference package rather than an optimised module design.

Table 2 Main thermal-stack parameters used in the electrothermal comparison, for the 20 kV voltage class. Thermal conductivities k are in $\text{W m}^{-1}\text{K}^{-1}$ and h in $\text{W m}^{-2}\text{K}^{-1}$.

Parameter	Sym.	Value	Parameter	Sym.	Value
Cooling	–	1-side	Cu conductivity	k_{Cu}	400
Spreading	–	45°	AlN conductivity	k_{AlN}	150
SiC class	BV	20 kV	AlN strength	E_{AlN}	20 kV/mm
SiC drift	$t_{\text{drift,SiC}}$	150 μm	AlN safety	S_{F}	1.2
SiC substrate	$t_{\text{sub,SiC}}$	200 μm	AlN thickness	t_{AlN}	1.2 mm
Si IGBT die	$t_{\text{die,Si}}$	650 μm	Cu baseplate	t_{base}	10 mm
SiC conductivity	k_{SiC}	300	Heat transfer	h	5000
Si conductivity	k_{Si}	148	Sink temp.	T_{sink}	300 K
Attach conduct.	k_{attach}	60	Max junction	$T_{\text{j,max}}$	448 K
DBC Cu thickness	t_{Cu}	0.3 mm			

3.2 Maximum-Current Capability Calculation

The first metric is the maximum thermally sustainable current I^* , defined for each candidate k , switching frequency f_{sw} , and duty cycle D as the highest current for

which the device remains below the imposed junction-temperature limit:

$$I_k^* = \max_I \{I : T_{j,k}(I, f_{\text{sw}}, D) \leq T_{j,\text{max}}\}. \quad (3)$$

The losses are evaluated from (1) at the junction-temperature estimate used in the thermal balance, with the temperature interpolation of Section 3.3, and $T_{j,k} = T_{\text{sink}} + R_{\text{th},k}P_{\text{tot},k}$; I_k^* is the current at which $T_{j,k} = T_{j,\text{max}}$. Repeating this over the $f_{\text{sw}}-D$ grid gives the capability surface for each technology. Unlike the superior-device map, which ranks all feasible devices at a prescribed current, the I^* map gives the thermal current envelope of each individual device at low computational cost. However, while this approach provides the quickest calculation, it does not clearly identify the superior device for a lower current operation.

3.3 Deterministic Self-Consistent Electrothermal Loss Comparison

The deterministic calculation described in this section is the reference method for device ranking. For each device k , the on-state voltage and switching energies are evaluated at the instantaneous junction-temperature estimate, interpolating the tabulated data over current with shape-preserving piecewise cubic interpolation and then linearly in temperature between two consecutive available temperatures T_1 and T_2 , as shown in (4).

$$X_k(I, T_j) = X_k(I, T_1) + \frac{T_j - T_1}{T_2 - T_1} [X_k(I, T_2) - X_k(I, T_1)], \quad (4)$$

where $X_k \in \{V_{\text{on},k}, E_{\text{on},k}, E_{\text{off},k}\}$. The self-consistent junction temperature follows from the fixed-point condition $T_{j,k} = T_{\text{sink}} + R_{\text{th},k}P_{\text{tot},k}(I, f_{\text{sw}}, D, T_{j,k})$, with $P_{\text{tot},k}$ evaluated from (1) at the current temperature estimate $T_{j,k}^{(n)}$ and $E_{\text{tot},k}$ selected according to the hard- or soft-switching case. The temperature is updated by relaxed fixed-point iteration (5).

$$T_{j,k}^{(n+1)} = (1 - \alpha)T_{j,k}^{(n)} + \alpha \left[T_{\text{sink}} + R_{\text{th},k}P_{\text{tot},k}^{(n)} \right], \quad (5)$$

with $\alpha = 0.45$, stopping when the change in junction temperature falls below $\varepsilon_T = 10^{-3}$ K. The conduction, switching, and total losses are then obtained from (1) at the converged $T_{j,k}$. A device is considered feasible only if the electrothermal iteration converges, the required current lies within the valid interpolation range, and the final junction temperature remains below the imposed limit $T_{j,\text{max}}$ (fixed at 448 K). The deterministic superior device is then selected from the feasible set, and the loss margin between the best and second-best feasible devices is also stored (6).

$$k_{\text{opt}} = \arg \min_{k \in \mathcal{K}_{\text{feas}}} P_{\text{tot},k}, \quad \Delta P = P_{\text{tot},\text{second}} - P_{\text{tot},\text{best}}. \quad (6)$$

Large ΔP indicates that the selected device is robustly superior, whereas small ΔP identifies transition regions where small changes in duty cycle, switching frequency, thermal resistance, or electrical data could alter the winner. The calculation is repeated over the full I - D - f_{sw} grid, storing at each point the winning device, the total losses, the converged peak junction temperature, the loss margin compared to other devices.

3.4 ML-Assisted Superior-Device Mapping

The full deterministic sweep can be computationally expensive. The operating grid contains $N_{\text{op}} = N_I N_D N_f$ points, where N_I , N_D , and N_f are the numbers of current, duty-cycle, and switching-frequency points, respectively. Since all N_{dev} candidate devices are evaluated at each operating point, the full sweep requires $N_{\text{eval,full}} = N_{\text{op}} N_{\text{dev}}$ deterministic device evaluations. The TCAD-derived $V_{\text{on}}(I, T)$, $E_{\text{on}}(I, T)$, and $E_{\text{off}}(I, T)$ data are sampled on a coarse current grid and interpolated within the solver. The comparison is then performed on a denser grid with $N_I = 45$, $N_D = 25$, and $N_f = 55$, giving $N_{\text{op}} = 61\,875$ operating points for each temperature and carrier-lifetime condition. This improves the resolution of transition regions without additional TCAD simulations.

Because the optimal device architecture changes mainly across the narrow transition boundaries, a surrogate ML model is used to reduce the number of deterministic evaluations. The surrogate operates in three steps.

1) *Sampling*. The electrothermal solver is evaluated at a subset of operating points, sampled uniformly in current and duty cycle and uniformly in $\log_{10}(f_{\text{sw}})$.

2) *Training*. A bagged decision-tree ensemble, implemented in MATLAB using `fitcensemble`, predicts the optimal device from $\mathbf{x} = [I, \log_{10}(f_{\text{sw}}), D]$. The deterministic optimum k_{opt} is used as the target, while the surrogate prediction is $\hat{k}_{\text{opt}} = g(\mathbf{x})$. Thermally infeasible points are assigned to an additional class, $k_{\text{opt}} = 0$.

3) *Deterministic correction*. Points are re-evaluated with the deterministic solver when the highest ensemble class score is below a certain threshold $C_{\text{th}} = 0.88$, or when a neighbouring point belongs to a different predicted class. These points form the correction set $\mathcal{C}$, limited to 25% of the operating grid.

The resulting hybrid classification is defined in Eq. (7) as

$$k_{\text{hyb}}(\mathbf{x}) = \begin{cases} k_{\text{opt}}(\mathbf{x}), & \mathbf{x} \in \mathcal{C}, \\ \hat{k}_{\text{opt}}(\mathbf{x}), & \mathbf{x} \notin \mathcal{C}. \end{cases} \quad (7)$$

If $\mathcal{C}$ excludes points already used for training and validation, the number of operating points requiring deterministic evaluation is $N_{\text{det,hyb}} = N_{\text{train}} + N_{\text{val}} + |\mathcal{C}|$. Since all N_{dev} devices are evaluated at each such point, this factor is common to both workflows. The (approximate) hybrid speed-up is therefore given by Eq. (8):

$$S_{\text{hyb}} \approx \frac{N_{\text{op}}}{N_{\text{det,hyb}}}. \quad (8)$$

The surrogate is then trained separately for each temperature and carrier-lifetime condition.

4 Results

4.1 Maximum-Current I^* Capability Map

Figs. 5 and 6 summarise the maximum-current capability maps for the 20 kV class. Figure 5(a) shows the three-dimensional map of the maximum allowable current I^* versus switching frequency and duty cycle for a selected carrier lifetime, and Fig. 5(b) the cutline at $D = 0.5$, assuming zero-voltage-switching (ZVS) operation so that turn-on losses are minimised (i.e., the comparison is governed by conduction and turn-off losses).

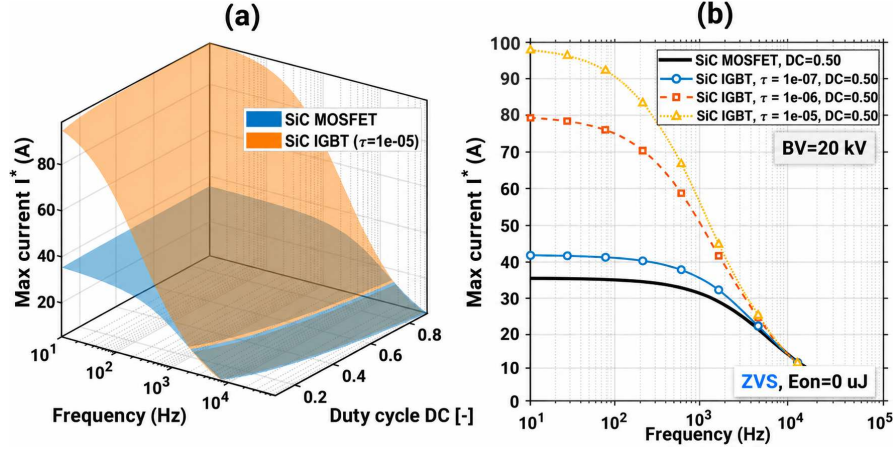


Fig. 5 (a) Three-dimensional maximum-current map for the 20 kV SiC MOSFET and SiC IGBT comparison. (b) Cutline at a fixed duty cycle of $D = 0.5$. ZVS operation is assumed for this calculation.

Under ZVS the SiC IGBT advantage is clear, driven by its lower conduction loss below 10 kHz, and becomes less pronounced at low duty cycle and low current where the SiC MOSFET, at equal active area, grows competitive. From roughly 100 Hz to 20 kHz the maximum allowable current of the SiC IGBT is nearly twice that of the SiC MOSFET. Including turn-on losses (Fig. 6) shifts the crossover below 1 kHz, and the $D = 0.5$ cutline shows an additional crossover between the 1 μ s and 0.1 μ s SiC IGBT cases.

Turn-on losses reduce the peak I^* from approximately 100 A to below 90 A, and the SiC IGBT curves lose their extended plateau, falling markedly from tens of hertz to a few kilohertz. The lifetime=0.1 μ s case, where conductivity modulation is weak, tracks the SiC MOSFET over most of the frequency range. At 6.5 kV the SiC IGBT advantage largely disappears: the SiC MOSFET reaches approximately 120 A in both hard-switching and ZVS scenarios and stays above the SiC IGBT across the whole frequency range (Fig. 7).

A further 20 kV comparison between the monolithic SiC MOSFET, the SiC IGBT, three series-connected 6.5 kV SiC MOSFETs, and three series-connected 6.5 kV Si IGBTs is shown for ZVS in Fig. 8 and for hard switching in Fig. 9. Under ZVS the

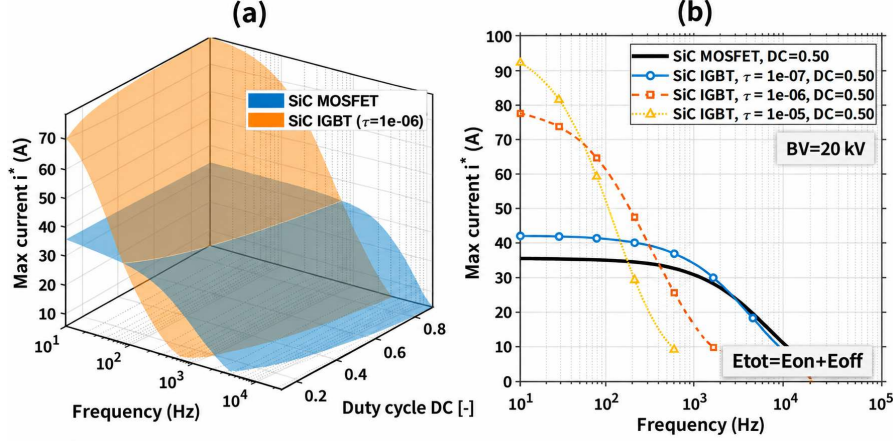


Fig. 6 (a) Three-dimensional maximum-current map for the 20 kV SiC MOSFET and SiC IGBT comparison. (b) Cutline at a fixed duty cycle of $D = 0.5$. Full hard-switching losses are included in this calculation.

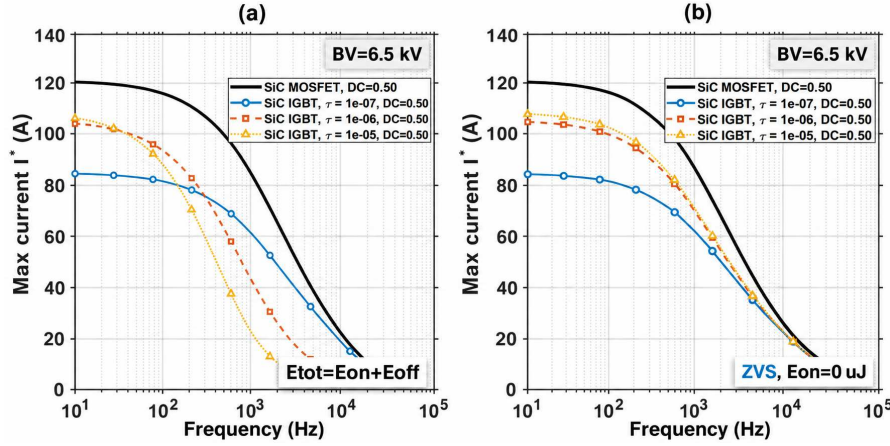


Fig. 7 Maximum-current comparison for the 6.5 kV class assuming (a) hard-switching losses and (b) a ZVS loss scenario. The duty cycle is fixed at $D = 0.5$.

SiC IGBT outperforms the other technologies over a broad operating range; the series-connected Si IGBT is the least performing configuration, staying below 30 A across the frequency range, while the series-connected SiC MOSFET improves at higher switching frequency and lower current.

Series-connected devices also require additional voltage margin, not included in the computation shown here, and voltage imbalance and unequal switching-energy sharing can raise their effective switching losses.

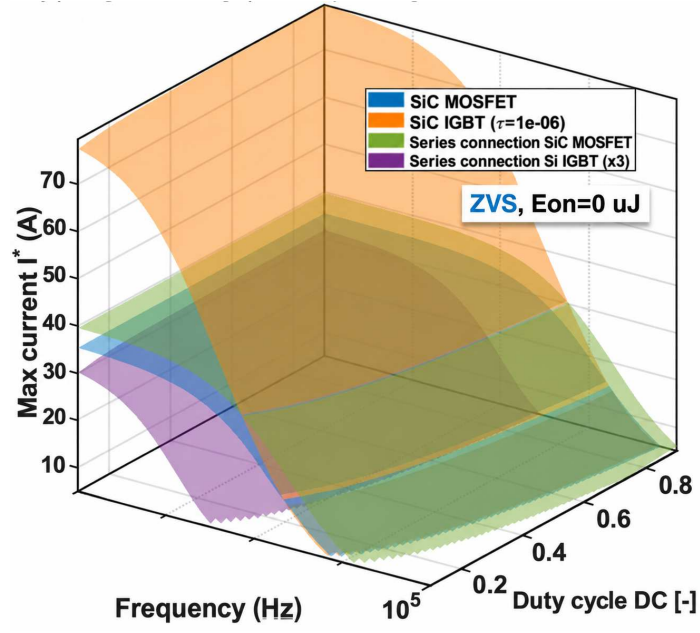


Fig. 8 Maximum-current map for the 20 kV comparison between the SiC MOSFET, SiC IGBT, series-connected Si IGBTs, and series-connected SiC MOSFETs under the ZVS approximation.

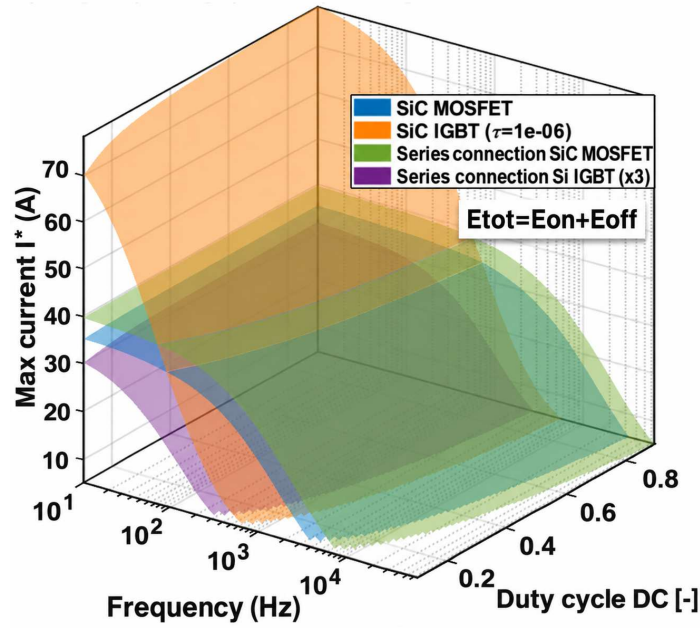


Fig. 9 Maximum-current map for the 20 kV comparison between the SiC MOSFET, SiC IGBT, series-connected Si IGBTs, and series-connected SiC MOSFETs under full hard-switching conditions.

4.2 Deterministic and ML-Assisted Superior-Device Maps

As an initial test, ML regressors were trained directly on the full V_{on} , E_{on} , and E_{off} map, with parity plots in Fig. 10. The regressors captured the main trends in the TCAD-derived data but did not reduce the overall calculation time: the overhead of training and evaluating separate surrogates gave an effective speed factor of about $0.5\times$, slower than the deterministic interpolation-based calculation. This route was therefore retained only as a benchmark.

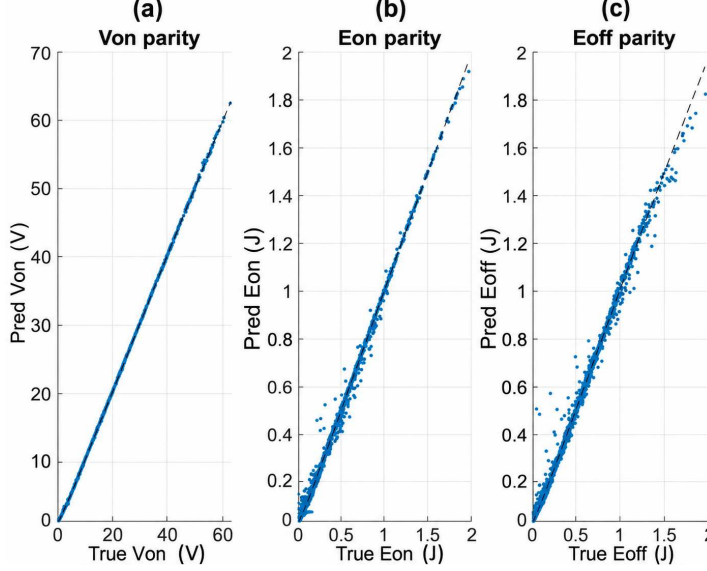


Fig. 10 Training summary for the direct ML electrical surrogate: (a) V_{on} , (b) E_{on} , and (c) E_{off} prediction.

Figure 11 shows the deterministic superior-device map from the full self-consistent solver. Under the ZVS approximation the SiC IGBT is favoured over a broad low-to medium-frequency region because of its lower conduction loss, while at lower current and higher switching frequency the series-connected SiC MOSFET becomes competitive and can outperform it.

The advantage of deterministic mapping over the total-current approach is evident from Fig. 11, where trends that are not captured in Figs. 6–9 become clearly visible. Its main drawback, however, is the higher computational cost, evaluated here on a standard laptop equipped with a multicore Intel i7 processor. Benchmarking 500 deterministic operating points required 1.448 s, giving an estimated full-map runtime of 179.2 s for the $N_{op} = 61\,875$ grid. The hybrid classifier of Section 3.4 was therefore used to reduce the computational cost.

The resulting hybrid map (Fig. 12) preserves the main device-selection regions of the deterministic solution. Prediction over the full grid required 46.7 s, a potential $3.8\times$ speed-up for the classifier-only stage. Deterministic correction near low-confidence and transition-boundary regions added 38.3 s for 9786 points, $9786/61875 \approx 15.8\%$, below

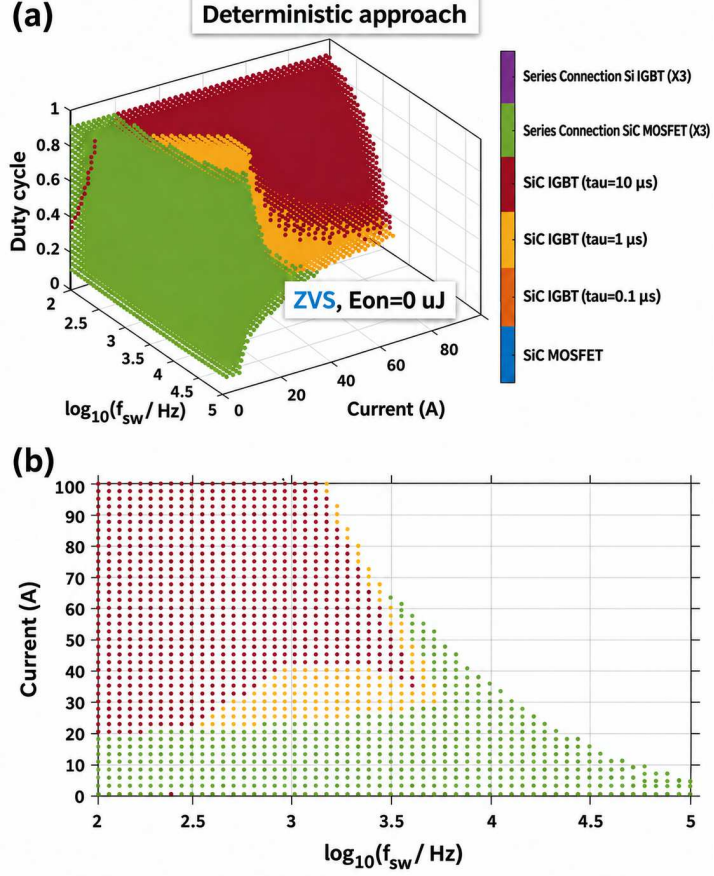


Fig. 11 (a) Power-loss superior-device maps obtained with the full deterministic self-consistent electrothermal approach. (b) Slice of the three-dimensional map at $D = 0.9$.

the 25% cap. The combined workflow therefore required 85.0 s, an effective $2.1\times$ speed-up excluding the one-time training cost, or 103.9 s and $1.7\times$ including it. The ML stage thus accelerates rather than replaces the deterministic model; the gain is moderate because the interpolation-based solver is already fast, but should grow for larger device libraries, denser grids, voltage-class sweeps, or additional parasitic configurations.

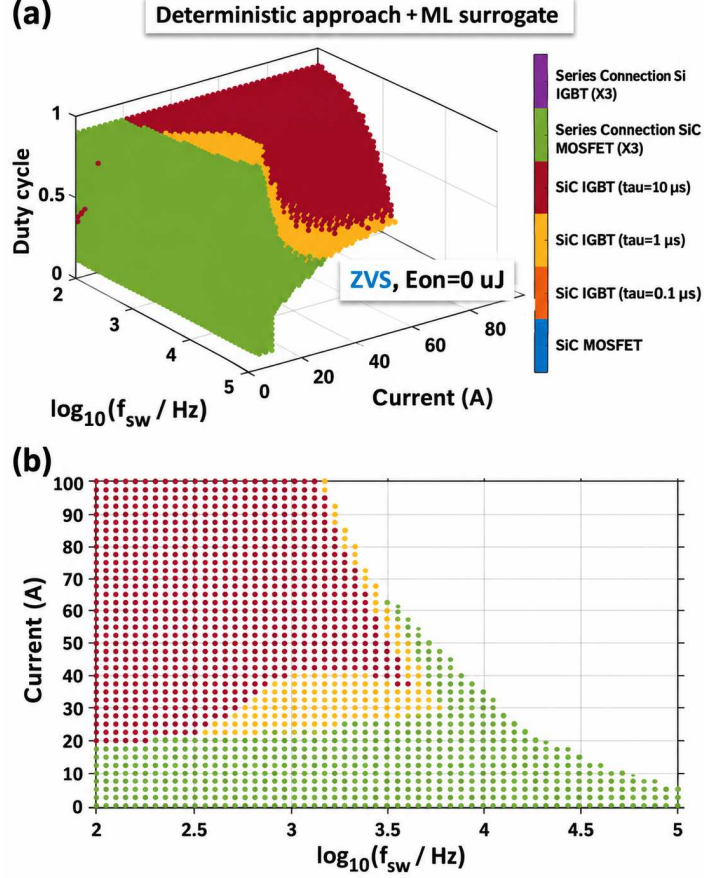


Fig. 12 (a) Power-loss superior-device map obtained with the hybrid deterministic–machine-learning approach. (b) Slice of the three-dimensional map at $D = 0.9$.

5 Conclusion

A physics-based electrothermal workflow has been developed to compare ultra-high-voltage SiC MOSFETs, SiC IGBTs, series-connected SiC MOSFETs, and series-connected Si IGBTs under hard- and soft-switching conditions. The preferred technology depends on current, switching frequency, duty cycle, thermal boundary conditions, and the assumed SiC IGBT carrier lifetime. The maximum-current and deterministic device-selection maps provide complementary information. The former gives a faster estimate of the thermally admissible current envelope, whereas the latter compares devices at fixed operating points using the self-consistent junction temperature and therefore captures transitions in device superiority more clearly. A machine-learning surrogate is used to reduce the computational cost of this deterministic mapping while retaining solver-based correction near transition boundaries.

The results show that SiC IGBTs can outperform series-connected SiC MOSFETs at high current and large duty cycle, particularly under soft switching, while

this advantage is reduced under hard switching and for shorter carrier lifetimes. Series-connected Si IGBTs generally show inferior performance over the investigated operating space. The proposed framework is therefore well suited to early-stage technology comparison over wide parameter ranges, while SPICE-based simulation remains necessary for detailed converter-level verification.

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