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Design and Performance Analysis of Novel Single-Fin Core Shell Junctionless FinFET (CS-JL-FinFET)

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Abstract

Aggressive scaling of conventional field-effect transistors intensifies short-channel effects, leakage current, degraded electrostatic control and mobility-related limitations, motivating the development of alternative device architectures with improved carrier transport and gate controllability. In this work, a single-fin core-shell junctionless FinFET (CS-JL-FinFET) is proposed using three-dimensional technology computer-aided design simulations. The proposed device employs core-shell doping to modify the internal electrostatic potential, carrier distribution and gate-to-channel coupling while retaining the junctionless operating principle. A conventional single-fin JL-FinFET with identical fundamental dimensions, material system, gate work function, bias conditions and simulation methodology is employed. The electrostatic and transport characteristics are evaluated through transfer and output characteristics, potential and electric-field distributions, transconductance, output conductance, capacitance, temperature-dependent behavior, intrinsic gain, Early voltage and circuit-level inverter operation. At the nominal operating condition, the proposed CS-JL-FinFET achieves an ON-state current of 10^{-5}A/μm and an OFF-state current of 10^{-16}A/μm, resulting in an I_{on}/I_{off} ratio of 10^{11}, compared with $10^{10}$for the conventional JL-FinFET. The proposed device also shows a subthreshold slope of 64 mV/dec, compared with 82.7 mV/dec for conventional JL-FinFET while the peak transconductance is reported to improve by 60-67%. The enhanced current modulation by increased output conductance, resulting in lower output resistance, intrinsic gain and Early voltage than the conventional device. Resistive-load inverter shows successful voltage inversion with a 0-0.5 V input swing. These results establish core-shell doping engineering as a promising approach for enhancing the current-driving and switching characteristics of nanoscale junctionless FinFET.

Keywords*: FinFET, Junctionless, Core-Shell, Field Effect Transistor, Subthreshold Slope*

1. Introduction

The continuous scaling of MOSFET has been a fundamental driver of increased integration density, computational capability and energy efficiency in modern very-large-scale integration (VLSI) systems.[1] As the channel dimensions approach the nanometer regime, conventional device scaling becomes constrained by short-channel effects (SCEs), degraded electrostatic integrity, threshold-voltage instability, drain-induced barrier lowering (DIBL), increased off-state leakage and subthreshold degradation. These effects arise primarily from the increasing influence of the source and drain electric fields on the channel potential as the channel length is reduced.[2] Maintaining strong gate control over the channel while achieving high drive current and low leakage current has become a critical requirement for nanoscale transistor design. The resulting trade-off between electrostatic control, carrier transport, power consumption and manufacturability has motivated extensive investigation of alternative transistor architectures beyond conventional planar MOSFETs.

Fin field-effect transistors emerged as an important architecture for addressing the electrostatic limitations of scaled planar MOSFETs. By forming the conducting channel in a 3D fin and controlling it using multiple gate surfaces, FinFET provide stronger gate-to-channel coupling and improved electrostatic control compared with conventional single-gate planar structures.[3] The multi-gate geometry enables more effective suppression of SCEs while maintaining a compact device footprint. [4] The applicability of the FinFET architecture to junctionless operation has attracted considerable research interest. Lee et al. (2009) introduced the junctionless multigate field-effect transistor (JL-MuGFET), showing that a thin and narrow multigate semiconductor body could be fully depleted by the gate without requiring conventional source/channel and channel/drain junctions [6]. Later, Sreenivasulu and Narendar (2022) investigated a 5-nm tri-gate junctionless SOI FinFET using 3D TCAD simulations and examined the influence of spacer engineering, nanofin

geometry and high-k gate-stack configurations on its electrical, power, analog and radio-frequency characteristics [7]. These studies show the suitability of multigate and FinFET architectures for maintaining electrostatic control at deeply scaled dimensions. Further scaling continues to impose stringent requirements on leakage suppression, threshold-voltage control, variability and the simultaneous optimization of current drive and electrostatic integrity. [15-17]

Junctionless field-effect transistors (JLFET) depict different approach to nanoscale transistor design by eliminating the abrupt semiconductor junctions used to define the source, channel and drain.[5] Lee et al. (2009) proposed the junctionless multigate transistor in which the semiconductor body has the same doping type and the same doping concentration as the source and drain, allowing the gate to control conduction through depletion of the uniformly doped body. Colinge et al. (2011) established the physical principles and design guidelines of the junctionless nanowire transistor (JNT), describing it as a gate-controlled resistor in which current flows through the semiconductor body rather than through a conventional surface inversion channel [13]. It offers potential advantages in terms of simplified junction formation and reduced dependence on abrupt doping gradients. The conventional JLFET introduces an inherent design trade-off because a high doping concentration is required to maintain sufficient carrier concentration and ON-state current. Colinge et al. (2011) identified the dependence of junctionless transistor characteristics on doping concentration, semiconductor dimensions and gate-oxide thickness, showing the importance of carefully balancing full depletion and current-carrying capability. The high doping required for junctionless operation can also increase impurity scattering and consequently degrade carrier mobility. [24-25] Bae and Yun (2020) investigated random dopant fluctuation (RDF), gate work-function variation (WFV) and oxide-thickness variation (OTV) in 14-nm junctionless FinFET and reported that RDF becomes the most significant source of variability as the device dimensions are scaled [8]. One promising approach to overcome these limitations is the controlled redistribution of doping within the semiconductor body rather than maintaining a uniformly doped channel. Kumar et al. (2015) investigated the impact of a shell doping profile on the electrical characteristics of junctionless FETs and shown that spatially non-uniform doping can modify carrier distribution and series resistance while improving important device characteristics. Their numerical study showed that the proposed shell doping profile could mitigate short-channel effects, improve subthreshold swing, increase the ON/OFF current ratio and substantially reduce OFF-state current for sub-20-nm devices [30]. These results indicate that the spatial distribution of dopants, rather than only the average doping concentration can play an important role in determining the electrostatic and transport properties of nanoscale junctionless devices.

The core-shell concept further develops this principle by introducing distinct semiconductor regions with different doping characteristics within the device cross-section.[23,34] Cristoloveanu and Ghibaudo (2022) investigated the fundamental advantages of core-shell junctionless FETs and shown that combining a heavily doped core with an undoped shell can address several limitations of classical junctionless transistors.[29] Their analysis showed that the core-shell configuration can provide normally-off operation, high mobile charge, enhanced carrier mobility, high current drive and reduced sensitivity to random dopant fluctuations while retaining the junctionless nature of the device. The underlying concept is to combine the carriers supplied by the heavily doped core with additional carriers induced in the lightly doped or undoped shell by the gate, thereby separating the functions of carrier supply and electrostatic control within the device body. This spatial separation provides a potentially attractive route for improving transport and electrostatic characteristics.[32]

The potential of shell and core-shell engineering has been investigated using different device architectures and structural configurations. Prasad and Mahadevaswamy (2021) investigated a tri-gate junctionless FET incorporating a rectangular core-shell architecture and examined the effect of core-shell engineering together with dielectric engineering on device performance [11]. Their work shown that modifying the internal doping configuration can provide an additional degree of freedom for optimizing junctionless transistor characteristics. Sreenivasulu et al. (2024) investigated a rectangular core-shell junctionless nanosheet FET combined with gate-oxide-stack and doping engineering [12]. Their structure employed vertically stacked nanosheet configurations with opposite core doping and was evaluated in terms of (Ion/Ioff), DIBL and subthreshold swing. These results show that core-shell doping engineering can be extended beyond conventional nanowire structures toward nanosheet-based architectures and can be combined with gate and dielectric engineering for further performance optimization [32].

The core-shell junctionless concept has also continued to evolve toward process-compatible and technologically relevant architectures. In 2024, a numerical study of a core-shell dual-metal-gate-stack junctionless accumulation-mode nanowire FET combined core-shell doping with dual-metal-gate and high-k gate-stack engineering, showing the continuing interest in jointly optimizing internal doping distribution and gate control. In 2025, Yan et al. investigated a planar core-shell junctionless transistor compatible with fully depleted silicon-on-insulator (FD-SOI) technology. Their structure employed a heavily doped core with an undoped shell and shown normally-off operation and enhanced mobility, while the device characteristics could be tuned through the core/shell dimensions, doping concentration and back-bias conditions [29].

Although these investigations have established the benefits of spatial doping engineering in junctionless devices, the reported core-shell architectures differ in geometry, doping polarity, gate configuration and device operating mechanism. Most recent studies have focused on nanowire, nanosheet, planar or gate-stack-based core-shell structures while systematic investigation of a core-shell configuration specifically integrated within a single-fin junctionless FinFET remains comparatively limited. The influence of an (n^+)-(p)-(n^+) doping arrangement across the fin cross-section on the electrostatic potential, carrier distribution, electric-field profile, current-density distribution and resulting DC characteristics requires further investigation. This configuration is fundamentally different from a conventional uniformly doped n-type junctionless FinFET because the highly doped n-type shell regions and lower-doped p-type core introduce a controlled spatial variation in doping polarity and concentration within the same fin body.

This work proposes and investigates a single-fin (n^+) -(p) -(n^+) core-shell junctionless FinFET using 3D technology computer-aided design simulations. In the proposed structure, the fin is divided into highly doped (n^+) shell regions surrounding a lower-doped (p)-type core, forming a single-fin (n^+)-(p)-(n^+) core-shell junctionless FinFET. The proposed doping configuration is intended to modify the internal electrostatic potential and carrier distribution while providing highly doped regions near the outer portions of the fin for carrier transport. The resulting interaction between the shell conduction regions and the lower-doped core may influence the depletion behaviour, electric-field distribution, carrier concentration and current-flow paths within the device. The proposed architecture provides an opportunity to investigate whether spatial doping engineering can improve the trade-off between ON-state current, OFF-state leakage, subthreshold behaviour and electrostatic integrity in a single-fin junctionless FinFET.

2. Device Design and Simulation Models

Figure. 1 shows the conceptual design of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET) and shows how three device-engineering concepts junctionless channel architecture, core-shell structure and tri-gate FinFET configuration are integrated into a single proposed device. Core-shell structure, is the principal structural modification introduced in the proposed device. As represented in Figure. 1, the core-shell concept consists of a high-mobility core surrounded by a low-resistance shell. The core is intended to provide an enhanced carrier-transport region, whereas the surrounding shell modifies the electrical conduction environment and contributes to the overall channel behaviour.

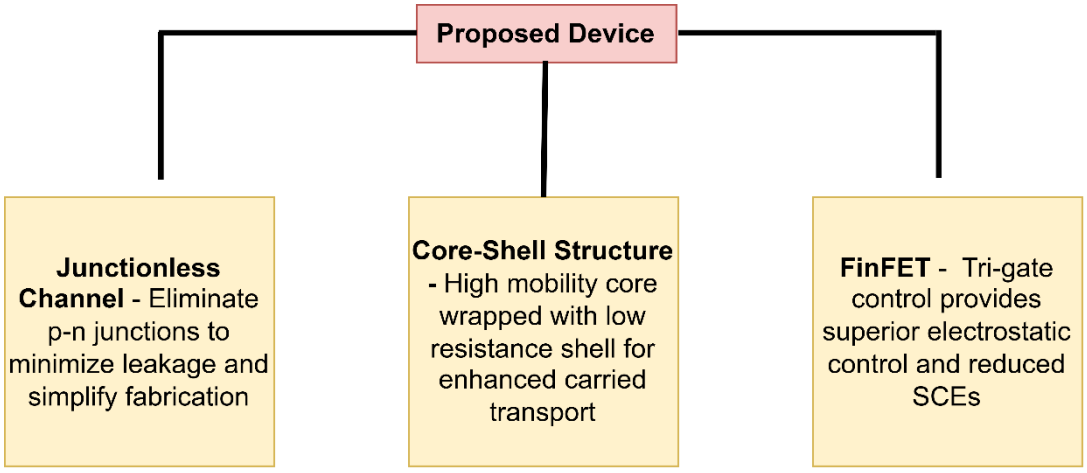


Figure 1: Conceptual framework of the proposed core-shell junctionless FinFET integrating junctionless channel architecture, core-shell engineering and tri-gate.

The core-shell configuration is introduced as a device-engineering approach for improving the trade-off between carrier transport and electrostatic control. FinFET tri-gate structure, the gate surrounds the fin through multiple surfaces, providing stronger electrostatic coupling between the gate and the channel than a conventional planar single-gate structure. The enhanced gate control is important because effective depletion of the highly doped channel is essential for achieving a low OFF-state current. Provides improved control over the channel potential and helps suppress short-channel effects (SCEs) arising from aggressive device scaling.

Table.1 Region Dimension and material of CS-JL-FinFET

Region name	Region dimension	Material
H_{fin}	40nm	Si
W_{fin}	6nm	Si
Shell	L=25nm, W=16nm	Si, 1.5e19 cm^{-3}
Core	L=25nm, W=8nm	Si, 1e15 cm^{-3}
Gate	L=14nm	Pt
Oxide (thickness)	1nm	SiO_2
Buried oxide (BOX)	64nm	SiO_2
Substrate	64nm	Si

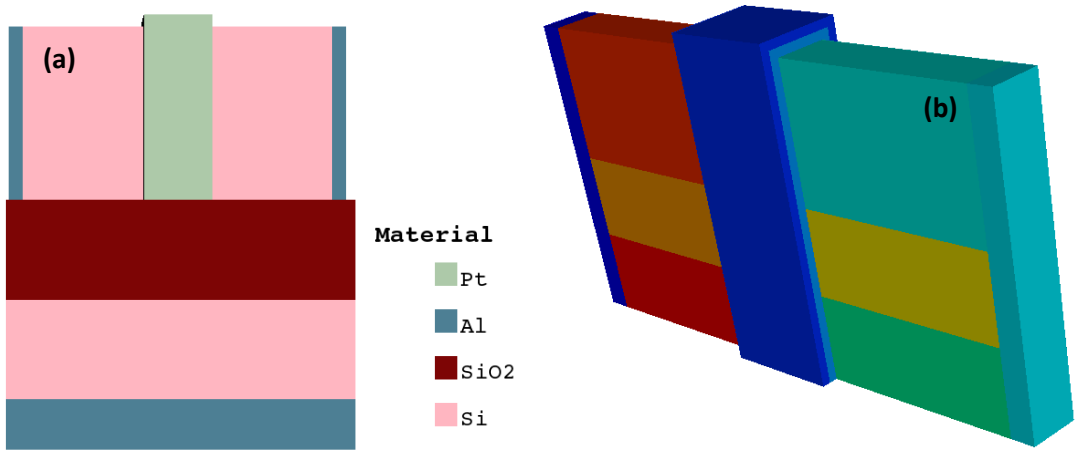


Figure 2: (a) Material composition and structural representation of the proposed CS-JL-FinFET (b) 3D structural representation of the proposed CS-JL-FinFET

Figure 2(a) shows the two-dimensional cross-sectional material configuration of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET). The material distribution consists of Si as the semiconductor body, SiO_2 as the gate dielectric, Pt as the gate electrode and Al as the source/drain contact material. **Figure 2(b)** extends this representation into a three-dimensional device structure, illustrating the spatial relationship between the gate, dielectric, semiconductor regions, and source/drain terminals. The 3-D representation is particularly important for the proposed FinFET because the device operation is governed by the gate's control over the fin from multiple surfaces rather than by a conventional planar single-gate configuration.

Figure 3 shows the detailed physical and dimensional structure of the proposed Core-Shell Junctionless FinFET, providing the geometrical basis used for subsequent TCAD simulations. The proposed device dimensions and doping comcentration with materials are mention in **Table.1** The electrostatic behaviour of the proposed device is governed by distribution of electric potential within the shell, core, oxide and surrounding semiconductor regions. Described by Poisson's equation, Carrier transport in the device is described using the drift-diffusion framework. For the proposed device, the dominant electron transport occurs through the n-type shell regions. The p-type core modifies the potential distribution between these conduction paths and consequently influences electron injection and confinement. In the TCAD analysis, recombination effects are considered through the Shockley-Read-Hall mechanism, because the high-doping regions and nanoscale dimensions can influence the carrier lifetime and equilibrium carrier distribution. Because the shell and core regions employ high doping concentrations, the carrier population can approach degenerate conditions. Therefore, Fermi–Dirac statistics are employed to obtain a more physically appropriate carrier distribution under heavily doped conditions.

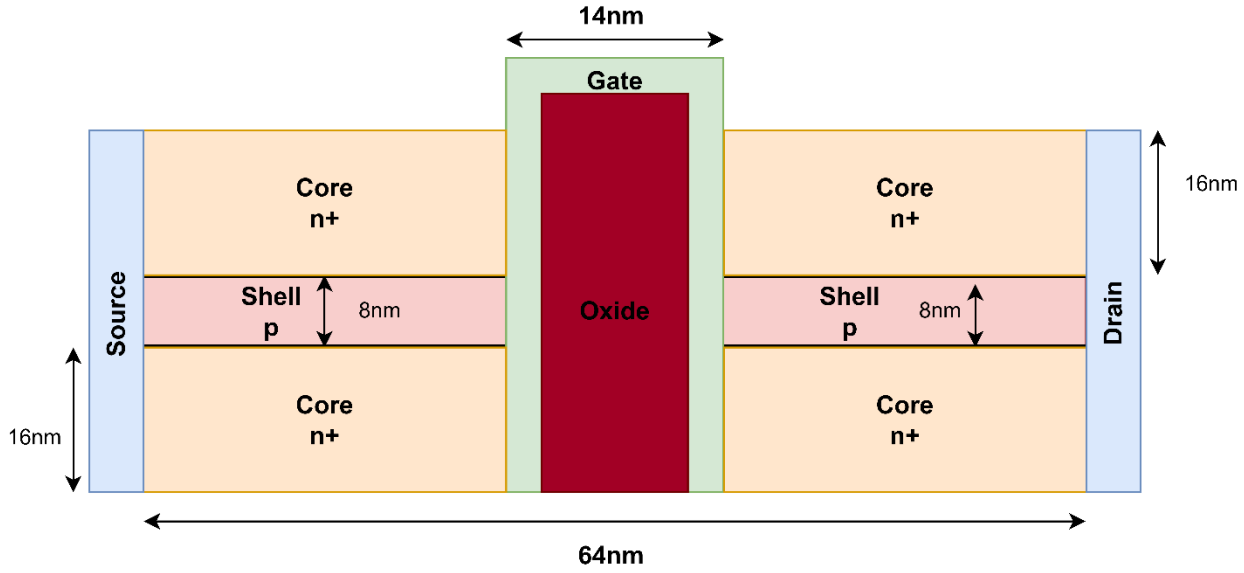


Figure 3: Cross-sectional geometry and dimensional configuration of the proposed CS-JL-FinFET.

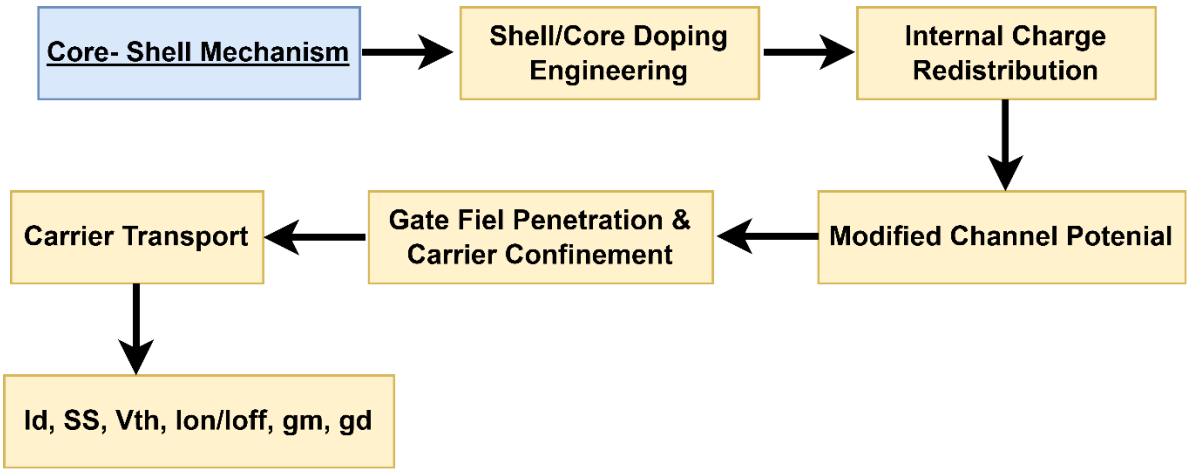


Figure 4: Schematic representation of the operating mechanism of the proposed core-shell junctionless FinFET

Figure 4 shows operating mechanism and device-performance pathway of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET). The framework establishes a direct relationship between the proposed core-shell mechanism, the associated doping engineering, the resulting internal charge redistribution and the consequent modification of carrier transport and channel electrostatics. The core-shell mechanism forms the fundamental basis of the proposed device. Channel is engineered using distinct core and shell regions allowing the electrical properties of the channel to be controlled through the spatial distribution of doping. The shell/core doping engineering introduces a difference in the carrier population between the two regions which leads to internal charge redistribution within the core-shell structure. The gate electric field interacts with the core-shell channel through the surrounding gate dielectric while the shell region influences how deeply the gate field penetrates into the active semiconductor and how carriers are spatially distributed within the core and shell.

3. Results & Discussion

The simulation analysis is conducted using Cogenda Visual TCAD.[4] Global settings were used by keeping external temperature = 300 K. [18] The drain voltage kept at 0.5V for proposed device and for the further analysis and the step size is kept at 0.05. This validation establishes the reliability of the CS-JL-FinFET. In this paper different performance analysis were done of the proposed device with comparison of conventional junctionless FinFET.

3.1 Transfer Characteristics of Conventional Junctionless FinFET (JL-FinFET)

Figure 5a shows $I_d - V_{gs}$characteristics of the conventional single-fin tri-gate JL-FinFET at different V_{ds} The device employs the same material system, dimensions, gate work function (5.2 eV) and simulation conditions as the proposed device (CS-JL-FinFET). At $V_{ds} = 0.5$V, the drain current increases from the subthreshold regime of $10^{-16} - 10^{-15}$A/µm to an ON-state current of 10^{-6}A/µm indicating effective gate-controlled channel conduction. Increasing $V_{ds}$from 0.05 to 1 V shifts the transfer characteristics toward higher drain current because of the increased electric field and stronger carrier transport.

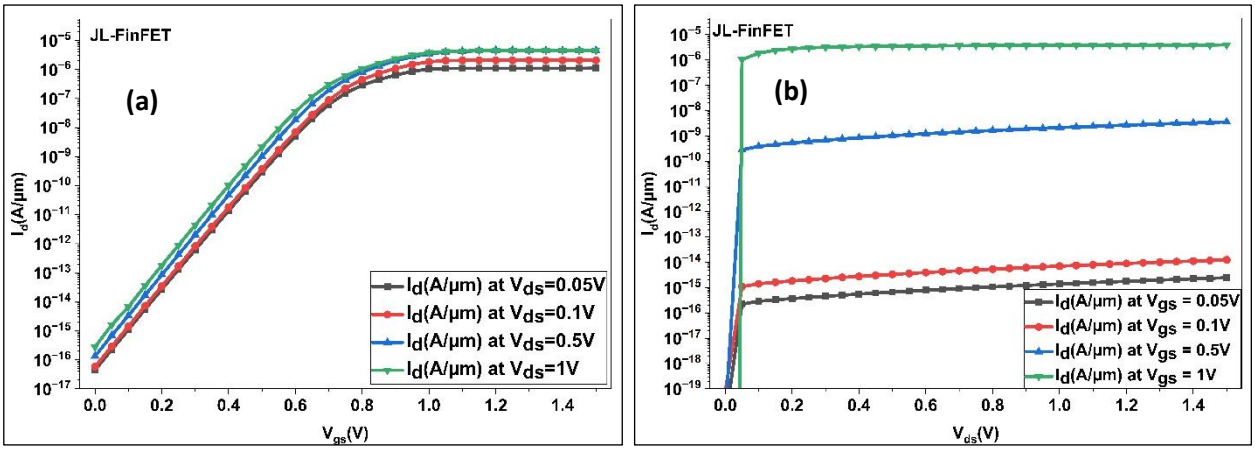


Figure 5: (a) I_d-V_{gs} Characteristic of JL-FinFET at different V_{ds} **(b)** I_d-V_{ds} Characteristic of JL-FinFET at different V_{gs}

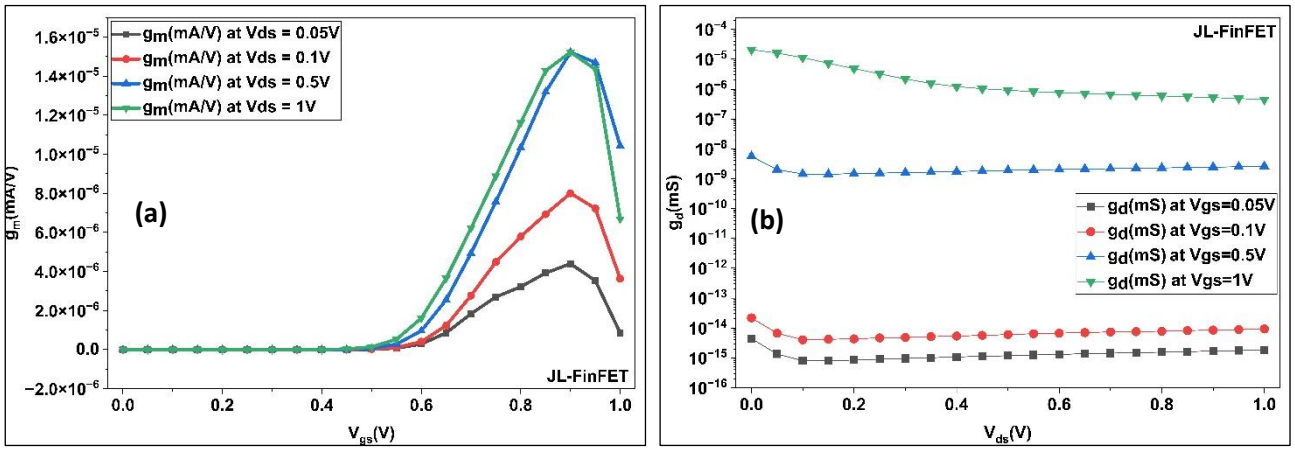


Figure 6: (a) Transconductance (gm) VS V_{gs} of JL-FinFET at different V_{ds} **(b)** Output conductance (gd) VS V_{ds} of JL-FinFET at different V_{gs}

Figure 5 (b) shows the $I_d - V_{ds}$output characteristics of the conventional JL-FinFET at different V_{gs} At $V_{gs} = 0.5$V, drain current increases in the low-V_{ds} region and exhibits a gradual increase, reaching 3×10^{-9}A/µm at $V_{ds} = 1.5$V. This relatively weak dependence of $I_d$on V_{ds}after the initial rise indicates the onset of channel pinch-off/quasi-saturation, although the finite positive slope in the saturation region indicates non-zero output conductance. At $V_{gs} = 1$V, strong channel accumulation produces the highest current, with $I_D$increasing abruptly to 10^{-6}A/µm at low $V_{DS}$and reaching ~ $3 - 4 \times 10^{-6}$A/µm at $V_{ds} = 1.5$V. The weak-gate-bias cases of $V_{gs} = 0.1$and 0.05V exhibit currents of $10^{-14} - 10^{-13}$A/µm and $10^{-16} - 10^{-15}$A/µm, respectively, over most of the V_{DS}range confirming strong suppression of conduction below the turn-on condition. The strong separation between the $V_{gs} = 1$V and low-V_{gs} characteristics shows the gate-controlled of the JL-FinFET. At $V_{gs} = 0.5$V the output current remains around the 10^{-9}A/µm range, lower than 10^{-6}A/µm obtained at $V_{gs} = 1$V showing the strong dependence of carrier transport on gate-induced channel modulation.

Figure 6 (a) shows the transconductance (g_m) for the conventional JL-FinFET at different V_{ds}. At low V_{gs}, $g_m$remains very small, $10^{-15} - 10^{-13}$mA/V, indicating weak modulation of the conducting channel. With increasing V_{GS}, $g_m$rises rapidly reflecting enhanced gate-induced carrier accumulation and increased sensitivity of drain current to gate voltage.

The $V_{DS} = 1$V characteristic exhibits the highest $g_m$over most of the rising region, followed by $V_{DS} = 0.5$, 0.1 and 0.05 V showing the influence of drain bias on carrier transport and channel charge modulation. Around $V_{GS} = 0.6 - 0.8$V, the transconductance reaches the $10^{-6} - 10^{-5}$mA/V range indicating the transition toward the high-conduction regime.

Figure 6(b) shows the output conductance, $g_d = \partial I_d/\partial V_{ds}$, of the conventional JL-FinFET at different V_{gs}. At $V_{gs} = 0.5$V, $g_d$initially decreases from 4-5 $\times 10^{-9}$S at very low $V_{DS}$and then approaches a nearly constant value of 2×10^{-9}S over $V_{DS} \approx 0.1$-1.0V. This relatively low and weakly varying $g_d$indicates that the device enters a quasi-saturation regime, where the drain voltage produces only a limited incremental change in drain current. At the higher gate bias of $V_{gs} = 1$V, the device exhibits larger output conductance, decreasing from 2×10^{-5}S at $V_{ds} \approx 0$V to about 4-5 $\times 10^{-7}$S at $V_{ds} = 1$V. The higher $g_d$is consistent with the considerably larger $I_d$observed at $V_{gs} = 1$V and indicates stronger drain-field modulation of the highly conducting channel. In the weak-conduction regime, $V_{gs} = 0.1$V and 0.05V, $g_d$remains in the $10^{-15} - 10^{-14}$S range showing strong suppression of drain-current modulation when the channel is weakly populated.

3.2 Electrostatic Behaviour of Conventional Junctionless FinFET (JL-FinFET)

A) Potential Variation at different V_{gs} of JL-FinFET

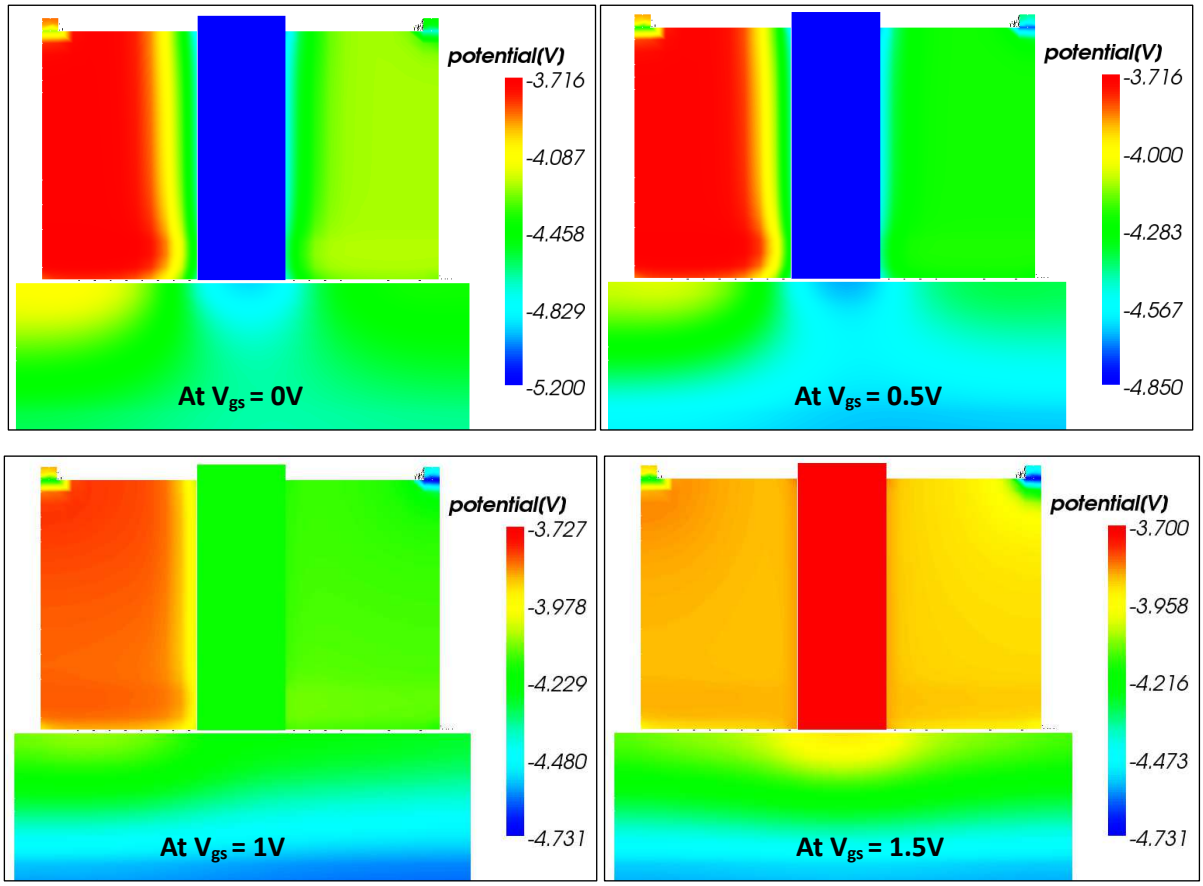


Figure 7: Potential plot of JL-FinFET at different Vgs

Figure 7 shows the electrostatic potential distribution of the conventional JL-FinFET. At $V_{gs} = 0$V, the potential distribution exhibits a pronounced negative-potential region beneath and around the gate, with the simulated potential extending from −3.716 to −5.20 V, indicating a strong electrostatic barrier and depletion of majority carriers in the uniformly doped channel. As V_{gs}increases to 0.5 V, the minimum potential increases to −4.85 V, while the potential contours beneath the gate become less negative and more spatially redistributed, showing progressive gate-induced modulation of the channel. At $V_{gs} = 1.0$V, the potential range becomes −3.727 to −4.731 V, with a substantial increase in channel potential and a smoother potential transition from the source/channel region toward the drain, indicating enhanced carrier accumulation and reduction of the depletion barrier. At the highest applied gate voltage of 1.5 V, the potential varies from −3.700 to −4.731 V and the channel region become higher in potential, confirming strong electrostatic gate control and the transition toward the highly conductive ON-state.

B) Electric Field variation at different V_{gs} of JL-FinFET

Figure 8 shows 2D electric-field distribution of the conventional JL-FinFET at different V_{gs}. At $V_{gs} = 0$V, the electric field reaches a maximum 5.473×10^6V/cm, with the strongest field concentrated near the gate-controlled channel region and gate/channel interfaces, indicating strong electrostatic potential gradients under the depleted-channel condition. At $V_{gs} = 0.5$V, the maximum field remains 5.473×10^6V/cm, but its spatial distribution becomes more confined around the central gated region. At $V_{gs}$to 1 V, the peak electric field decreases to 5.35×10^6V/cm, while the high-field region becomes narrower and more localized near the channel surface/interface. At $V_{gs} = 1.5$V, the maximum electric field further decreases to 5.28×10^6V/cm, accompanied by a comparatively smoother field distribution throughout the channel. This reduction in peak field with increasing gate bias indicates that the applied gate voltage progressively alters the channel charge distribution, transitioning the JL-FinFET from a depleted state toward majority-carrier accumulation, thereby reducing the sharpness of the internal potential gradient. The results are consistent with the potential plot in **Figure 8** where increasing V_{gs} produces progressive electrostatic modulation of the channel.

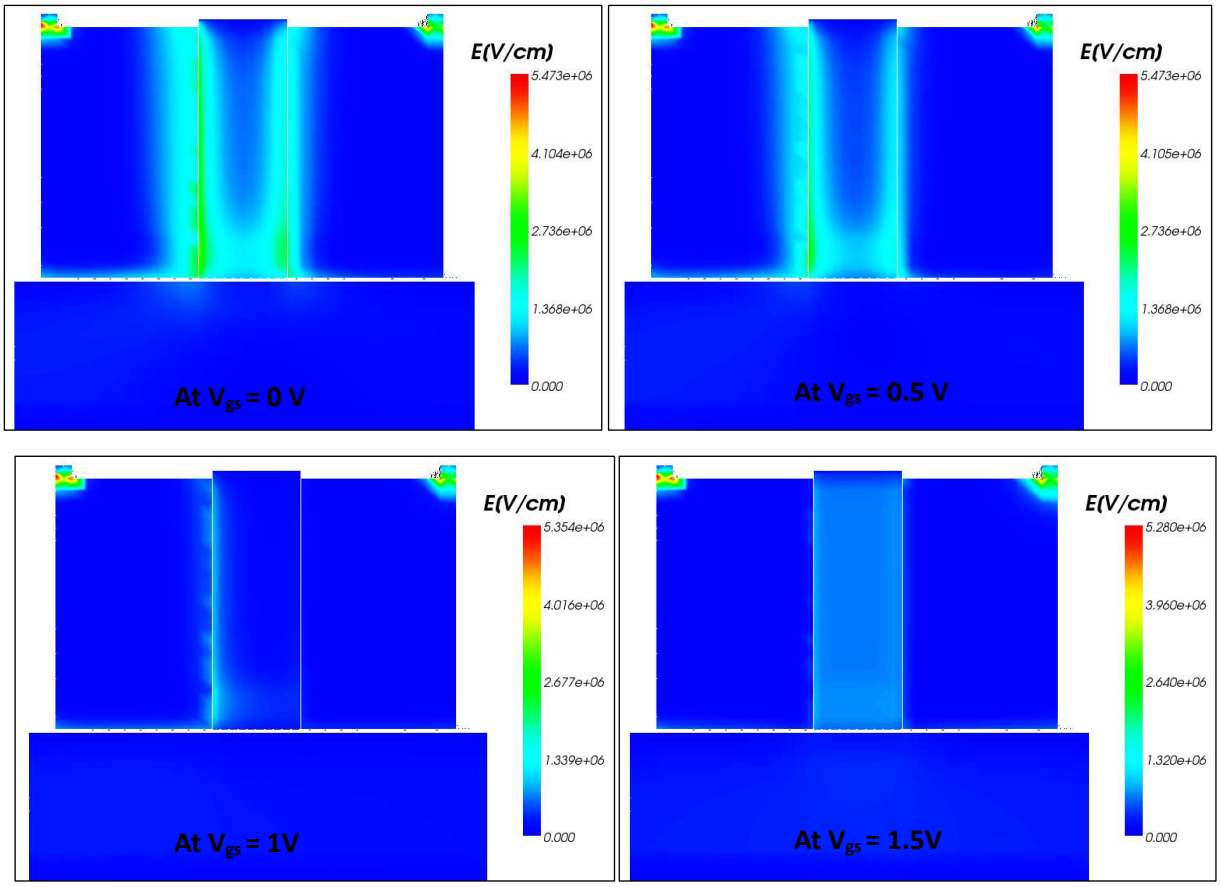


Figure 8: Electric Field plot of JL-FinFET at different V_{gs}

3.3 Transfer Characteristics of Core- Shell Junctionless FinFET (CS-JL-FinFET)

Figure 9 (a) shows the transfer characteristics ($I_d - V_{gs}$) of the proposed core-shell junctionless FinFET (CS-JL-FinFET) at different V_{ds}. At low gate bias, all characteristics exhibit extremely low drain currents, indicating effective suppression of the conducting path in the OFF-state. With increasing V_{gs}, the drain current increases rapidly over several orders of magnitude showing strong gate-controlled modulation of the carrier concentration within the shell-controlled conduction region. This behaviour originates from the junctionless operating mechanism, in which the gate electrostatically controls the uniformly doped semiconductor region without requiring conventional source/channel and channel/drain junctions. The increase in V_{ds}shifts the transfer characteristics toward higher drain current because of the enhanced electric field and drain-assisted carrier transport. At operating condition of $V_{ds} = 0.5$V which is used as the default drain bias for the proposed device, the CS-JL-FinFET achieves an ON-state current of 1.2×10^{-5}A/μm, while the OFF-state current remains of the order of 10^{-16}A/μm. I_{on}/I_{off}ratio of the order of $10^{11}$is obtained. The high ON-state current together

with low OFF-state leakage shows the potential of the proposed core-shell architecture for achieving improved switching performance.

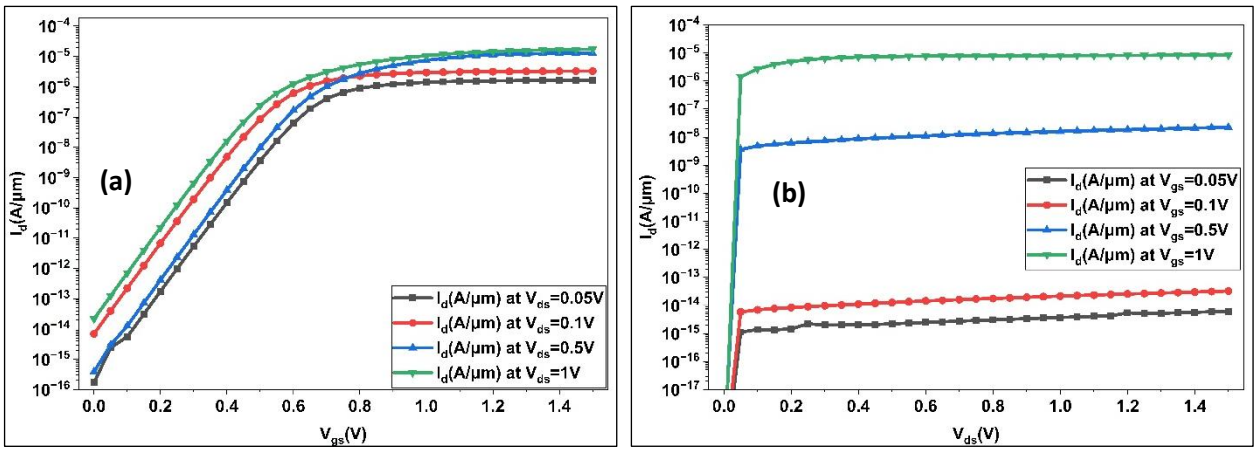


Figure 9: **(a)** I_d-V_{gs} Characteristic of CS-JL-FinFET at different V_{ds} **(b)** I_d-V_{ds} Characteristic of CS- JL-FinFET at different V_{gs}

Figure 9 (b) shows output characteristics ($I_d - V_{ds}$) of the proposed CS-JL-FinFET at different V_{ds}. At low V_{ds}, all characteristics exhibit increase in drain current, corresponding to the linear transport region. With further increase in V_{ds}, the slope of each characteristic decreases, indicating the transition toward a quasi-saturation regime. A strong dependence of the drain current on gate bias is observed with the $V_{gs} = 1$V characteristic reaching $6 - 8 \times 10^{-6}$A/μm, whereas the current at $V_{gs} = 0.05$V remains of the order of 10^{-15}A/μm. At the selected operating condition of $V_{ds} = 0.5$V, the drain current is 1.5×10^{-8}A/μm at $V_{GS} = 0.5$V and increases to the 10^{-6}A/μm range at $V_{gs} = 1$V.

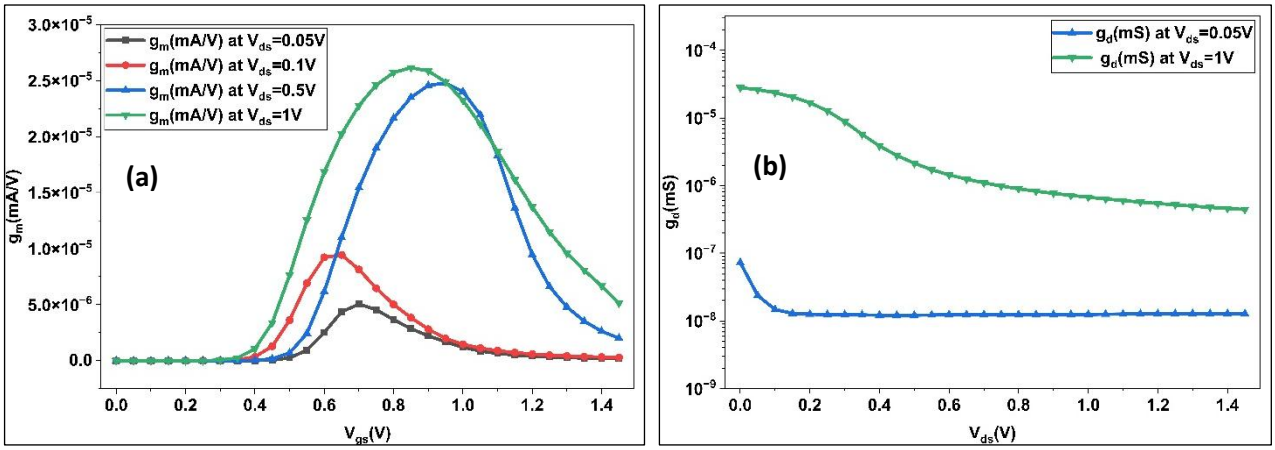


Figure.10: (a) Transconductance(gm) VS V_{gs} of CS-JL-FinFET at different V_{ds} **(b)** Output conductance (gd) VS V_{ds} of CS-JL-FinFET at different V_{gs}

Figure 10 (a) shows the transconductance (g_m) versus gate-to-source voltage (V_{GS}) characteristics of the proposed CS-JL-FinFET) at different Vds. The transconductance, defined as $g_m = \partial I_D / \partial V_{GS}$at constant V_{DS}, represents the effectiveness of the gate voltage in modulating the drain current and is an important indicator of gate controllability and current-driving capability. At low V_{gs}, 0.3-0.35 V, all curves exhibit very small g_m, corresponding to the weak-conduction region where the carrier concentration in the uniformly doped junctionless channel is strongly suppressed by gate-induced depletion. As V_{gs}increases, the gate restores the conducting channel, producing an increase in $I_d$and a steep increase in g_m. The increase becomes more at higher V_{ds}, with the peak transconductance increasing from 0.5×10^{-6}mA/V at $V_{ds} = 0.05$V to about 0.9×10^{-6}mA/V at $V_{ds} = 0.1$V, while higher values of 2.5×10^{-6}mA/V and 2.6×10^{-6}mA/V are obtained for $V_{ds} = 0.5$ and 1 V, respectively. For the nominal operating condition of $V_{ds} = 0.5$V, which is used as the default bias for the proposed device, the maximum $g_m$is 2.5×10^{-6}mA/V at $V_{gs} \approx 0.9$V. This high transconductance shows electrostatic control of the core-shell channel and strong gate-induced modulation of the drain current. After reaching the maximum, g_m decreases with further increase in V_{gs}, showing that the incremental increase in drain current becomes smaller as the device approaches its high-conduction regime.

Figure 10 (b) shows the output conductance (g_d) as a function of $V_{ds}$for the proposed (CS-JL-FinFET) at two gate-bias conditions, $V_{gs} = 0.05$V and $V_{gs} = 1$V. The output conductance is an important small-signal parameter that represents the sensitivity of the drain current to variations in drain voltage and is defined as $g_d = \partial I_D / \partial V_{DS}$at constant V_{gs}. At the low gate bias of $V_{gs} = 0.05$V, g_d reaches 7×10^{-8}mS at $V_{DS} = 0$V and decreases to 1.3×10^{-8}mS within the first 0.1–0.15 V of drain bias. Beyond this region, $g_d$remains constant at 1.2–1.4 $\times 10^{-8}$mS over the V_{DS}range up to 1.5 V. This low and almost invariant output conductance shows weak dependence of the drain current on drain-voltage variations under the low-gate-bias condition which is better results for output resistance and analog operation. At $V_{gs} = 1$V, the device exhibits higher output conductance, 2.5×10^{-5}mS at $V_{DS} = 0$V, followed by a continuous reduction as V_{ds}increases. The conductance decreases in the low-V_{ds} region and gradually reaches 4–5 $\times 10^{-7}$mS at $V_{ds} = 1.4$–1.5V. Higher $g_d$at $V_{gs} = 1$V is the stronger conducting state of the junctionless channel, where the drain voltage has a greater influence on the drain current.

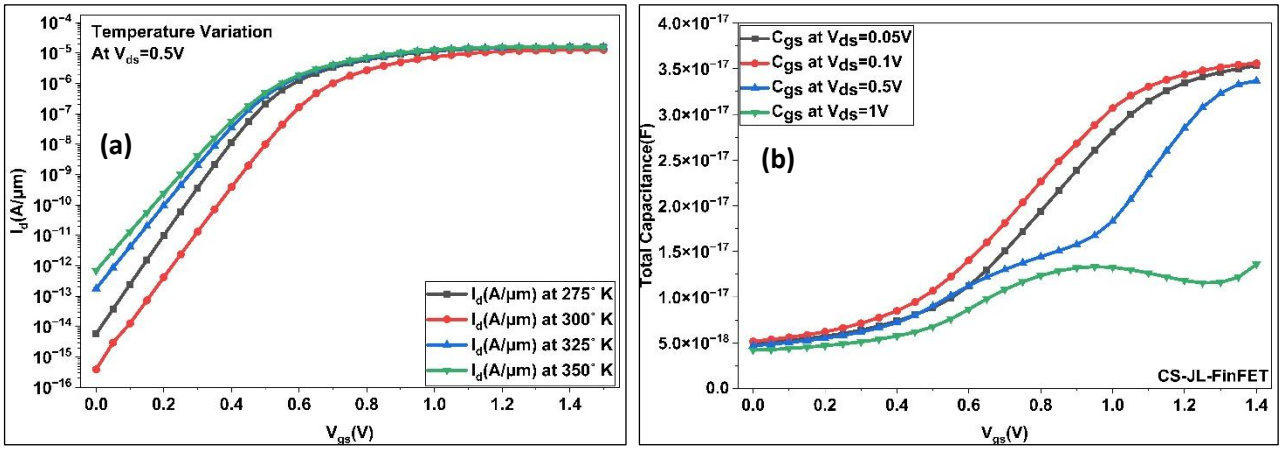


Figure 11: (a) I_d-V_{gs} of CS- JL-FinFET at different Temperature **(b)** Total Capacitance of CS-JL-FinFET at different V_{ds}

Figure 11 (a) shows the temperature-dependent $I_d - V_{gs}$characteristics of the proposed CS-JL-FinFET at $V_{ds} = 0.5$ V, showing temperatures of 275, 300, 325 and 350 K. The drain current increases with increasing temperature, with the 350 K characteristic exhibiting the highest current, followed by 325 K, 275 K and 300 K in the low-V_{GS} region. At $V_{gs} = 0$ V, the current is 10^{-12}–10^{-13} A/μm at 350 K, whereas it is around 10^{-14} A/μmat 325 K and 10^{-15}-10^{-16} A/μm at 275-300 K. This increase in off-state current with temperature is associated with enhanced thermally generated carriers and increased intrinsic carrier concentration, which reduce the effective potential barrier for carrier transport through the junctionless channel. The transfer curves also exhibit a negative shift in the effective threshold voltage with increasing temperature. The turn-on transition occurs at lower gate voltage as the temperature increases, indicating that the electrostatic condition required for strong carrier conduction is achieved more easily at high temperature. As temperature increases, thermally activated carriers partially compensate the depletion induced by the gate, thereby increasing the subthreshold leakage and shifting the transfer characteristic toward lower V_{gs}. At $V_{gs} \approx 0.5$ V, the drain current at 350 K is in the 10^{-6} A/μm range, while the 300 K device remains in the 10^{-8}–10^{-7} A/μm range, showing the strong temperature dependence of the subthreshold-to-on-state transition. **Figure. 11(a)** shows that the proposed core-shell maintains strong gate-controlled conduction across 275-350 K, while its temperature sensitivity appears as an increase in off-state/subthreshold current and a shift of the turn-on region toward lower gate voltage at high temperature.

Figure 11 (b) shows total gate capacitance for the CS-JL-FinFET. At low gate bias ($V_{gs} < 0.4$ V), all the curves exhibit low capacitance, 4.5–7 $\times 10^{-18}$F indicating weak electrostatic coupling between the gate and the semiconductor because the channel is in the depleted/off-state. As V_{gs}increases, the capacitance rises due to enhanced gate-induced carrier accumulation and increasing channel charge showing the transition toward the conducting state. For $V_{ds} = 0.05$, 0.1 and 1 V, an increase in capacitance occurs over $V_{gs} = 0.6$-1.2V, with the capacitance reaching 3.4-3.6 $\times 10^{-17}$F at higher gate voltages. The $V_{ds} = 0.05$V and $V_{ds} = 1$V in the high-V_{gs} region, suggesting that the capacitance becomes controlled by gate-induced channel charge rather than by drain-bias variation once the device enters strong conduction. $V_{ds} = 0.5$V characteristic exhibits a different behavior: C_{gs}increases to 1.3 $\times 10^{-17}$F near $V_{gs} \approx 0.9$–1.0V, followed by a reduction to 1.15-1.2 $\times 10^{-17}$F around $V_{gs} \approx 1.2$–1.3V, before increasing again toward 1.7–1.8 $\times 10^{-17}$F at $V_{gs} = 1.5$V.

3.4 Electrostatic Behaviour of Core- Shell Junctionless FinFET (CS-JL-FinFET)

(A) Potential at different V_{gs} of CS-JL-FinFET

Figure 12 shows electrostatic potential distribution of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET) at different gate biases, under $V_{ds} = 0.5$V. At $V_{gs} = 0$V, the potential varies from −3.716 to −5.200 V, producing a strongly negative potential region in the channel and indicating substantial depletion of the uniformly doped semiconductor. When V_{gs} increases to 0.5 V, the minimum potential rises to −4.850 V, accompanied by a redistribution of the potential around the gate-controlled core-shell region, showing gate-induced modulation of the channel electrostatics. At $V_{gs} = 1$ V, the potential range becomes −3.727 to −4.731 V, while the channel region exhibits a considerably modified potential profile, indicating enhanced majority-carrier accumulation and reduction of the depleted-channel barrier. At $V_{gs} = 1.5$V, the potential extends from −3.700 to −4.731 V, with the channel reaching its highly accumulated conductive state. Since the proposed device operates on the junctionless principle, this evolution is attributed to depletion-to-accumulation modulation of the uniformly doped core-shell channel, rather than conventional inversion-layer formation.

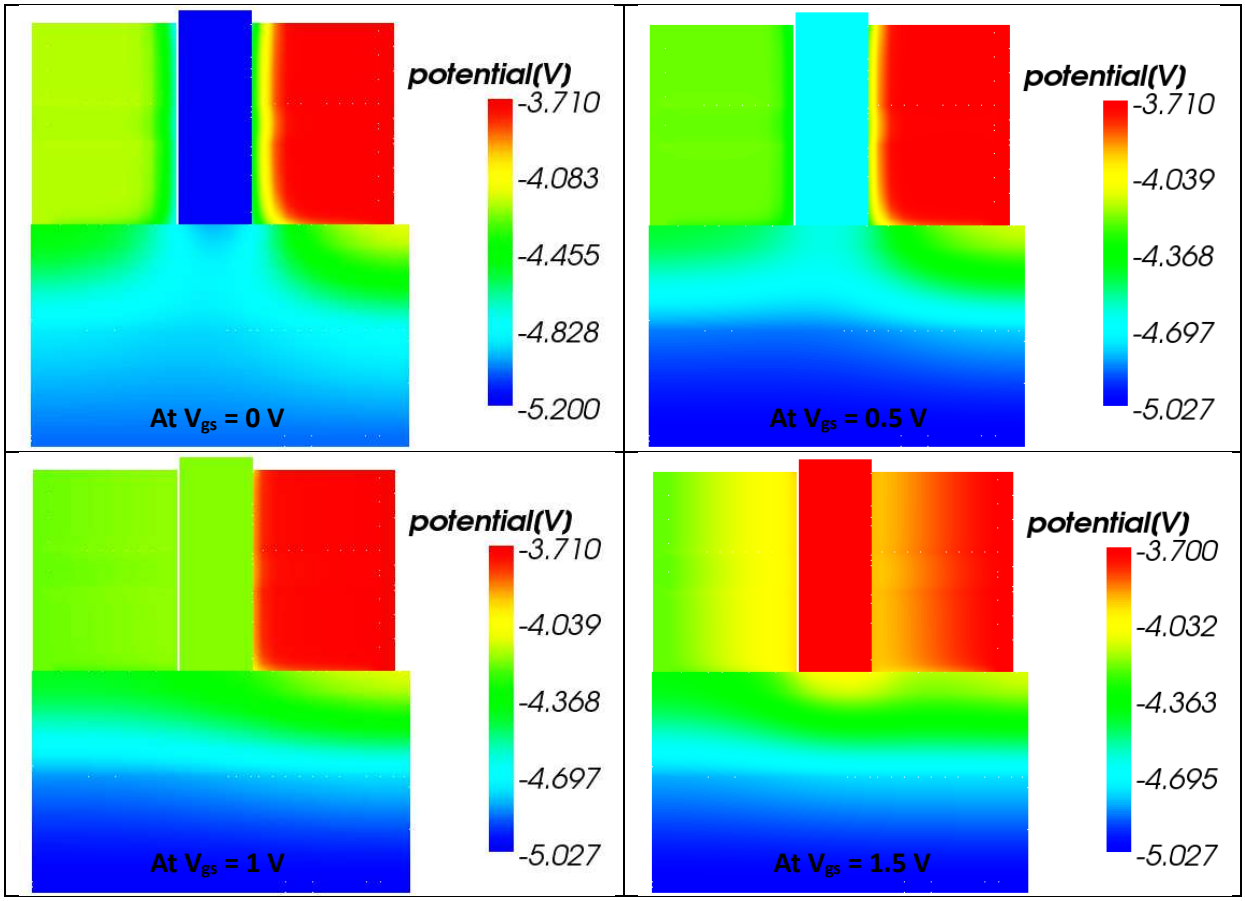


Figure 12: Potential plot of CS-JL-FinFET at different V_{gs}

Figure 13 shows electric-field distribution of the proposed CS-JL-FinFET at different V_{gs} with the drain bias maintained at $V_{ds} = 0.5$V. At $V_{gs} = 0$V, the peak electric field reaches 7.76×10^6V/cm, with the field strongly concentrated around the gate-controlled core-shell channel and its interfaces, corresponding to the highly depleted OFF-state. As V_{gs} increases to 0.4 V, the peak field decreases to 6.619×10^6V/cm, indicating redistribution of the electric potential and channel charge. At $V_{gs} = 1.0$V, the maximum field is reduced to 2.953×10^6V/cm, while the high-field region becomes more localized within the channel. At $V_{gs} = 1.5$V, the peak electric field further decreases to 8.758×10^5V/cm, producing a considerably smoother and weaker field distribution across the conductive region. Thus, the peak electric field decreases

from 7.76 MV/cm to 0.876 MV/cm, corresponding to 88.7% reduction over the investigated gate-voltage range. This behavior is associated with the depletion-to-accumulation mechanism of the junctionless device, where increasing positive gate bias attracts and accumulates majority carriers within the uniformly doped core-shell channel reducing the electrostatic potential gradient required to sustain channel conduction.

(B) Electric Field at different V_{gs} of CS-JL-FinFET

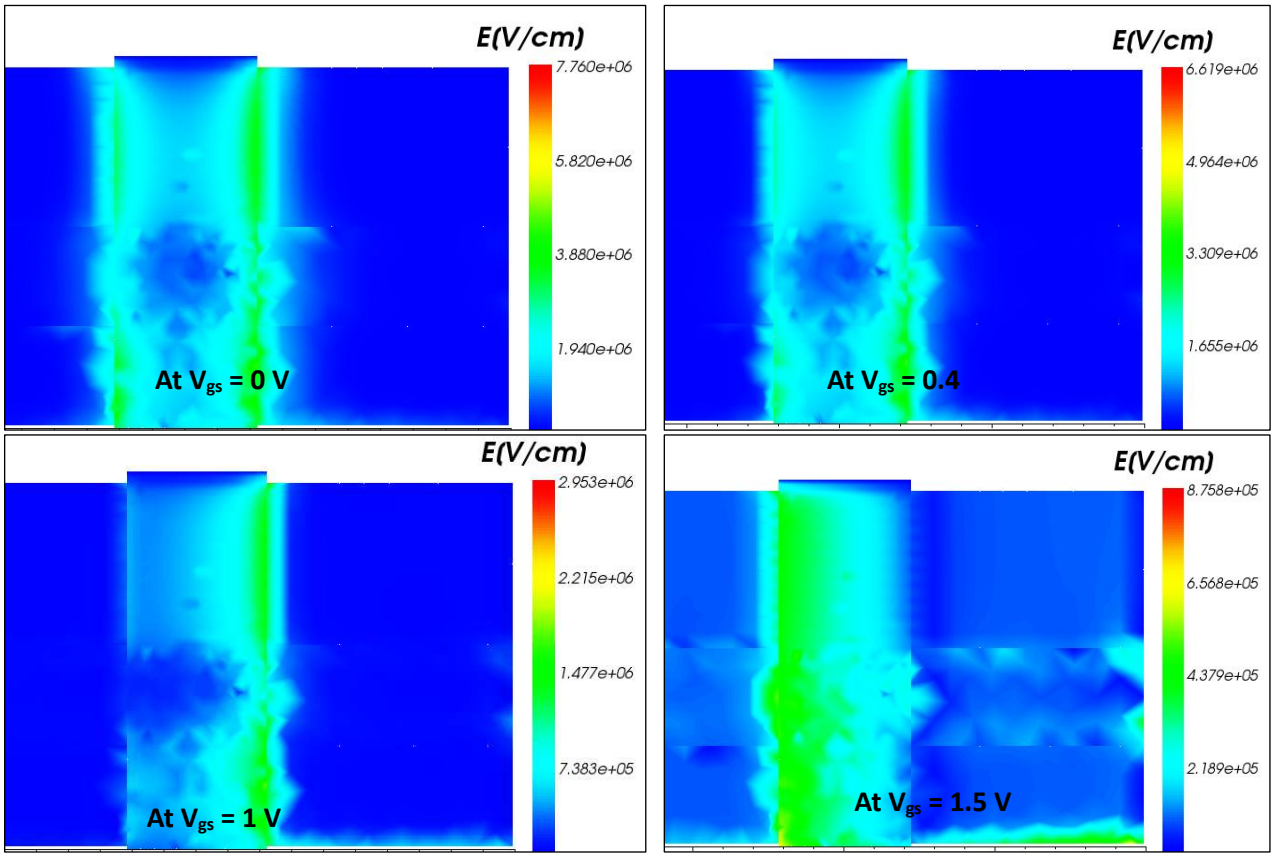


Figure 13: Electric field plot of CS-JL-FinFET at different V_{gs}

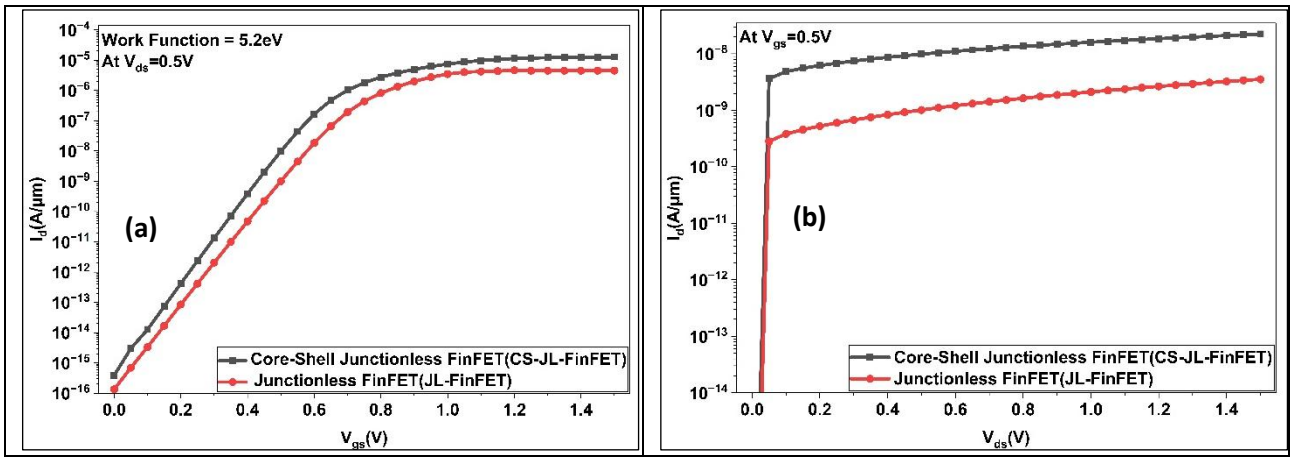


Figure 14: (a) Id-Vg Characteristic Comparison of Conventional JL-FinFET & CS-JL-FinFET **(b)** Id-Vd Characteristic Comparison of Conventional JL FinFET & CS-JL-FinFET

Figure 14 (a) shows the comparative transfer characteristics ($I_d - V_{gs}$) of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET) and the conventional Junctionless FinFET (JL-FinFET). Both devices are considered with the same

fundamental material system and device dimensions. The gate work function is fixed at 5.2 eV, allowing the improvement in electrical characteristics to be primarily associated with the core-shell device architecture rather than a change in gate-metal work function. In the subthreshold region, the proposed CS-JL-FinFET exhibits a lower and more controlled leakage-current regime while showing an earlier increase in drain current with increasing V_{gs}. The black curve corresponding to the proposed CS-JL-FinFET reaches an $I_{\text{on}}/I_{\text{off}}$ ratio of 10^{11}, whereas the conventional JL-FinFET, represented by the red curve, provides 10^{10}. Thus, the proposed core-shell achieves a one-order-of-magnitude (10×) improvement in the $I_{\text{on}}/I_{\text{off}}$ratio. This improvement is important for low-power digital applications because a high $I_{\text{on}}/I_{\text{off}}$ratio indicates strong current-driving capability in the ON-state and effective suppression of unwanted leakage in the OFF-state.

From a device-physics perspective, these results show the principal advantage of introducing the core-shell architecture into the junctionless FinFET. The conventional JL-FinFET relies on gate-induced depletion and accumulation of a uniformly doped semiconductor body. In the proposed CS-JL-FinFET, the 8-nm core and 16-nm shell regions modify the spatial distribution of carriers and the gate-controlled electrostatic potential throughout the channel. The surrounding shell regions increase the effective electrostatic interaction between the gate and the channel, while the reduced core dimension assists gate control over the central conducting region. This configuration therefore provides a more efficient mechanism for suppressing the depleted-state carrier concentration while maintaining a high carrier concentration during the ON-state. The resulting combination of higher I_{ON}, extremely low I_{OFF} and one-order improvement in $I_{\text{on}}/I_{\text{off}}$ provides strong evidence that core-shell engineering is an effective structural approach for improving the performance of junctionless FinFETs.

Figure 14 (b) presents the output characteristics ($I_d - V_{ds}$) of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET) and the conventional Junctionless FinFET (JL-FinFET) at a fixed gate-to-source voltage of $V_{gs} = 0.5$V. The comparison is performed using the same material system and comparable device dimensions, while the proposed device employs the core-shell channel architecture with an 8-nm core and two 16-nm shell regions. The drain current is plotted over $V_{ds} = 0 - 1.5$V enabling low-current behavior as well as the output-current variation in the higher drain-bias regime. The black curve represents the proposed CS-JL-FinFET, whereas the red curve corresponds to the conventional JL-FinFET. At very low drain bias, both devices exhibit increase in I_d as V_{ds} is increased from zero. This initial region corresponds to the low-field/linear operating regime, where the applied drain voltage increases carrier transport from source toward drain. The proposed CS-JL-FinFET exhibits a higher drain current than the conventional JL-FinFET from the beginning of the conducting region. Around $V_{ds} \approx 0.05 - 0.1$V, the CS-JL-FinFET reaches a drain current of $4 \times 10^{-9}$to 5×10^{-9}A/μm, whereas the conventional JL-FinFET reaches $4 \times 10^{-10}$to 5×10^{-10}A/μm.

With further increase in V_{ds}, the drain current of both devices continues to increase, but the rate of increase becomes considerably smaller. At $V_{ds} = 1.0$V, the proposed CS-JL-FinFET provides an I_d of 8×10^{-9}–1×10^{-8} A/μm, while the conventional JL-FinFET produces 2×10^{-9}–3×10^{-9} A/μm. At the maximum plotted drain voltage of 1.5 V, the proposed device reaches 1.1×10^{-8}–1.2×10^{-8} A/μm, whereas the conventional JL-FinFET remains around 3×10^{-9}–4×10^{-9} A/μm. Therefore, the proposed device maintains 3-4× higher output current in the high-V_{ds} region. The proposed device shows $I_{\text{on}} \sim 10^{-5}$A/μm and an $I_{\text{on}}/I_{\text{off}} \sim 10^{11}$ compared with 10^{-6}A/μm and 10^{10} respectively for the conventional JL-FinFET.

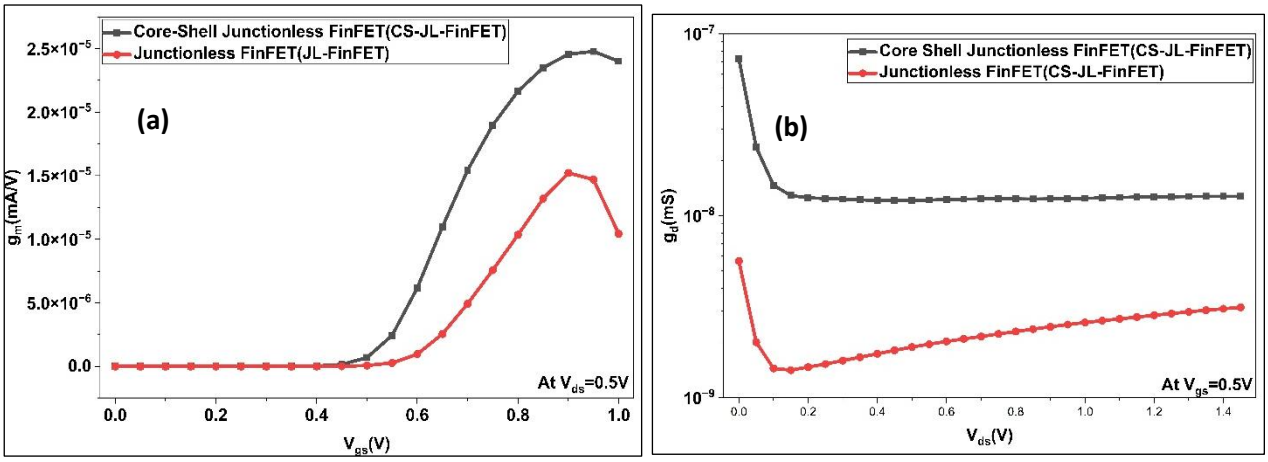


Figure 15: (a) Transconductance (gm) Characteristic Comparison of Conventional JL-FinFET & CS-JL-FinFET **(b)** Output Conductance (gd) Characteristic Comparison of Conventional JL-FinFET & CS-JL-FinFET

Figure 15 (a) compares the transconductance (g_m) for the proposed CS-JL-FinFET and the conventional JL-FinFET at $V_{ds} = 0.5$V. The comparison is important because $g_m = \partial I_D/\partial V_{GS}$ shows the ability of the gate voltage to modulate the drain current and is therefore a direct measure of the gate-control efficiency, carrier modulation capability and potential high-speed/analog performance of the device. Both devices are evaluated under the same basic material and dimensional conditions. At low gate voltages, below $V_{gs} = 0.4$–0.45V, the transconductance of both devices remains almost zero because the channel in the depleted or weak-conduction regime and a small variation in gate voltage produces only a limited change in drain current. As V_{gs} increases beyond 0.45 V, the $g_m$of the proposed CS-JL-FinFET begins to increase rapidly. In comparison, the conventional JL-FinFET exhibits a delayed and weaker increase, with its substantial transconductance enhancement occurring at $V_{gs} = 0.55$–0.60V. This earlier onset of high transconductance in the proposed device is consistent with the improved gate electrostatic control obtained from the core-shell channel configuration. The proposed device reaches a maximum $g_m$of 2.4–2.5×10^{-5}mA/V at around $V_{gs} \approx 0.9$–0.95V, conventional JL-FinFET reaches a maximum of 1.5×10^{-5}mA/V at $V_{gs} \approx 0.9$V. The proposed device provides 1.6–1.7 ×higher peak transconductance, corresponding to an improvement of roughly 60–67% over the conventional JL-FinFET. This enhancement shows that the proposed structural modification improves not only the drain-current capability but also the efficiency with which the gate voltage controls the channel current.

Figure 15 (b) compares the drain/output conductance (g_d) of the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET) with the conventional Junctionless FinFET (JL-FinFET) at 0.5 V. Since $g_d = \partial I_D/\partial V_{DS}$, it shows the sensitivity of the drain current to variations in drain voltage and important indicator of output-channel modulation and intrinsic analog performance. Lower $g_d$is generally desirable because it corresponds to higher output resistance and improved intrinsic voltage gain. At very low V_{ds}, the proposed CS-JL-FinFET exhibits a relatively high g_d, initially 5×10^{-8}S, followed by a sharp reduction as V_{ds} increases. The conductance decreases during the initial 0–0.1 V region and subsequently reaches 1.2–1.3×10^{-8}S. This initial reduction indicates the transition from the low-field/linear transport regime toward the saturation-dominated operating region. Once V_{ds} exceeds 0.1–0.2 V, the relatively flat $g_d$characteristic shows that the drain current becomes less sensitive to further increases in drain voltage, indicating comparatively stable output characteristics. The conventional JL-FinFET shows lower $g_d$throughout the V_{ds} range. Its $g_d$begins at 5×10^{-9}S, decreases to a minimum of 1.4-1.6×10^{-9}S around $V_{DS} \approx$ 0.1-0.15V, and then exhibits a gradual increase with increasing V_{ds}, reaching 2.5–3×10^{-9}S near $V_{ds} = 1.5$V. The gradual increase in $g_d$at higher drain bias indicates stronger drain-induced modulation of the channel current in the conventional structure.

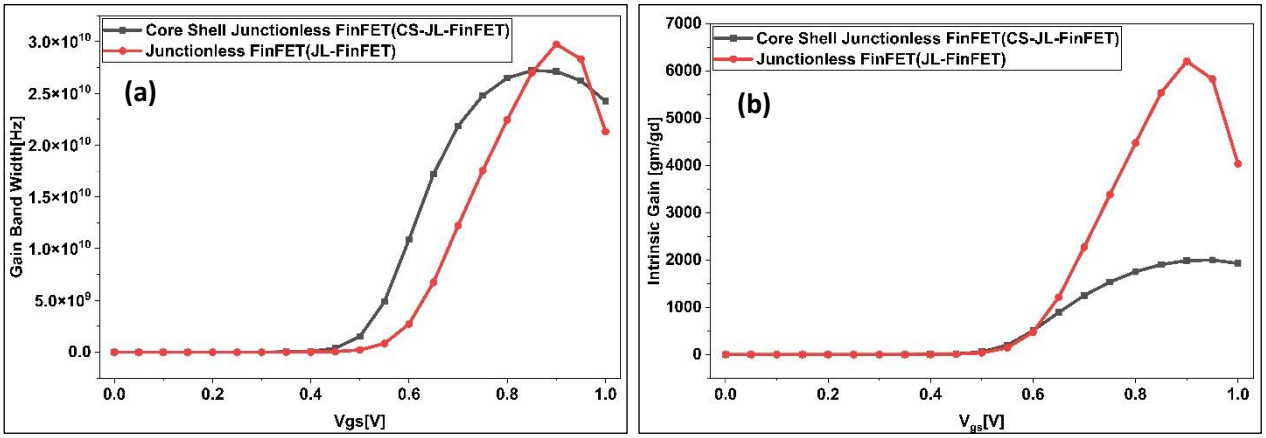


Figure16: (a) Gain Band Width Comparison of Conventional JL-FinFET & CS-JL-FinFET **(b)** I_d-V_g Characteristic Comparison of Conventional JL-FinFET & CS-JL-FinFET

Figure 16 (a) shows the gain-bandwidth performance of the proposed CS-JL-FinFET in comparison with JL-FinFET with the drain-to-source voltage $V_{ds} = 0.5$V. Gain-bandwidth is an important high-frequency figure of merit because it reflects the ability of the device to provide high transconductance and high-speed operation. In a transistor, the gain-bandwidth behaviour is strongly related to the relationship between the transconductance $g_m$and the gate/input capacitance; therefore, the evolution of this parameter with gate voltage provides useful information about the suitability of the proposed device for high-frequency and RF-oriented VLSI applications. At low gate voltages, $V_{gs} < 0.4$V, both devices exhibit an almost negligible gain-bandwidth response. As V_{gs} reaches 0.45-0.50 V, the gain-bandwidth response begins to increase, indicating the onset of strong channel conduction and a rapid increase in g_m. Difference between the two devices becomes evident in the transition region. The proposed CS-JL-FinFET exhibits a much earlier and steeper

increase in gain-bandwidth, beginning around $V_{gs} \approx 0.45$V and reaching 5×10^9Hz near $V_{gs} \approx 0.55$V. It subsequently increases rapidly, reaching 1.7×10^{10}Hz at $V_{gs} \approx 0.65$V and 2.3×10^{10}Hz at $V_{gs} \approx 0.75$V. The device reaches a maximum/near-maximum gain-bandwidth of 2.7×10^{10}Hz around $V_{gs} \approx 0.80$–0.85V. The conventional JL-FinFET shows a delayed gain-bandwidth enhancement. Its response remains close to zero until $V_{gs} \approx 0.50$–0.55V, after which it increases progressively. It reaches 2.5×10^9Hz around $V_{gs} \approx 0.60$V, 1.2×10^{10}Hz around $V_{gs} \approx 0.70$V and 2.2×10^{10}Hz around $V_{gs} \approx 0.80$V. The JL-FinFET eventually reaches the highest peak in the plotted comparison, 2.9–3.0 $\times 10^{10}$Hz at $V_{gs} \approx 0.90$V.

Figure 16(b) compares the intrinsic voltage gain, $A_v = g_m/g_d$ of the proposed CS-JL-FinFET with the conventional JL-FinFET at $V_{ds} = 0.5$V. Since intrinsic gain is determined by the ratio of transconductance to drain conductance, the characteristic provides an important assessment of the device's suitability for analog and mixed-signal applications, where high voltage gain is desirable. At low gate voltages ($V_{gs} <$ 0.4–0.45 V), both devices exhibit nearly negligible intrinsic gain because the devices remain in the weak-inversion/off-state, resulting in very small g_m. As V_{gs} approaches the conduction region, the intrinsic gain of both devices increases rapidly. The proposed CS-JL-FinFET begins its gain enhancement at $V_{GS} = 0.45$–0.50 V and reaches around 1.0×10^3near $V_{GS} \approx 0.65$V. The gain subsequently increases to 1.5×10^3at $V_{gs} \approx 0.75$–0.80 V and approaches a maximum of 2.0×10^3around $V_{gs} = 0.90$–0.95 V. Beyond this region, the gain remains relatively stable and shows a slight reduction toward $V_{GS} = 1.0$V, where it is 1.9×10^3.

Conventional JL-FinFET shows stronger increase in the plotted intrinsic-gain ratio after $V_{gs} = 0.55$V. Its gain reaches 1.0×10^3near $V_{gs} = 0.65$V, increases to 3.3×10^3at $V_{gs} \approx 0.75$V and reaches a maximum of 6.2×10^3around $V_{gs} =$ 0.90V. The gain decreases to 5.8×10^3at $V_{gs} = 0.95$V and 4.0×10^3at $V_{gs} = 1.0$V. CS-JL-FinFET exhibits the intended improvements in several digital characteristics, **Figure 16(b)** reveals an important trade-off in the analog domain: the conventional JL-FinFET provides a substantially higher intrinsic gain than the proposed CS-JL-FinFET over the strong-inversion region. The maximum gain of the conventional device is ~ $6200/2000 \approx 3.1$times that of the proposed device. This behaviour should not automatically be interpreted as a failure of the proposed architecture; rather, it indicates that the core-shell engineering modifies the balance between transconductance and drain conductance.

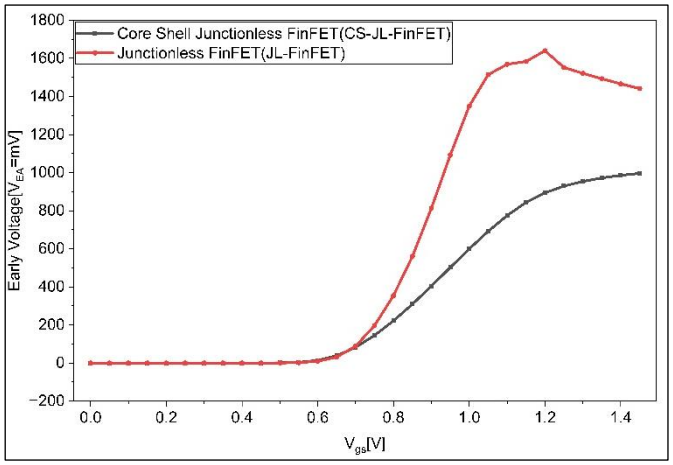


Figure 17: Early Voltage Comparison of Conventional JL-FinFET & CS-JL-FinFET at different V_{ds}

Figure 17 shows the variation of the Early voltage (V_{EA}) with gate-to-source voltage (V_{gs}) for the proposed device (CS-JL-FinFET) and conventional JL-FinFET. The Early voltage represents the sensitivity of drain current to drain voltage in the saturation region. A larger Early voltage indicates weaker channel-length modulation and a more ideal current-source behaviour. At low V_{gs}, below 0.5-0.55 V, both devices exhibit an Early voltage close to zero. This behaviour is associated with the weak-conduction/off-state regime, where the drain current is extremely small and meaningful extraction of the Early voltage becomes less. As V_{gs}increases beyond 0.55 V, both devices enter the strong conduction region and V_{EA}increases rapidly. Conventional JL-FinFET reaching 400 mV at $V_{gs} \approx 0.8$V, followed by a steep rise to 800-850 mV at $V_{gs} \approx 0.9$V. It reaches 1.3-1.5 V (1300-1500 mV) around $V_{gs} = 1.0$–1.1 V and attains a maximum of 1630 mV at $V_{gs} \approx$ 1.2V. The Early voltage gradually decreases, reaching 1500 mV at $V_{gs} \approx 1.3$V and 1440 mV at $V_{gs} = 1.45$V. CS-JL-FinFET shows more gradual increase in Early voltage. conventional JL-FinFET possesses a higher Early voltage over

most of the strong-inversion region, with a maximum of 1.63 V, compared with 1V for the CS-JL-FinFET. JL-FinFET exhibits weaker apparent channel-length modulation and consequently a more favourable output-resistance characteristic. The relationship can be expressed as

$$V_{EA} \approx \frac{I_D}{g_d}$$

where $I_d$is the drain current and $g_d$is the drain conductance. Higher V_{EA}corresponds to a smaller $g_d$for a given drain current. The comparative analysis was performed against a conventional single-fin JL-FinFET under identical material, dimensional, gate-work-function and bias conditions as shown in Table 2.

Table 2: Performance Table of JL-FinFET and CS-JL-FinFET

Parameters	**Proposed Device**	**Single Fin Junctionless FinFET**
Intrinsic Gain (A_v) =g_m/g_d	0.68	1.24
Cut-off Frequency (f_T)=$g_m/2\pi C_{gg}$ (GHz)	$0.92 * 10^9$	$0.64 * 10^9$
Early Voltage (V_A)=I_d/g_d (V)	0.34V	0.60V
Output Resistance (R_{out})=$1/g_d$ (kΩ)	$7.64 * 10^4$	$4.60 * 10^5$
Subthreshold Slope (SS) =$dV_g/d(\log I_d)$	64	82.7
Current Ratio I_{on}/I_{off}	10^{11}	10^{10}
g_m (mA/V)	8.54×10^{-6}	$3.01 * 10^{-6}$
g_d (mS)	$1.49 * 10^{-8}$	$2.37 * 10^{-9}$
OFF State Current I_d (A/μm)	10^{-16}	10^{-16}
ON State Current I_d(A/μm)	10^{-5}	10^{-6}
Vth(V)	0.44	0.49
I_d(A/μm)	$4.64 * 10^{-5}$	$1.79*10^{-6}$
DIBL (mV/V)	67	89

4. Circuit Implementation

Figure 18 depict the resistive-load inverter configuration using the proposed Core-Shell Junctionless FinFET (CS-JL-FinFET) for circuit-level operation. The circuit employs the proposed device with its source terminal connected to ground and its drain connected to a 1-kΩ load resistor (R_1) which is connected to a 0.5-V DC supply (V_2). The gate terminal is driven by a periodic pulse source V_1, with a low-level voltage of 0 V and a high-level voltage of 0.5 V. The applied pulse has 50 ps rise time, 50 ps fall time, 5 ns pulse width and 10 ns period providing an input switching frequency of ~100 MHz. The drain voltage is monitored using the indicated probe allowing the transient response of the device-based inverter to be evaluated.

Figure 19(a) shows time-domain input and output waveforms of the inverter. The upper waveform represents the inverter output, whereas the lower waveform represents the applied input pulse. When the input voltage is at its low level ($V_{IN} =$ 0 V), the CS-JL-FinFET remains in the OFF/weak-conduction state, resulting in a small drain current. The voltage drops across the 1-kΩ load resistor is small and the output node is pulled toward the supply voltage, producing an output of ~ 0.5 V. When the input rises to 0.5 V, the proposed device enters its conducting state, increasing the current through the resistive load and producing a voltage drop across R_1. Hence, the circuit exhibits the fundamental inverting behavior.

Figure 19(b) presents the DC transfer characteristic. The linear red characteristic represents the voltage relationship associated with the resistive load, while the nonlinear green characteristic represents the transistor response. Their intersection defines the operating point of the inverter for the corresponding bias condition. The transition region of the device characteristic occurs around $V \approx 0.25$V indicating that the output voltage changes rapidly within the intermediate

input-voltage region. At low input voltage, the transistor current is strongly suppressed and the output remains close to the supply voltage of 0.5 V. The circuit behaviour can be understood from the resistive-load relationship,

$$V_{OUT} = V_{dd} - I_d R_L,$$

where $V_{dd} = 0.5\text{V}$ and $R_L = 1\text{k}\Omega$. Thus, the drain current generated by the CS-JL-FinFET directly determines the output voltage. This also establishes an important connection with the earlier $I_d - V_{gs}$ characteristics: the high I_{ON} of the proposed device facilitates a larger voltage drop across the load during the ON-state, while its extremely low OFF-state current allows the output node to remain close to V_{dd} during the OFF-state. Therefore, $I_{\text{on}}/I_{\text{off}} \sim 10^{11}$ has direct circuit-level relevance to the inverter operation. The use of a 0.5-V supply and 0-0.5-V input swing also makes the circuit relevant to low-voltage VLSI operation.

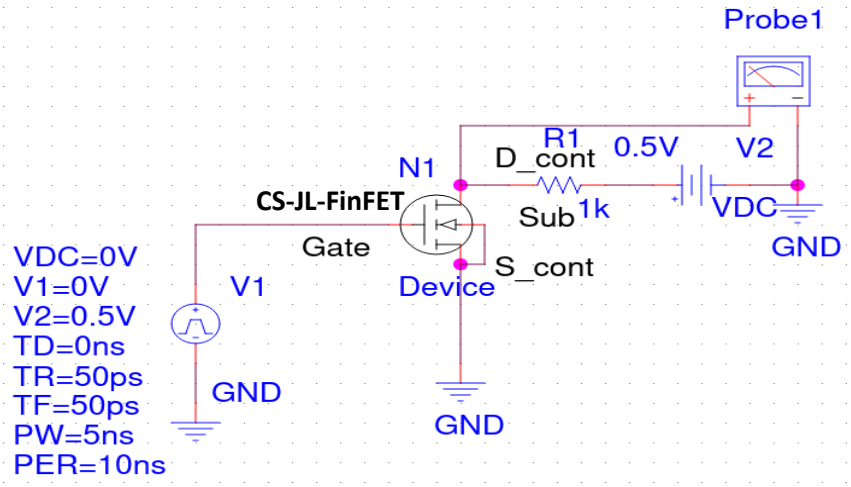


Figure 18: Resistive-load inverter configuration based on the proposed core-shell junctionless FinFET

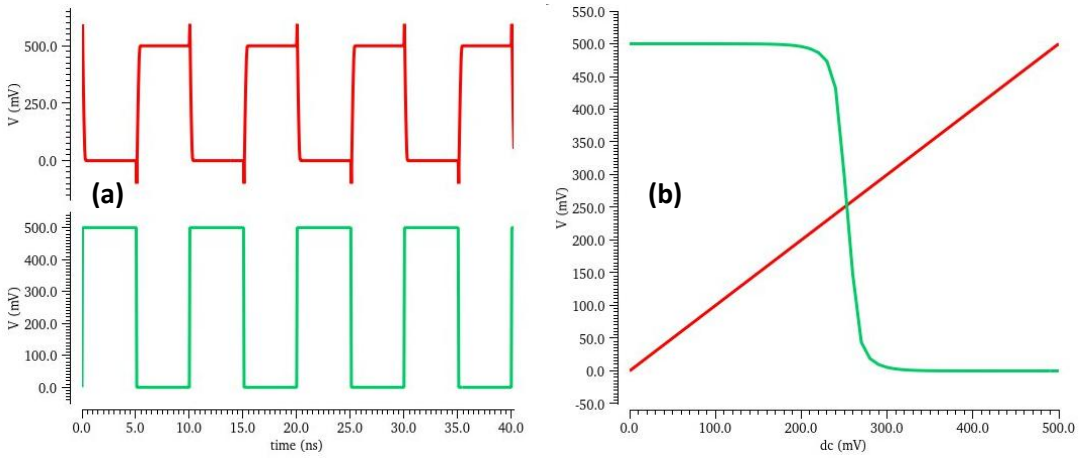


Figure 19: (a) Transient input and output voltage responses **(b)** DC voltage-transfer characteristic

Table 3 Comparison Table from Literature Review

	Technology Node	Ion, Ioff and Ion/Ioff Ratio	SS (mV/dec)	V_{th} (V)	DIBL (mV/V)
Dou, Cunhua, et al (2025) [14]	22nm	Ion=10^{-6}, Ioff=10^{-14} & Ion/Ioff=10^{8}	90	0.8	100
Y. -C. Lu et al (2024) [31]	100nm	Ion/Ioff=10^{7}	64	0.1	85
V. B. Sreenivasulu et al (2024) [33]	30nm	Ion=10^{-7}, Ioff=10^{-21}, Ion/Ioff=10^{6}	60.65	0.4	6.9
Som Arnab et al(2026) [26]	20nm	Ion/Ioff=10^{9}	65	0.5	-
Shekhar Verma et al. (2023]) [19]	14nm	Ion=10^{-6}, Ioff =10^{-19}, Ion/Ioff=10^{13}	43.2	0.4	15.4
Proposed Device	14nm	Ion=10^{-5}, Ioff= 10^{-16}, Ion/Ioff=10^{11}	64	0.4	67

Conclusion

This work presented 3D TCAD of a Core-Shell Junctionless FinFET (CS-JL-FinFET) design to overcome the limitations with conventional junctionless FinFETs while improving gate-controlled carrier transport in nanoscale devices. The proposed device integrates a core-shell doping with a single-fin tri-gate structure. At $V_{ds} = 0.5$V, the proposed CS-JL-FinFET achieves an I_{on} of 10^{-5}A/µm while maintaining an $I_{OFF}$of 10^{-16}A/µm, resulting in an I_{on}/I_{off} ratio of 10^{11}. This represents one order-of-magnitude improvement in switching ratio over the conventional JL-FinFET. The proposed device also shows a subthreshold swing of 64 mV/dec indicating effective gate control in the subthreshold regime. The peak transconductance is 60-67% higher than that of the reference JL-FinFET. The study also establishes an important digital-analog performance trade-off. Although the CS-JL-FinFET provides higher drain current and transconductance, its higher output conductance results in lower output resistance, intrinsic gain and Early voltage than the conventional JL-FinFET. Temperature analysis from 275-350 K further confirms stable gate-controlled conduction, although increased temperature produces higher subthreshold/off-state leakage and a negative shift in the effective threshold voltage. The low absolute gate capacitance indicates the potential for reduced capacitive loading and improved switching-energy characteristics. Implementation of the proposed device in a 0.5-V resistive-load inverter shows functional voltage inversion, establishing its feasibility for circuit-level integration. Its performance has been compared with recent devices as shown in Table 3. Future work will focus on optimization of core thickness, shell thickness, core/shell doping concentrations, oxide thickness, gate work function and fin dimensions to further improve the balance between I_{on}, I_{off}, SS, DIBL, g_m, g_d, intrinsic gain and high-frequency performance. Such investigations can establish an optimized CS-JL-FinFET architecture capable of simultaneously addressing high-performance digital switching and analog/RF requirements.

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Author contributions

The design work, overall draft and the result analysis is written by Neeraj Nayan Prakash, the comparison and performance analysis written by Vishal Narula, the concluding remarks are added by Amit Saini.

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Declarations

Competing interests

The authors declare no competing interests.

Ethics statements

This is software design and simulation work carried out on 3D TCAD. So, it does not harm environment or human being.

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