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A Thermally Stable, Low-Noise, Dual-Channel, Chopper-Stabilized Current-Feedback Instrumentation Amplifier for MEMS Flow-Meter Sensors

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Abstract

A low-noise, low-power, chopper-stabilized current-feedback instrumentation amplifier (CFIA) for MEMS flow-meter readout circuits is presented. The key factors for instrumentation amplifiers—flicker noise and offset—are mitigated using a chopper-stabilized technique. A ripple reduction loop suppresses ripples, while a fill-in technique avoids glitches and intermodulation distortion. Subthreshold operation of transistors enables low power consumption. The CFIA uses folded cascode stages and a Monticelli class AB output for high current drive and 1 V swing. Designed in 0.18 μm CMOS, the amplifier achieves an open-loop gain of 122.3 dB at 10 mHz with closed-loop gains of 100, 200, 400, and 800. It consumes 97 μA and has an input-referred noise of 29.3 nV/ $\sqrt{\text{Hz}}$. The power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) are 102.2 dB and 154.46 dB, respectively. The closed-loop gain remains constant at 46.1 dB from 0 $^{\circ}\text{C}$ to 100 $^{\circ}\text{C}$, over the entire frequency range, demonstrating excellent thermal stability and frequency compensation. Monte Carlo analysis confirms an input-referred offset of $-26.097 \mu\text{V}$ with a standard deviation of 25.107 μV , ensuring robust performance under process variations.

Keywords: CFIA; chopper-stabilized; fill-in technique; ripple reduction loop; Monticelli class AB; thermal stability

1. Introduction

MEMS flow sensors are utilized across a wide range of applications, including medical devices, natural gas flow meters, industrial flow control systems, portable anemometers, smart home sensors, and more. MEMS thermal flow sensors were first introduced in 1974 by Van Putten and Middelhoek [1]. Since then, numerous other MEMS thermal flow sensors have been developed [2, 3]. The thermal MEMS flow sensors can be classified into three major types based on the performance mechanism. The first type is the hot-wire sensor [4], in which a heater at constant temperature or constant current experiences flow, and the heater's cooling rate represents the flow rate. The second type is called the calorimetric sensor [2], in which two thermal sensors are placed around the heater, and the temperature difference between the sensors indicates the flow rate. The third type of thermal flow MEMS sensor is the time of flight sensor, where one sensor and one heater are used to measure the transient time of a thermal pulse. These different kinds of flow sensors have various performances. For instance, a calorimetric flow sensor exhibits good sensitivity at low flow rates, while it suffers from limited dynamic range caused by saturation at the higher flow rates [2]. On the other hand, hot-wire flow sensors show lower sensitivity and a larger flow range. This article presents the design of an instrumentation amplifier, a key component of the readout circuit, for a calorimetric thermal flow sensor. The sensor employs the constant temperature difference (CTD) method to regulate the heater's temperature, ensuring high sensitivity in the flow sensor's performance [5]. As mentioned, instrumentation amplifiers play a crucial role in today's sensors that are used in many applications such as medical sensors, automobiles, home sensors, and so on, all of them used in the Internet of Things (IOT) [6]. Most micro-electro-mechanical systems (MEMS) sensors, such as flow meters, use a resistive sensor, for instance, as a thermometer for the calorimetric sensors, where two or more thermal sensors are placed around a heater to measure the temperature asymmetry caused by the passing gas fluid [7]. Resistive bridges, such as wheatstone bridge, are used to convert resistor changes to signals [8]. To amplify the output signal of a resistive bridge, the instrumentation amplifier needs design requirements such as high common mode rejection ratio (CMRR), High Input

Impedance, power efficiency, and rail-to-rail sensing capability [4]. In the CMOS technology, the conventional instrumentation amplifiers suffer from some issues, including a large input offset in the range of several mV, offset drift of several $\mu\text{V}/^\circ\text{C}$, and flicker noise at low frequencies near the DC amount [2]. Several dynamic offset cancellation methods are introduced, including auto-zero (AZ) and chopping and offset stabilization, and their combination techniques to mitigate low-frequency errors [9]. Among all the mentioned methods, the chopping method is the best candidate for achieving low flicker noise corner of about several Hz, low input offset of about μV , and low offset drift of around a few $\text{nV}/\sqrt{\text{Hz}}$. Previous chopper-stabilized current-feedback instrumentation amplifiers (CFIAs) suffer from several limitations that hinder their application in MEMS flow-meter readout circuits. First, they typically rely on a low-pass filter to remove the up-converted ripple, which inherently restricts the amplifier's bandwidth. Second, charge injection and mismatches in the ripple reduction loop often leave residual offset and glitches, degrading DC accuracy. Third, the gain is determined by the ratio of two transconductors, leading to gain inaccuracy without calibration. Fourth, many existing designs consume excessive power ($>100 \mu\text{A}$) and operate at higher supply voltages ($\geq 3.3 \text{ V}$). Moreover, the thermal stability of these amplifiers is rarely characterized, yet MEMS flow sensors are often deployed in environments with wide temperature variations. To address these shortcomings, this paper presents a dual-channel chopper-stabilized CFIA that integrates a fill-in glitch cancellation technique, an active ripple reduction loop (RRL), and explicit thermal stability characterization over $0\text{--}100^\circ\text{C}$, all in a $0.18 \mu\text{m}$ CMOS process with a 1.8 V supply. To the best of our knowledge, this is the first CFIA to combine these features simultaneously.

2. Conventional Instrumentation Amplifier as Part of the Readout Circuit for a Thermal Flow Sensor

The chopper amplifier is a type of instrumentation amplifier that employs the chopping method to achieve low flicker noise and minimal input offset. A simplified representation of the chopper amplifier is illustrated in Figure 1. The chopper amplifier operates by utilizing two choppers positioned at the input and output of the amplifier, G_{m1} . The output stage, G_{m2} , is not subjected to chopping, as its input-referred offset and noise are attenuated by the gain of the first stage.

The chopper frequency is set to 50 kHz . This value is chosen as a trade-off between several factors. First, it is sufficiently higher than the estimated $1/f$ noise corner of the input PMOS transistors and also above the corner of the NMOS devices in the signal path, ensuring that offset and flicker noise from both transistor types are up-converted well above the signal band of interest (which for MEMS flow-meter readout is below 100 Hz) and effectively suppressed. Second, it is significantly lower than the unity gain bandwidth (757 kHz) to avoid excessive ripple due to finite settling and to maintain sufficient loop gain for ripple reduction. Third, a moderate frequency of 50 kHz limits dynamic power dissipation in the chopper switches and the fill-in logic, contributing to the low $97 \mu\text{A}$ total current. Higher chopper frequencies (e.g., 100 kHz) were simulated and resulted in reduced ripple but increased glitch energy and power, without meaningful improvement in noise performance. Lower frequencies (e.g., 10 kHz) caused visible residual $1/f$ noise. Additionally, the chopping period ($20 \mu\text{s}$) is more than adequate for the internal nodes of the amplifier to settle completely after each clock transition, ensuring stable operation. Thus, 50 kHz is selected as the optimal point.

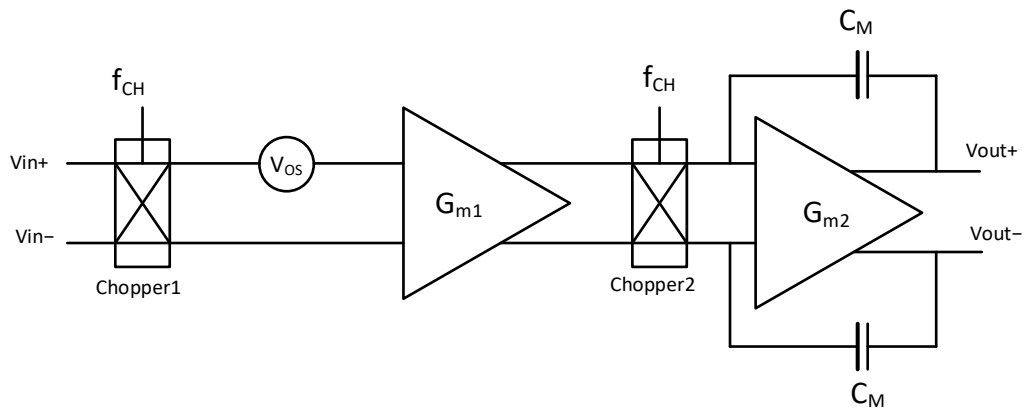


Figure 1. Simplified diagram of the chopper amplifier.

In contrast to the auto-zero (AZ) technique, the chopping method effectively addresses noise folding and aliasing challenges. Nevertheless, it introduces two primary drawbacks: ripple and glitch. Ripple occurs due to the chopper amplifier's input offset, with the upmodulated offset defined as in Equation (1).

$$V_{out,ripple} = \frac{V_{os} \times G_m}{2C_M \times f_{CH}} \quad (1)$$

where V_{os} is the input offset, G_m is the transconductance of the amplifier, C_M is the Miller capacitance of the designed amplifier, and f_{CH} is the chopping frequency.

The ripple generation process resulting from the input offset is depicted in Figure 2a. Initially, the input offset of the transconductance amplifier (V_{os}) is transformed into a current, I_{chop} (represented by the red signal), which is equal to $G_m V_{os}$. This transformation occurs by modulating I_{chop} at the chopper frequency, f_{chop} . The resulting ripples, caused by the input offset, appear in I_{out} (represented by the dark red signal) and are equal to $2G_m V_{os}$. To eliminate ripple, we can use a low-pass filter (LPF), but in that case, the amplifier's bandwidth is restricted to the chopper frequency. We need to use an optimized ripple reduction technique that is mentioned in this paper. The glitch problem in the chopper amplifier is shown in Figure 2b. As a consequence of the limited bandwidth of the amplifier, the delay is caused at the output of the G_m , I_{chop} (red signal); therefore, at the edge of the chopper clocks, the glitch is created by the demodulation chopper I_{out} (dark red signal). These glitches produce distortions at the frequency of twice the frequency of the chopping frequency ($2f_{chop}$). The glitches produce intermodulation distortion (IMD) during the down-conversion and up-conversion operation of the chopper. To reduce glitches, the fill-in technique is the best candidate that has recently been reported [10]. For the fill-in technique, a dual-channel current-feedback instrumentation chopper amplifier is used, with a ripple reduction loop for each channel. The important advantage of the dual channel is the reduction in the low level of noise as a result of the correlation efficiency of the channels [11]. Moreover, the chopper amplifier does not have a noise folding problem for the reason of the lack of sampling operation that is used in the AZ method. Therefore, the dual-channel chopping method achieves a low noise level [12].

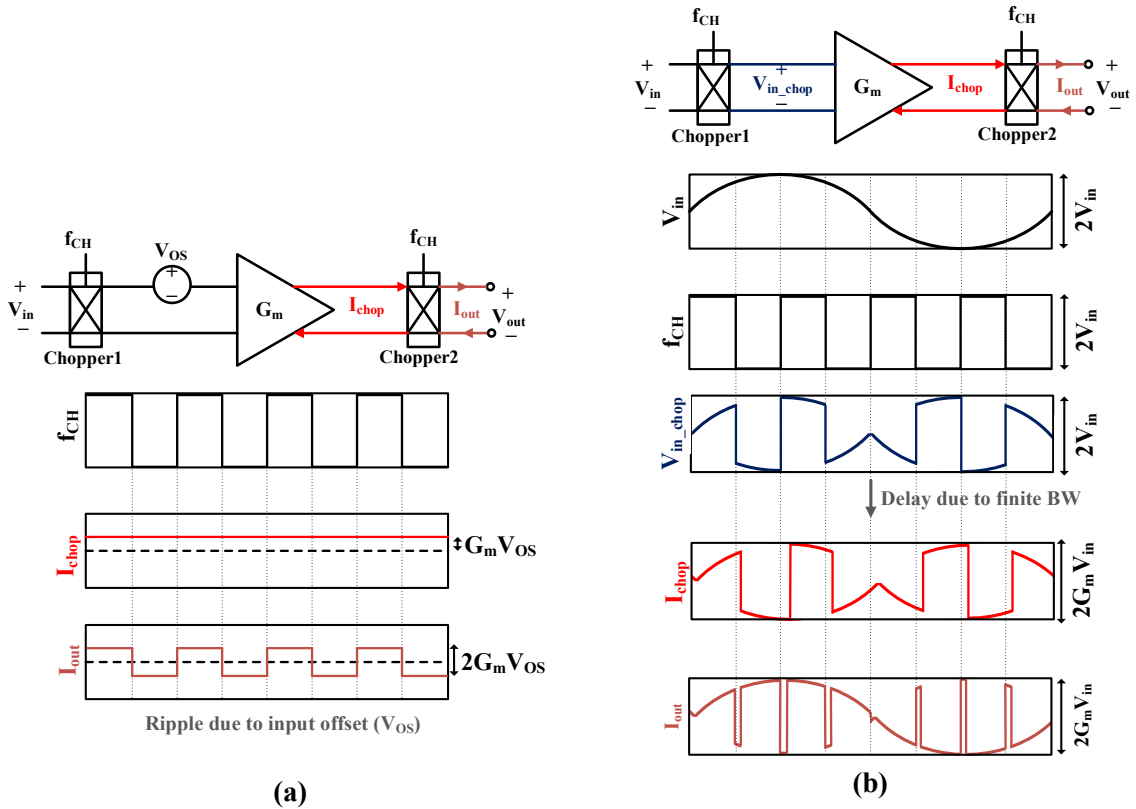


Figure 2. Two problems of the chopper amplifier: (a) ripple and (b) glitch.

In the dual-channel structure that is shown in Figure 3, the noise sources of each channel are summed by an adder, and the equivalent noise at the adder is equal to Equation (2).

$$V_{neq(rms)}^2 = (V_{n1(rms)}^2 + V_{n2(rms)}^2 - 2\alpha V_{n1(rms)} \cdot V_{n2(rms)}) \cdot A^2 \quad (2)$$

where A is the voltage gain of channel amplifiers, α correlation factor between the two channel paths. For $\alpha > 0.5$, the total noise of the dual channel $V_{neq(rms)}^2$ can be lower than the noise sources of each channel $V_{n1(rms)}^2$ and $V_{n2(rms)}^2$.

For achieving low-noise CFIA and low IMD, we utilize a dual-channel chopping CFIA with a fill-in technique for reducing glitches originating from the delayed output signal of the operational transconductance amplifier at the edge of the chopper clocks. [13]. The input-referred noise is lowered by using a nonzero correlation factor between two channels of the CFIAs. An innovative ripple reduction loop is exploited for reaching acceptable low ripples without using a low-pass filter and restricting bandwidth.

To reduce flicker noise, one of the key parameters to consider is the length of the designed transistors. Flicker noise can be expressed using Equation (3).

$$V_{nf}^2 = \frac{k_f}{W \cdot L \cdot Cox \cdot f} \quad (3)$$

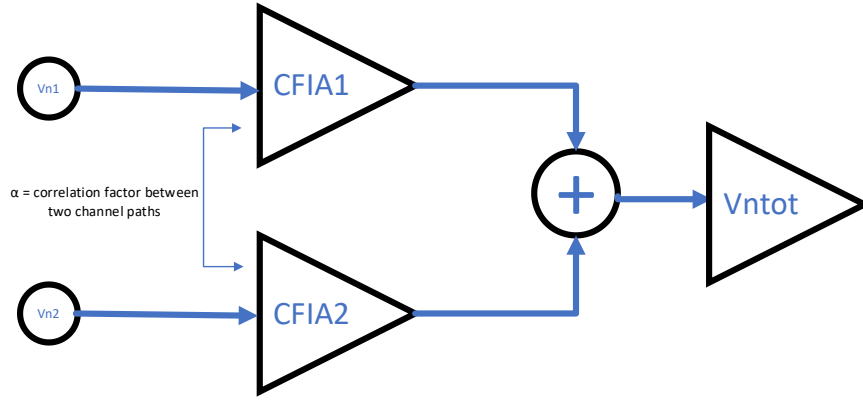


Figure 3. Dual-channel structure noise sources summation.

Here, K_f represents the flicker noise coefficient factor. By incorporating the width-to-length ratio (W/L) of the transistors, Equation (3) can be reformulated as Equation (4).

$$V_{nf}^2 = \frac{k_f}{\left(\frac{W}{L}\right) \cdot L^2 \cdot Cox \cdot f} \propto \frac{1}{L^2} \quad (4)$$

As observed in Equation (4), increasing the length of the transistors results in a reduction in flicker noise. By equating the flicker noise with the thermal noise of the transistor, the flicker corner can be determined, as shown in Equation (5).

$$V_{nf}^2 = V_{nThermal}^2 \rightarrow \frac{k_f}{W \cdot L \cdot Cox \cdot f} = \frac{4KT\gamma}{g_m} \rightarrow f_{co} = \frac{k_f \cdot g_m}{W \cdot L \cdot Cox \cdot 4K \cdot T \cdot \gamma} \quad (5)$$

As observed, increasing the channel length of transistors leads to a reduction in the flicker corner. However, a high level of transconductance can result in a significantly higher flicker corner.

Section 3 describes the proposed low-noise dual-channel chopper-stabilized current-feedback instrumentation amplifier with the fill-in technique and circuit implementation of each part of the proposed structure. Section 4 shows the simulation results. Section 5 provides a discussion that interprets the results, compares them with previous work, discusses implications, and outlines future research. Section 6 concludes the paper.

3. Proposed Low-Noise Dual-Channel Chopper-Stabilized CFIA

In this section, the proposed low-noise dual-channel chopper-stabilized current-feedback instrumentation amplifier using the fill-in technique for reducing glitches and a ripple reduction loop circuit is described. The top-level block diagram of the proposed structure is described in Section 3.1, and the circuit implementation of this structure is explained in Section 3.2.

3.1. Top Level Description of the Proposed Structure

The top-level block diagram of the overall proposed low-noise dual-channel chopper-stabilized current-feedback instrumentation amplifier is shown in Figure 4.

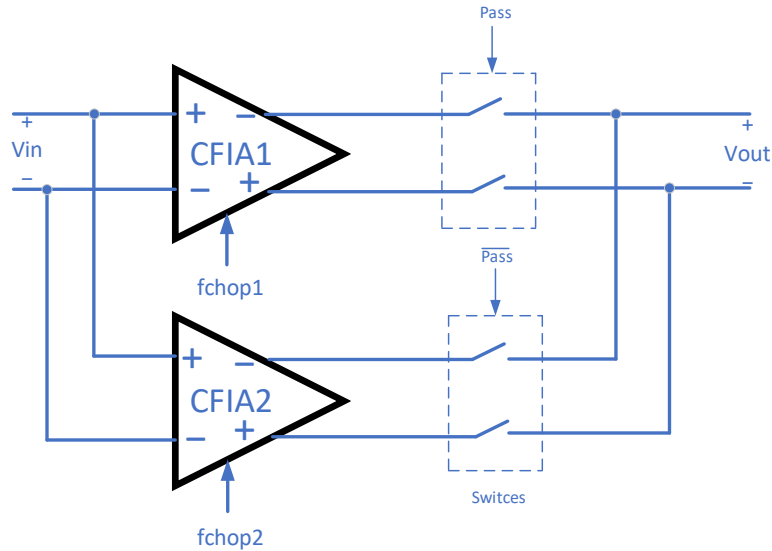


Figure 4. The top-level block diagram of the overall proposed low-noise dual-channel chopper-stabilized CFIA.

The simulated output signals of the channels are shown in Figure 5. The two channels have their own clocks with a 180-degree phase difference. The glitch is generated at the edge of the chopper clocks, distorting the signal. Using the fill-in technique—enabling each channel to send its signal to the output at the appropriate time—eliminates the glitches and reduces the distortion. As shown in Figure 5, the final output is pure and has no glitch.

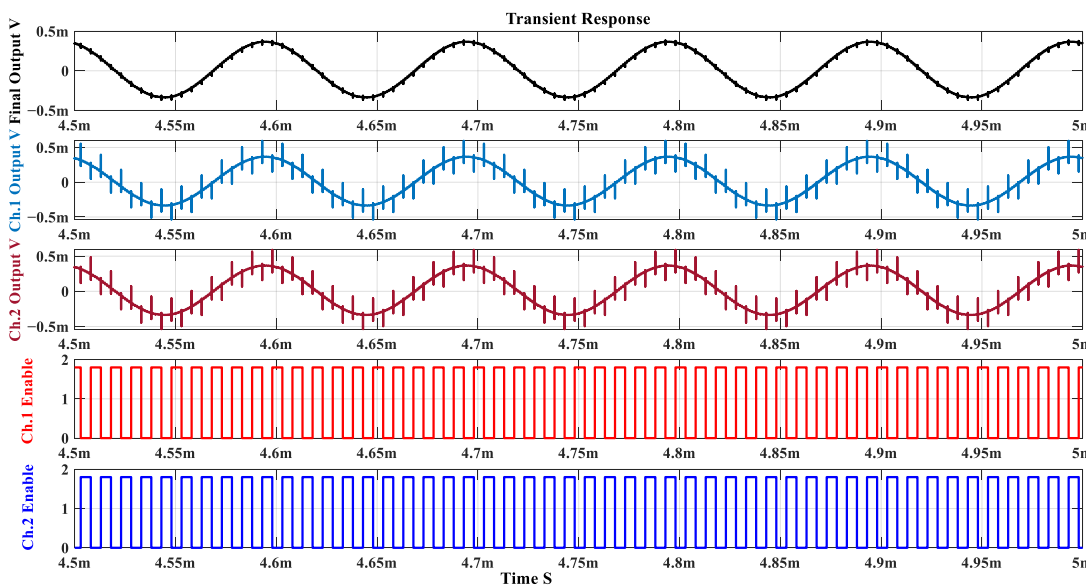


Figure 5. Simulated waveforms of channel 1 output (Ch. 1 Output), channel 2 output (Ch. 2 Output), the final fill-in output (final output), and the enable clocks (Ch. 1 Enable and Ch. 2 Enable). The fill-in output is free of glitches, demonstrating the effectiveness of the fill-in technique.

As mentioned in the introduction part, one of the important challenges in the chopping amplifiers is the ripples created by the input offset of the amplifiers. A ripple reduction loop is a standard method for chopper amplifiers that does not reduce the bandwidth. As shown in Figure 6, a ripple reduction loop is added for each chopping CFIA channel to reduce the ripples.

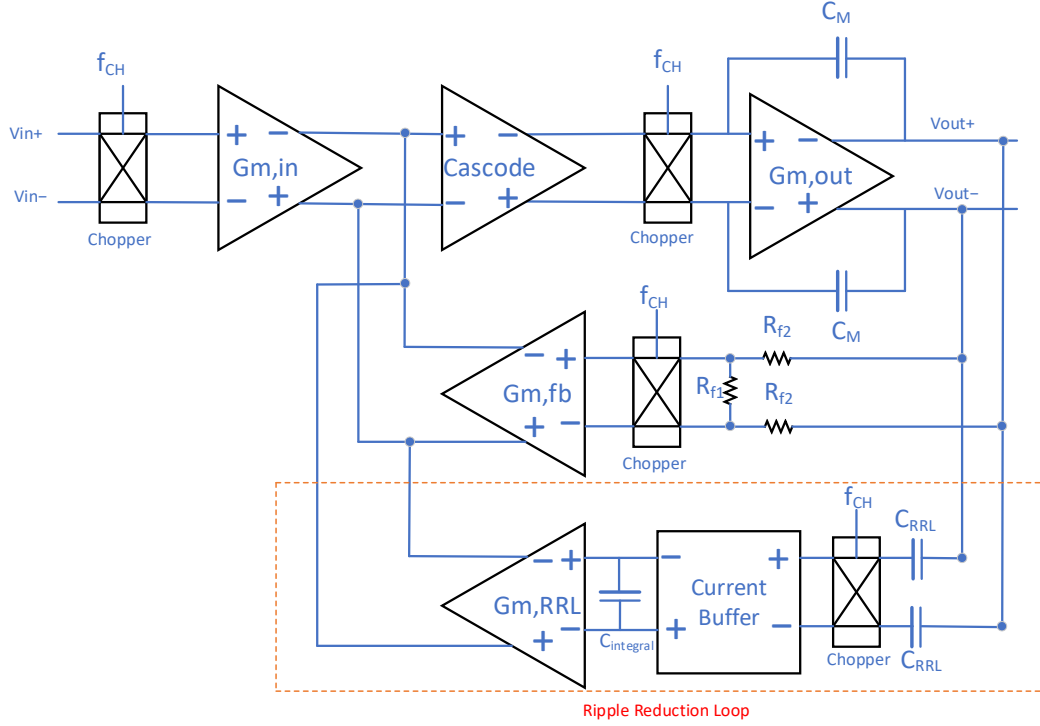


Figure 6. A ripple reduction loop is added to the channel 1 chopping CFIA.

The operation of the shown ripple reduction loop is that the second chopper at the output of the $G_{m,in}$ modulates the input offset at the chopping frequency, and then the integrator converts the current type ripple to a voltage at the output of the $G_{m,fb}$. The ripple reduction loop capacitor (C_{RRL}) detects the integrated ripple and converts it to the current, which the third chopper demodulates. After passing the current buffer (CB), $C_{integral}$ converts the current offset to the voltage offset and then the transconductance, $G_{m,RRL}$, adds the current type offset to the output of the $G_{m,in}$ in the opposite direction to cancel the input offset.

3.2. Circuit Implementation of the Proposed Structure

The transistor level of the CFIA is shown in Figure 7. This structure consists of an input stage, current-feedback, and ripple reduction loop PMOS pairs, a folded cascode, and an output power class AB Monticelli stage. A common mode feedback circuit part is used at the differential output of the folded cascode stage for tuning the DC voltage to a suitable level. The achievable open-loop gain of more than 120 dB can increase the closed-loop gain accuracy. Miller capacitors between the input and output of the last stage can compensate for the required phase margin to guarantee stability.

The transistor level of the proposed current buffer (CB), which is used at the ripple reduction loop part with its voltage buffer and CMFB part, is shown in Figure 8.

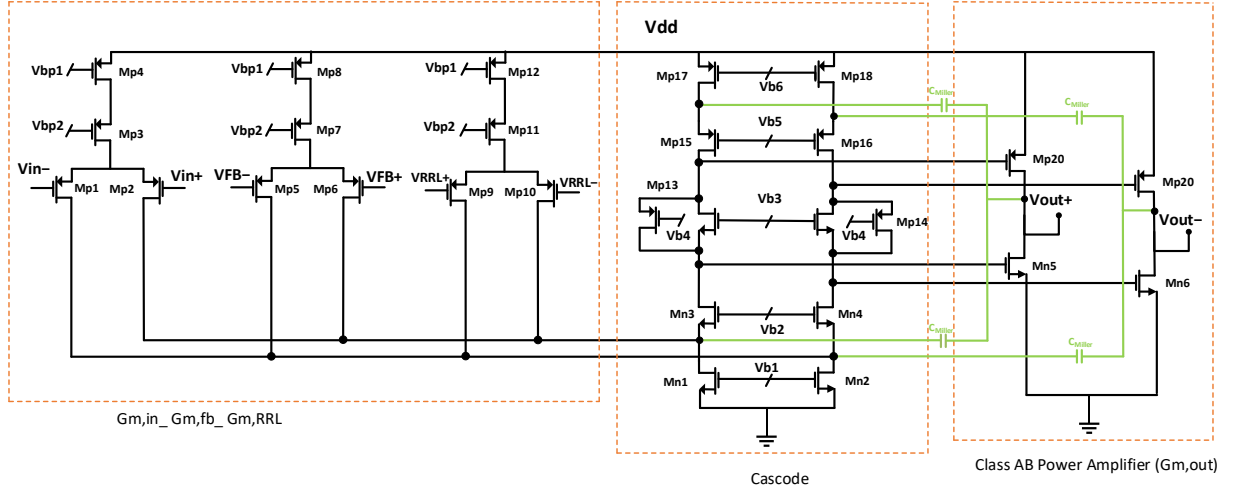


Figure 7. Transistor level of CFIA.

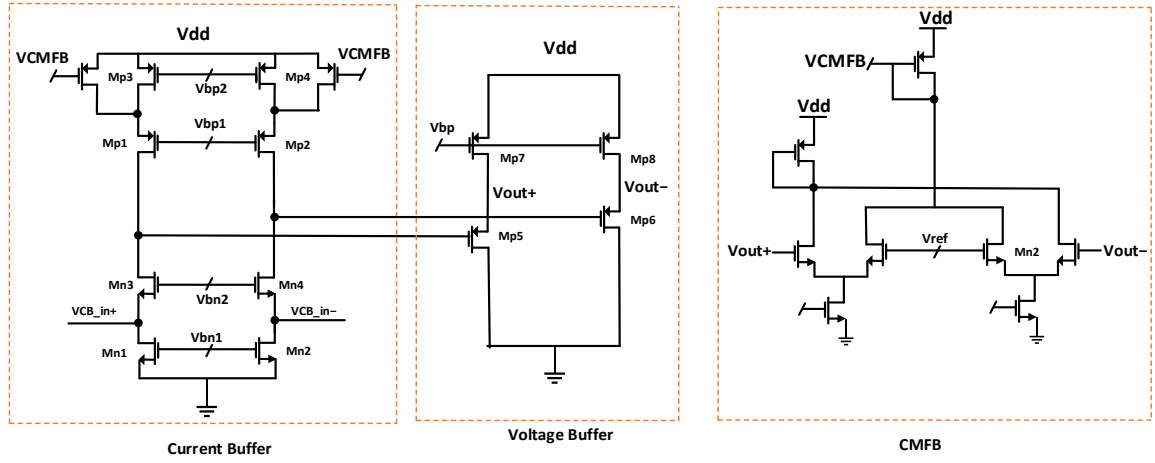


Figure 8. The transistor level of the proposed current buffer is used at the RRL.

4. Results

4.1. Main Performance Results

Figure 9 shows the transient response of a simulated low-noise dual-channel chopper-stabilized CFIA with a closed-loop gain of 200 and an input sine wave of 100 Hz frequency. This figure consists of the final dual-channel output, channel 1 output, and channel 2 output. As shown, the glitches in the final output signal are smaller than those in either of the two individual channels. Therefore, the glitch reduction effect of the dual-channel structure and the fill-in technique is evident. Chopper clocks are simulated with 1 ns rise/fall time and 0.5 ns skew, consistent with typical clock buffers in 0.18 μm CMOS.

The total harmonic distortion (THD) of the proposed CFIA is simulated with a 100 Hz, 1 Vpp differential input at a closed-loop gain of 200, yielding a THD of -62 dB.

The frequency response of the closed-loop low-noise dual-channel CFIA is shown in Figure 10. As shown, a gain of 46.1 dB at 1 Hz and unity gain bandwidth of 757 kHz is obtained.

As shown in Figure 11, the open-loop gain is obtained at 122.3 dB at 10 mHz. The open-loop unity gain bandwidth is 757 kHz; therefore, as shown, the phase margin is 63° at UGBW.

As shown in Figure 12, the common mode rejection ratio amount, which is the ratio of differential mode gain to common mode gain, is obtained at 154.46 dB at 10 Hz, which is the best result for resistive bridges that are used in flow-meter sensors.

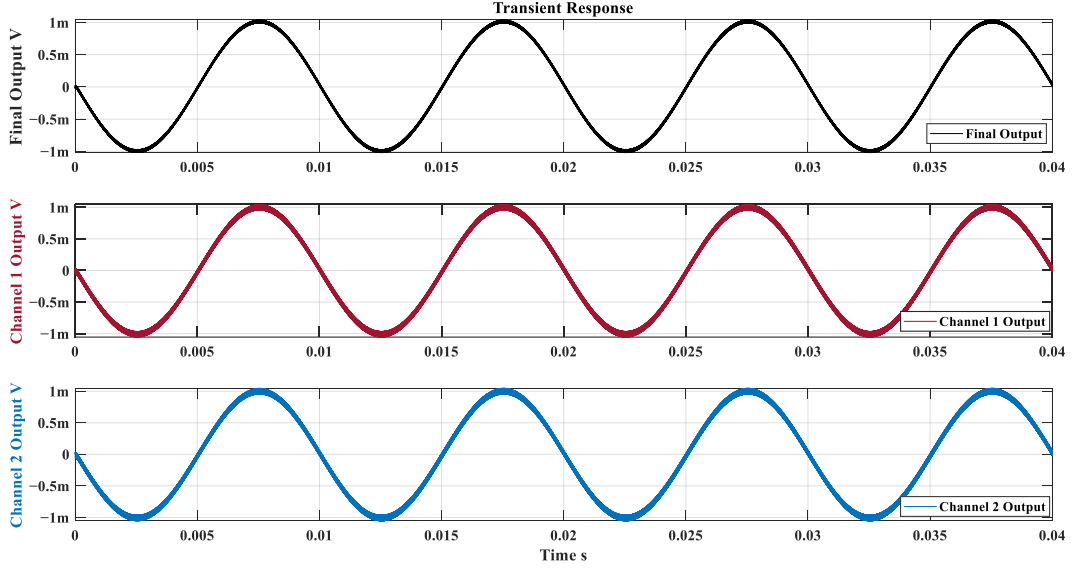


Figure 9. Transient response of the proposed low-noise dual-channel chopper-stabilized CFIA.

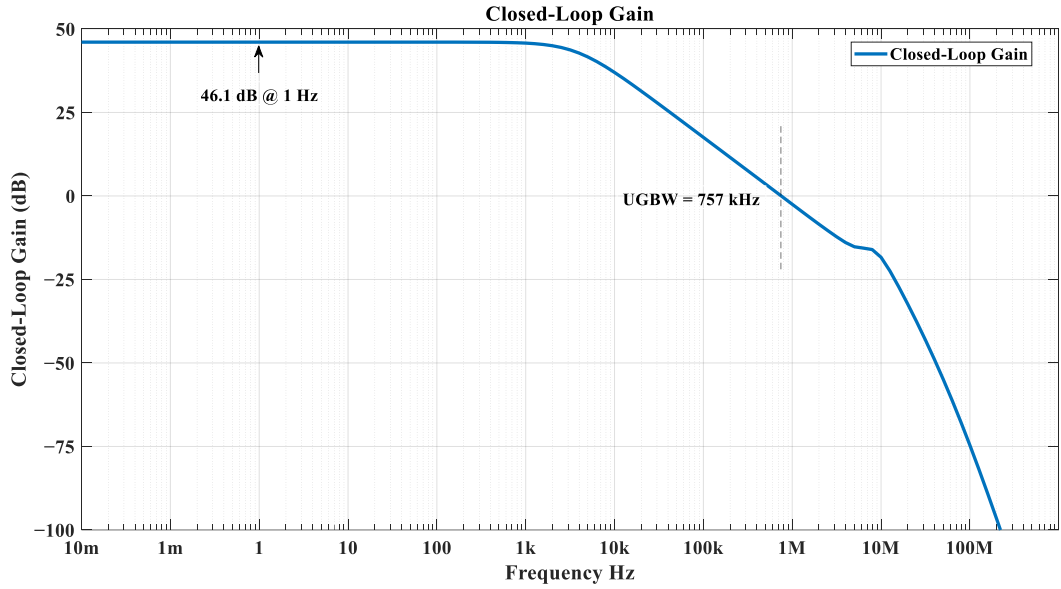


Figure 10. Frequency response of the proposed low-noise dual-channel chopper-stabilized CFIA.

The simulation results of the designed low-noise dual-channel chopper-stabilized CFIA for power supply rejection ratio are shown in Figure 13, where the PSRR is 102.2 dB at 10 Hz.

As shown in Figure 14, the thermal noise floor of dual-channel CFIA is 29.3 nV/ $\sqrt{\text{Hz}}$. This value is first observed in the standard AC noise analysis (without chopping) at sufficiently high frequencies (1 kHz) where the 1/f noise becomes negligible and the spectrum flattens. When chopper stabilization is applied (50 kHz clocks, fill-in technique), the same thermal floor extends down to 1 Hz because the 1/f noise is up-converted and suppressed. This is confirmed through separate transient noise simulations, which yield an input-referred noise density of 29.3 nV/ $\sqrt{\text{Hz}}$ at 1 Hz, identical to the high-frequency value from the AC analysis. This value is well within the acceptable range for a low-frequency sensor readout.

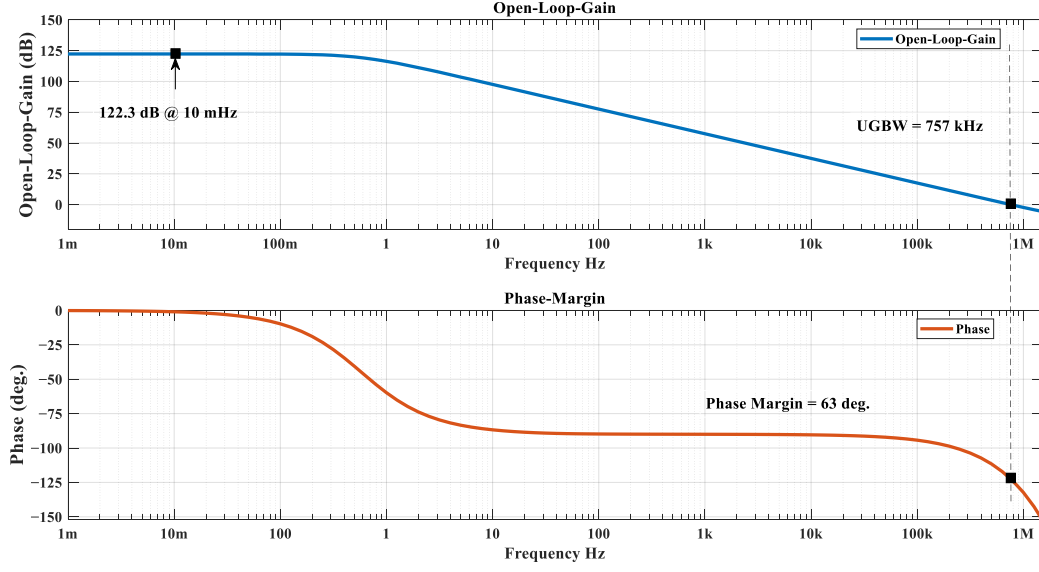


Figure 11. Gain of open-loop CFIA and phase margin at UGBW.

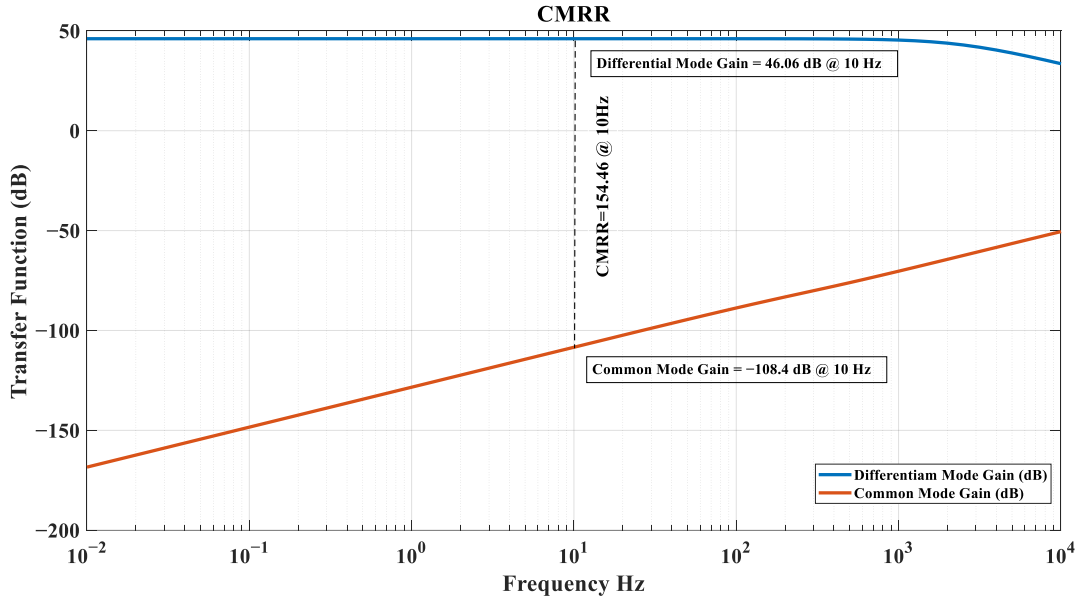


Figure 12. Simulation results of the differential mode gain, common mode gain, and CMRR transfer function.

The total current consumption of the dual-channel CFIA is 97 μ A from a 1.8 V supply. Table 1 provides a detailed breakdown of this current among the key building blocks.

Table 1. Current consumption breakdown of the proposed dual-channel CFIA.

Block	Current (μ A)	Percentage
Folded cascode input stages (2 $\times$)	40	41.2%
Ripple reduction loops (2 $\times$)	24	24.7%
Monticelli class AB output stage	18	18.6%
Biasing and fill-in logic	15	15.5%
Total	97	100%

The noise efficiency factor can be evaluated through Equation (6)

$$NEF = V_{rms,ni} \times \sqrt{\frac{2 \times I_{tot}}{\pi \times U_T \times 4kT \times BW}} \quad (6)$$

where $V_{rms,ni}$ is the RMS value of input-referred noise, I_{tot} is the total current consumption, equal to 97 μ A, U_T is the thermal voltage, and BW is the bandwidth of the amplifier. The calculated NEF is 10.4.

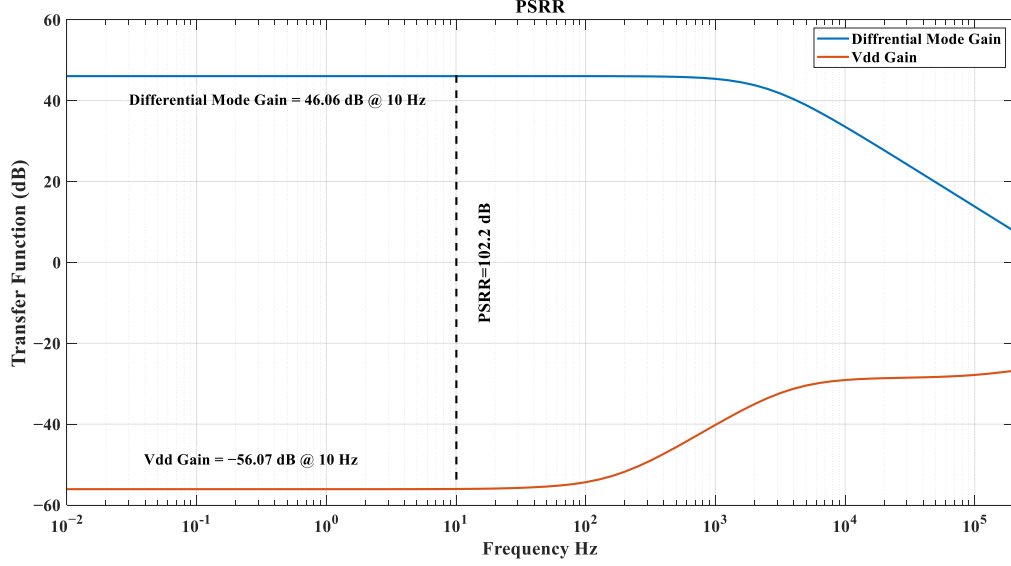


Figure 13. Simulation results of the differential mode, power supply, and PSRR transfer function.

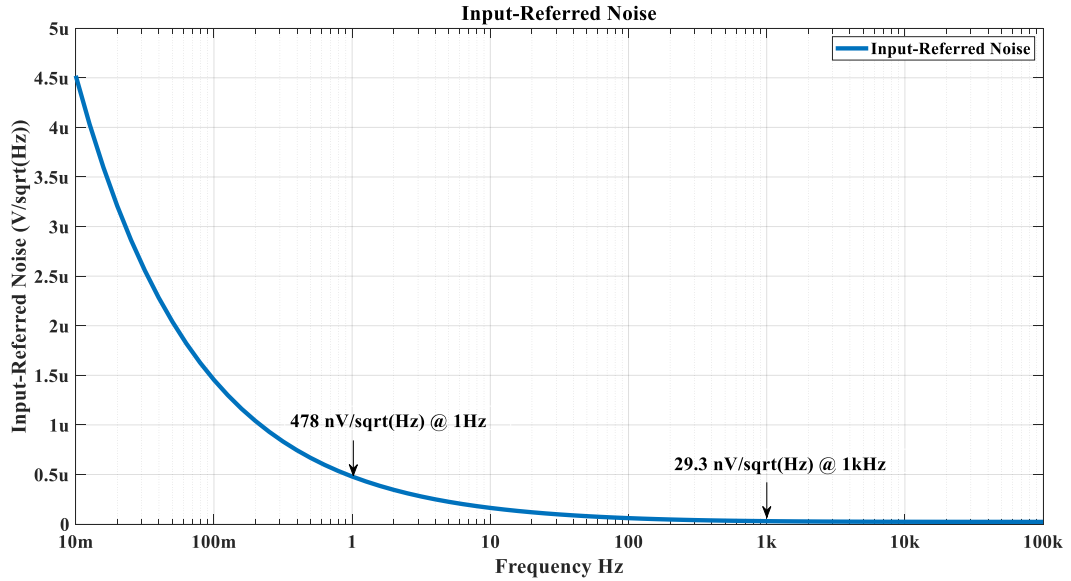


Figure 14. Simulated input-referred noise of dual-channel CFIA. With chopping active, transient noise simulation yields a flat thermal noise floor of 29.3 nV/ $\sqrt{\text{Hz}}$.

The frequency response of the closed-loop amplifier is simulated at five different temperatures: 0 $^{\circ}\text{C}$, 25 $^{\circ}\text{C}$, 50 $^{\circ}\text{C}$, 75 $^{\circ}\text{C}$, and 100 $^{\circ}\text{C}$. As shown in Figure 15, the closed-loop gain remains constant at 46.1 dB across the entire frequency range for all examined temperatures. No gain variation or peaking is observed, indicating excellent frequency compensation and phase margin. Moreover, the gain shows no dependence on temperature, confirming the thermal stability of the feedback network and the overall amplifier design. This flat, temperature-independent response is crucial for accurate MEMS flow-meter readout under slow sensor signals and varying ambient temperature.

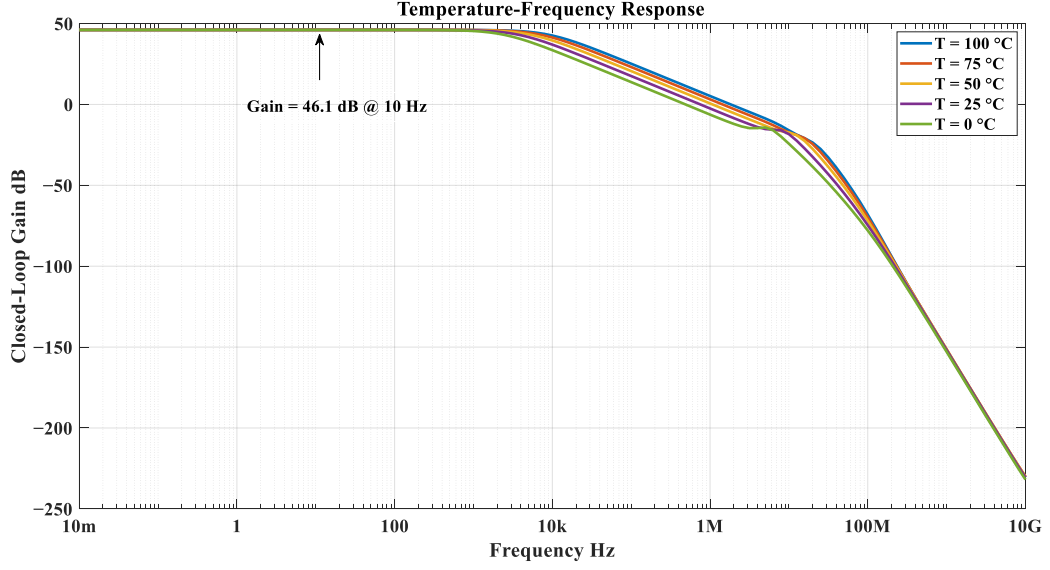


Figure 15. Closed-loop gain of the proposed CFIA versus frequency for temperatures ranging from 0 °C to 100 °C. All curves are virtually identical, confirming temperature-independent operation.

To evaluate the statistical variation in the input-referred offset caused by process mismatches, a Monte Carlo simulation is performed with 500 runs. The chopper clocks and fill-in clocks are active during the transient simulation. Figure 16 shows the resulting histogram of the input-referred offset. The distribution is approximately Gaussian, with a mean of $-26.097 \mu\text{V}$ and a standard deviation of $25.107 \mu\text{V}$. The $3\text{-}\sigma$ offset ($\pm 75.3 \mu\text{V}$) is well below the 0.5 mV requirement for at least a 10-bit output ADC. These results confirm that the proposed dual-channel chopper stabilization, together with the fill-in and ripple reduction techniques, which effectively suppresses offset variations and ensures robust performance under typical manufacturing fluctuations.

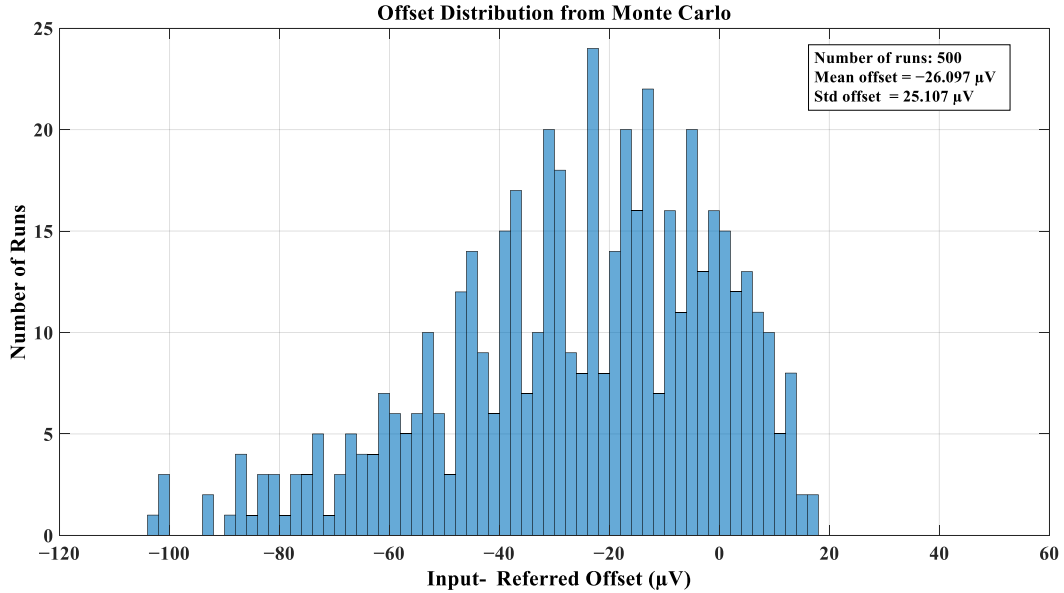


Figure 16. Histogram of the input-referred offset from 500 Monte Carlo runs.

To assess the robustness of the proposed CFIA against fabrication process, supply voltage, and temperature variations (PVT), a corner analysis is performed. The simulation covered three process corners (TT, FF, SS), three temperatures (0 °C, 27 °C, 100 °C), and two supply voltages (1.71 V and 1.89 V, representing $\pm 5\%$ deviation from the nominal 1.8 V). The closed-loop gain and input-referred offset are extracted for each corner. Table 2 summarizes the results. The closed-loop gain remains between 45.7 dB and 46.1 dB—a variation of less than -0.5 dB from the nominal 46.1 dB. The

input-referred offset stays below 31 μV across all corners, and the worst-case offset is observed at the slow corner (SS) with low temperature and low supply. These results confirm that the amplifier maintains its specified performance under extreme operating conditions, making it suitable for industrial MEMS flow-meter readout circuits where temperature and supply voltage can vary significantly.

Table 2. PVT corner simulation results (closed-loop gain and input-referred offset).

Process	Temperature ($^{\circ}\text{C}$)	VDD (V)	Closed-Loop Gain (dB)	Input-Referred Offset (μV)
TT	27	1.80	46.1	-16.91
TT	100	1.80	46.1	-7.41
TT	0	1.80	46.1	-26.72
FF	27	1.80	46.1	-5.44
FF	100	1.71	46.1	-11.09
FF	100	1.89	46.1	-3.04
FF	0	1.71	45.9	-30.53
FF	0	1.89	46.1	-6.02
SS	27	1.80	46.1	-28.2
SS	100	1.71	46.1	-26.37
SS	100	1.89	46	-29.03
SS	0	1.71	45.7	-30.95
SS	0	1.89	46.1	-29.8

The results confirm that the proposed CFIA is robust against PVT variations, with negligible degradation in gain and offset. The worst-case gain variation (-0.5 dB) and offset (≤ 31 μV) are well within the requirements of the target MEMS flow-meter readout application.

4.2. Post-Layout Validation

To assess the impact of layout parasitics on the amplifier's stability and performance, post-layout simulations are performed. The physical layout is extracted using standard RC extraction tools, and the resulting netlist (including parasitic capacitances and resistances) is back-annotated into the schematic for transient and AC analyses.

The pre-layout and post-layout results are compared in Table 3. The phase margin decreased from 63° to 59° —a reduction of only 4° —and remained well above the typical stability requirement of 45° . The unity gain bandwidth dropped by 1.2% (from 757 kHz to 748 kHz), and the DC gain decreased by 2.7 dB (from 122.3 dB to 119.6 dB). The input-referred offset increased by less than 1 μV .

These results confirm that the parasitic effects introduced by the layout do not compromise the amplifier's stability or performance. The design is robust and ready for fabrication.

Table 3. Pre-layout vs. post-layout simulation results (TT, 27 $^{\circ}\text{C}$).

Parameter	Pre-Layout	Post-Layout	Change
Phase margin ($^{\circ}$)	63	59	-4
Unity gain bandwidth (kHz)	757	748	-1.2%
DC gain (dB)	122.3	119.6	-2.7
Input-referred offset (μV)	-16.91	-17.54	-0.63

5. Discussion

The proposed dual-channel chopper-stabilized CFIA achieves a competitive balance of low offset, moderate noise, high CMRR/PSRR, and excellent thermal stability, making it a promising candidate for MEMS flow-meter readout circuits. In this section, we interpret the main results, compare them with previous studies, discuss the broader implications, practical sensor interface analysis and outline open challenges and future work.

5.1. Interpretation of Key Results

The Monte Carlo simulation (500 runs) yields an input-referred offset of $-26.097 \pm 25.107 \mu\text{V}$ (mean $\pm \sigma$). The $3\text{-}\sigma$ offset ($\pm 75.3 \mu\text{V}$) is two orders of magnitude lower than the 0.5 mV requirement for a 10-bit ADC, confirming that the dual-channel chopping, fill-in glitch suppression, and active ripple reduction loop (RRL) effectively cancel systematic and random mismatches. Unlike conventional chopper amplifiers that rely on a low-pass filter to remove ripple (which inherently limits bandwidth), the proposed RRL eliminates ripple without bandwidth reduction, preserving the amplifier's speed (unity gain bandwidth of 757 kHz).

The CMRR of 154.46 dB and PSRR of 102.2 dB are excellent for a low-voltage (1.8 V) CMOS design. Such high CMRR is particularly beneficial for resistive bridge sensors, where large common mode voltages can otherwise corrupt the differential signal. The input-referred noise of $29.3 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz is dominated by thermal noise, and the chopper effectively removes $1/f$ noise; consequently, the actual low-frequency noise (down to 1 Hz) is expected to be close to this thermal floor, as discussed in Section 4. Furthermore, the closed-loop gain remains constant at 46.1 dB from 0°C to 100°C over the whole frequency range—a rarely demonstrated feature that ensures reliable operation in thermally variable industrial environments without external temperature compensation.

5.2. Comparison with Previous Studies

Table 4 places this work in the context of several state-of-the-art instrumentation amplifiers [8,14–16]. While designs such as [15] achieve lower input-referred noise ($10 \text{ nV}/\sqrt{\text{Hz}}$) and [15] a lower NEF (4.3), they operate at higher supply voltages ($\geq 3.3 \text{ V}$) and often lack explicit thermal stability characterization. The proposed CFIA offers a distinct combination of features: it is the only design among those compared that explicitly demonstrates temperature-independent closed-loop gain ($0\text{--}100^\circ\text{C}$) and uses a dual-channel fill-in technique to eliminate glitches. Moreover, the active ripple reduction loop avoids the bandwidth penalty of a low-pass filter, an advantage shared with [8] but not with [14,16]. In terms of DC precision, the simulated CMRR (154.46 dB) and PSRR (102.2 dB) are competitive, and the Monte Carlo offset analysis provides statistical confidence in the design's robustness against process variations—an aspect that many prior works do not report. Table 4 compares the key performance metrics of the proposed CFIA with those of previously reported chopper-stabilized instrumentation amplifiers. While some reference designs operate at higher supply voltages ($\geq 3.3 \text{ V}$) or under different measurement conditions, the table is intended to illustrate the overall state-of-the-art and to highlight the distinct advantages of this work, particularly its low voltage (1.8 V), explicit thermal stability, and glitch-free operation.

Table 4. Summary performance of the designed low-noise dual-channel chopper-stabilized CFIA and its comparison to similar instrumentation amplifiers.

	This Work ¹	[14] ²	[15]	[16]	[8]
Dynamic technique	Chopping + fill-in + RRL	Auto-zero + chopping + ping-pong	Multipath + chopping + RRL	Chopping + input resistance boosting	Multipath + chopping + floating HPF + fill-in
Process (μm)	0.18	0.5	0.18	0.32	0.18
Supply (V)	1.8	3~5	3.3	3.3	1.8
Current (μA)	97	1700	123	170	46.5
DC gain (dB)	122.3	1000	-	201.2	123
CMRR (dB)	154.46	142	100	120	90
PSRR (dB)	102.2	138	90	115	111
BW (kHz)	757	800	1920	40	874
Input-referred noise $\text{nV}/\sqrt{\text{Hz}}$	29.3	27	10	18	6.42
NEF	10.4	43	4.3	10.6	2.3

¹ This work is based on pre-layout simulations (post-layout results are also provided in Section 4.2); all other works include measured silicon data. ² Designs with a supply voltage $\geq 3.3 \text{ V}$ are included for context; direct comparison of power and noise should account for the different operating conditions.

The proposed CFIA achieves an NEF of 10.4, which is higher than some state-of-the-art designs (e.g., ref. [8] with NEF = 2.3). This is primarily due to three factors. First, the design prioritizes thermal stability (0–100 °C) and high CMRR (154.46 dB), which require larger bias currents and more robust biasing, increasing power consumption. Second, the dual-channel architecture with fill-in and dual ripple reduction loops adds overhead that is not present in single-channel, NEF-optimized designs. Third, the input stage uses a PMOS differential pair with moderate inversion to reduce 1/f noise and improve matching, rather than deep subthreshold which would lower transconductance efficiency (gm/ID). For the target MEMS flow-meter application, where sensor bandwidth is low (<100 Hz) and ambient temperature varies widely, the trade-off of higher NEF for excellent thermal stability and DC precision is justified.

5.3. Broader Implications for MEMS Sensor Readout

The results suggest that the proposed CFIA can serve as a reliable analog front-end not only for MEMS flow meters but also for other resistive bridge sensors (e.g., pressure, humidity, gas sensors) that demand high common mode rejection, low offset, and low power. The combination of chopper stabilization, fill-in glitch cancellation, and active ripple reduction represents a systematic approach to overcoming the inherent drawbacks of chopper amplifiers. The explicit demonstration of thermal stability and Monte Carlo offset distribution adds practical value for designers who need to guarantee performance across temperature and manufacturing spreads.

5.4. Practical Sensor Interface Analysis

The practical impact of the CFIA's input-referred noise can be quantified by calculating the minimum resolvable flow velocity (flow resolution). This calculation links the amplifier's electrical noise to the physical measurand of the MEMS flow sensor.

The total RMS noise voltage at the output of the CFIA is determined by the input-referred noise density and the system bandwidth. For a noise-limited system with bandwidth BW = 1 kHz (equal to the ADC sampling rate), the total RMS noise is:

$$V_{n,rms} = \text{Noise Density} \times \sqrt{BW} = 29.3 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{1000 \text{ Hz}} = 0.93 \text{ } \mu\text{V}_{rms} \quad (7)$$

The sensitivity of a typical calorimetric MEMS flow sensor depends on the heating power and the readout bridge configuration. From the literature, a representative sensitivity for such sensors is 100 mV/(m/s) [7]. The corresponding minimum detectable flow velocity is then:

$$\text{Flow Resolution} = \frac{V_{n,rms}}{S} = \frac{0.93 \text{ } \mu\text{V}}{100 \text{ mV}/(\text{m/s})} = 9.3 \text{ } \mu\text{m/s} \quad (8)$$

This value corresponds to approximately 9.3 $\mu\text{m/s}$, which is more than adequate for high-precision micro-flow measurement applications. The calculation demonstrates that the noise performance of the proposed CFIA does not limit the flow resolution; rather, the sensor itself is likely the dominant factor.

5.5. Limitations and Future Work

This study is based entirely on simulations; no fabricated chip has been tested, and experimental validation is essential to confirm the predicted CMRR, noise, offset, and thermal behavior. While post-layout simulations accounted for extracted RC parasitics, other factors such as package stress and measurement setup limitations can only be assessed through measurement. Furthermore, the power consumption (97 μA) could be further reduced by employing dynamic biasing techniques or by migrating to a more advanced CMOS node.

Future research directions include integrating the CFIA with an on-chip PWM-based ADC to form a complete sensor readout system-on-chip (SoC). Such an integrated solution would be attractive for ultra-low-power wireless sensing nodes. Additionally, exploring the use of calibration loops to further suppress residual offset and ripple could extend the applicability to 12-bit or higher resolution measurement systems.

6. Conclusions

This paper presented a low-noise, low-power, dual-channel chopper-stabilized CFIA for MEMS flow-meter readout circuits. The design combines a fill-in glitch cancellation technique and an active ripple reduction loop to overcome the two main drawbacks of chopper amplifiers without sacrificing bandwidth. Simulated in a standard 0.18 μm

CMOS process, the amplifier consumes 97 μA from a 1.8 V supply and achieves a unity gain bandwidth of 757 kHz, an input-referred noise of 29.3 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, a CMRR of 154.5 dB, and a PSRR of 102.2 dB. The closed-loop gain remains constant at 46.1 dB over a temperature range of 0–100 °C. Monte Carlo simulations confirm an input-referred offset of $-26.097 \pm 25.107 \mu\text{V}$, demonstrating robust offset cancelation. These features make the proposed CFIA highly suitable for accurate, thermally stable readout of MEMS flow meters and other resistive bridge sensors.

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References

1. Van Putten, A.; Middelhoek, S. Integrated silicon anemometer. *Electron. Lett.* **1974**, *10*, 425–426.
2. Kuo, J.T.; Yu, L.; Meng, E. Micromachined thermal flow sensors—A review. *Micromachines* **2012**, *3*, 550–573.
3. Wang, Y.-H.; Chen, C.-P.; Chang, C.-M.; Lin, C.-P.; Lin, C.-H.; Fu, L.-M.; Lee, C.-Y. MEMS-based gas flow sensors. *Microfluid. Nanofluidics* **2009**, *6*, 333–346.
4. Melani, M.; Bertini, L.; Marinis, M.D.; Lange, P.; Ascoli, F.D.; Fanucci, L. Hot Wire Anemometric MEMS Sensor for Water Flow Monitoring. In Proceedings of the 2008 Design, Automation and Test in Europe, Munich, Germany, 10–14 March 2008.
5. Xu, W.; Wang, X.; Zhao, X.; Ke, Z.; Lee, Y.K. An Integrated CMOS Mems Gas Flow Sensor with Detection Limit Towards Micrometer Per Second. In Proceedings of the 2020 IEEE 33rd International Conference on Micro Electro Mechanical Systems (MEMS), Vancouver, BC, Canada, 18–22 January 2020.
6. Vashi, S.; Ram, J.; Modi, J.; Verma, S.; Prakash, C. Internet of Things (IoT): A vision, architectural elements, and security issues. In Proceedings of the 2017 International Conference on I-SMAC (IoT in Social, Mobile, Analytics and Cloud) (I-SMAC), Palladam, India, 10–11 February 2017.
7. Ahmed, M.; Xu, W.; Mohamad, S.; Boussaid, F.; Lee, Y.K.; Bermak, A. Fully Integrated Bidirectional CMOS-MEMS Flow Sensor With Low Power Pulse Operation. *IEEE Sens. J.* **2019**, *19*, 3415–3424. <https://doi.org/10.1109/JSEN.2019.2891784>.
8. Yoo, M.; Kang, S.; Jin, B.; Son, H.; Kim, K.; Wi, J.; Nam, G.; Bae, N.H.; Ko, H. Low-Noise Operational Amplifier Using Dual-Path Dual-Chopper Fill-in Technique. *IEEE Sens. J.* **2024**, *24*, 12550–12559. <https://doi.org/10.1109/JSEN.2024.3368023>.
9. Witte, J.F.; Huijsing, J.H.; Makinwa, K.A.A. A chopper and auto-zero offset-stabilized CMOS instrumentation amplifier. In Proceedings of the 2009 Symposium on VLSI Circuits, Kyoto, Japan, 16–18 June 2009; pp. 210–211.
10. Rooijers, T.; Karmakar, S.; Kusuda, Y.; Huijsing, J.H.; Makinwa, K.A.A. A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers. *IEEE J. Solid-State Circuits* **2021**, *56*, 3583–3592. <https://doi.org/10.1109/JSSC.2021.3107350>.
11. Vejdani, P.; Nabki, F. Dual-Path and Dual-Chopper Amplifier Signal Conditioning Circuit With Improved SNR and Ultra-Low Power Consumption for MEMS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 2253–2262. <https://doi.org/10.1109/TCSI.2019.2893861>.
12. Choi, G.; Nam, K.; Yoo, M.; Kang, S.; Jin, B.; Kim, K.; Son, H.; Ko, H. Current-Feedback Instrumentation Amplifier Using Dual-Chopper Fill-In Technique. *Appl. Sci.* **2022**, *12*, 10471.
13. Rooijers, T.; Huijsing, J.H.; Makinwa, K.A.A. A Chopper-Stabilized Amplifier with a Relaxed Fill-In Technique and 22.6pA Input Current. In Proceedings of the 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 19–23 February 2023.
14. Pertijs, M.A.P.; Kindt, W.J. A 140 dB-CMRR Current-Feedback Instrumentation Amplifier Employing Ping-Pong Auto-Zeroing and Chopping. *IEEE J. Solid-State Circuits* **2010**, *45*, 2044–2056. <https://doi.org/10.1109/JSSC.2010.2060253>.
15. Yoo, M.; Kwon, Y.; Kim, H.; Choi, G.; Nam, K.; Ko, H. Low-Noise Resistive Bridge Sensor Analog Front-End Using Chopper-Stabilized Multipath Current Feedback Instrumentation Amplifier and Automatic Offset Cancellation Loop. *IEEE Access* **2022**, *10*, 12385–12394. <https://doi.org/10.1109/ACCESS.2022.3144688>.
16. Butti, F.; Piotta, M.; Bruschi, P. A Chopper Instrumentation Amplifier With Input Resistance Boosting by Means of Synchronous Dynamic Element Matching. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 753–764. <https://doi.org/10.1109/TCSI.2016.2633384>.