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Topological-Insulator Heterophase Gate Stacks for Transistor Electrostatics

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Abstract

Conventional gate-stack scaling reduces dielectric thickness and increases permittivity while largely treating the position and electronic character of the gate-side screening boundary as fixed. As equivalent oxide thickness is reduced, however, finite interfacial responses can increasingly constrain gate control [1–5]. Here we show that this screening boundary can itself be engineered by converting the surface of the topological insulator Bi_2Se_3 into insulating high-$\boldsymbol{\kappa}$ BiF_3. Position-resolved calculations reveal a gap-opened immediate amorphous-BiF_3/crystalline-Bi_2Se_3 interface and a reconstructed gap-closed Bi_2Se_3-derived state in the adjacent subinterface layer, accompanied by a localized interfacial dipole. Independently, capacitor measurements resolve a finite series response consistent with the electronic compressibility of this buried boundary, which reduces rather than enhances the nominal stack capacitance. Despite this capacitance penalty, MoS_2 transistors with closely matched BiF_3 thicknesses and a common BiF_3/MoS_2 channel-side material interface exhibit near-thermionic switching, negligible hysteresis, and approximately sevenfold lower drain-induced barrier lowering than BiF_3-only controls. These results identify the position and electronic character of the gate-side screening boundary as additional design variables for transistor electrostatics beyond nominal dielectric capacitance.

1 Introduction

Continued transistor scaling requires control not only over the dielectric between gate and channel, but also over the electronic boundaries at which the gate field is screened. Gate-stack scaling is conventionally described by dielectric thickness and permittivity, yet the applied potential is partitioned across the bulk insulator and finite screening and interfacial responses at conductor/dielectric and dielectric/semiconductor boundaries. As the equivalent oxide thickness (EOT) approaches the subnanometre regime, contributions arising from electrode screening, interfacial bonding, polarization, and chemical or structural reconstruction need not scale with the physical dielectric thickness and can therefore constitute an increasing fraction of the total electrostatic response [1–5]. The position and electronic character of the gate-side screening boundary are thus potentially as important as the dielectric that separates it from the channel.

Two-dimensional (2D) van der Waals (vdW) semiconductors provide a stringent setting in which to expose this distinction. Their atomically thin bodies suppress semiconductor-body electrostatic length scales, whereas their chemically inert surfaces make conventional three-dimensional high-κ integration difficult and susceptible to interfacial disorder, fixed charge, trap states, and carrier scattering [6–8]. Hexagonal boron nitride encapsulation, seeded atomic-layer deposition, native dielectrics, and emerging vdW high-κ materials have therefore focused primarily on improving the dielectric and its interface with the semiconductor [9–14]. These advances leave a complementary question largely open: whether the gate-side screening boundary itself can be deliberately created, displaced, and electronically reconstructed independently of the semiconductor-side interface.

Topological insulators provide a route to this form of boundary engineering. Their bulk electronic structure supports boundary-localized states whose spatial distribution can be displaced or reconstructed when the surface environment is modified [15–18]. Such states have predominantly been considered as transport channels [19, 20]. By contrast, their use as an electrostatically active boundary of a gate stack remains largely unexplored. Because the surface of Bi_2Se_3 can be selectively converted into wide-gap BiF_3 [21], surface conversion provides a means to separate the chemical surface from the electronically active Bi_2Se_3-derived boundary beneath it. This possibility motivates a gate architecture in which the location of screening is an engineered property of the heterophase material itself rather than a fixed consequence of depositing a metal electrode onto a dielectric.

Here we realize this concept in a topological-insulator heterophase gate stack (TIHGS) formed by selective conversion of Bi_2Se_3. Fluorination creates an insulating amorphous BiF_3 phase while retaining electrically conducting crystalline Bi_2Se_3 underneath. Position-resolved electronic-structure calculations show that the immediate heterophase interface becomes gap-opened whereas an electronically active, gap-closed Bi_2Se_3-derived state is reconstructed in the adjacent subinterface layer; a localized interface dipole accompanies this reconstruction. Independent capacitor measurements reveal a finite electronic-compressibility response associated with the buried boundary, which reduces rather than

enhances the nominal stack capacitance. Nevertheless, TIHGS-gated MoS_2 transistors exhibit near-thermionic switching, negligible hysteresis, and strongly suppressed drain-bias sensitivity relative to a closely thickness-matched BiF_3-only control. Together, these structural, microscopic, electrostatic, and transistor-level measurements establish screening-boundary position and electronic character as gate-stack variables complementary to conventional high-κ and EOT scaling.

2 Results and Discussion

Figure 1 contrasts conventional gate-stack electrostatics with screening-boundary relocation in the TIHGS. In a conventional high-κ stack, the gate-side interfacial capacitance ($C_{\mathrm{d,g}}$), dielectric capacitance, channel-side interfacial capacitance ($C_{\mathrm{d,ch}}$), and, for a 2D channel, the van der Waals-gap capacitance (C_{vdW}) contribute in series. Of these terms, $C_{\mathrm{d,g}}$ is central to the present work: it represents the finite electrostatic response of the gate-electrode/dielectric boundary arising from electrode screening and interface-specific electronic, bonding, polarization, and chemical or structural effects. Unlike the bulk dielectric capacitance, which increases as the physical dielectric thickness is reduced, this gate-side boundary contribution need not scale proportionally and can therefore account for an increasing fraction of the total electrostatic response at small EOT [1–5]. By comparison, $C_{\mathrm{d,ch}}$ denotes the local dielectric/semiconductor interfacial response, and C_{vdW} denotes the geometric contribution associated with the vdW separation at a 2D semiconductor interface. The bias-dependent semiconductor-body response is outside the gate-stack contribution defined here and is omitted from Fig. 1 for clarity. The resulting design question is therefore whether the gate-side screening boundary represented by $C_{\mathrm{d,g}}$ must remain fixed at the external metal/dielectric interface.

In the TIHGS, selective surface conversion creates insulating BiF_3 while residual Bi_2Se_3 remains electrically coupled to the gate electrode. This architecture displaces the gate-side electrostatic termination from a conventional externally formed metal/dielectric boundary to a heterophase-induced buried electronic boundary. Importantly, the chemical conversion front and the electronic screening boundary need not coincide atomically: the position-resolved calculations below show a gap-opened a-BiF_3/c-Bi_2Se_3 interface and a reconstructed gap-closed state in the adjacent c-Bi_2Se_3 subinterface layer (Fig. 3c,d). We therefore use "buried screening boundary" to denote this electronically active heterophase-associated boundary region rather than an ideal atomically sharp conductor/dielectric plane. In the

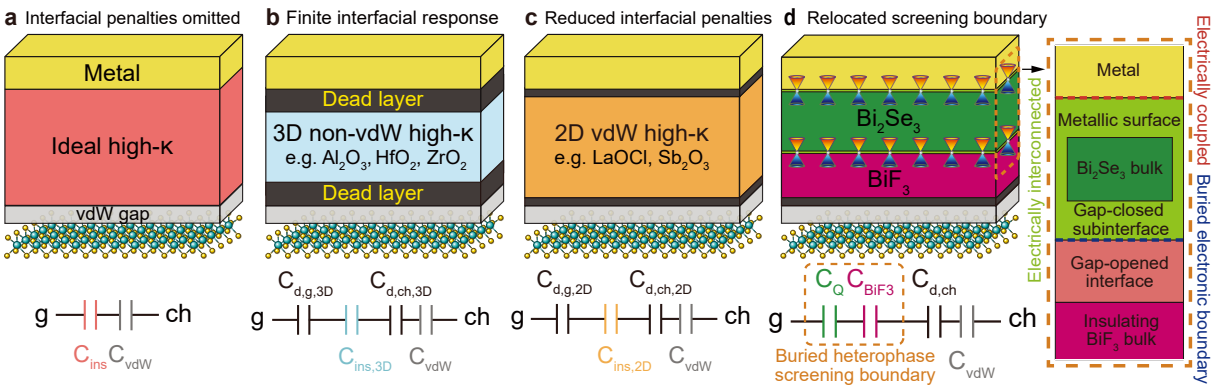


Fig. 1 Screening-boundary relocation in a topological-insulator heterophase gate stack (TIHGS). a–d, Schematics and equivalent-capacitance models for gate-dielectric structures with a two-dimensional (2D) van der Waals (vdW) channel; the bias-dependent semiconductor-body capacitance is omitted. **a**, Idealized gate stack without finite interfacial-capacitance penalties. **b**, Conventional three-dimensional (3D) non-vdW high-κ dielectric with gate-side and channel-side interfacial capacitances ($C_{\mathrm{d,g,3D}}$ and $C_{\mathrm{d,ch,3D}}$), vdW-gap capacitance (C_{vdW}), and insulator capacitance ($C_{\mathrm{ins,3D}}$). **c**, 2D vdW high-κ dielectric retaining finite gate-side and channel-side interfacial contributions ($C_{\mathrm{d,g,2D}}$ and $C_{\mathrm{d,ch,2D}}$) in series with C_{vdW} and $C_{\mathrm{ins,2D}}$. **d**, TIHGS formed by surface conversion of Bi_2Se_3 into insulating BiF_3 while retaining conducting Bi_2Se_3 electrically coupled to the gate electrode. The microscopic schematic distinguishes the gap-opened amorphous-BiF_3/crystalline-Bi_2Se_3 chemical interface from the adjacent gap-closed Bi_2Se_3-derived subinterface electronic boundary. This heterophase-induced buried electronic boundary is associated with the active gate-side screening condition, with the effective electronic-compressibility response associated with the boundary represented by C_Q in series with $C_{\mathrm{BiF_3}}$ and the channel-side interfacial contributions.

reduced series-capacitance model, its finite electronic response is represented as

$$\frac{1}{C_{\mathrm{g,TIHGS}}} = \frac{1}{C_Q} + \frac{1}{C_{\mathrm{BiF_3}}} + \frac{1}{C_{\mathrm{d,ch}}} + \frac{1}{C_{\mathrm{vdW}}},$$

where C_Q denotes the effective electronic-compressibility response associated with the buried electronic boundary. Here, $C_{\mathrm{g,TIHGS}}$ denotes the gate-to-channel-interface contribution represented in Fig. 1, including the channel-side interfacial and vdW-gap terms, whereas C_{TIHGS} used below for the capacitor analysis denotes only the BiF_3/buried-boundary element, such that $C_{\mathrm{TIHGS}}^{-1} = C_{\mathrm{BiF_3}}^{-1} + C_Q^{-1}$. The defining architectural change is therefore $C_{\mathrm{d,g}} \rightarrow C_Q$: the physical origin, spatial position and electronic character of the gate-side series response become properties of an intentionally generated heterophase boundary rather than of an externally deposited metal/dielectric contact. This notation does not imply that C_Q is larger than $C_{\mathrm{d,g}}$ or that the gate-side series response is eliminated; indeed, the measurements below show that finite C_Q reduces the nominal TIHGS capacitance. The electrostatic scope and limitations of this reduced boundary model are discussed in Supplementary Note 1.

We established the conversion-defined geometry independently through structural and chemical characterization. Cross-sectional transmission electron microscopy (TEM) of fluorinated structures shows an amorphous converted BiF_3 region above residual crystalline Bi_2Se_3, with the conversion depth approaching a self-limited value of ∼40–43 nm. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) combined with energy-dispersive X-ray spectroscopy (EDS) further resolves the corresponding compositional stratification (Extended Data Fig. 1). Atomic force microscopy (AFM),

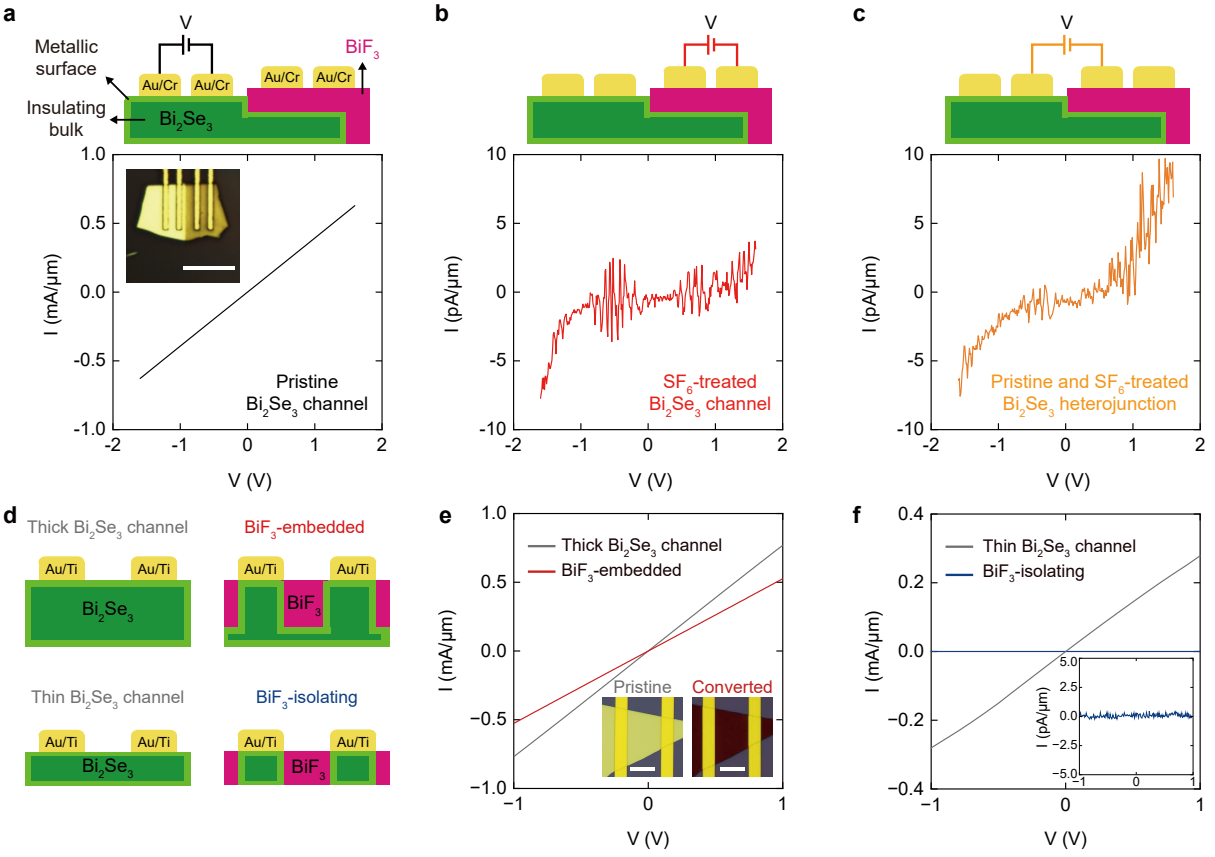


Fig. 2 Electrical isolation and buried conduction in the topological-insulator heterophase gate stack. a–c, Device schematics (top) and corresponding current–voltage (I–V) characteristics (bottom) of **a**, pristine Bi_2Se_3; **b**, SF_6-converted Bi_2Se_3; and **c**, a lateral pristine/converted heterojunction. The converted region suppresses conduction from the mA μm^{-1} to the pA μm^{-1} range. Scale bar in **a**, 10 μm. **d**, Schematics illustrating partial surface conversion of a Bi_2Se_3 flake thicker than the conversion depth and complete conversion of a thinner flake. **e**, I–V characteristics of a thick Bi_2Se_3 channel before and after partial surface conversion, showing persistent conduction through the residual Bi_2Se_3. Insets, corresponding optical micrographs. Scale bars, 20 μm. **f**, I–V characteristics of a thin Bi_2Se_3 channel before and after complete conversion, showing electrical isolation after fluorination. Inset, current on the pA scale after conversion.

Raman spectroscopy and X-ray photoelectron spectroscopy (XPS) independently support spatially selective chemical conversion rather than additive deposition: for a 5-s treatment, the ∼3.3-nm surface-height increase measured by AFM is substantially smaller than the ∼13.1-nm converted-layer thickness measured by TEM, consistent with conversion and expansion of the parent Bi_2Se_3, while XPS directly reveals Bi–F bonding (Extended Data Fig. 2). The conversion-depth dependence and its relation to fluorine penetration are discussed in Supplementary Note 2.

A functional TIHGS requires two conditions to coexist: the converted surface phase must provide dielectric isolation, while the residual Bi_2Se_3 beneath it must remain electrically conducting. A pristine Bi_2Se_3 channel carries current in the mA μm^{-1} range, whereas a fully converted channel and a lateral pristine/converted junction are suppressed to the pA μm^{-1} range (Fig. 2a–c). The converted region therefore acts as an electrically isolating barrier rather than simply a resistive modification of Bi_2Se_3. Comparable electrical isolation was not reproduced by O_2-plasma treatment, under which Bi_2Se_3 remained conductive even after prolonged exposure (Extended Data Fig. 3a–h).

The complementary requirement of buried conduction is established by conversion-depth-dependent transport. Bi_2Se_3 flakes thicker than the self-limited conversion depth remain conductive after partial fluorination, whereas thinner flakes become electrically isolated after complete conversion (Fig. 2d–f). Quantitative transfer-length measurements across a locally converted region further show nearly unchanged contact resistance (∼157 versus ∼161 Ω) together with a ∼3.5-fold increase in sheet resistance, consistent with an electrically continuous Bi_2Se_3 pathway persisting beneath the insulating converted region (Extended Data Fig. 3i–m). These measurements establish the vertically stratified insulating-BiF_3/conducting-Bi_2Se_3 configuration required for the buried gate-side screening boundary.

The electrically stratified BiF_3/Bi_2Se_3 structure raises a central microscopic question: where does the electronically active boundary reside after surface conversion? Pristine c-Bi_2Se_3 exhibits a Dirac-like surface-state dispersion within a calculated 0.31-eV bulk gap, with the Dirac-point energy (E_D) located ∼0.043 eV below the Fermi level (E_F) and finite spectral weight extending to E_F (Fig. 3a,b). Formation of the a-BiF_3/c-Bi_2Se_3 heterophase produces a spatially resolved reconstruction. The immediate heterophase interface becomes gap-opened, with an interface-projected gap of ∼0.72 eV, whereas the adjacent c-Bi_2Se_3 subinterface QL develops a reconstructed gap-closed Bi_2Se_3-derived Dirac-like feature centred ∼0.146 eV below E_F and retaining finite near-E_F spectral weight (Fig. 3c,d). The opposite surface remains pristine-like. The direct microscopic result is therefore a spatial separation between the gap-opened chemical interface and an electronically active gap-closed subinterface boundary, rather than simple survival of the original Bi_2Se_3 surface state.

The calculated dipole-moment profile is strongly localized near the a-BiF_3/c-Bi_2Se_3 heterophase interface (Fig. 3e), showing that formation of the heterophase is accompanied by localized interfacial charge redistribution. We do not assign the shift of the reconstructed Dirac-like feature uniquely to this dipole, because chemical reconstruction, local bonding and band bending are not independently decomposed. Instead, the position-resolved band reconstruction and localized dipole provide complementary microscopic evidence that surface conversion reorganizes and spatially relocates the Bi_2Se_3-derived electronic boundary. Whether this boundary also exhibits finite electronic compressibility is tested independently below by capacitance measurements. We therefore interpret the calculations conservatively as evidence for a reconstructed Bi_2Se_3-derived buried electronic boundary, without assigning an independently determined topological invariant to the chemically reconstructed interface (Supplementary Note 3). Complementary calculations confirm that amorphous BiF_3 remains insulating, with a calculated band gap of 3.94 eV; the crystalline and amorphous BiF_3 electronic structures and calculated dielectric properties are summarized in Extended Data Fig. 4 and Extended Data Table 1.

Capacitor measurements provide an independent electrostatic test of the buried electronic boundary. Crystalline TIHGS-43 (cN) MIM capacitors containing a ∼43-nm-thick converted BiF_3 layer exhibit nearly bias-independent capacitance and a mean BiF_3-thickness-normalized effective relative permittivity $\varepsilon_{\mathrm{eff,TIHGS}} = 16.50$ (Fig. 3f,g). Polycrystalline TIHGS-13 (p20) and TIHGS-43 (p50) similarly yield $\varepsilon_{\mathrm{eff,TIHGS}} \approx 15$–16, whereas the fully converted BiF_3-only reference yields $\varepsilon_{\mathrm{BiF_3}} = 28.65$ on average. The lower TIHGS capacitance is represented by

$$\frac{1}{C_{\mathrm{TIHGS}}} = \frac{1}{C_{\mathrm{BiF_3}}} + \frac{1}{C_Q},$$

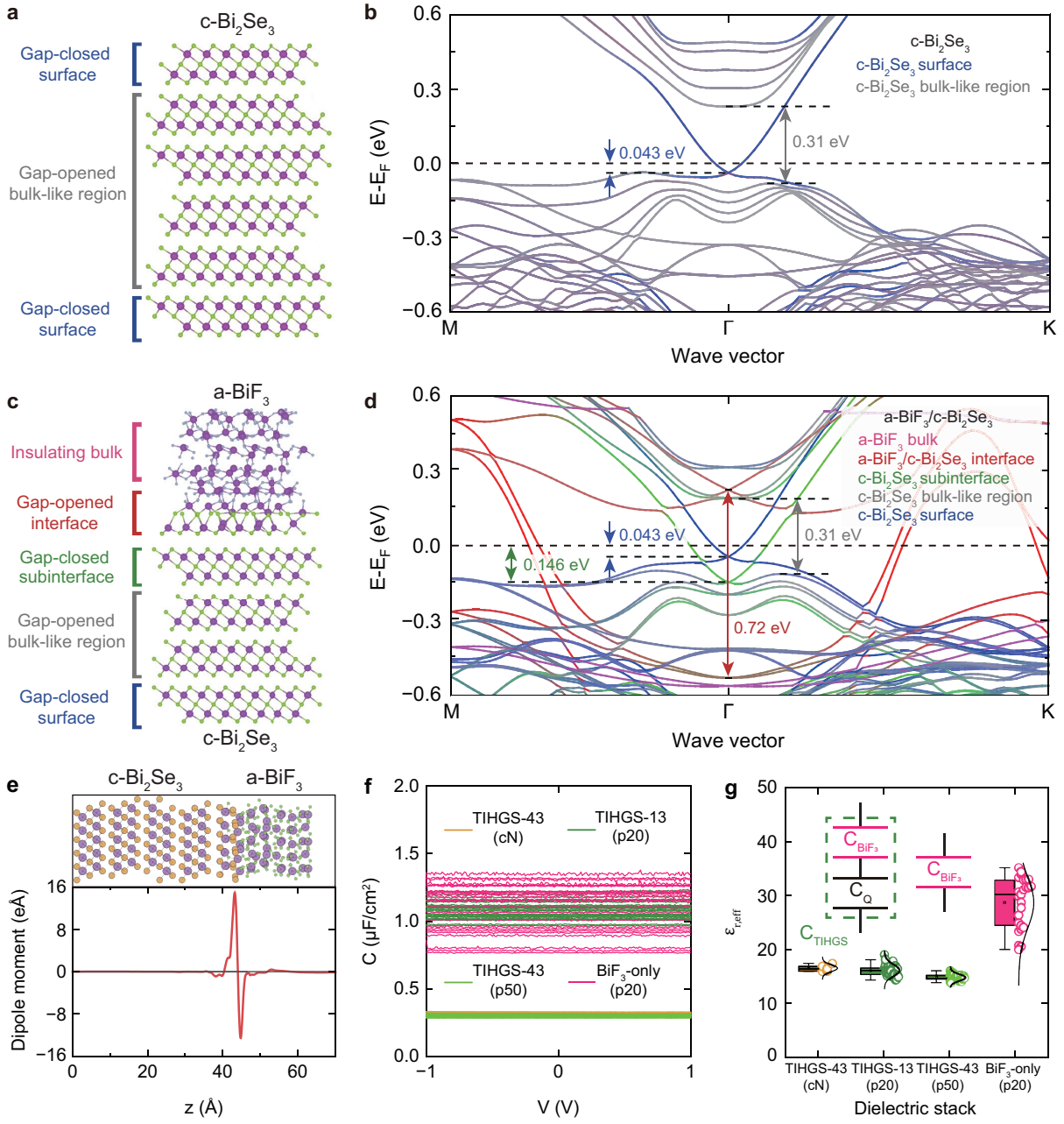


Fig. 3 Electronic reconstruction and electrostatic response of the buried TIHGS boundary. a, Six-quintuple-layer (QL) crystalline Bi_2Se_3 (c-Bi_2Se_3) (0001) slab used to model the pristine surface, with gap-closed outer QLs and a gap-opened bulk-like interior. **b**, Surface-weighted electronic band structure of **a**. Bulk-projected states are grey and surface-weighted states blue; the calculated bulk gap is 0.31 eV and the Dirac point lies ∼0.043 eV below the Fermi level (E_F). **c**, Structural model of amorphous BiF_3 (a-BiF_3) interfaced with four-QL c-Bi_2Se_3, showing the immediate heterophase interface, adjacent subinterface QL, bulk-like region, and opposite surface. **d**, Position-resolved electronic structure of **c**. The immediate interface is gap-opened by ∼0.72 eV, whereas the adjacent subinterface QL exhibits a reconstructed gap-closed Bi_2Se_3-derived Dirac-like feature centred ∼0.146 eV below E_F with finite near-E_F spectral weight. The opposite surface remains pristine-like. **e**, Calculated out-of-plane dipole-moment profile, showing a response localized near the heterophase interface. **f**, Capacitance–voltage (C–V) characteristics of BiF_3-only (p20), TIHGS-13 (p20), TIHGS-43 (p50) and TIHGS-43 (cN) MIM capacitors (n = 25, 33, 24 and 5, respectively). TIHGS-13 and TIHGS-43 contain ∼13- and ∼43-nm converted BiF_3; p20 and p50 denote nominal starting polycrystalline Bi_2Se_3 thicknesses, and cN crystalline Bi_2Se_3 with nominal starting thickness N. **g**, Distributions of ε_{BiF_3} and the BiF_3-thickness-normalized $\varepsilon_{eff,TIHGS}$. Inset, series-capacitance representation of C_{BiF_3} and effective interfacial quantum capacitance C_Q. Boxes indicate the interquartile range, with centre lines denoting the median, and individual symbols represent separate capacitors.

where the independently measured BiF_3 reference gives effective C_Q values of ∼2.52 and ∼0.631 μF cm^{-2} for TIHGS-13 (p20) and TIHGS-43 (p50), respectively (Supplementary Note 4). Their geometry dependence shows that C_Q is an effective interfacial response rather than a universal material constant. Most importantly, the finite C_Q is a series response that reduces the measured stack capacitance. Combined with the independently calculated near-E_F subinterface spectral weight, this finite electronic response provides mutually consistent microscopic and electrostatic evidence for an electronically compressible buried boundary. The weak dependence of $\varepsilon_{\mathrm{eff,TIHGS}}$ on the residual Bi_2Se_3 thickness further disfavors a dominant bulk contribution (Extended Data Fig. 5f). The broader dielectric-property context is shown in Extended Data Fig. 5g.

For this boundary architecture to function as a gate stack, the converted BiF_3 phase must also retain sufficient electrical isolation. Within the approximately $|V| \leq 0.5$ V gate-voltage window relevant to the demonstrated transistors, the TIHGS MIM current density remains below 10^{-2} A cm^{-2}, while the measured transistor gate-leakage current remains well below the drain current. At higher fields, the leakage characteristics evolve from field-assisted emission towards Fowler–Nordheim tunnelling. The localized dipole in Fig. 3e provides microscopic evidence of interfacial charge redistribution, whereas Extended Data Fig. 6 distinguishes the measured leakage regimes and the vacuum-referenced, contact-equilibrated and high-field band-alignment configurations. The complete transport analysis and its limitations are discussed in Supplementary Note 5. Frequency-dependent capacitor measurements further show modest dispersion and low loss from 1 kHz to 1 MHz (Extended Data Fig. 5c–e), and WSe_2/TIHGS MISCAPs reproduce a stack-level $\varepsilon_{\mathrm{eff,TIHGS}} \approx 16$ after semiconductor integration (Extended Data Fig. 7, Extended Data Table 2, and Supplementary Notes 6 and 7).

We next tested whether the relocated gate-side boundary can improve functional gate control despite the lower nominal stack capacitance, using MoS_2 FETs incorporating either a TIHGS or a fully converted BiF_3-only dielectric. The devices retain a common BiF_3/MoS_2 channel-side material interface, closely matched physical BiF_3 thicknesses of ∼43 nm, and comparable channel lengths, while differing principally in their gate-side boundary condition (Fig. 4a,c). The representative TIHGS-gated transistor exhibits an on–off current ratio exceeding 10^6, a minimum room-temperature subthreshold swing (SS) of ∼65 mV dec^{-1} and negligible hysteresis, compared with ∼ 10^5, ∼ 83 mV dec^{-1} and larger hysteresis for the BiF_3-gated control (Fig. 4b–e). Because the channel-side material interface and insulating-layer thickness are closely matched while the TIHGS has the lower nominal capacitance, these differences cannot be attributed simply to a thinner or higher-capacitance dielectric.

The distinction is strongest in the drain-bias response: the TIHGS-gated device exhibits a DIBL of ∼12 mV V^{-1}, compared with ∼87 mV V^{-1} for the BiF_3-gated control (Fig. 4f). An air-oxidized BiO_x/Bi_2Se_3 control reaches SS ∼ 73 mV dec^{-1} but retains a much larger DIBL of ∼ 75.7 mV V^{-1}, showing that formation of a self-derived insulating surface phase alone does not reproduce the combined switching and drain-bias response of the TIHGS (Extended Data Fig. 8). Across three measured devices per gate-stack configuration, the TIHGS-gated devices occupy the low-SS/low-leakage region, while literature benchmarking places the representative device in the low-SS/low-hysteresis region without implying direct device-to-device ranking (Fig. 4g and Extended Data Fig. 8h) [22–28]. These matched controls associate the improved functional gate control with the changed gate-side boundary condition. Finite C_Q is not assigned as its causal mechanism; rather, it provides an independent electrostatic signature consistent with an electronically compressible relocated boundary, while the separate contributions of the reconstructed state, interface dipole, fixed charge and structural disorder are not resolved here.

3 Conclusion

The TIHGS demonstrates that the spatial position and electronic character of the gate-side screening boundary can be engineered independently of the semiconductor-side interface. Selective conversion of Bi_2Se_3 creates insulating BiF_3 while retaining conducting Bi_2Se_3 beneath it. At this heterophase boundary, the immediate chemical interface is gap-opened, whereas a reconstructed gap-closed Bi_2Se_3-derived state emerges in the adjacent subinterface layer, accompanied by localized interfacial charge redistribution. The finite near-E_F spectral weight and independently measured series quantum-capacitance response together support an electronically compressible buried boundary, while the latter lowers rather than enhances the nominal stack capacitance. Nevertheless, matched MoS_2 transistors exhibit near-thermionic switching, negligible hysteresis and strongly suppressed drain-bias sensitivity relative to BiF_3-only controls. The resulting separation between chemical interface, electronic screening boundary

and nominal dielectric capacitance extends gate-stack design beyond conventional high-κ and *EOT* optimization, introducing boundary position and electronic structure as independent variables for transistor electrostatics.

4 Methods

4.1 First-Principles Calculations

Density functional theory (DFT) calculations were performed using the Vienna *Ab initio* Simulation Package (VASP) [29]. All DFT calculations used the Perdew–Burke–Ernzerhof (PBE) functional within the generalized gradient approximation (GGA) [30], projector-augmented-wave (PAW) potentials [31], and spin–orbit coupling (SOC); this framework is hereafter denoted PBE+SOC. A plane-wave energy cutoff of 520 eV was used. Structures used for the DFT analyses were relaxed until the residual Hellmann–Feynman force on each atom was below 0.01 eV Å^{-1}. Long-range dispersion interactions were included using the DFT-D3 method with Becke–Johnson damping [32]. The first-principles calculations presented in Fig. 3a–e and Extended Data Fig. 4, together with the calculated properties summarized in Extended Data Table 1, were obtained within this DFT framework. Dielectric responses were evaluated using density-functional perturbation theory (DFPT) [33].

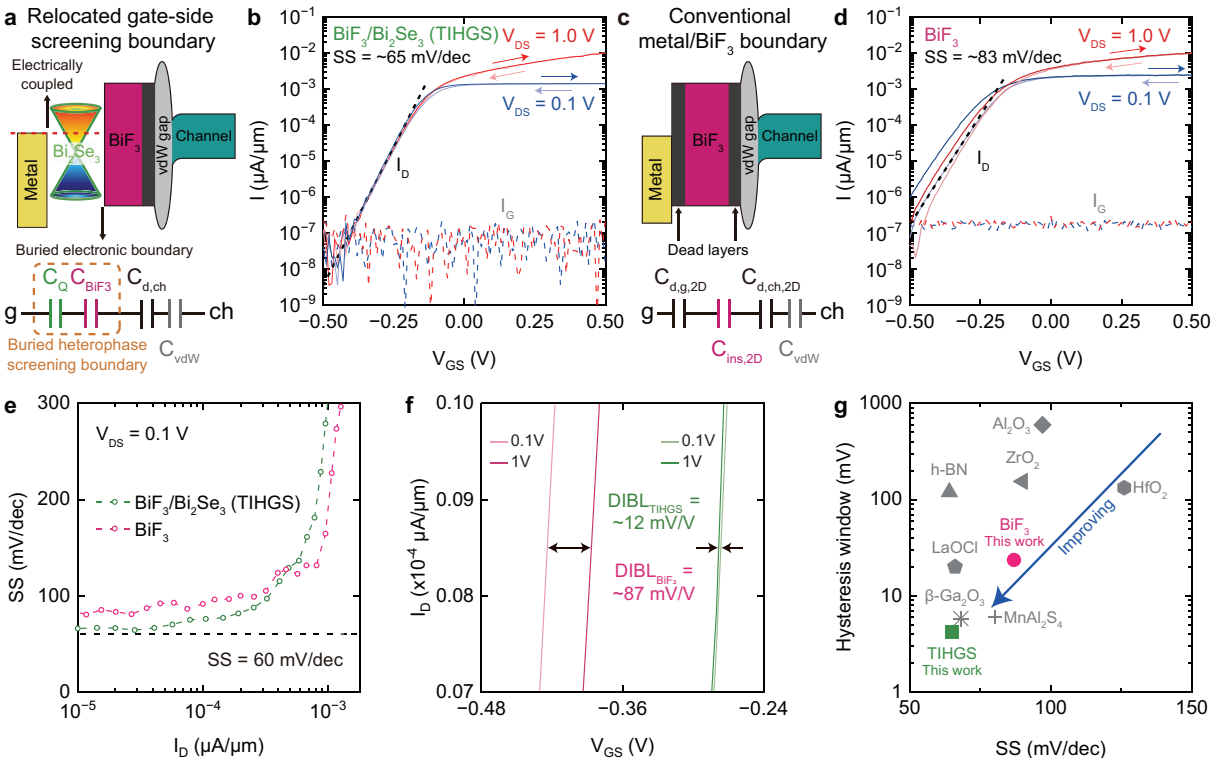


Fig. 4 Enhanced electrostatic control in TIHGS-gated MoS_2 transistors. a,c, Schematics of the TIHGS-gated MoS_2 field-effect transistor (FET) **(a)** and BiF_3-gated control FET **(c)** with their corresponding gate-side electrostatic boundary conditions. In the TIHGS-gated device, residual Bi_2Se_3 remains electrically coupled to the gate electrode, and the heterophase-induced buried electronic boundary within the Bi_2Se_3 subinterface region defines the active gate-side screening condition. The physical BiF_3 thicknesses are closely matched at ~43 nm in both devices. **b,d**, Forward and reverse transfer characteristics of representative TIHGS-gated **(b)** and BiF_3-gated **(d)** devices. The TIHGS-gated device exhibits a minimum subthreshold swing (*SS*) of ~65 mV dec^{-1} and negligible hysteresis, compared with ~83 mV dec^{-1} and larger hysteresis for the BiF_3-gated control. Dashed traces denote gate-leakage current. **e**, Drain-current-dependent *SS*. The dashed line marks the room-temperature thermionic limit of 60 mV dec^{-1}. **f**, Threshold-voltage shift used to determine drain-induced barrier lowering (DIBL), yielding ~12 and ~87 mV V^{-1} for the TIHGS- and BiF_3-gated devices, respectively. **g**, Comparison of *SS* and hysteresis window for the TIHGS- and BiF_3-gated devices from this work and representative reported MoS_2 FETs employing different gate dielectrics [22–28]. Literature values correspond to devices with different geometries and were obtained using different gate-voltage ranges, sweep conditions, and extraction protocols; they are therefore shown for contextual benchmarking rather than direct device-to-device ranking.

Amorphous BiF_3, Bi_2Se_3, and Bi_2O_3 structures were generated using melt–quench molecular-dynamics simulations with the SevenNet-Omni-i12 machine-learning interatomic potential [34]. The resulting amorphous structures were subsequently relaxed within the DFT framework described above before electronic-structure and dielectric calculations.

For bulk Bi_2Se_3, Bi_2O_3, and BiF_3 structures, the Brillouin zone was sampled using k-point meshes corresponding to a reciprocal-space density of 100 k-points per $Å^{-3}$. The pristine Bi_2Se_3 slab and the a-BiF_3/c-Bi_2Se_3 heterophase slab were sampled using $5 \times 5 \times 1$ k-point meshes.

For the pristine Bi_2Se_3 surface calculation, a six-quintuple-layer (QL) crystalline Bi_2Se_3 slab terminated along the (0001) direction was used (Fig. 3a,b). To minimize direct interactions between adjacent periodic images, all slab structures were constructed with a vacuum spacing greater than 15 Å.

For the heterophase calculation, an amorphous BiF_3 region was interfaced with a four-QL crystalline Bi_2Se_3 slab to model the buried BiF_3/Bi_2Se_3 boundary. The QL-resolved electronic structures were obtained directly from the VASP calculations by projecting the electronic states onto individual Bi_2Se_3 QLs at different distances from the heterophase boundary. We compare the subinterface QL, corresponding to the first Bi_2Se_3 QL directly beneath the BiF_3/Bi_2Se_3 interface, with the surface QL at the opposite side of the four-QL slab, corresponding to the fourth Bi_2Se_3 QL counted from the heterophase boundary (Fig. 3c,d).

4.2 SRIM Simulations

Stopping and range of ions in matter (SRIM) simulations were performed using the SRIM-2013 package [35]. We used a 50-nm-thick stoichiometric Bi_2Se_3 layer as a representative target geometry. The displacement energies of Bi and Se were set to 30 eV based on the values reported by Konobeyev *et al.* [36]. Because the ion-energy distribution incident on the sample surface was not measured experimentally, F^+ incident energies of 0.5, 1, 2.5, and 5 keV were examined as a sensitivity range for the accessible ballistic penetration length scale. The 5-keV calculation was deliberately included as a high-energy upper-bound case and should not be interpreted as the dominant fluorine-ion energy under the experimental plasma conditions. For each incident energy, we simulated 10,000 ions to obtain statistically stable fluorine depth distributions. To compare incident energies, the resulting fluorine depth profiles were area-normalized and smoothed with a Gaussian filter.

The SRIM calculations describe ballistic ion transport only and do not include plasma chemistry, transport of neutral reactive species, fluorine diffusion, sputter erosion, dynamic changes in target composition or density, surface charging, plasma-sheath evolution, or formation of BiF_3. The calculations therefore provide a ballistic length-scale constraint on fluorine penetration rather than a quantitative description of fluorination kinetics, as discussed in Supplementary Note 2.

4.3 Synthesis of Polycrystalline Bi_2Se_3 Films

Polycrystalline Bi_2Se_3 films were synthesized by solution deposition followed by thermal selenization. Precursor solutions with concentrations of 5 and 10 wt% were prepared by dissolving bis{tris[*N*-ethoxy-2,2-dimethylpropanamidato]bismuth(III)} ($[Bi(edpa)_3]_2$) in tetrahydrofuran (THF) and stirring for 60 min to obtain homogeneous solutions. The solutions were spin-coated onto 300-nm-thick SiO_2/Si substrates that had been rendered hydrophilic by ultraviolet–ozone treatment for 600 s. Spin coating was performed at 1,000 rpm for 10 s followed by 2,000 rpm for 30 s. The resulting precursor layers were immediately annealed at 100 °C for 1 min to remove residual solvent. The 5 and 10 wt% precursor concentrations produced Bi_2Se_3 films with nominal thicknesses of approximately 20 and 50 nm, respectively, after selenization.

For selenization, the precursor-coated substrates were placed in a quartz-tube furnace with 0.2 g of Se powder (99.99%, Sigma-Aldrich) positioned upstream. The furnace was purged and maintained under 99.9999% Ar at a flow rate of 1,000 standard cubic centimetres per minute (sccm) and a pressure of 3 Torr. The temperature was increased to 300 °C at a rate of 15 °C min^{-1} and maintained for 60 min to induce precursor decomposition and selenization, yielding large-area polycrystalline Bi_2Se_3 films. After selenization, the furnace was turned off and allowed to cool naturally to room temperature under the Ar atmosphere.

4.4 Spatially Selective Fluorination of Bi_2Se_3

Crystalline Bi_2Se_3 flakes used for spatially selective fluorination and transport measurements were mechanically exfoliated from bulk single crystals and transferred onto highly doped Si substrates capped with 285 nm SiO_2. Selected regions of the Bi_2Se_3 surface were exposed using electron-beam lithography (Vistec EBPG 5000), while the regions intended to remain pristine were protected with polymethyl methacrylate (PMMA).

Surface conversion was performed in an Oxford Instruments PlasmaLab 80 Plus system using an SF_6/Ar plasma with SF_6 and Ar flow rates of 10 and 5 sccm, respectively, a chamber pressure of 50 mTorr, and a radio-frequency (RF) power of 50 W. The converted-layer thickness increased with plasma-treatment time and approached a self-limited thickness of ∼40–43 nm after ∼20–25 s of treatment (Extended Data Fig. 1). A 5-s treatment produced a ∼13.1-nm-thick converted surface layer under the conditions used for the thickness-calibration experiment, whereas a 25-s treatment produced a ∼42.5–43-nm-thick converted layer. Regions protected by PMMA remained unexposed to the SF_6 plasma.

For the plasma-control experiments in Extended Data Fig. 3a–h, Bi_2Se_3 was exposed to O_2 plasma at an O_2 flow rate of 30 sccm, a chamber pressure of 30 mTorr, and an RF power of 50 W for either 10 or 60 s.

For lateral transport and transfer-length-method structures, we patterned metal electrodes using electron-beam lithography and deposited 5/50 nm Cr/Au via electron-beam evaporation (MASA IM-9912), followed by lift-off. Hexagonal boron nitride (h-BN) flakes were deterministically transferred onto the devices as protective encapsulation using a dry-release transfer process based on polypropylene carbonate (PPC) and polydimethylsiloxane (PDMS).

4.5 Fabrication of BiF_3 and TIHGS MIM Capacitors

Polycrystalline Bi_2Se_3 films with nominal starting thicknesses of approximately 20 and 50 nm were used to fabricate the fully converted BiF_3 reference and partially converted topological-insulator heterophase gate stack (TIHGS) capacitor structures. The films were transferred onto substrates coated with 5 nm Ti and 50 nm Au on 285-nm-thick SiO_2/Si using a wet-transfer process.

Fluorination was carried out using the SF_6/Ar plasma conditions described above. Three polycrystalline conversion configurations were used. A nominally 20-nm-thick starting Bi_2Se_3 film treated for 5 s produced a ∼13-nm-thick converted BiF_3 layer while retaining underlying Bi_2Se_3 and was denoted TIHGS-13 (p20). A nominally 50-nm-thick starting film treated for 25 s produced a ∼43-nm-thick converted BiF_3 layer while retaining underlying Bi_2Se_3 and was denoted TIHGS-43 (p50). In contrast, a nominally 20-nm-thick starting film treated for 25 s was fully converted and used as the BiF_3-only reference [BiF_3-only (p20)]. Atomic force microscopy independently determined the post-conversion physical thickness of this fully converted BiF_3 layer to be ∼23 nm, and this measured thickness was used for extraction of ε_{BiF_3}. For the partially converted TIHGS structures, the converted BiF_3 thickness and nominal starting Bi_2Se_3 thickness are reported independently because fluorination is accompanied by volume expansion and the residual Bi_2Se_3 thickness cannot be obtained by simple subtraction.

For capacitance measurements of the polycrystalline structures, a 30-nm-thick Al_2O_3 layer was deposited after fluorination by atomic layer deposition (ALD) at 300 °C using trimethylaluminum (TMA) and H_2O as the Al and O precursors, respectively. Each ALD cycle consisted of a 0.5-s TMA pulse, a 2-s Ar purge, a 0.5-s H_2O pulse, and a 2-s Ar purge, and a total of 270 cycles was used to obtain the nominal 30-nm thickness. Independently fabricated 30-nm Al_2O_3 reference capacitors prepared under the same ALD conditions were used to determine the Al_2O_3 dielectric response and to de-embed its series contribution from the BiF_3-only and TIHGS structures. Top electrodes were defined using a shadow mask, followed by electron-beam evaporation of 15 nm Pt, 150 nm Ag, and 20 nm Au, giving an Au/Ag/Pt top-electrode stack.

Crystalline-Bi_2Se_3-based TIHGS MIM capacitors were fabricated separately from mechanically exfoliated Bi_2Se_3 flakes with nominal starting thicknesses of 49, 65, 91, 128, or 179 nm. The Bi_2Se_3 flakes were first transferred onto bottom electrodes comprising 5 nm Ti and 50 nm Au. These samples were fluorinated under conditions producing a ∼43-nm-thick converted BiF_3 layer and are denoted TIHGS-43 (cN), where N is the nominal starting crystalline-Bi_2Se_3 thickness in nanometres. Following fluorination, 100-nm-thick Au top electrodes were deposited directly onto the converted BiF_3 surface without an intervening Ti adhesion layer, yielding Au/BiF_3/Bi_2Se_3/Au/Ti MIM structures.

4.6 Fabrication of WSe_2/TIHGS MISCAPs

Metal–insulator–semiconductor capacitors (MISCAPs) were fabricated using crystalline-Bi_2Se_3-based TIHGS structures containing a ∼43-nm-thick converted BiF_3 layer. Bi_2Se_3 flakes were first transferred onto bottom electrodes comprising 5 nm Ti and 50 nm Au. A 37.37-nm-thick WSe_2 flake, as determined by atomic force microscopy, was deterministically transferred onto the BiF_3 surface using a PPC/PDMS-based dry-release transfer process, thereby forming the semiconductor/dielectric interface. Following lithography, top electrodes comprising 15 nm Pt, 150 nm Ag, and 20 nm Au were deposited by electron-beam evaporation. The completed MISCAP therefore had an Au/Ag/Pt/WSe_2/BiF_3/Bi_2Se_3/Au/Ti vertical stack. The underlying Bi_2Se_3 remained electrically coupled to the bottom Au/Ti electrode, while WSe_2 formed the semiconductor side of the MISCAP.

4.7 Fabrication of MoS_2 Field-Effect Transistors

MoS_2 FETs were fabricated using three gate-stack configurations: a TIHGS comprising partially converted BiF_3/Bi_2Se_3, a fully converted BiF_3-only dielectric, and an air-oxidized BiO_x/Bi_2Se_3 control stack.

For the TIHGS-gated devices, Bi_2Se_3 flakes thicker than the self-limited fluorination depth were partially converted so that an insulating BiF_3 region directly faced the MoS_2 channel while electrically conducting Bi_2Se_3 remained beneath the converted region and was electrically coupled to the metal gate. For the BiF_3-gated control devices, Bi_2Se_3 flakes thinner than the self-limited conversion depth were fully fluorinated, producing a BiF_3-only dielectric in direct contact with the metal gate. Thus, the TIHGS-gated and BiF_3-gated devices shared a common BiF_3/MoS_2 channel-side interface but differed in their gate-side electrostatic boundary.

Mechanically exfoliated MoS_2 flakes were assembled onto the respective gate-stack structures as follows. Bi_2Se_3 flakes were first transferred onto bottom electrodes comprising 5 nm Ti and 50 nm Au and were then partially or fully fluorinated under the conditions described above to form the TIHGS or BiF_3-only gate stack, respectively. MoS_2 flakes approximately 20 nm thick and 30 μm in lateral dimension were subsequently transferred onto the BiF_3 surface using a PPC/PDMS-based dry-release transfer process. Source and drain electrodes were patterned by electron-beam lithography and formed by electron-beam evaporation of 5 nm Ti followed by 50 nm Au, with Ti directly contacting MoS_2.

For the chemically derived interface control, Bi_2Se_3 was exposed to ambient air for 2 days to form an oxidized BiO_x surface layer. The corresponding oxide thickness was estimated to be ∼1.94 nm based on the previously reported oxidation behaviour of Bi_2Se_3 [37]. MoS_2 was subsequently integrated onto the BiO_x/Bi_2Se_3 stack using the same device-assembly procedure, and source/drain electrodes were fabricated as described above.

For the representative devices compared in Fig. 4, the insulating BiF_3 thicknesses were closely matched. For the BiF_3-gated control, AFM measured a Bi_2Se_3 thickness of 37.2 nm before fluorination and a post-conversion BiF_3 thickness of 42.8 nm after complete fluorination. The TIHGS-gated device contained an approximately 43-nm-thick converted BiF_3 region while retaining electrically conducting Bi_2Se_3 underneath. Thus, the two devices had closely matched insulating-layer thicknesses while retaining distinct gate-side screening boundaries. The MoS_2 channel dimensions (length × width) were 8.56 μm × 2.93 μm for the TIHGS-gated device and 9.30 μm × 2.12 μm for the BiF_3-gated control.

4.8 Structural and Chemical Characterization

Optical microscopy was performed using Olympus BX60 and MX63L microscopes. Atomic force microscopy (AFM) in Extended Data Fig. 2a,b was performed using a Bruker Dimension Icon in PeakForce Tapping mode with a ScanAsyst-Air cantilever having a nominal tip radius of ∼2 nm. AFM was used to determine flake thicknesses, converted-layer-associated surface-height changes, and the WSe_2 thickness used in the MISCAP analysis.

Cross-sectional transmission electron microscopy (TEM) was performed using a JEOL JEM-2200FS. Cross-sectional specimens were prepared by focused-ion-beam milling using a JEOL JIB-4700F. We used high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and energy-dispersive X-ray spectroscopy (EDS) to examine the spatial distributions of Bi, Se, O, Ti, and Au across the fluorinated heterostructures.

Raman spectroscopy in Extended Data Fig. 2c,d was performed using a WITec Alpha 300 RA+ system with a continuous-wave excitation laser with a wavelength of 532 nm and a power of 10 μW. Raman

mapping was used to compare pristine and plasma-treated regions and to monitor the characteristic Bi_2Se_3 phonon modes.

X-ray photoelectron spectroscopy (XPS) in Extended Data Fig. 2e–h was performed using a Kratos Axis Ultra system equipped with a monochromatic Al Kα X-ray source with an energy of 1486.96 eV. The analysed area was $\sim 0.3 \times 0.7$ mm^2. We acquired high-resolution spectra using a pass energy of 20 eV, an energy step of 0.1 eV, and an X-ray spot size of $\sim$200 μm. Because the finite escape depth of the emitted photoelectrons limits the information depth of XPS, the measured spectra predominantly probe the near-surface chemical composition. This surface sensitivity enables characterization of the chemical changes induced by SF_6 fluorination.

Optical microscopy, AFM, and Raman measurements were performed under ambient laboratory conditions unless otherwise noted. TEM/STEM and XPS measurements were performed under the vacuum conditions intrinsic to the corresponding instruments.

4.9 Electrical Measurements and Parameter Extraction

Electrical measurements were performed at room temperature using a Keithley 2636B source-measure unit for current–voltage measurements and a Keysight E4980A inductance–capacitance–resistance (LCR) meter for capacitance and conductance measurements. Devices were measured using electrical probes or wire-bonded sample holders, as appropriate. Transistor characteristics were measured in the dark to suppress photoinduced current. All measurements were performed in ambient air.

For the transfer-length-method (TLM) analysis in Extended Data Fig. 3i–m, the total two-terminal resistance was obtained from the linear low-bias I–V response and fitted as

$$R_{\mathrm{T}} = 2R_{\mathrm{C}} + R_{\mathrm{Sh}}\frac{L_{\mathrm{X}}}{W},$$

where R_{C} is the contact resistance per contact, R_{Sh} is the channel sheet resistance, L_{X} is the electrode spacing, and W is the channel width. R_{C} was obtained from one half of the fitted zero-length intercept, and R_{Sh} was obtained from the fitted slope after accounting for the measured channel width.

For the MIM capacitors in Fig. 3f,g, capacitance–voltage measurements were performed at 1 MHz using an alternating-current (AC) excitation amplitude of 0.05 V. All capacitances reported in the main text were normalized by the active capacitor area. For the Al_2O_3-capped polycrystalline structures, the independently measured Al_2O_3 capacitance was de-embedded according to

$$\frac{1}{C_{\mathrm{total}}} = \frac{1}{C_{\mathrm{Al_2O_3}}} + \frac{1}{C_X},$$

where $C_X = C_{\mathrm{BiF_3}}$ for the fully converted BiF_3-only structure and $C_X = C_{\mathrm{TIHGS}}$ for the partially converted TIHGS structure. The BiF_3 relative permittivity was calculated using

$$C_{\mathrm{BiF_3}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{BiF_3}}}{t_{\mathrm{BiF_3}}},$$

where $t_{\mathrm{BiF_3}}$ is the independently determined physical thickness of the BiF_3 layer. For the BiF_3-only (p20) reference, AFM yielded $t_{\mathrm{BiF_3}} \approx 23$ nm, which was used to extract a mean $\varepsilon_{\mathrm{BiF_3}}$ of 28.65 and a median value of 30.16. For TIHGS structures, the BiF_3-thickness-normalized effective relative permittivity was defined as

$$\varepsilon_{\mathrm{eff,TIHGS}} = \frac{C_{\mathrm{TIHGS}} t_{\mathrm{BiF_3}}}{\varepsilon_0}.$$

The electrically conducting residual Bi_2Se_3 was not included in the geometric dielectric thickness. The effective interfacial quantum capacitance was obtained using

$$\frac{1}{C_{\mathrm{TIHGS}}} = \frac{1}{C_{\mathrm{BiF_3}}} + \frac{1}{C_Q}.$$

Accordingly, C_Q is treated as an effective interfacial electronic-compressibility response rather than as an intrinsic dielectric capacitance or a universal material constant.

Frequency-dependent capacitance and loss measurements shown in Extended Data Fig. 5c–e were performed from 1 kHz to 1 MHz using a direct-current (DC) bias of 0.1 V and an AC excitation amplitude

of 0.05 V. The current-density–voltage measurement and corresponding field-dependent transport analyses shown in Extended Data Fig. 6a–c were obtained using the Keithley 2636B. For the TIHGS MIM leakage measurements, the bias voltage was applied to the top Au electrode in direct contact with BiF_3, while the bottom Au/Ti electrode electrically coupled to the residual Bi_2Se_3 was grounded. Under positive top-electrode bias ($V > 0$), electron injection therefore occurs from the residual Bi_2Se_3 side across the buried BiF_3/Bi_2Se_3 interface into BiF_3. For field-dependent leakage analysis, the electric field was calculated as $E = |V|/t_{BiF_3}$, using only the physical thickness of the insulating BiF_3 layer.

For the WSe_2/TIHGS MISCAP characterized in Extended Data Fig. 7, capacitance–voltage and parallel-conductance characteristics were measured from 10 kHz to 1 MHz over the gate-voltage range $-1\ \mathrm{V} \le V_G \le 1\ \mathrm{V}$ using an AC excitation amplitude of 0.05 V. The flat-band condition was extracted from the 10-kHz capacitance characteristic because the accumulation-to-depletion transition remained within the accessible low-leakage gate-voltage range at this frequency. The flat-band voltage was identified from the zero crossing of $\mathrm{d}^2C/\mathrm{d}V_G^2$ associated with the principal accumulation–depletion inflection. The graphical consistency analysis used to extract $\varepsilon_{\mathrm{eff,TIHGS}}$, together with the subsequent extraction of C_{TIHGS}, effective semiconductor screening length $L_{\mathrm{D,eff}}$, and apparent majority-carrier concentration N_{app}, is described in Supplementary Note 4. The effective electrically active trap density, $D_{\mathrm{it,eff}}$, was obtained using the 10-kHz/1-MHz high–low-frequency capacitance method described in Supplementary Note 7. The extracted electrostatic parameters are summarized in Extended Data Table 2. Because the 10-kHz characteristic is not a true quasi-static limit and an independently resolved frequency-dependent TIHGS capacitance was not available, $D_{\mathrm{it,eff}}$ is interpreted as an effective electrically active trap response sampled within the experimental frequency window rather than as a unique microscopic density of states exclusively at the WSe_2/BiF_3 interface.

For the MoS_2 field-effect transistors (FETs) characterized in Fig. 4 and Extended Data Fig. 8, output characteristics were measured over $0 \le V_{DS} \le 1.0$ V, where V_{DS} is the drain–source voltage, at gate–source voltages $-0.3\ \mathrm{V} \le V_{GS} \le 0.5$ V. Transfer characteristics were measured over $-0.5\ \mathrm{V} \le V_{GS} \le 0.5$ V at $0.1\ \mathrm{V} \le V_{DS} \le 1.0$ V. Forward and reverse gate-voltage sweeps were measured under otherwise identical bias conditions, while the gate-leakage current was recorded simultaneously with the drain current.

The local subthreshold swing was calculated from

$$SS = \left(\frac{\mathrm{d} \log_{10} I_D}{\mathrm{d}V_{GS}} \right)^{-1},$$

using the measured transfer characteristics, and the minimum SS within the experimentally resolved subthreshold regime is reported unless otherwise stated. No smoothing was applied to the transfer characteristics before SS extraction.

Threshold voltage (V_{th}) was extracted by linearly extrapolating the I_D–V_{GS} characteristic from the point of maximum transconductance to $I_D = 0$. We applied the same extraction procedure at $V_{DS} = 0.1$ and 1.0 V. Drain-induced barrier lowering was calculated as

$$DIBL = -\frac{V_{\mathrm{th}}(V_{DS} = 1.0\ \mathrm{V}) - V_{\mathrm{th}}(V_{DS} = 0.1\ \mathrm{V})}{1.0\ \mathrm{V} - 0.1\ \mathrm{V}},$$

and is reported in units of $\mathrm{mV\ V^{-1}}$.

We defined the hysteresis window as the difference in threshold voltage between the forward and reverse sweeps, with a gate-voltage step size of 0.01 V at an effective sweep rate of 7.7 $\mathrm{mV\ s^{-1}}$ for the forward and reverse measurements. The same definition was used when comparing the TIHGS-gated, BiF_3-gated, and BiO_x/Bi_2Se_3-gated devices.

For the device-to-device comparison in Extended Data Fig. 8h, the minimum SS of each device was extracted from the transfer characteristic measured at $V_{DS} = 0.1$ V using the same local-derivative procedure described above. The gate-leakage metric was defined as the magnitude of the simultaneously measured gate current, $|I_G|$, at the maximum applied gate voltage $V_{GS} = 0.5$ V and $V_{DS} = 0.1$ V, normalized by the corresponding channel width. Three separate devices were evaluated for each gate-stack configuration ($n = 3$ for TIHGS-, BiF_3-, and BiO_x/Bi_2Se_3-gated devices).

4.10 Statistics and Reproducibility

No inferential statistical hypothesis tests were applied. For the MIM-capacitor statistics in Fig. 3f,g, the sample sizes were $n = 25$, 33, 24, and 5 independent capacitors for BiF_3-only (p20), TIHGS-13 (p20), TIHGS-43 (p50), and TIHGS-43 (cN), respectively. The Al_2O_3 reference in Extended Data Fig. 5a,b comprised $n = 75$ independent capacitors. For the device-to-device transistor comparison in Extended Data Fig. 8h, three independent devices were evaluated for each gate-stack configuration ($n = 3$). Mean and median values are reported where indicated.

Data Availability

The data supporting the findings of this study are provided with the Article and its Source Data files. Additional raw data are available in [repository name] at [repository DOI].

Code Availability

No custom code central to the conclusions of this study was developed.

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Author Information

Contributions. M.S., J.K., M.G.U., and W.K. contributed equally to this work. H.H.Y. conceived the ideas and designed the experiments. S.H.C., H.-J.S., C.-H.L., M.C., S.B.C., Z.S., K.P., and H.H.Y. proposed theoretical interpretations. H.U.L., D.W.J., and S.B.C. performed DFT calculations and SRIM simulations. S.A.T. provided high-quality Bi_2Se_3, MoS_2, WSe_2, and h-BN crystals. D.H.L. and W.S. offered wafer-scale Bi_2Se_3 films. M.S., M.G.U., W.K., J.P., X.C., and H.H.Y. developed and optimized the SF_6/Ar plasma process for controlled surface conversion of Bi_2Se_3 into BiF_3. M.S., M.G.U., W.K., J.P., D.L., G.J., S.M., and H.H.Y. fabricated the devices. L.Y. obtained TEM images. J.L. carried out XPS. M.S., W.K., J.P., S.C., K.S.K., Z.S., and H.H.Y. characterized the devices using TEM, HAADF-STEM, EDS, AFM, Raman, and XPS datasets. M.S., J.K., W.K., J.P., K.P., and H.H.Y. performed the electrical measurements. G.J., S.M., Y.T.M., and X.C. helped with the electrical measurements. Y.D., S.H.C., K.S.K., D.-H.K., H.-J.S., W.S., S.A.T., C.-H.L., M.C., S.B.C., Z.S., and K.P. commented on

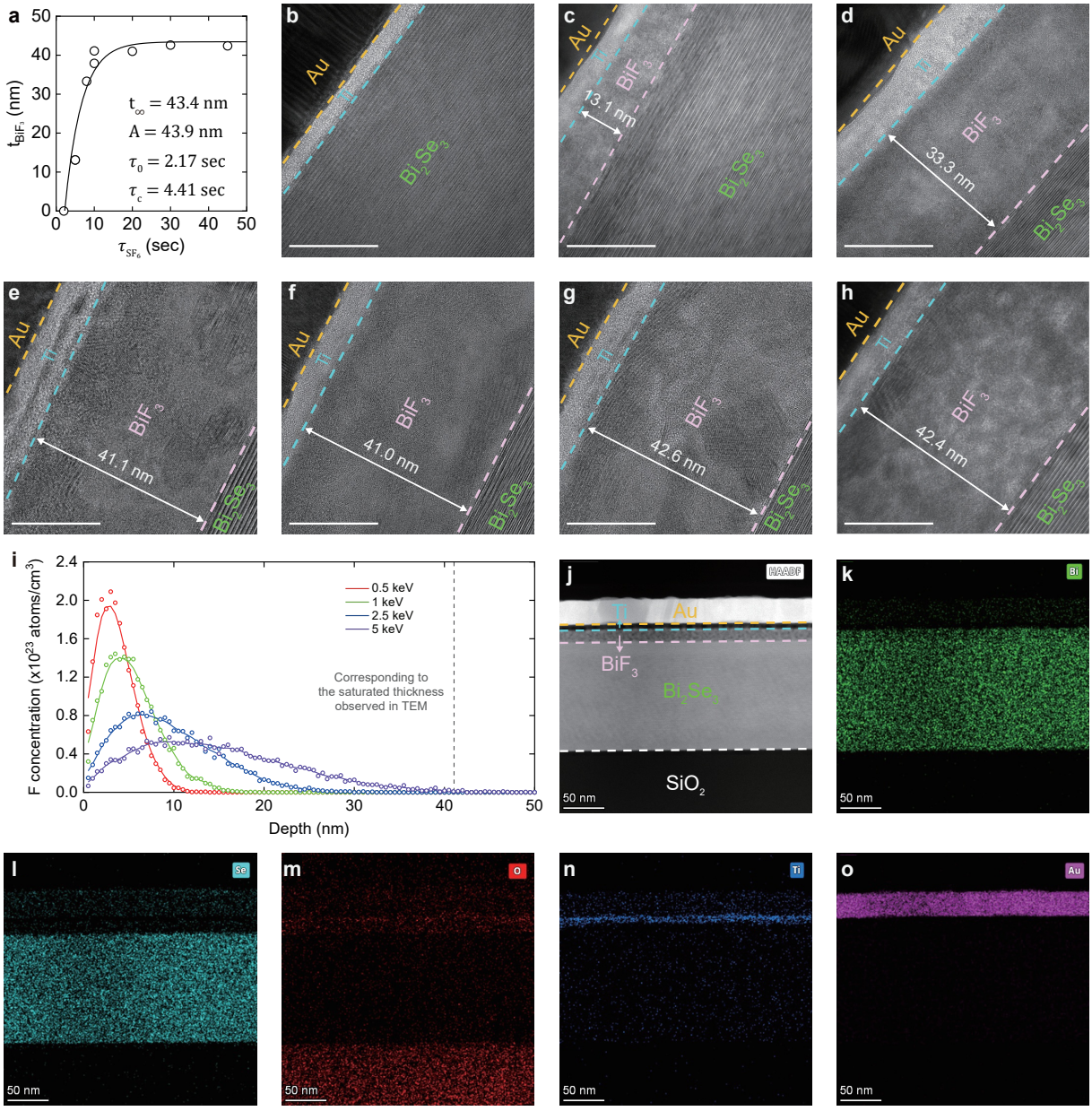
the experimental results and assisted with the data analysis. Y.D., D.-H.K., H.-J.S., M.C., S.B.C., Z.S., and K.P. suggested insights for organizing the data. H.H.Y. wrote the manuscript. S.B.C., Z.S., K.P., and H.H.Y. supervised the research. All authors participated extensively in the scientific discussion and contributed to the manuscript.

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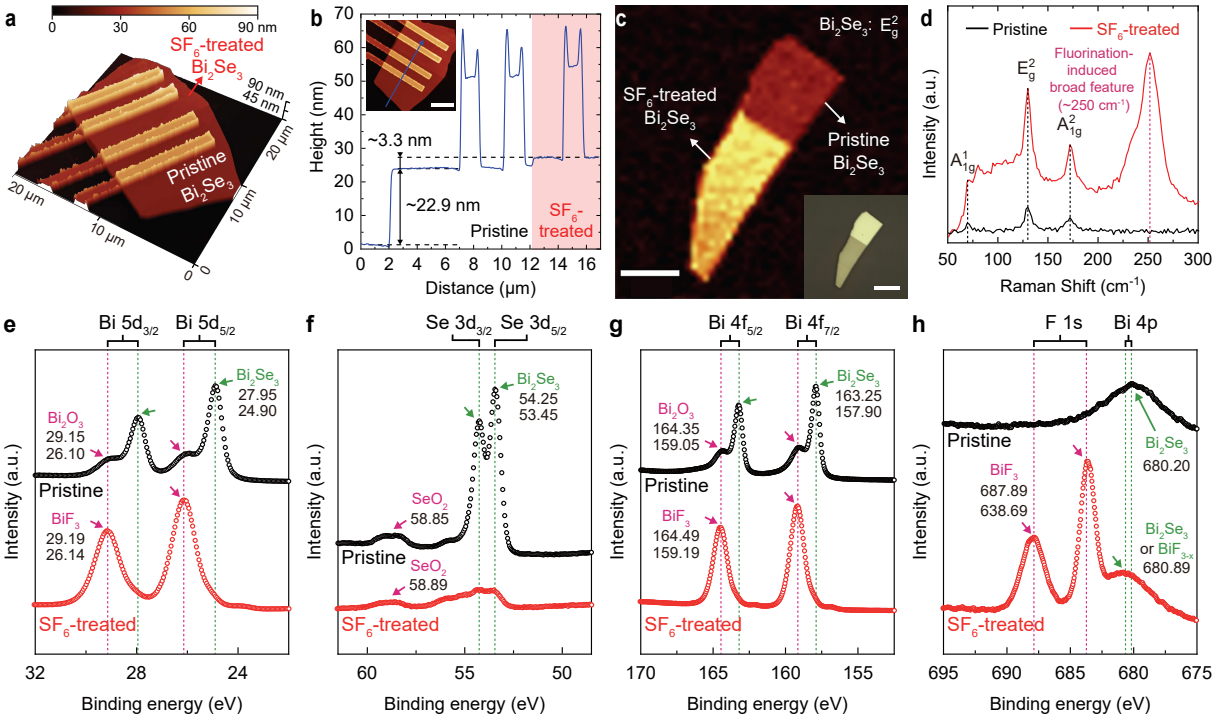
Ethics Declarations

Competing interests. The authors declare no competing interests.

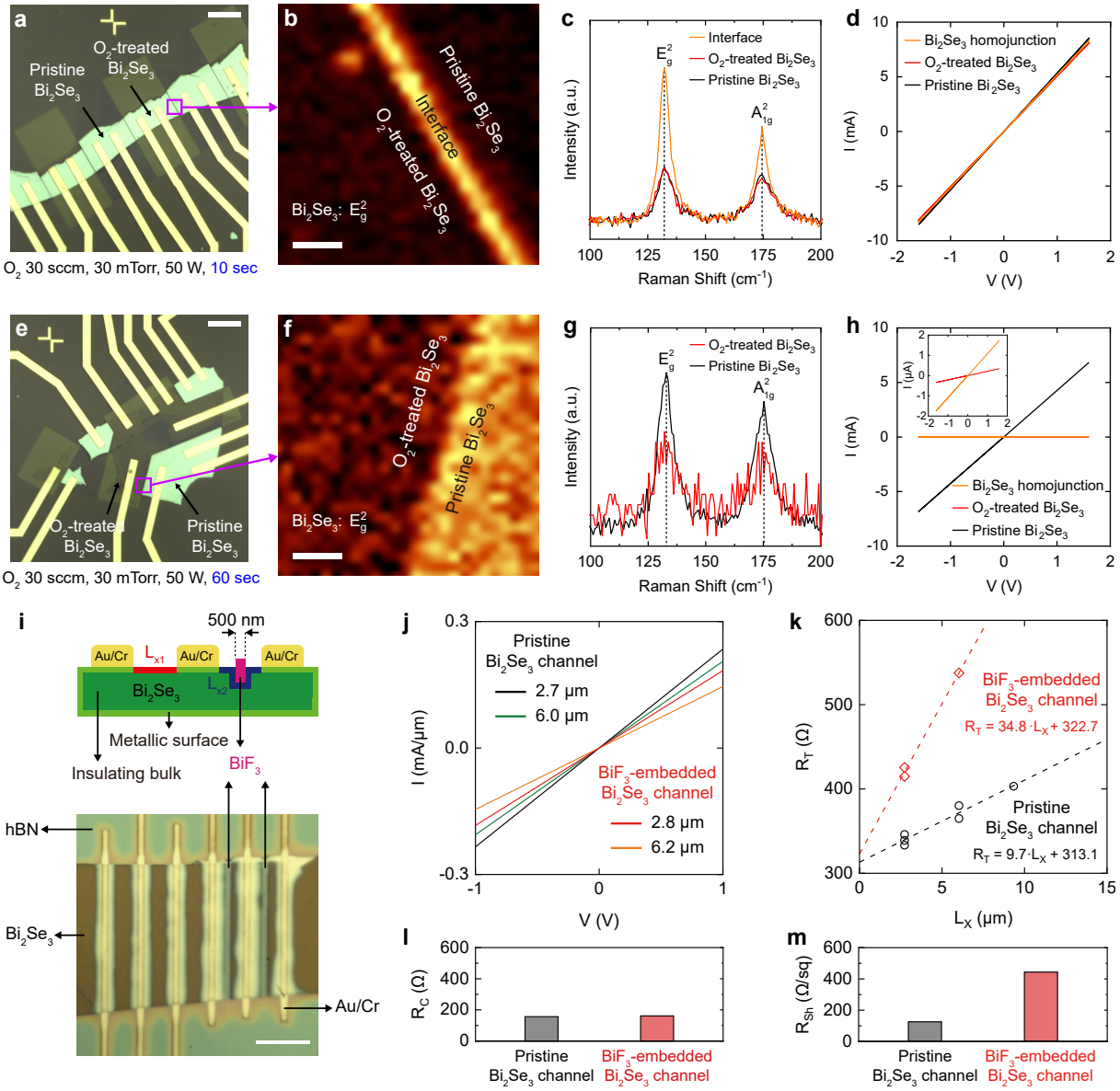
Extended Data Figures and Tables



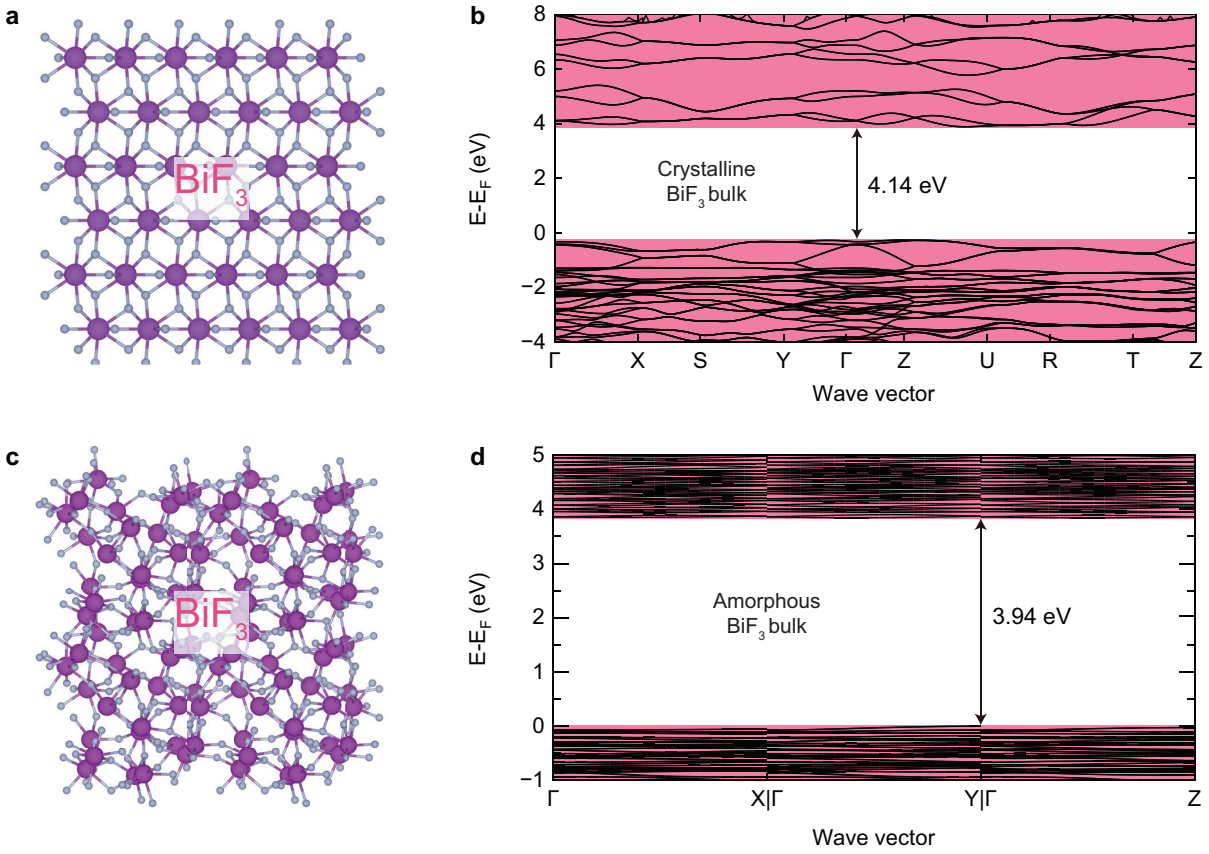
Extended Data Fig. 1 Self-limited surface conversion and fluorine-penetration length scale. a, Converted BiF_3 thickness (t_{BiF_3}) as a function of SF_6 plasma-treatment time (τ_{SF_6}). The line is an empirical saturating-exponential fit used to parameterize the observed approach to a limiting thickness; the fitted time constant is not assigned a unique microscopic kinetic meaning. **b**–**h**, Cross-sectional transmission electron microscopy (TEM) images after plasma exposure for 2, 5, 8, 10, 20, 30 and 45 s, respectively. Scale bars, 20 nm. **i**, Fluorine depth distributions in Bi_2Se_3 calculated using Stopping and Range of Ions in Matter (SRIM) simulations for assumed F^+ incident energies of 0.5, 1, 2.5 and 5 keV. The dashed line marks the experimentally observed ~40–43-nm saturation scale. The 5-keV case is included as a deliberately high-energy upper-bound calculation; the simulations constrain an accessible ballistic penetration length scale and do not represent the measured plasma ion-energy distribution or fluorination kinetics. **j**–**o**, High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image **(j)** and corresponding energy-dispersive X-ray spectroscopy (EDS) elemental maps of Bi **(k)**, Se **(l)**, O **(m)**, Ti **(n)** and Au **(o)**. Se is concentrated predominantly in the residual Bi_2Se_3, whereas the converted region remains Bi-containing. Scale bars, 50 nm.



Extended Data Fig. 2 Spatially selective conversion of Bi_2Se_3 into BiF_3. a,b, Atomic force microscopy (AFM) topography across pristine and SF_6-treated Bi_2Se_3 regions **(a)** and corresponding line-height profile **(b)**, showing a surface-height increase of ∼3.3 nm after fluorination. The difference between the converted-layer thickness (∼13.1 nm), independently determined by cross-sectional TEM under the same 5-s treatment condition, and the measured surface-height increase (∼3.3 nm) indicates that the converted layer cannot be explained by additive deposition and is consistent with consumption and volumetric expansion of the underlying Bi_2Se_3. Scale bar of inset in **b**, 5 μm. **c**, Raman map of the Bi_2Se_3 E_g^2 mode across pristine and treated regions; inset, corresponding optical micrograph. Scale bar, 7 μm; inset scale bar, 10 μm. **d**, Raman spectra showing the characteristic Bi_2Se_3 modes and an additional broad feature near 250 cm^{-1} after fluorination. **e–h**, X-ray photoelectron spectroscopy (XPS) of pristine and treated Bi_2Se_3: Bi 5d **(e)**, Se 3d **(f)**, Bi 4f **(g)**, and F 1s/Bi 4p **(h)**. Fluorination suppresses the Bi_2Se_3-derived Bi and Se components, introduces Bi–F components in the Bi spectra, and produces an F 1s feature near 687.9 eV, supporting formation of a fluorinated Bi-containing surface phase.



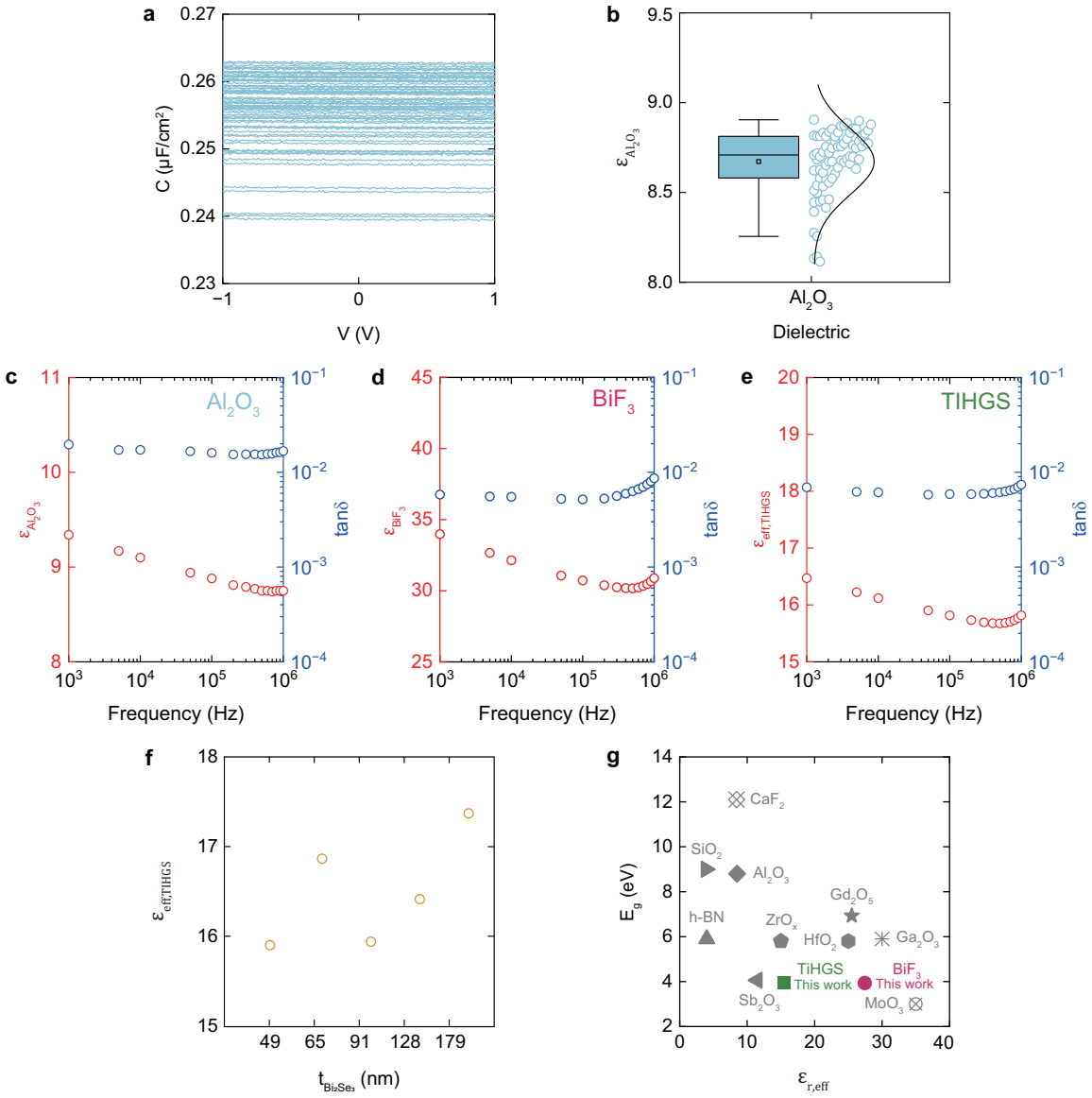
Extended Data Fig. 3 O_2-plasma control and quantitative buried conduction in Bi_2Se_3. a–d, Bi_2Se_3 after 10 s of O_2-plasma treatment: optical micrograph **(a)**, Raman map of the E_g^2 mode **(b)**, Raman spectra from pristine, treated, and interfacial regions **(c)**, and current–voltage (I–V) characteristics of pristine, treated, and lateral pristine/treated structures **(d)**. Scale bars, 50 μm in **a** and 1 μm in **b**. **e–h**, Corresponding measurements after 60 s of O_2-plasma treatment: optical micrograph **(e)**, Raman map **(f)**, Raman spectra **(g)**, and I–V characteristics **(h)**. The treated region remains conductive, unlike after SF_6 fluorination. Scale bars, 50 μm in **e** and 1 μm in **f**. O_2-plasma treatment was performed at 30 sccm, 30 mTorr, and 50 W. **i–m**, Transfer-length-method (TLM) analysis of conduction through residual Bi_2Se_3 beneath a locally converted BiF_3 region. **i**, Schematic and optical micrograph of the TLM geometry containing a ~500-nm-wide converted region; scale bar, 5 μm. **j**, Representative I–V characteristics. **k**, Total resistance versus channel length, with linear fits $R_T = 9.7L_X + 313.1$ and $R_T = 34.8L_X + 322.7$ for pristine and converted structures, respectively. **l,m**, Extracted contact resistance and sheet resistance. The contact resistance remains ~157–161 Ω, whereas the sheet resistance increases by ~3.5-fold after local conversion.



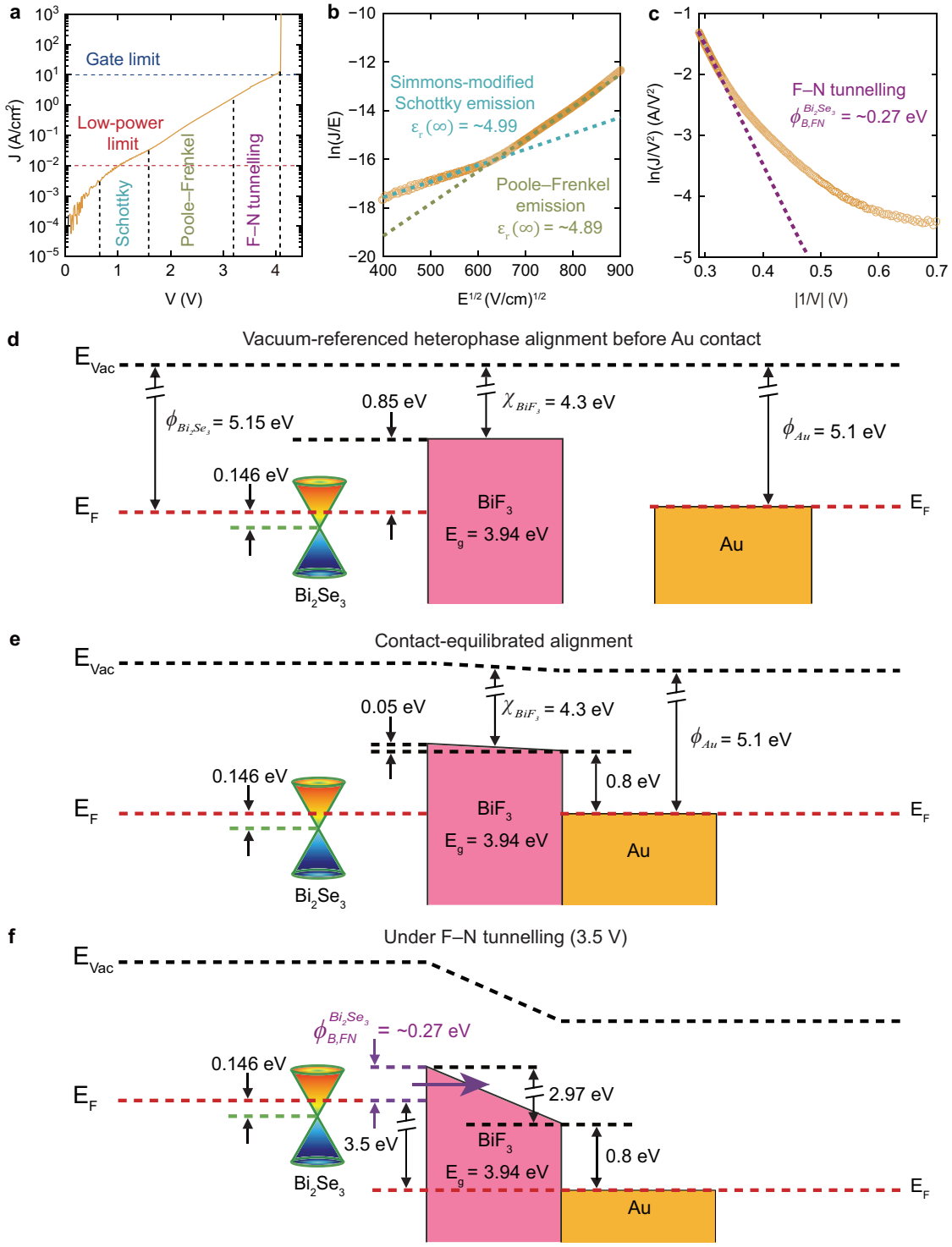
Extended Data Fig. 4 Calculated electronic band structures of crystalline and amorphous BiF_3. **a**, Structural model of crystalline BiF_3. **b**, Calculated electronic band structure of crystalline BiF_3 along the Γ–X–S–Y–Γ–Z–U–R–T–Z high-symmetry path, showing an insulating band gap of 4.14 eV. **c**, Structural model of amorphous BiF_3. **d**, Calculated electronic band structure of amorphous BiF_3 along the Γ–X, Γ–Y, and Γ–Z reciprocal-space directions, showing an insulating band gap of 3.94 eV. Energies in **b** and **d** are plotted relative to the calculated Fermi level (E_F).

Extended Data Table 1 Calculated band gaps and dielectric properties of Bi_2Se_3, BiF_3, and Bi_2O_3 in crystalline and amorphous phases. The static relative permittivity [$\varepsilon_r(0)$] includes both electronic and ionic contributions, whereas the high-frequency relative permittivity [$\varepsilon_r(\infty)$] represents the ion-clamped electronic contribution. The refractive index (n) was calculated from the averaged $\varepsilon_r(\infty)$. Stoichiometric Bi_2O_3 is included only as a theoretical reference for the oxidized BiO_x phase in the BiO_x/Bi_2Se_3 control gate stack demonstrated in Extended Data Fig. 8.

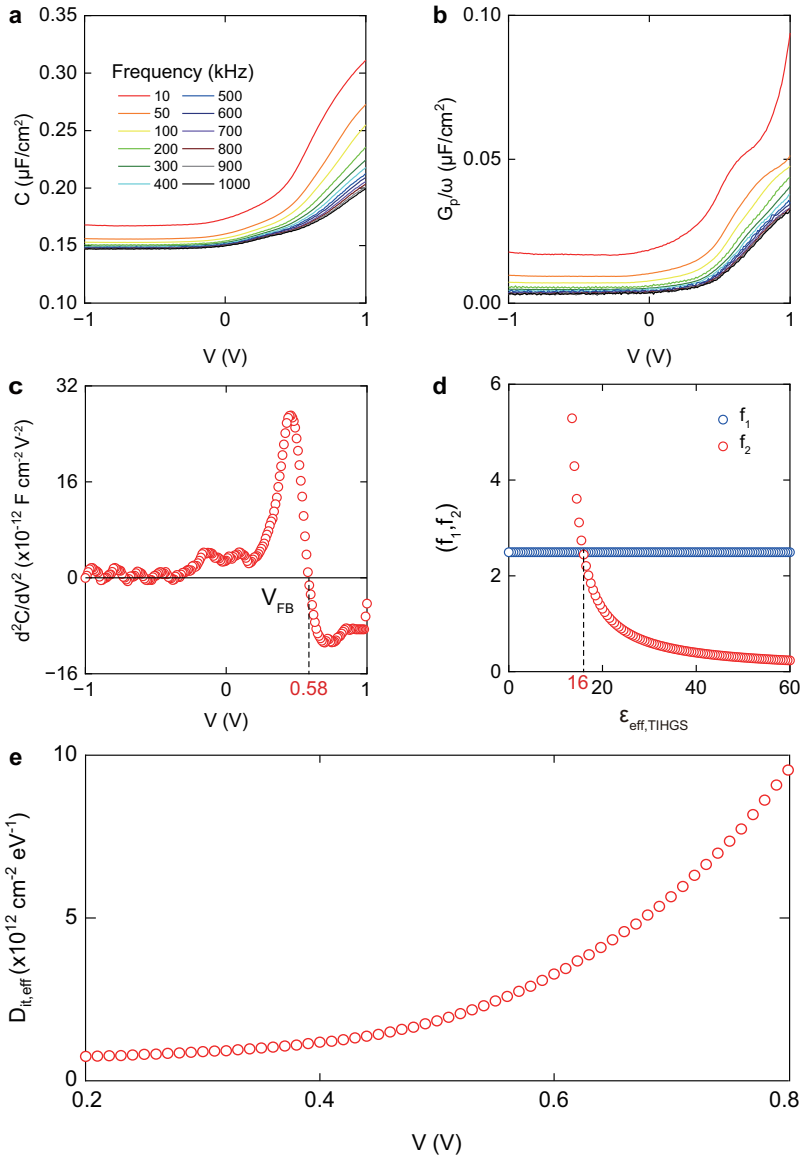
Phase	Material	Band gap (eV)	Relative permittivity		n
			$\varepsilon_r(0)$	$\varepsilon_r(\infty)$	
Crystalline	Bi_2Se_3	0.310	38.057	37.851	6.152
Amorphous	Bi_2Se_3	0.777	42.715	13.329	3.651
Crystalline	BiF_3	4.140	29.385	3.227	1.796
Amorphous	BiF_3	3.936	25.311	4.056	2.014
Crystalline	Bi_2O_3	2.038	32.023	6.110	2.472
Amorphous	Bi_2O_3	2.096	34.938	6.118	2.473



Extended Data Fig. 5 Reference dielectric response, thickness dependence and dielectric-property context of TIHGS electrostatics. a, Capacitance–voltage (C–V) characteristics of Au/Ag/Pt/Al_2O_3/Au/Ti MIM reference capacitors measured at 1 MHz with a 0.05-V AC excitation (n = 75). **b**, Distribution of the extracted Al_2O_3 relative permittivity; mean and median values are 8.67 and 8.71. This reference response was used to de-embed the Al_2O_3 series contribution from the polycrystalline capacitor structures in Fig. 3f,g. **c**–**e**, Frequency-dependent relative permittivity and loss tangent ($\tan\delta$) of 30-nm Al_2O_3 **(c)**, 30-nm Al_2O_3/23-nm BiF_3-only (p20) **(d)**, and 30-nm Al_2O_3/TIHGS-43 (p50) **(e)**. **f**, Effective relative permittivity $\varepsilon_{\mathrm{eff,TIHGS}}$ of TIHGS-43 (cN) versus nominal starting c-Bi_2Se_3 thickness. $\varepsilon_{\mathrm{eff,TIHGS}}$ remains ∼15.9–17.4 as the starting thickness varies from ∼49 to ∼179 nm, without systematic thickness dependence. **g**, Relative permittivity versus band gap (E_g) for BiF_3, the TIHGS and representative gate dielectrics [5]. For the TIHGS, the ordinate is the BiF_3-thickness-normalized stack response $\varepsilon_{\mathrm{eff,TIHGS}}$ and the abscissa is the amorphous-BiF_3 band gap; the marker therefore provides dielectric-property context rather than an intrinsic material dielectric constant or EOT advantage.



Extended Data Fig. 6 Field-assisted leakage and band alignment of the TIHGS MIM capacitor. a, Current-density–voltage (J–V) characteristic of an Au/BiF_3/Bi_2Se_3/Au/Ti TIHGS MIM capacitor, with the low-power operating range and higher-field transport regimes indicated. **b**, Simmons-modified Schottky and Poole–Frenkel representations, yielding effective high-frequency relative permittivities of ∼4.99 and ∼4.89, respectively. **c**, Fowler–Nordheim representation of the high-field regime; the linear region gives a model-dependent effective injection barrier $\Phi_{B,FN} \approx 0.27$ eV. **d**, Vacuum-referenced heterophase alignment before Au contact, constructed from $\phi_{Bi_2Se_3} = 5.15$ eV and $\chi_{BiF_3} = 4.3$ eV, giving a nominal 0.85-eV separation. The reconstructed Bi_2Se_3-derived feature is shown ∼0.146 eV below E_F. This reference construction does not independently resolve interface dipoles, chemical reconstruction or band bending. **e**, Contact-equilibrated schematic after Au contact. With $\phi_{Au} = 5.1$ eV, the Au/Bi_2Se_3 work-function difference is ∼0.05 eV and the vacuum-referenced Au/BiF_3 separation ∼0.8 eV; these values are not interpreted as independently measured equilibrium band offsets. **f**, High-field band profile at $V = 3.5$ V. Barrier tilting enables tunnelling towards BiF_3 conduction-band states, with the Fowler–Nordheim slope yielding an effective Bi_2Se_3-to-BiF_3 injection barrier of ∼0.27 eV.



Extended Data Fig. 7 Semiconductor-integrated electrostatics of a WSe_2/TIHGS MISCAP. a, Capacitance–voltage (C–V) characteristics of an Au/Ag/Pt/WSe_2/BiF_3/Bi_2Se_3/Au/Ti MISCAP measured from 10 kHz to 1 MHz over the gate-voltage range -1 V $\leq V_G \leq 1$ V using an AC excitation amplitude of 0.05 V. **b**, Corresponding parallel-conductance response, G_p/ω, as a function of gate voltage at different measurement frequencies. No well-resolved G_p/ω maximum suitable for conventional conductance-method extraction is observed within the accessible low-leakage bias window. **c**, Second derivative of the 10-kHz C–V characteristic used to determine the flat-band voltage. The physically relevant zero crossing associated with the principal accumulation-to-depletion inflection gives $V_{FB} \approx 0.58$ V. At higher frequencies, the corresponding transition extends beyond the accessible low-leakage bias range and is therefore not used for flat-band extraction. **d**, Graphical consistency analysis of the TIHGS response at the independently determined V_{FB}. The experimentally determined function f_1 is compared with f_2 calculated as a function of trial $\varepsilon_{eff,TIHGS}$, with the intersection yielding $\varepsilon_{eff,TIHGS} \approx 16$. **e**, Effective electrically active trap density ($D_{it,eff}$) obtained from the 10-kHz and 1-MHz C–V characteristics using the high–low-frequency capacitance method. Quantitative interpretation is restricted to the bias-dependent depletion-to-accumulation transition, excluding the nearly gate-voltage-independent depletion floor and strong-accumulation regimes. The minimum value within the selected analysis range is $\sim 7.48 \times 10^{11}$ cm^{-2} eV^{-1}.

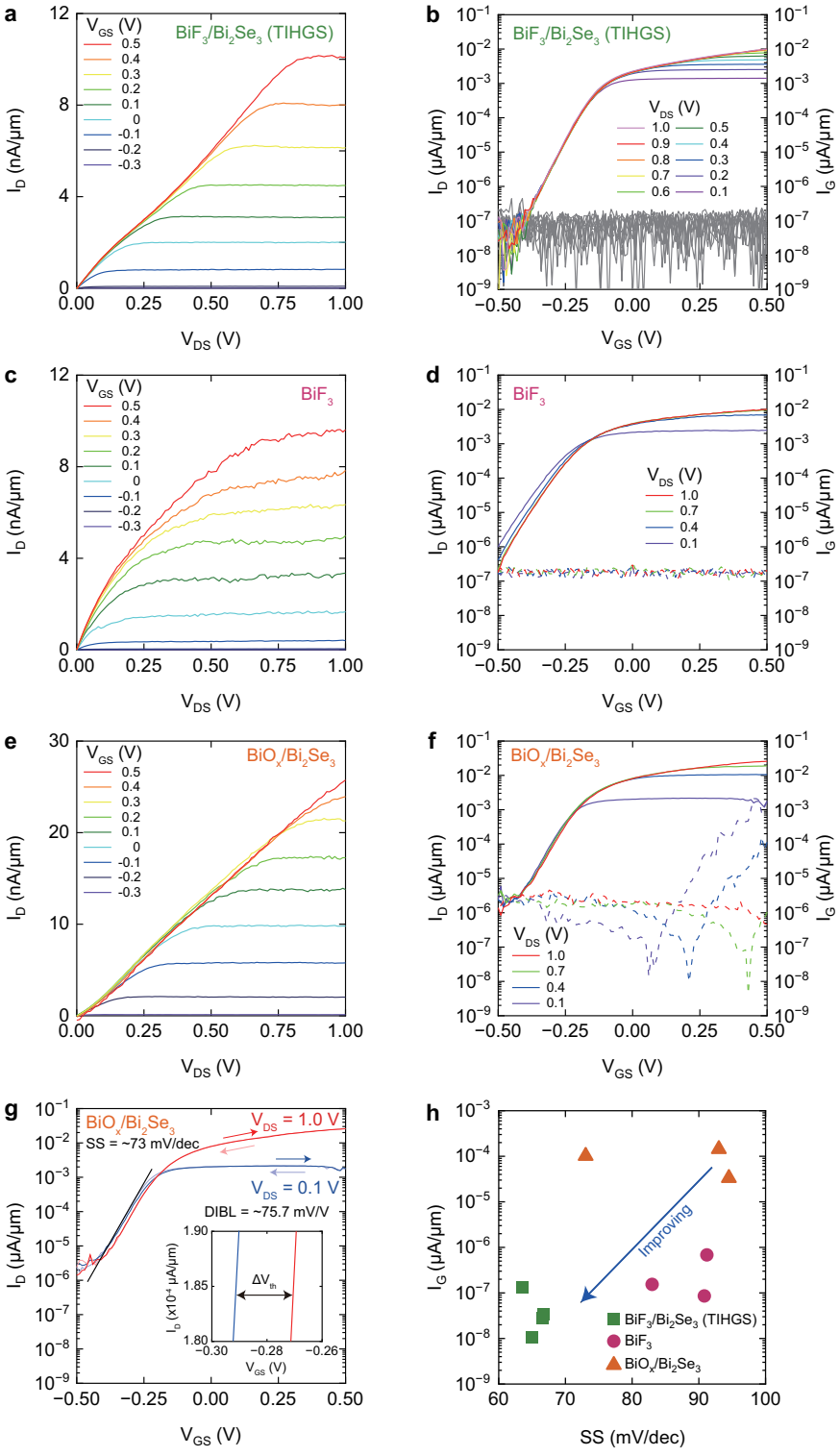
Extended Data Table 2 Electrostatic response of BiF_3 and TIHGS structures and parameters extracted from the WSe_2/TIHGS MISCAP. a, Experimentally extracted dielectric response of BiF_3 and TIHGS capacitor structures. For TIHGS structures, $\varepsilon_{\mathrm{eff,TIHGS}}$ denotes the BiF_3-thickness-normalized effective relative permittivity of the complete BiF_3/Bi_2Se_3 electrostatic boundary system and should not be interpreted as the intrinsic dielectric constant of BiF_3. For the fully converted BiF_3-only (p20) reference, $\varepsilon_{\mathrm{BiF_3}}$ was extracted using the independently measured post-conversion BiF_3 thickness of ∼23 nm. TIHGS-13 and TIHGS-43 denote structures containing ∼13- and ∼43-nm-thick converted BiF_3 layers, respectively; p20 and p50 denote nominal starting polycrystalline Bi_2Se_3 thicknesses of 20 and 50 nm, respectively; and cN denotes crystalline Bi_2Se_3 with nominal starting thickness N. **b**, Electrostatic parameters extracted from the Au/Ag/Pt/WSe_2/BiF_3/Bi_2Se_3/Au/Ti MISCAP. Flat-band quantities were obtained from the 10-kHz C–V characteristic. C_{g} denotes the effective TIHGS capacitance corresponding to $\varepsilon_{\mathrm{eff,TIHGS}} \approx 16$ and a ∼43-nm-thick converted BiF_3 layer. $L_{\mathrm{D,eff}}$ and N_{app} denote the effective semiconductor screening length and apparent majority-carrier concentration, respectively, evaluated using $\varepsilon_{\perp,\mathrm{WSe_2}} = 4.2$, as adopted in continuum electrostatic modelling of bulk-like WSe_2 flakes [38]. $D_{\mathrm{it,eff}}^{\mathrm{min}}$ denotes the minimum effective electrically active trap density extracted from the 10-kHz/1-MHz high–low-frequency analysis within the selected bias-dependent transition region. Detailed extraction procedures and limitations are provided in Supplementary Notes 6 and 7.

a, Dielectric response of BiF_3 and TIHGS

Structure	Sample configuration	Electrostatic quantity	Value
Crystalline TIHGS MIM	TIHGS-43 (cN) N = 49, 65, 91, 128, or 179 nm	Mean $\varepsilon_{\mathrm{eff,TIHGS}}$	**16.50**
		Median $\varepsilon_{\mathrm{eff,TIHGS}}$	**16.41**
WSe_2/TIHGS MISCAP	Au/Ag/Pt/WSe_2/a-BiF_3/ c-Bi_2Se_3/Au/Ti (∼43-nm converted BiF_3)	$\varepsilon_{\mathrm{eff,TIHGS}}$	**∼16**
Polycrystalline TIHGS MIM	TIHGS-13 (p20)	Mean $\varepsilon_{\mathrm{eff,TIHGS}}$	**16.12**
		Median $\varepsilon_{\mathrm{eff,TIHGS}}$	**16.10**
	TIHGS-43 (p50)	Mean $\varepsilon_{\mathrm{eff,TIHGS}}$	**14.83**
		Median $\varepsilon_{\mathrm{eff,TIHGS}}$	**14.72**
Fully converted BiF_3-only MIM	BiF_3-only (p20) ($t_{\mathrm{BiF_3}} \approx 23$ nm)	Mean $\varepsilon_{\mathrm{BiF_3}}$	**28.65**
		Median $\varepsilon_{\mathrm{BiF_3}}$	**30.16**

b, Electrostatic parameters extracted from the WSe_2/TIHGS MISCAP

$t_{\mathrm{WSe_2}}$ (nm)	V_{FB} (V)	C_{FB} (10^{-7} F cm^{-2})	C_{g} (10^{-7} F cm^{-2})	$L_{\mathrm{D,eff}}$ (nm)	N_{app} (10^{17} cm^{-3})	$D_{\mathrm{it,eff}}^{\mathrm{min}}$ (10^{11} cm^{-2} eV^{-1})
37.37	0.58	2.34	3.29	4.60	2.83	7.48



Extended Data Fig. 8 Extended transistor characteristics, control devices and device-to-device comparison. **a,b**, Output characteristics **(a)** and drain-bias-dependent transfer characteristics **(b)** of the TIHGS-gated MoS_2 FET. Gate leakage remains below the drain current throughout the switching range. **c,d**, Corresponding characteristics of the BiF_3-gated control FET. **e**–**g**, Characteristics of the air-oxidized BiO_x/Bi_2Se_3-gated MoS_2 control. **e**, Transfer characteristics at $V_{DS} = 0.1$ and 1.0 V, showing a minimum SS of ~ 73 mV dec^{-1}, an on–off current ratio of $\sim 10^4$ and $DIBL \approx 75.7$ mV V^{-1}. **f**, Drain-bias-dependent transfer characteristics with simultaneously measured gate leakage. **g**, Output characteristics. **h**, Device-to-device comparison of minimum SS and gate-leakage current per unit channel width for TIHGS-, BiF_3-, and BiO_x/Bi_2Se_3-gated devices. Gate leakage was evaluated at $V_{GS} = 0.5$ V and $V_{DS} = 0.1$ V; each marker represents one device ($n = 3$ per gate-stack configuration).

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