

Fault-Tolerant Fractional Control and Active Reconfiguration of Redundant Interleaved DC–DC Converters for UAV and Avionic DC Networks

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Research Article

Keywords: fault-tolerant control, fractional-order control, interleaved buck converter, UAV power system, more-electric aircraft, open-circuit fault, sensor fault, active reconfiguration, survivability

Posted Date: September 23rd, 2026

DOI: <https://doi.org/10.21203/rs.3.rs-11088802/v1>

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Additional Declarations: The authors declare no competing interests.

Fault-Tolerant Fractional Control and Active Reconfiguration of Redundant Interleaved DC–DC Converters for UAV and Avionic DC Networks

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Abstract

Fault tolerance in airborne DC power conversion is not only a component-level reliability problem; it is also a transient-energy problem because a fault must be detected, classified, isolated, and compensated before the protected bus leaves its admissible voltage region. This paper develops a mathematically explicit fault-tolerant architecture for a three-active-plus-one-spare interleaved buck converter representative of a 270 V-to-28 V UAV/avionic DC interface. The proposed framework combines four layers that are commonly investigated separately: an averaged multiphase converter model, model-based open-circuit fault residuals, Kirchhoff-consistency sensor-fault discrimination, and a fractional-order PI bus-restoration strategy. An exact residual expression is derived for an open-circuit phase under the averaged model, establishing finite threshold crossing whenever the commanded duty is nonzero. A second residual, constructed from the capacitor current balance, distinguishes an actuator-side open-circuit fault from a single current-sensor bias under ideal noise-free conditions. A capacitor ride-through condition is also introduced to determine an explicit upper bound on the admissible detection and reconfiguration delay. For the fractional-order controller, the post-reconfiguration stability problem is reformulated through a commensurate-order representation, which enables a direct Matignon-sector stability assessment for the selected fractional order. Numerical experiments are conducted using a fixed-step averaged model that incorporates phase-parameter mismatch, a switch open-circuit fault, a subsequent current-sensor bias, a load increase, and an input-bus sag. The faulted phase is detected after 0.08 ms, the spare phase is engaged at 0.20 ms after fault inception, and the sensor bias is classified after 0.06 ms. With the selected parameters, the fractional controller maintains the 28 V bus above 27.35 V under the compound fault scenario and reduces the post-fault voltage integral absolute error by approximately 21.6% relative to the integer-order PI benchmark considered in this study. A 16-corner parameter study retains the bus voltage above 27.28 V. These results are model-based rather than flight-hardware validation; accordingly, the paper distinguishes mathematical guarantees from simulation-based evidence and states the assumptions required for practical implementation.

Keywords: fault-tolerant control; fractional-order control; interleaved buck converter; UAV power system; more-electric aircraft; open-circuit fault; sensor fault; active reconfiguration; survivability.

1 Introduction

The progressive electrification of aircraft replaces hydraulic and pneumatic functions with electrically supplied actuators, pumps, avionics, thermal systems, and propulsion auxiliaries. This shift increases the strategic importance of the onboard DC network and, in particular, of the power-electronic interfaces that connect buses of different voltage levels. Multiport and reconfigurable conversion have therefore received sustained attention in more-electric-aircraft architectures, where

high efficiency, galvanic or functional separation, low mass, and continuity of supply must be reconciled [1, 2]. Recent work has also moved fault tolerance from an isolated converter function toward coordinated energy-management and network reconfiguration [3, 4].

Aerospace power electronics imposes a distinctive reliability burden. Semiconductor faults may arise abruptly, while component stress, altitude, thermal cycling, and electromagnetic constraints restrict the amount of hardware redundancy that can simply be added without penalty. A fault-tolerant converter must therefore answer two questions simultaneously. First, can the faulty element be identified with sufficient selectivity? Second, can the healthy hardware maintain the protected bus during the finite interval in which detection, isolation, and reconfiguration take place? The second question is often obscured when fault tolerance is discussed only in logical terms.

Redundant-leg DC–DC converters and open-circuit fault diagnosis are established ideas. Jagtap and More [6] combined switch-fault diagnosis with redundant-switch reconfiguration in a boost converter, while Chawla and Kumar [7] considered a fault-tolerant interleaved buck structure with a redundant phase. Related converter-level approaches include open-switch compensation in modified boost structures [10], bidirectional fault-tolerant converters for DC energy-storage interfaces [11], and topologies designed for both open- and short-circuit semiconductor failures [8]. At the aircraft-system level, fault-current protection remains a distinct design problem [12]; bus-energy support using bidirectional conversion and storage has also been investigated for aircraft voltage transients [13]. Lang et al. [4] further demonstrated how a reconfigurable power-generation center can preserve power transfer after a converter failure. These studies motivate the present work, but they do not by themselves provide a unified mathematical relation among residual generation, fault classification, stored bus energy, reconfiguration delay, and fractional memory in the restoration controller.

Fractional-order control introduces an additional design degree of freedom through noninteger integration or differentiation. The $PI^\lambda D^\mu$ framework of Podlubny [14] is now classical, and the stability of commensurate fractional systems can be studied through the Matignon sector condition [17]. Fractional fault-tolerant control has also been considered at the abstract systems level [18]. The question pursued here is narrower and more physical: can a fractional restoration law be embedded in a redundant converter architecture without hiding the fault-management mechanism behind a black-box optimizer?

The paper answers this question with a deliberately transparent model. A 270 V source feeds a regulated 28 V DC bus through three active interleaved phases and one spare phase. A model-based observer residual identifies an open-circuit phase. A Kirchhoff current-balance residual then provides analytical redundancy for distinguishing current-sensor bias from actuator-side loss. The spare phase is activated after fault isolation, while the bus-current command is generated by a PI^λ restoration law. The main contributions are:

1. an averaged redundant multiphase model in which the active-set variable makes pre-fault, faulted, and post-reconfiguration dynamics explicit;
2. a closed-form open-circuit observer-error expression and a complementary capacitor-balance residual for ideal actuator/sensor fault discrimination;
3. a capacitor ride-through inequality linking allowable bus droop directly to current deficit and total detection-plus-reconfiguration delay;
4. a commensurate stability test for the post-reconfiguration fractional restoration loop at $\lambda = 4/5$;
5. a reproducible compound numerical scenario containing an open-circuit phase fault, sensor bias, load step, input-bus sag, and phase-parameter mismatch, followed by a 16-corner sensitivity study.

The aim is not to claim aircraft qualification from simulation. The numerical values define a representative avionic DC case study, and all hardware-specific conclusions are confined to the mathematical model stated below.

2 Redundant converter architecture

2.1 Three-active-plus-one-spare topology

Consider four buck phases connected in parallel to a common output capacitor. Three phases operate in the healthy mode and the fourth is available as a redundant phase. The architecture is sketched in Fig. 1. The active set is denoted by

$$\mathcal{A}(t) \subset \{1, 2, 3, 4\}, \quad m(t) = |\mathcal{A}(t)|.$$

Before a fault,

$$\mathcal{A}_0 = \{1, 2, 3\}.$$

If phase 2 develops an open-circuit fault, it is removed and phase 4 is activated, giving

$$\mathcal{A}_r = \{1, 3, 4\}.$$

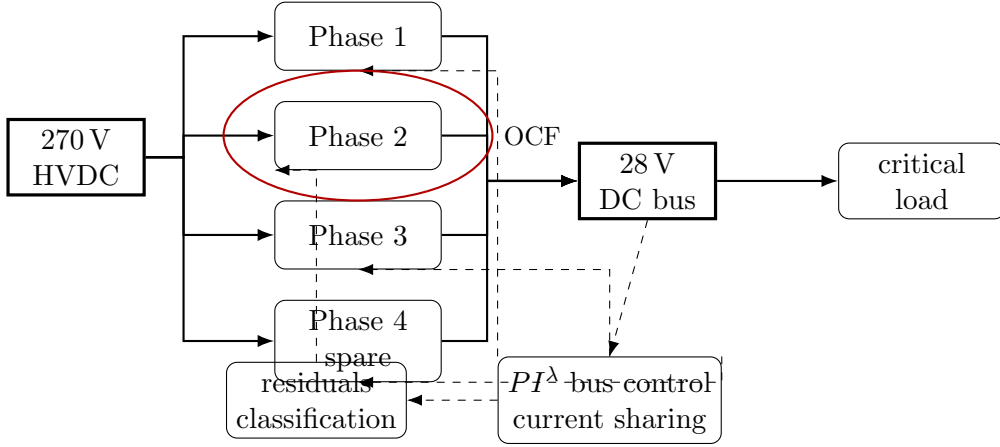


Figure 1: Redundant interleaved converter architecture used in the model. Phase 4 is a spare leg and becomes active after isolation of a faulted phase.

2.2 Averaged phase and bus equations

Let i_j be the inductor current of phase j , $d_j \in [0, d_{\max}]$ its commanded duty ratio, V_h the high-voltage input, v the regulated output voltage, and I_L the load current. Let $a_j(t) \in \{0, 1\}$ denote electrical availability: $a_j = 1$ if the commanded switch action reaches the power stage and $a_j = 0$ for an open-circuit/isolation condition. The averaged model is

$$L_j \dot{i}_j = a_j d_j V_h - v - r_j i_j, \quad j = 1, \dots, 4, \quad (1)$$

together with

$$C \dot{v} = \sum_{j=1}^4 i_j - I_L. \quad (2)$$

When a phase is physically isolated and its current reaches zero, the nonnegative-current constraint $i_j \geq 0$ is imposed. Equation (1) is an averaged, continuous-conduction representation; switching ripple and dead-time effects are not included in the present analysis.

The current reference is distributed over the commanded active set:

$$i_j^* = \begin{cases} I^*/m(t), & j \in \mathcal{A}(t), \\ 0, & j \notin \mathcal{A}(t), \end{cases} \quad (3)$$

where I^* is the total current command generated by the outer restoration loop. A proportional inner current law with voltage feedforward is used in the numerical study,

$$d_j = \text{sat}_{[0, d_{\max}]} \left[\frac{v + r_0 i_j^c + K_c(i_j^* - i_j^c)}{V_h} \right], \quad (4)$$

where i_j^c is either the measured current or an observer substitute after a sensor fault is declared, and r_0 is a nominal resistance.

3 Fault residuals and analytical redundancy

3.1 Open-circuit phase observer

For a phase believed to be active, consider the current observer

$$\dot{\hat{i}}_j = \frac{d_j V_h - v - r_0 \hat{i}_j}{L_0} + \ell(i_j^m - \hat{i}_j), \quad (5)$$

with residual

$$\rho_j = |i_j^m - \hat{i}_j|.$$

The superscript m denotes the measured current. The observer is intentionally simple: its purpose is not optimal state estimation but the generation of a physically interpretable mismatch signal.

Proposition 3.1 (Ideal open-circuit residual growth). *Assume $L_j = L_0 = L$, $r_j = r_0 = r$, a healthy current sensor, and locally constant d_j and V_h immediately after fault time t_f . Suppose the commanded phase develops an open-circuit fault so that the actual applied duty becomes zero while the observer continues to use $d_j > 0$. If $i_j(t_f) = \hat{i}_j(t_f)$, then for $t \geq t_f$*

$$|i_j(t) - \hat{i}_j(t)| = \frac{d_j V_h / L}{r/L + \ell} \left(1 - e^{-(r/L + \ell)(t - t_f)} \right). \quad (6)$$

Hence every threshold

$$0 < \delta < \frac{d_j V_h / L}{r/L + \ell}$$

is crossed in finite time.

Proof. After the open circuit,

$$\dot{i}_j = \frac{-v - r i_j}{L},$$

whereas the observer retains the commanded term $d_j V_h / L$. Setting $\tilde{i} = i_j - \hat{i}_j$ gives

$$\dot{\tilde{i}} = -\left(\frac{r}{L} + \ell\right) \tilde{i} - \frac{d_j V_h}{L}.$$

Solving this scalar linear equation from $\tilde{i}(t_f) = 0$ yields (6). The residual is monotone toward a strictly positive asymptote, proving finite threshold crossing. $\square$

The proposition explains why an open-circuit switch can be detected from the discrepancy between commanded electrical excitation and measured current evolution. Parameter mismatch and noise alter the residual floor, so practical thresholds must be chosen above the healthy uncertainty band.

3.2 Bus-current consistency residual

An individual observer residual alone does not identify whether the inconsistency originates in the actuator or in its current sensor. Equation (2) provides independent analytical redundancy. Define

$$\rho_\Sigma = \left| \sum_{j=1}^4 i_j^m - I_L - C\dot{v} \right|. \quad (7)$$

Proposition 3.2 (Ideal sensor-bias discrimination). *Assume the averaged bus equation (2) is exact. If all current sensors are healthy, then $\rho_\Sigma = 0$ independently of an actuator-side open circuit. If a single current sensor k has additive bias b_k while the others remain healthy, then*

$$\rho_\Sigma = |b_k|.$$

Proof. With healthy sensors, $\sum_j i_j^m = \sum_j i_j = I_L + C\dot{v}$ by (2). For a single biased sensor, $i_k^m = i_k + b_k$, so substitution in (7) gives $\rho_\Sigma = |b_k|$. $\square$

This yields the ideal logic

$$\rho_j > \delta_i, \quad \rho_\Sigma \leq \delta_\Sigma \implies \text{actuator/open-circuit candidate,}$$

whereas

$$\rho_j > \delta_i, \quad \rho_\Sigma > \delta_\Sigma \implies \text{sensor candidate.}$$

In hardware, $\dot{v}$ would be obtained from a filtered difference or an observer; therefore the strict equalities of Proposition 3.2 become thresholded relations.

4 Reconfiguration and survivability bound

4.1 Spare-phase activation

After an actuator-side fault is confirmed, the faulted phase is removed from $\mathcal{A}$ and the spare phase is inserted. Denote

$$\Delta t_r = t_r - t_f$$

as the total time from physical fault inception to completion of spare engagement. This interval includes detection dwell, logic execution, gate disable, and spare enabling.

The most direct bus-survivability question can be answered without solving the full converter dynamics.

Theorem 4.1 (Capacitor ride-through bound). *Suppose that during $[t_f, t_r]$ the current deficit satisfies*

$$0 \leq I_L(t) - \sum_{j=1}^4 i_j(t) \leq \Delta I_{\max}.$$

Then

$$v(t_r) \geq v(t_f) - \frac{\Delta I_{\max}}{C} \Delta t_r. \quad (8)$$

Consequently, the condition

$$\Delta t_r \leq \frac{C[v(t_f) - v_{\min}]}{\Delta I_{\max}} \quad (9)$$

is sufficient to keep $v(t_r) \geq v_{\min}$.

Proof. Equation (2) gives

$$\dot{v} = -\frac{1}{C} \left(I_L - \sum_j i_j \right) \geq -\frac{\Delta I_{\max}}{C}.$$

Integration from t_f to t_r yields (8); imposing $v(t_r) \geq v_{\min}$ gives (9). $\square$

For a pre-fault 20 A load equally shared by three phases, loss of one phase corresponds initially to a deficit of approximately 6.67 A. With $C = 2.2$ mF and an internally selected design floor $v_{\min} = 27$ V, (9) gives

$$\Delta t_r \leq 0.33 \text{ ms.}$$

The simulated 0.20 ms fault-to-spare interval therefore lies inside this conservative first-order ride-through limit.

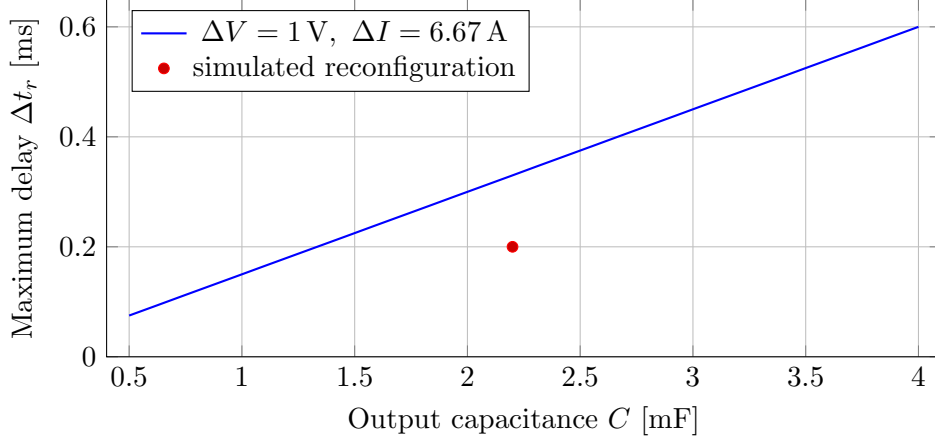


Figure 2: Capacitor ride-through design map from Theorem 4.1. The plotted delay bound is a sufficient condition under the assumed current-deficit envelope, not an aircraft certification limit.

5 Fractional bus-restoration law

5.1 Fractional integral action

Let

$$e_v(t) = v^* - v(t), \quad v^* = 28 \text{ V.}$$

The total current reference is

$$I^*(t) = I_L(t) + K_p e_v(t) + K_i \mathcal{I}^\lambda e_v(t), \quad 0 < \lambda \leq 1, \quad (10)$$

where

$$\mathcal{I}^\lambda e_v(t) = \frac{1}{\Gamma(\lambda)} \int_0^t (t - \tau)^{\lambda-1} e_v(\tau) d\tau. \quad (11)$$

At $\lambda = 1$, (10) becomes an ordinary PI restoration law. For $0 < \lambda < 1$, past voltage error receives a power-law weighting rather than the uniform accumulation associated with the integer integrator [14].

The load-current feedforward in (10) removes the static burden from the feedback law in the ideal model. The feedback term then compensates bus energy lost during faults, spare activation, and load changes.

5.2 Reduced post-reconfiguration stability

After reconfiguration, suppose the inner phase-current loops are fast relative to the bus loop so that

$$\sum_j i_j \approx I^*.$$

Substituting (10) into (2) gives the reduced error equation

$$C\dot{e}_v + K_p e_v + K_i \mathcal{I}^\lambda e_v = 0.$$

Its characteristic equation is

$$Cs^{1+\lambda} + K_p s^\lambda + K_i = 0. \quad (12)$$

For the numerical design we take

$$\lambda = \frac{4}{5}, \quad K_p = 2.0, \quad K_i = 500, \quad C = 2.2 \text{ mF}.$$

With the commensurate base order $q = 1/5$ and $w = s^q$, (12) becomes

$$P(w) = 0.0022w^9 + 2w^4 + 500 = 0. \quad (13)$$

Theorem 5.1 (Sector stability of the selected restoration loop). *The reduced post-reconfiguration loop defined by (12) with $\lambda = 4/5$, $C = 2.2 \text{ mF}$, $K_p = 2$, and $K_i = 500$ is asymptotically stable in the commensurate fractional sense.*

Proof. The derivative orders in (12) are $9/5$, $4/5$, and 0 , all integer multiples of $q = 1/5$. By the Matignon criterion [17], asymptotic stability requires every root w_k of (13) to satisfy

$$|\arg(w_k)| > \frac{q\pi}{2} = \frac{\pi}{10} = 18^\circ.$$

The distinct upper-half-plane/real roots and their absolute arguments are listed in Table 1. The smallest absolute root angle is 26.066° , which exceeds 18° . $\square$

Table 1: Representative roots of (13). Complex conjugates are omitted.

$\Re(w_k)$	$\Im(w_k)$	$ \arg(w_k) $ [deg]
3.6322	1.7768	26.066
2.1698	3.0300	54.394
-0.9935	4.1550	103.448
-2.6364	2.3818	137.904
-4.3442	0	180.000

Remark 5.2. Theorem 5.1 concerns the reduced post-reconfiguration bus loop. It is not a proof of global stability for the complete switched, saturated, fault-detection system. The distinction is important: the fault logic is hybrid, whereas the theorem addresses the fixed post-reconfiguration mode.

6 Numerical experiment

6.1 Parameters and event sequence

Table 2 lists the baseline parameters. The phase values are intentionally mismatched to avoid an artificially symmetric current-sharing case.

Table 2: Baseline numerical parameters.

Quantity	Symbol	Value
High-voltage bus	V_h	270 V, then 235 V
Regulated bus	v^*	28 V
Phase inductances	$L_{1:4}$	250 μH , 260 μH , 240 μH and 255 μH
Phase resistances	$r_{1:4}$	30 m Ω , 32 m Ω , 28 m Ω and 31 m Ω
Output capacitance	C	2.2 mF
Initial load current	I_L	20 A
Post-step load current	I_L	28 A
Inner current gain	K_c	4 V/A
Fractional order	λ	0.8
Fractional gains	(K_p, K_i)	(2.0, 500)
Integer PI gains	(K_p, K_i)	(2.0, 1500)
Observer injection	ℓ	800 s $^{-1}$
Individual residual threshold	δ_i	0.45 A
KCL residual threshold	δ_Σ	0.8 A
Fault dwell time	–	0.08 ms
Logic/gate reconfiguration delay	–	0.12 ms
Integration step	h	20 μs

The compound sequence is:

1. $t = 25$ ms: phase 2 experiences an open-circuit actuator fault;
2. after residual dwell, phase 2 is isolated and phase 4 is activated;
3. $t = 50$ ms: the phase-1 current measurement receives a +2 A bias; once classified, the controller substitutes $\hat{i}_1$ for the corrupted measurement;
4. $t = 70$ ms: load current increases from 20 A to 28 A;
5. $t = 90$ ms: the input bus decreases from 270 V to 235 V.

The comparison with an integer PI uses the same plant, fault logic, thresholds, event sequence, and proportional gain. The integral gains were selected to give similar nominal regulation without duty saturation; no claim of globally optimal tuning is made.

6.2 Fractional discretization

The fractional integral is evaluated with the causal convolution

$$\mathcal{I}^\lambda e(t_n) \approx h^\lambda \sum_{k=0}^n c_k e(t_{n-k}), \quad c_0 = 1, \quad c_k = c_{k-1} \frac{k-1+\lambda}{k}. \quad (14)$$

The averaged electrical states are advanced with an explicit fixed-step update. Since the purpose is comparative fault-transient analysis rather than switching-waveform reconstruction, the numerical model does not resolve PWM ripple.

7 Results

7.1 Open-circuit recovery and bus regulation

The phase-2 observer residual exceeds its threshold after 0.08 ms. With the additional 0.12 ms logic/gate delay, phase 4 enters the active set at $t = 25.20$ ms. Figure 3 shows the bus response.

The largest downward excursion is 27.350 V with the fractional controller and 27.346 V with the integer PI. The main difference appears in the restoration tail: the fractional case returns to a ± 0.1 V band after approximately 3.76 ms, compared with 4.62 ms for the PI benchmark.

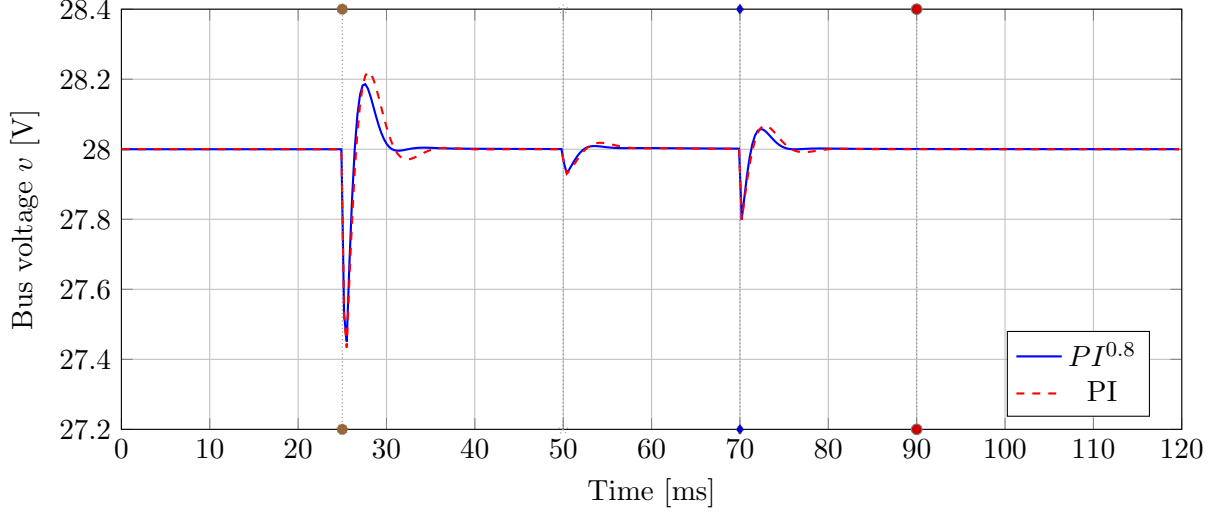


Figure 3: Bus-voltage response for the compound scenario. Event times are shown by vertical dotted lines at 25 ms, 50 ms, 70 ms and 90 ms.

Over the interval from the first fault at 25 ms to the end of the simulation, the voltage integral absolute error is

$$\text{IAE}_{PI^{0.8}} = 1.302 \times 10^{-3} \text{ V s},$$

whereas

$$\text{IAE}_{PI} = 1.661 \times 10^{-3} \text{ V s}.$$

For this particular tuning and scenario, the reduction is approximately 21.6%. This percentage should be interpreted as a case-study result, not a universal superiority statement for fractional control.

7.2 Current transfer to the spare phase

Figure 4 resolves the phase currents around the open-circuit event. Phase 2 loses excitation at 25 ms; after reconfiguration, phase 4 assumes one-third of the total current command while phases 1 and 3 remain active. The current-transfer mechanism is therefore explicit rather than represented as an abstract “fault-tolerant mode.”

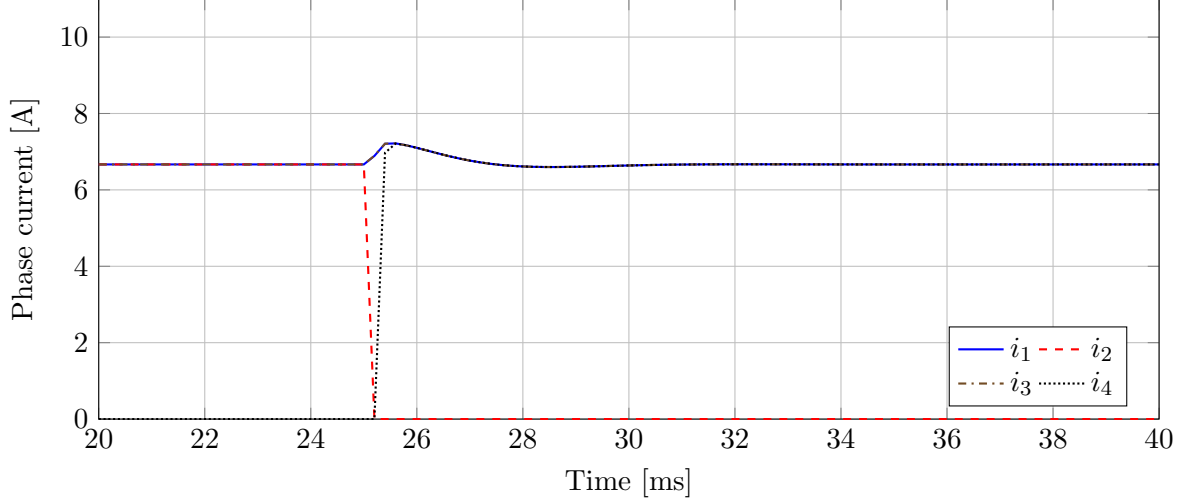


Figure 4: Phase currents during the open-circuit fault and spare-leg engagement. Phase 4 is initially idle and becomes active after the phase-2 fault is confirmed.

7.3 Actuator/sensor fault classification

At 25 ms, the phase-2 residual grows strongly while the bus-current consistency residual remains close to zero; the logic therefore identifies an actuator-side inconsistency. At 50 ms, the +2 A current-sensor bias drives both the phase-1 residual and ρ_Σ , producing the opposite classification. In the ideal numerical model the sensor bias is declared after 0.06 ms.

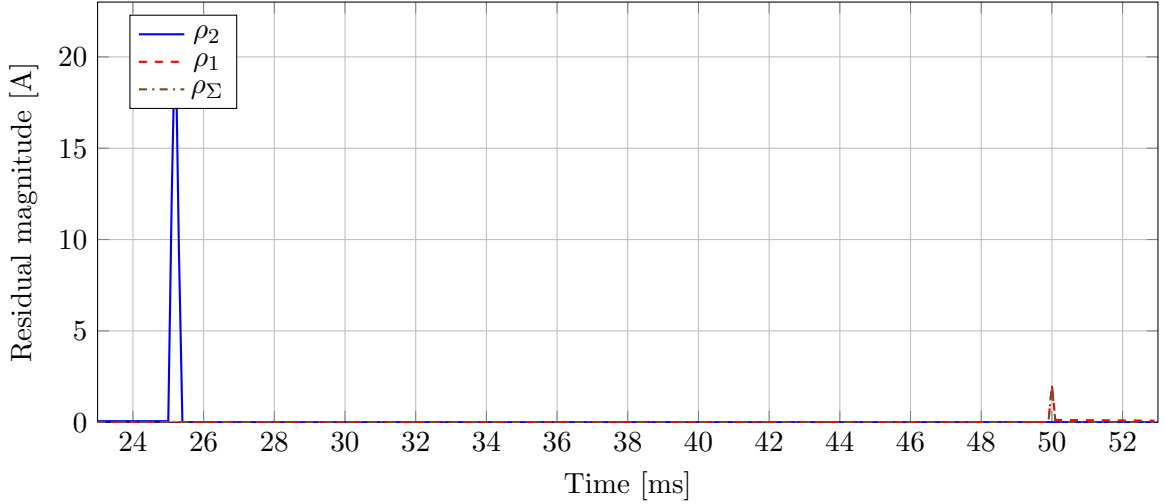


Figure 5: Residual behavior around the phase-2 open circuit at 25 ms and the phase-1 sensor bias at 50 ms. The KCL residual remains small for the actuator fault but reacts to the sensor bias.

7.4 Event-wise comparison

Table 3 summarizes the voltage envelopes. The line-sag event is largely rejected by the voltage feedforward in the averaged duty law, which is why its residual bus deviation is very small.

Table 3: Voltage envelopes in the baseline compound scenario.

Event window	$PI^{0.8}$		PI	
	min [V]	max [V]	min [V]	max [V]
Open-circuit/reconfiguration	27.350	28.187	27.346	28.221
Sensor bias/substitution	27.930	28.009	27.929	28.018
20–28 A load step	27.798	28.058	27.796	28.067
270–235 V input sag	28.0002	28.0007	28.0000	28.0001

The result is nuanced. The fractional controller does not radically change the first capacitor-supported voltage dip because that dip is dominated by fault-detection and spare-engagement delay. Its benefit appears primarily in the post-event restoration integral and overshoot. This separation between *fault-management speed* and *closed-loop recovery shape* is one of the reasons to retain the explicit ride-through analysis of Section 4 rather than attributing all survivability to the controller.

7.5 Sixteen-corner parameter study

A deterministic corner sweep was carried out over

$$C \in \{0.9, 1.1\}C_0, \quad L_j \in \{0.9, 1.1\}L_{j0}, \quad r_j \in \{0.8, 1.2\}r_{j0},$$

and post-step load current

$$I_L^+ \in \{26 \text{ A}, 30 \text{ A}\}.$$

The same controller and thresholds were retained in all $2^4 = 16$ cases. Table 4 reports the extrema over the sweep.

Table 4: Extrema over the 16 deterministic parameter corners.

Metric	Range over 16 corners
Minimum bus voltage	27.282 V to 27.410 V
Maximum bus voltage	28.170 V to 28.206 V
Open-circuit detection delay	0.08 ms
Sensor-bias detection delay	0.06 ms

The fixed detection delays in this ideal sweep are a consequence of the coarse threshold/dwell implementation and the absence of measurement noise. They should not be read as robustness guarantees for hardware. What the sweep does show is that the selected bus capacitance and reconfiguration timing retain substantial voltage margin under the stated bounded parameter changes.

8 Discussion

The architecture separates three mechanisms that are often conflated.

First, the capacitor provides the immediate energy buffer. Theorem 4.1 shows that no controller can compensate for arbitrarily long diagnostic delay when the load exceeds the healthy-phase current available during the fault interval. Increasing controller bandwidth does not remove this physical energy constraint.

Second, reconfiguration restores current-producing hardware. In the simulated single-phase open circuit, the decisive event is not the eventual convergence of the fractional loop but the activation of phase 4 before the capacitor-supported bus droop becomes excessive. This is why the spare leg and the fault logic should be designed jointly rather than as independent subsystems.

Third, the fractional integral shapes the restoration after the topology has been repaired. Its power-law memory changes how accumulated voltage error is returned to zero. In the present case

this reduces the overall post-fault voltage IAE and shortens the return to a narrow voltage band, while leaving the first few hundred microseconds primarily governed by stored capacitor energy and current-transfer delay.

The KCL residual also deserves a careful interpretation. Proposition 3.2 is exact only for the averaged model and ideal measurements. In a switching converter, capacitor ESR, current-sensor delay, PWM ripple, quantization, and numerical differentiation of v create a nonzero healthy residual. A flight implementation would therefore require bandwidth separation and threshold design from measured noise statistics. The analytical result remains useful because it identifies *which physical identity* can provide sensor redundancy; it does not remove the engineering task of robust residual conditioning.

The study is relevant to UAV and avionic DC networks because these platforms place high value on continuity of critical loads and on graceful degradation after a component fault. It should not, however, be interpreted as compliance with a specific airworthiness or military power-quality standard. The internal 27 V design floor used in Fig. 2 is a modeling choice for this case study.

9 Limitations and implementation path

The present work has four principal limitations.

1. **Averaged power stage.** Switching ripple, dead time, nonlinear semiconductor drops, thermal dynamics, and magnetic saturation are absent.
2. **Idealized load-current knowledge.** Equation (10) uses I_L feedforward. Hardware can replace this with a measured, estimated, or scheduled load term, but sensor delay must then be included.
3. **Noise-free fault classification.** The residual thresholds were tested under parameter mismatch but not under stochastic measurement noise or EMI-corrupted sensing.
4. **No hardware-in-the-loop or experimental validation.** The numerical evidence establishes reproducibility within the stated model, not technology readiness.

A logical validation sequence is therefore: switched-model verification, processor-in-the-loop implementation of the residual logic, hardware-in-the-loop fault injection, and finally a laboratory redundant converter prototype with controlled open-circuit and sensor faults. Thermal and EMI measurements should be included before any claim about aerospace hardware suitability.

10 Conclusion

A fault-tolerant redundant DC–DC converter was formulated as a coupled problem of diagnosis, stored-energy ride-through, active reconfiguration, and fractional restoration. The model yields several results that remain transparent at the equation level. An open-circuit phase produces a finite observer-residual threshold crossing under nonzero commanded duty. The capacitor current balance provides a second residual that, in the ideal averaged model, separates actuator-side current loss from a single additive current-sensor bias. The capacitor ride-through inequality converts the abstract concept of “fast reconfiguration” into a quantitative delay bound. After reconfiguration, the selected $PI^{0.8}$ bus loop satisfies a direct commensurate Matignon-sector test.

In the representative 270 V-to-28 V numerical case, the open-circuit fault was detected in 0.08 ms, the spare phase was engaged 0.20 ms after fault inception, and a later 2 A sensor bias was classified in 0.06 ms. The fractional controller kept the bus above 27.35 V in the compound scenario and reduced the post-fault voltage IAE by about 21.6% relative to the selected integer PI benchmark. A 16-corner deterministic sweep retained the bus above 27.28 V. These results support the mathematical architecture, while experimental validation remains necessary before claims of aircraft-level reliability or qualification can be made.

Declarations

Funding. To be completed by the authors before submission.

Competing interests. The authors declare no competing interests.

Author contributions. Taylan Demir and Atakan Koçyiğit: conceptualization, methodology, mathematical analysis, numerical investigation, writing, review, and approval. The final contribution statement should be confirmed by both authors before submission.

Data and code availability. No external experimental data are used. All numerical parameters, event times, and plotted coordinates are contained in this L^AT_EX source. The numerical scheme is specified by Eqs. (1)–(14). A separate implementation script should be archived with the submitted manuscript if required by the target journal.

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