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A BDPR-Feedback-Based LNA with Programmable RF Metrics in Real-World Settings for Wideband Wireless Communication Systems

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ABSTRACT

This work presents a low-voltage (0.6 V), low-power Low-Noise Amplifier (LNA) operating in the 1.8 – 4.0 GHz wide-band wireless communication standards. The proposed LNA, implemented in the Cadence simulation environment using a standard 45 nm PDK, integrates a tunable bulk-driven pseudo-resistor (BDPR) feedback network with the conventional architecture. Simulation results show a noise figure of 1.66 dB, a forward gain of 14.18 dB, and an input return loss of 33.7 dB at 3.6 GHz, and almost the same can be achieved across the 1.8 – 4.0 GHz wide-band by tuning the bulk bias voltage, (V_{bulk}). Closely matched RF metrics achieved by the post-layout simulation validates the robustness of the proposed LNA against the parasitics. PVT analysis demonstrates its less sensitivity against the process corner variations, supply voltage fluctuations and temperature changes, whereas, Monte Carlo analysis reveals its high yield against the device-mismatches during fabrication. Moreover, the V_{bulk} -tuning leads to achieve almost the same RF metrics in these real-world scenarios, and hence, offers an effective and simple on-chip programming mechanism in real-world scenarios. Finally, low power consumption (only 6 mW) and compact design (active area is $\approx 0.080 \text{ mm}^2$) makes the proposed LNA well-suited for 5G, IoT, and wearable RF front-ends.

A wide set of Wireless communication standards includes LTE Band 3 (1.8 GHz), UMTS/LTE Band 1 (2.1 GHz), Wi-Fi/Bluetooth/ZigBee (2.4 GHz), LTE Band 7 (2.6 GHz), and 5G NR Bands n77/n78 (3.3 – 4.0 GHz)¹⁻³. This wide-band frequency range (1.8 – 4.0 GHz) is ideal for various contemporary communication and sensing devices, IoT devices, wearable and biomedical equipment, S-band radar and satellite communication, and even other devices. Moreover, the recent explosion of wearable electronics-based products, such as health monitors and smart watches, wireless sensor nodes, and so forth, has dramatically increased the global need of compact, energy-efficient, and low-noise radio frequency (RF) front-end architecture that can be reconfigured to operate in this wide-band spectrum.

In RF front-end architecture, low-noise amplifiers (LNAs) are key components that set the overall noise performance of a receiver. In the literature number of LNAs have been reported working across various frequency range with reconfigurability. Pu et. al⁴ reported an LNA in the frequency range of 0.7 – 2.5 GHz, Neha et. al reported LNAs working in 1.8 – 2.1 GHz⁵, and in 1.3 – 2.3 GHz⁶. A dual-band LNA that worked in both 2.4 GHz narrow-band and a wide band (3.1 – 10.6 GHz) has been reported in⁷, whereas, in⁸ a reconfigurable balun-LNA working in 2.4 GHz and sub-GHz (0.05 – 0.7 GHz) frequency range has been reported. To the best of our knowledge, no LNAs have been reported in the literature working in the wireless band spanning over 1.8 – 4.0 GHz with tunable band selection.

In practical RF integrated circuits, process variations, device mismatch, and modeling inaccuracies can cause the fabricated LNAs to deviate from its nominal simulated performance⁹⁻¹³. To improve the flexibility of LNA operation, several tunable and reconfigurable techniques have been reported. A floating-gate MOS-based approach¹⁴ employs indirect control of the transistor operating point to provide tunability in analog and RF circuits. Transformer-based tuning¹⁵ has also been investigated for continuously reconfigurable LNAs, where a tuning stage and an active phase-shifting path modify the effective transformer response and consequently adjust the input impedance over different operating frequencies. For low-power and wideband operation, complementary current-reuse architectures combined with active shunt feedback have been used to reduce current consumption while providing input matching without conventional inductors¹⁶. In another approach, inter-stage series L-C resonators with varactors are employed to provide frequency-selective matching and image rejection. The varactor bias changes the resonant frequency, allowing the circuit to compensate for frequency mismatch caused by process variation and model

error¹⁷. However, all the above-mentioned techniques achieve the tunability through dedicated tuning elements which increase circuit complexity, may introduce additional parasitic, noise, area, or power considerations, and is not necessarily located directly within the feedback element responsible for controlling the LNA characteristics. Therefore, a simple and localized method for adjusting the feedback behavior after fabrication is desirable.

This work addresses the issue of controlling LNA RF metrics across the 1.8 – 4.0 GHz wireless frequency spectrum, and proposes a localized method to achieve dynamic feedback behavior. Use of large-valued Resistive feedback¹⁸ is not practical for on-chip integration¹⁹, as CMOS implementation of such resistor introduces excessive thermal noise and consumes considerable chip area. Therefore, we propose the bulk-driven pseudo-resistor (BDPR)^{20,21} as the feedback element, which is a MOSFET operating in the subthreshold region. The bulk terminal of this MOSFET employed in the feedback path is utilized as an additional tuning degree of freedom. By changing the bulk voltage, the electrical characteristics of the pseudo-MOSFET and consequently the effective feedback behavior can be adjusted without directly modifying the main RF signal path. This provides a means of compensating performance deviations caused by device mismatch and process variation. If the fabricated LNA exhibits a deviation from the desired operating point, the bulk voltage can be adjusted to shift the feedback characteristics and bring the LNA performance closer to the target condition. Thus, the proposed approach introduces a simple feedback-level tuning mechanism that can potentially provide performance adjustment in the real-world scenarios without requiring a dedicated calibration loop. Therefore, this research contributes to develop sustainable, high-performance wireless communication systems, thereby supporting the sustainable development goal (SDG) 9.

Results and Discussion

This section presents, analyses, and discusses the results obtained from the rigorous Cadence simulation runs for the tunable-BDPR-based LNA proposed in this work. The schematics of the proposed LNA is shown in Fig. 1A, wherein, the tunability of the BDPR-based feedback resistance has been realized by the V_{bulk} -variation (0.0 – 1.0) V. The frequency range of interest in these simulations is kept within 1.8 – 2.4 GHz. The key RF performance metrics of interest are the input resistance, the forward gain, the input return loss, and the noise figure.

Figure 1B illustrates that the BDPR-based feedback resistance (R_F) increases as the bulk bias voltage (V_{bulk}) increases from 0.0 V to 1.0 V. This trend is explained as follows. Increase in V_{bulk} increases the threshold voltage (V_{Th}), decreases the drain current (I_D), and hence, increases the output resistance ($r_0 = \frac{1}{\lambda I_D}$) which, in turn, increases R_F [Eqns. (S3)-(S7) in the Supplementary Material]. This increase in R_F also results in an increase in the real part of the input impedance (R_{in}) [Eqn. S26 in the Supplementary Material] of the proposed LNA as V_{bulk} increases from 0 V to 1.0 V, which is observed in Figure 1C. From this figure, it can be revealed that R_{in} remains close to the desired 50 Ω reference for all V_{bulk} values; $R_{in} = 47 \Omega$ at $V_{bulk} = 0$ V and 53 Ω at $V_{bulk} = 1.0$ V. Therefore, the proposed LNA maintains a V_{bulk} -dependent control over R_{in} to match with the standard RF system environments offered by the BDPR structure.

Figure 1D demonstrates that the simulated forward gain of the proposed LNA maintains a typical gain profile across the 1.8 – 4.0 GHz frequency band for all V_{bulk} values, and the gain profile shifts upward and broadened as V_{bulk} increases. Increase in V_{bulk} increases R_F , for which the overall transconductance (G_m) and hence, the overall gain (A_v) increases [Eqns. (S39)-(S41) in the Supplementary Material], resulting in an upward shifting of the gain profile, as well as its rolling off at the higher frequencies. These plots also demonstrate that the increase in V_{bulk} flattens the gain profile, indicating more improvement in the gain stability over a wider frequency band. This can be attributed to the increased R_F , and hence, the improved feedback factor ($\frac{1}{R_F}$ for the voltage-shunt feedback topology²²). This gain tunability without altering the physical components makes the proposed LNA adaptable to varying signal strengths and protocol requirements.

The simulated input return loss (IRL) of the proposed LNA as presented in Figure 1E shows that IRL is ≤ 10 dB for 1.8 – 4.0 GHz at $V_{bulk} = 0$ V, and increases as V_{bulk} increases. The IRL is closer to 10 dB for 1.8 – 2.1 GHz, more sharply increases from 10 dB to approx 33 dB for 2.1 to $\approx 3.2 - 3.5$ GHz, and then, decreases to 12 dB to approx 25 dB at 4.0 GHz, as V_{bulk} increases from 0 V to 1.0 V. This increase in IRL with the increase in V_{bulk} is attributed to the increase in R_{in} as V_{bulk} increases (explained earlier). These findings reveal that the input impedance (Z_{in}) of the proposed LNA matches with the characteristic 50 Ω source resistance better and better for the frequency region of interest (1.8-4.0 GHz) as V_{bulk} increases from 0 V to 1.0 V. This tunable and improved Z_{in} -matching is due to the programmable-BDPR-based feedback network introduced in the proposed LNA. As a result, the LNA can dynamically adapt its input matching characteristics across multiple frequency bands without requiring external switchable matching components, and hence, enables compatibility and confirms programmability with a wide set of wireless communication standards.

The noise figure (NF) is inversely proportional to the magnitude of R_{in} , and the square magnitude of the forward gain (A_v) [Eqn. (S48) in the Supplementary Material]. As R_{in} and A_v both increase with the increase in V_{bulk} (explained earlier), the plots presented in Figure 1F demonstrate an almost parallel downwards shift of NF as V_{bulk} increases. Therefore, increased V_{bulk} reshapes the NF in a better way than that occurs at $V_{bulk} = 0$ V. Moreover, the NF remains below 3 dB across the entire

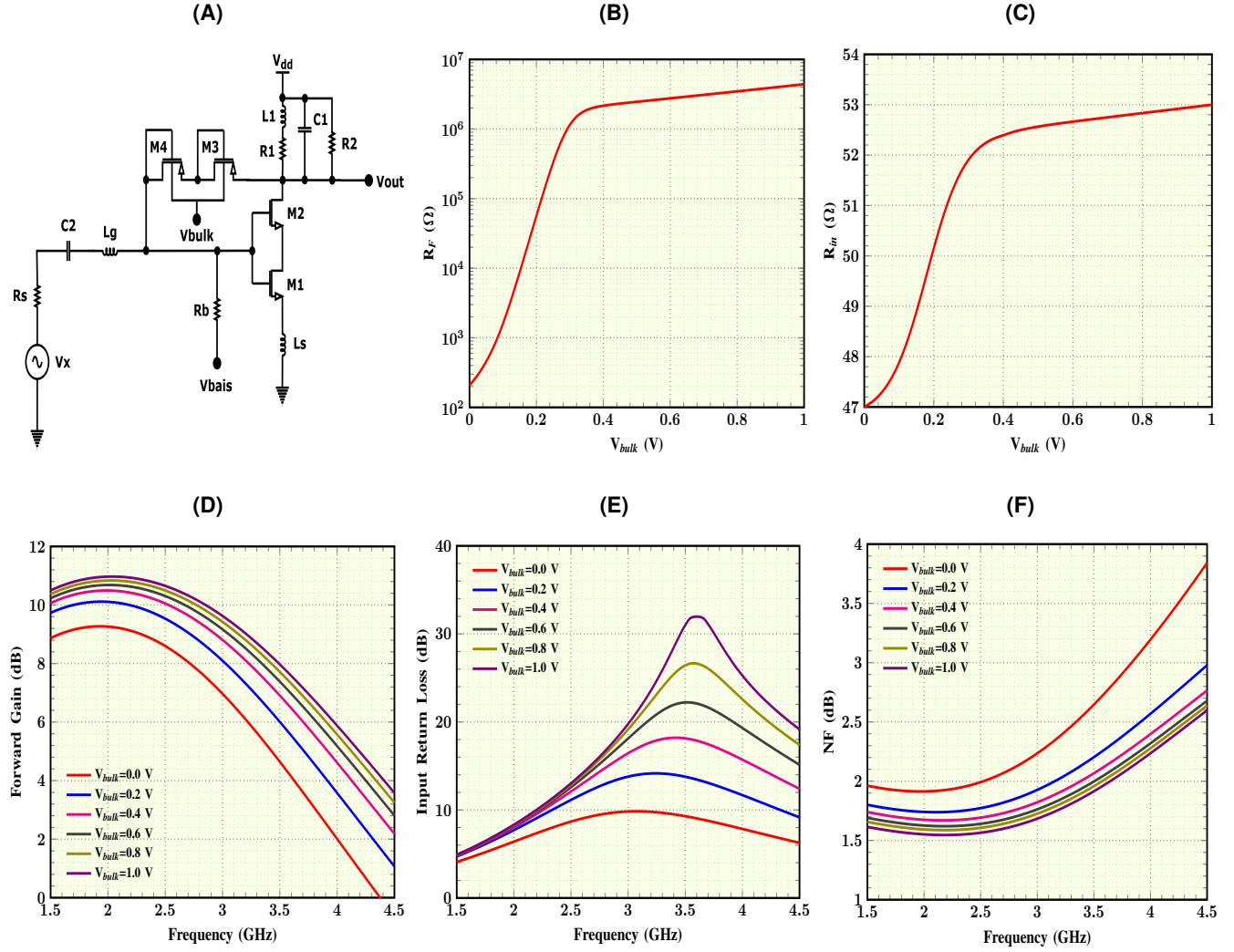


Figure 1. (A) The schematic of the proposed LNA. (B) R_F Vs. V_{bulk} (C) R_{in} Vs. V_{bulk} . (D) Forward Gain, (E) Input Return Loss, and (F) NF of the proposed LNA for different V_{bulk} values at $T = 300$ K.

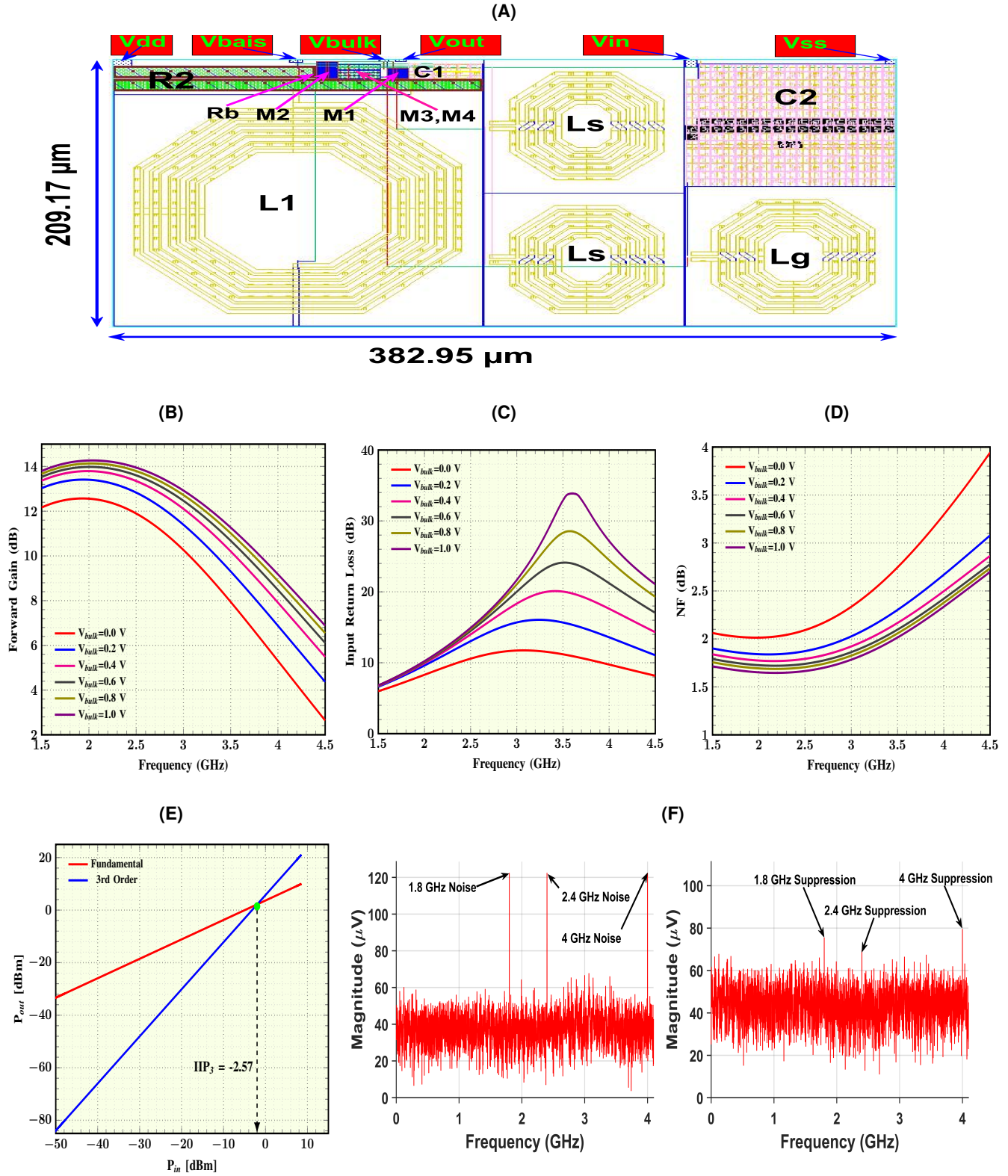


Figure 2. (A) Post-layout view of the proposed LNA in 45 nm CMOS technology.(B) Forward gain, (C) Input Return Loss, (D) NF, and (E) Third-order input intercept point (IIP3) of the proposed LNA at T = 300 K for post-layout simulation. (F) Signal with added Noise (left) and reduced Noise (right) at T = 300 K.

1.8 – 4.0 GHz operating range for all $V_{bulk} > 0$ values. This consistency indicates that the proposed BDPR feedback-based LNA maintains stable noise performance even under varying V_{bulk} conditions.

Post-layout Simulation Results Figure 2A presents the post-layout view of the proposed LNA, designed and implemented in a 45 nm CMOS process. The total active area is $209.17 \mu m \times 382.95 \mu m$, corresponding to approximately ($\approx 0.080 mm^2$), making the circuit compact and suitable for RF system-on-chip (SoC) integration. During layout, careful attention has been given to reduce parasitic components and hence, to preserve circuit symmetry, especially in the differential and RF signal paths. On-chip spiral inductors were used to implement source and load matching, while metal–insulator–metal (MIM) capacitors provide stable and low-loss decoupling and resonance tuning. Wider metal traces and multiple via stacks were used to route RF signals, reducing series resistance and improving high-frequency current-handling capability.

Plots of key RF metrics (gain, IRL, and NF) obtained from post-layout simulations, and presented in Figs. 2B, 2C, and 2D respectively, demonstrate that all these metrics closely match with their respective pre-layout plots presented in Figs. 1D, 1E, and 1F, confirming robustness and manufacturability for practical RF front-end applications. Additionally, V_{bulk} -programmability provides tuning the RF-metrics across the 1.8 – 4.0 GHz for post-layout simulations.

Figure 2E shows the plot of the simulated input third-order intercept point (IIP3) of the proposed LNA, which is a measure of its linearity and signal-handling capacity in crowded frequency environments. This plot marks an IIP3 of -2.57 dBm at a tone spacing of 1 MHz. This value indicates a moderate linearity performance of the proposed LNA, which balances power efficiency with decent protection against signal distortion, and can handle relatively strong unwanted signals (blockers) without corrupting the desired weak signal. Owing to the incorporation of a BDPR-based tunable feedback network, the proposed design achieved enhanced linearity relative to conventional LNAs. Therefore, it can be argued that the proposed LNA is excellent for mobile handsets, Wi-Fi devices, or consumer IoT receivers, and provides enough linearity to handle typical urban interference while keeping power consumption low.

Figure 2F illustrates the frequency-domain noise response of the proposed LNA before and after noise reduction. We apply a 4.5 GHz input signal and add 1.8 GHz, 2.4 GHz, and 4 GHz noise components. The left pane of Fig. 2F shows the added noise components observed at 1.8 GHz, 2.4 GHz, and 4 GHz, whereas the right one of Fig. 2F demonstrates the reduced noise levels after applying the proposed noise suppression technique. The results indicate effective noise reduction across the operating frequency range of 1.8–4 GHz.

PVT Analysis Box-plots of Figure 3 show the pictorial representation of process-voltage-temperature (PVT) analysis of the proposed LNA. The spread of each box plot represents the variation of an RF metric across the 1.8 – 4.0 GHz for a given V_{bulk} .

Figure 3A shows that V_{DD} variation at $V_{bulk} = 0$ V does not affect the spread of IRL at all, while its magnitude is the least (8 – 11 dB) meaning that input impedance matching is the worst although remains almost frequency-independent. At $V_{bulk} = 0.2$ V, the peak of the box-plot increases to 15 – 16 dB with slightly wider yet almost uniform spread at higher V_{dd} values. At $V_{bulk} = 1.0$ V, the peak of the box-plot increases significantly ≈ 25 – ≈ 35 dB with much wider spread at higher V_{dd} biases. That is, an improved R_{in} -matching can be achieved at the cost of increased frequency-sensitivity as V_{bulk} increases. The similar trend holds for the gain and the noise figure, as observed in Figures 3B and Figure 3C. Therefore, V_{bulk} -programmability can be an effective tool to trade off between the improved RF metric and the higher frequency-sensitivity in case of V_{dd} -fluctuations.

The effects of temperature variation on the RF metrics (IRL, gain and NF) with increasing V_{bulk} voltages are plotted in Figs. 3D, 3E and 3F, respectively. These plots also demonstrate that the increased V_{bulk} enhances impedance-matching, increases gain and decreases NF at the cost of increased frequency sensitivity, particularly for low-temperature operation. Therefore, similar to V_{dd} -fluctuations, both temperature and frequency sensitivity can be handled for improved RF metrics through appropriate programming of V_{bulk} .

The change in process corner has the similar effects on the RF metrics as observed in Figs. 3G, 3H and 3I: worst metrics yet least frequency-sensitive for no bulk bias, whereas, the better metrics with higher frequency-sensitivity at increased V_{bulk} . TT corner shows the best yet greatest frequency sensitivity, whereas, SS/SF corners shows the optimum metrics with moderate frequency sensitivity. Again, programming V_{bulk} appropriately mitigates the effects of process corner variation.

Monte Carlo Simulation Figure 4 presents the Monte Carlo simulation results of noise figure of the proposed LNA for 200 samples under three different bulk bias voltages ($V_{bulk} = 0.0$ V, 0.2 V and 1.0 V) at three different operating frequencies (1.8, 2.4 and 4.0 GHz) to demonstrate the effects of sample variations in real-world settings. These plots clearly show more improved mean performance (lower μ), and the standard deviation (lower σ) obtained at $V_{bulk} > 0$ V than those observed at $V_{bulk} = 0$ V at the mentioned frequencies. That is, when V_{bulk} increases from 0 V, less noise is added to the signal due to the lower μ , and the proposed LNA becomes more robust against the manufacturing variations due to the lower σ .

The noise floor (average noise performance), and the yield ($\pm 3\sigma$) of the proposed LNA under the said conditions are tabulated in Table 1. At all three frequencies, significant improvement in the noise floor has been observed for an increase of $V_{bulk} = 0.0 \rightarrow 1.0$ V than the same observed for an increase of $V_{bulk} = 0.0 \rightarrow 0.2$ V, being the greatest at the frequency of 4.0 GHz (0.65 dB from $V_{bulk}=0.0V \rightarrow 0.2V$, and 0.97 dB from $V_{bulk}=0.0V \rightarrow 1.0V$). The drops in NF reflect a major advantage in receiver sensitivity. In terms of yield it can be argued that the normal distribution for 200 samples observed in all the plots of

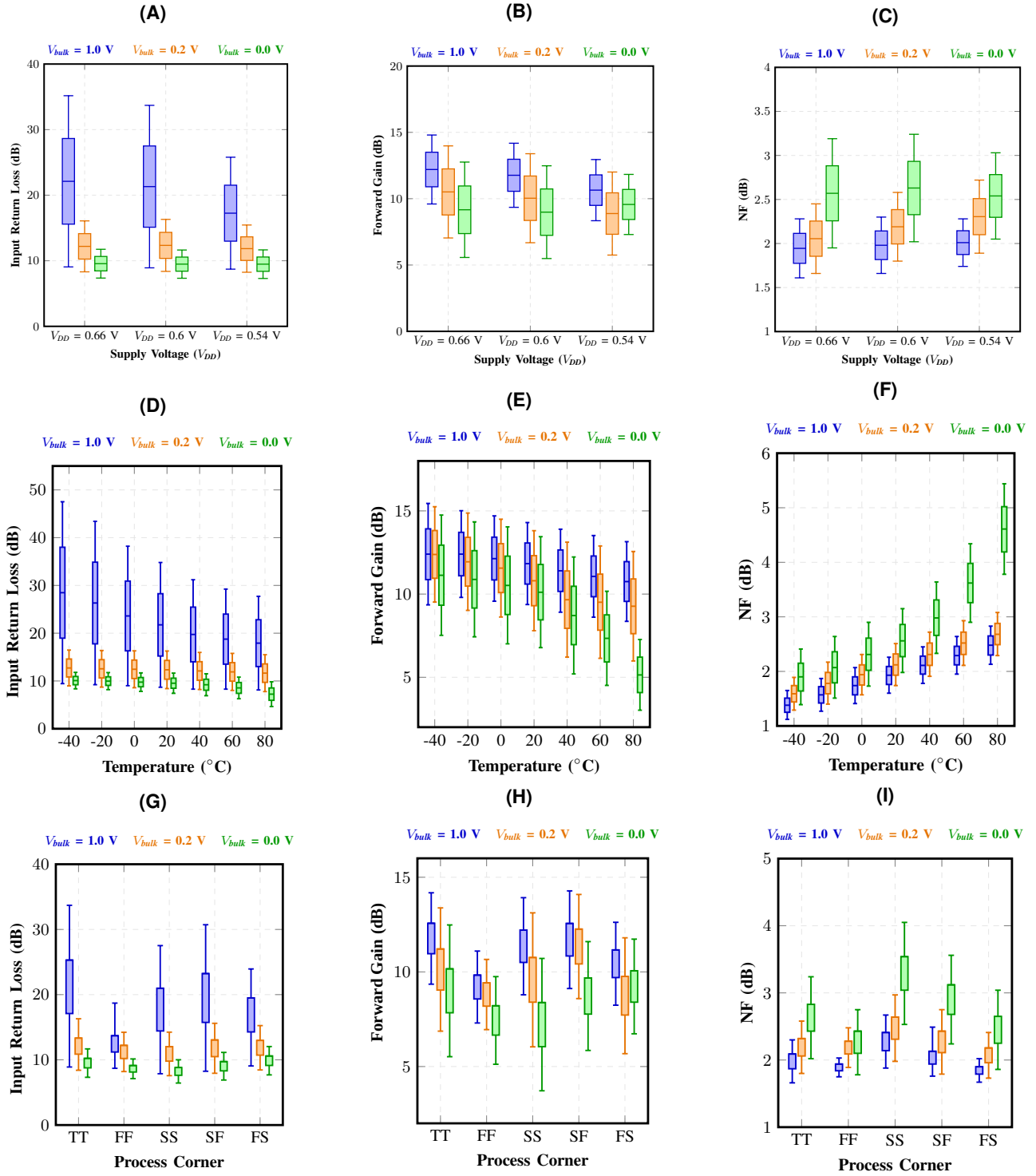


Figure 3. PVT simulation results with $V_{bulk} = 0.0$ V, 0.2 and 1.0 V across the frequency range of 1.8-4.0 GHz. Effects of Supply voltage (V_{DD}) fluctuations on (A) Input return loss, (B) Forward gain, and (C) NF. Effects of temperature variations on (D) Input return loss, (E) Forward gain, and (F) NF. Effects of different process corners on (G) Input return loss, (H) Forward gain, and (I) NF.

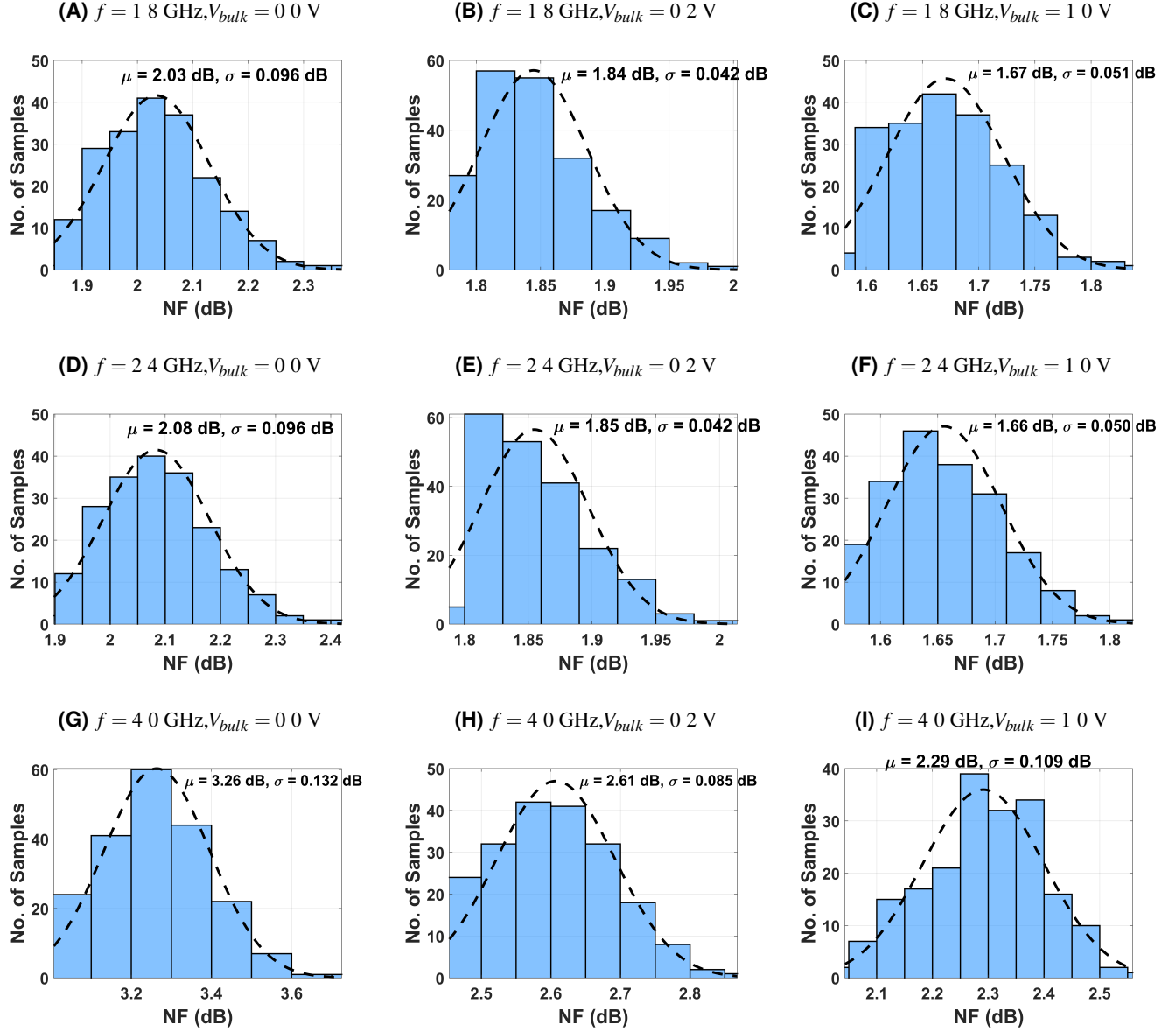


Figure 4. Monte Carlo simulation results for NF of the proposed LNA with (A) $V_{bulk} = 0.0 \text{ V}$, (B) $V_{bulk} = 0.2 \text{ V}$, and (C) $V_{bulk} = 1.0 \text{ V}$ at 1.8 GHz , (D) $V_{bulk} = 0.0 \text{ V}$, (E) $V_{bulk} = 0.2 \text{ V}$, and (F) $V_{bulk} = 1.0 \text{ V}$ at 2.4 GHz , and (G) $V_{bulk} = 0.0 \text{ V}$, (H) $V_{bulk} = 0.2 \text{ V}$, and (I) $V_{bulk} = 1.0 \text{ V}$ at 4.0 GHz .

Figure 4, 99.73% of the manufactured chips will fall within the $\mu \pm 3\sigma$ range²³.

The σ -drop is lower for $V_{bulk}=0\text{ V} \rightarrow 1\text{ V}$ than that for $V_{bulk}=0\text{ V} \rightarrow 0\text{ V}$, meaning that σ -drop gets worsened as V_{bulk} increases more from zero bias. Nonetheless, the worst-case yield (3- σ Worst-Case NF) is higher for $V_{bulk}=0\text{ V} \rightarrow 1\text{ V}$ than that for $V_{bulk}=0\text{ V} \rightarrow 0\text{ V}$ as seen from Table 1 which reveals that the absolute worst performing chips of $V_{bulk}=1\text{ V}$ will outperform the average chip from the 0 V biased chip more than the chips of $V_{bulk}=0\text{ V}$ do. Indeed, increase in V_{bulk} tightens the process and local device mismatch sensitivity resulting in a highly reproducible circuit layout across different silicon wafers. Finally, it can be argued that the V_{bulk} -programmability can be an effective tool to tune the manufacturing variations in the real-world settings across the $1.8 - 4.0\text{ GHz}$.

Table 1. Monte Carlo Analysis

Metric	$V_{bulk}=0\text{ V}$	$V_{bulk}=0\text{ V}$	$V_{bulk}=1\text{ V}$	$V_{bulk}=0\text{ V} \rightarrow 0\text{ V}$	$V_{bulk}=0\text{ V} \rightarrow 1\text{ V}$
1.8 GHz					
μ (dB)	2.03	1.84	1.67	0.19	0.36
σ (dB)	0.096	0.042	0.051	56.25%	46.88%
Yield (dB)	2.318	1.966	1.823	15.19%	21.35%
2.4 GHz					
μ (dB)	2.08	1.85	1.66	0.23	0.42
σ (dB)	0.096	0.042	0.05	56.25%	47.92%
Yield (dB)	2.368	1.976	1.81	16.55%	23.56%
4.0 GHz					
μ (dB)	3.26	2.61	2.29	0.65	0.97
σ (dB)	0.132	0.085	0.109	35.61%	17.42%
Yield (dB)	3.656	2.865	2.617	21.64%	28.42%

State-of-the-Art Comparison Table 2 provides a comparison between the proposed LNA and several recently published designs. The proposed LNA is implemented in 45 nm CMOS technology, which is a more advanced process node than the 65 nm-250 nm technologies used in several referenced works. The smaller feature size reduces parasitic capacitances and enables operation at lower supply voltages. As shown, the proposed design operates at 0.6 V supply, making it suitable for battery-powered and energy-constrained wireless front-ends. In terms of bandwidth, the proposed LNA supports a wide operating range of $1.8 - 4.0\text{ GHz}$ enabling compatibility with multiple communication standards. Compared to works limited to narrower frequency ranges, this broadband capability results from the use of programmable BDPR-based feedback network integrated with inductive source degeneration and self-cascode input configuration, which together allow tunable impedance matching, gain shaping, and noise figure improvement across a wide frequency spectrum. The input return loss of the proposed design reaches to 33.7 dB, indicating strong input matching and minimal reflection. This is significantly better than several prior designs that report values between 9.4 dB to 19 dB. The improved matching arises from the combined effects of source degeneration and the tunable high-resistance BDPR feedback network. The forward gain of the proposed LNA is 14 dB. While some designs achieve higher gain, they do so at the expense of increased power consumption or narrower bandwidth. In this design, the gain is intentionally balanced to optimize noise performance and stability across a broad operating band. The noise figure (NF) of $1.66 - 2.32\text{ dB}$ demonstrates competitive noise performance within the targeted $1.8 - 4.0\text{ GHz}$ range. Although certain narrowband designs achieve lower NF values, they typically lack reconfigurability and consume higher power. The NF in the proposed design remains below 3 dB across the full band due to the combined effect of inductive source degeneration and BDPR-based tunable feedback resistance. A key advantage of the proposed LNA is its low power consumption of 6 mW. Compared to prior designs consuming between 11.94 mW and 31.2 mW, this represents a substantial reduction in power while maintaining competitive gain and low-noise characteristics. These make the proposed architecture particularly suitable for portable, wearable, and IoT-based transceivers where power budget is limited. Table 2 also compares a figure of merit (FoM) of the proposed LNA with some recently published designs, where FoM is defined as

$$\text{FoM} = \frac{\text{Gain}_{\text{MAX}}[\text{dB}] \times \text{BW}[\text{GHz}]}{(\text{NF}_{\text{min}}[\text{dB}] - 1) \times P_{\text{DC}}[\text{mW}]} \quad (1)$$

Using the FoM expression, the proposed LNA achieves a maximum FoM of 7.89. This result indicates a favorable overall performance considering the gain, bandwidth, minimum noise figure, and DC power consumption compared to the designs listed in Table 2.

Table 2. Comparative Analysis of the state-of-the-Art LNAs.

SoA	Node (nm)	Supply (V)	Fr. Range (GHz)	Input Return Loss (dB)	Forward Gain (dB)	NF (dB)	IIP ₃ (dB)	Power (mW)	Area (mm ²)	FoM
Neha <i>et al.</i> ⁵ (2022)	250	5	1.3–2.3	8	17.5	1.25	21.5	750	0.325	10.1
Hamdi <i>et al.</i> ²⁴ (2022)	130	1.2	94	19	32	3	−16.7	19	—	—
Pu <i>et al.</i> ⁴ (2023)	28	1.1	0.3–3	27.5	24.6	2.0–2.5	1.3	19	—	3.49
Kim <i>et al.</i> ²⁵ (2023)	90	1.2	4.4–5	9.4	19.9	1.73	−15.4	11.94	0.72	1.37
Ben <i>et al.</i> ²⁶ (2024)	250	3.3	26–28	13.46	26	2.35	—	30	0.85	1.28
Zeng <i>et al.</i> ²⁷ (2024)	65	1.2	19–28.5	22	14.6	2.3–4	−9.6	25.6	0.255	4.16
Lee <i>et al.</i> ²⁸ (2024)	180	1	1.8–2.1	10.57	17.3	1.89–2.52	—	17.8	0.82	0.32
Reddy <i>et al.</i> ⁷ (2025)	180	1.8	3.1–10.6	16	17.5	5.9	−14.9	14.79	0.719	1.81
Murad <i>et al.</i> ²⁹ (2025)	130	1.2	24.5	27	21	5.6	−2	31.2	0.71	—
Ji <i>et al.</i> ³⁰ (2025)	90	1.2	15–28	42	19.3	2.9–3.6	−26	9.7	0.11	—
Cui <i>et al.</i> ³¹ (2025)	28	0.9	26–46	8	12.6	2.9–4.2	—	22	0.23	6.03
Park <i>et al.</i> ³² (2025)	28	1.2	6.1–41.5	8	10.5	4.7–7.3	3	25.2	0.36	3.95
Michailidis <i>et al.</i> ³³ (2025)	65	1.2	4–6.5	33	15.6	2.7	2.5	22	0.21	1.04
Lee <i>et al.</i> ³⁴ (2025)	65	2	9.2–18	6.1	24.7	2.3–3.5	—	11.4	0.23	—
Prashar <i>et al.</i> ¹⁴ (2026)	45	1.2	20–30	10	19	3	—	10.28	—	9.24
Li <i>et al.</i> ³⁵ (2026)	40	0.9	7–14	10	21.5	3	−4.6	25.5	0.21	2.95
This work (2026)	45	0.6	1.8–4	33.7	14.18	1.66–2.32	−2.5	6	0.0801	7.89

Conclusion

This work presents a BDPR-based programmable LNA implemented in the Cadence simulation environment using standard 45 nm PDK that can operate in 1.8 – 4.0 GHz wideband wireless frequency range. The proposed architecture combines the BDPR-based tunable feedback network with the conventional inductive source degeneration and self-cascode input stage to achieve wide-band impedance matching and improved linearity. Simulation results show a noise figure (NF) of 1.66 dB, a forward gain of 14.18 dB, and an input return loss of 33.7 dB at 3.6 GHz, and almost the same can be achieved across the 1.8 – 4.0 GHz frequency range through programmability of the bulk bias voltage (0.0 – 1.0 V). This frequency reconfigurability enables the coverage of multiple standards, including LTE Band 3 (1.8 GHz), UMTS/LTE Band 1 (2.1 GHz), Wi-Fi/Bluetooth/ZigBee (2.4 GHz), LTE Band 7 (2.6 GHz), and 5G NR sub-6 GHz (3.3 – 4.0 GHz). Close match with the post-layout simulation results reveals the robustness of the proposed LNA. Owing to its low power consumption (only 6 mW) and compact design (active area is $\approx 0.080 \text{ mm}^2$), the proposed LNA is well-suited for 5G, IoT, and wearable RF front-ends. The most important contribution of the proposed LNA is its tunable RF-metrics achievement through the bulk-bias-programmability even under real-world scenarios, as revealed from the PVT and Monte Carlo analyses. That is real-world factors which include process corner change, supply voltage fluctuations, temperature variation, and device-mismatch during fabrication- conventionally each of which has been handled by employing different techniques and/or additional circuitry, can be effectively handled by bulk-bias programmability. Therefore, the proposed BDPR-based tunable LNA offers a compact, robust, and low-power solution to achieve tunable RF metrics across the wideband 1.8 – 4.0 GHz wireless communication spectrum even under the real-world scenarios by leveraging a unique bulk-bias programmability without requiring additional circuitry.

Methods

Figure 1A shows the overall schematics of the proposed LNA, and integrates three key features: bulk-driven pseudo-resistor (BDPR)-based feedback, inductive source degeneration, and a self-cascode input stage (brief overview of these features is described in Section S1 of the Supplementary Material). Together, these elements achieve programmable wideband operation, including impedance matching, linearity, low-noise performance, and post-fabrication performance adjustment without changing the main RF signal path over the 1.8 – 4.0 GHz frequency range. The details of each of these features are described below.

The BDPR-based feedback network plays a central role in controlling the amplifier's input impedance and linearity and is the core concept in the proposed LNA. It is implemented using two MOSFETs (M3, M4) configured as a bulk-driven pseudo-resistor. In this arrangement, the source terminal of M3 is connected to the output node, while the drain and gate are tied together, forming a diode-connected structure. The BDPR operates in the subthreshold region, where it exhibits extremely high resistance (typically from hundreds of $\text{M}\Omega$ to several $\text{G}\Omega$ within a compact silicon footprint). The body terminal of the transistor serves as a control node, allowing the effective resistance of the BDPR to be tuned through the bulk bias voltage. This tunability helps maintain stable impedance matching and consistent gain across the wide operating frequency range. The bulk-driven configuration also enhances linearity. Using a BDPR instead of a passive resistor reduces chip area and lowers power consumption while maintaining the wideband feedback behavior required for broadband impedance matching. As a result, BDPR-based feedback is well-suited for compact and low-power RF front-ends, including biomedical and wearable devices where size and energy efficiency are critical.

The input stage is formed with a self-cascode input pair configuration, which uses two NMOS transistors, M1 and M2, connected in a stacked arrangement. In this structure, the source of M2 is tied to the drain of M1. Both transistors share a common gate bias. This configuration effectively increases the output resistance and enhances voltage gain without increasing the transistor dimensions (i.e., the chip area) or the power consumption. The lower device, M1, operates in the saturation region, while the upper device, M2, functions in the triode or linear region, forming a composite transistor with improved intrinsic gain. As a result, the self-cascode pair behaves like a single transistor with a higher effective output impedance and better isolation between the input and output nodes. The self-cascode structure also provides improved linearity and frequency response, making it attractive for wideband and low-power LNA designs. Because it achieves higher gain using standard transistors, it is well-suited for biomedical and wearable RF applications, where compactness, energy efficiency, and signal integrity are equally important.

In the input stage, the source terminal of the input transistor, M1, is connected to a degeneration inductor, L_s . The inductor introduces a series feedback path that plays several important roles in amplifier performance. First, the inclusion of L_s helps achieve input impedance matching between the LNA and the preceding stage or antenna, reducing signal reflections and power loss. Second, the inductive feedback improves the linearity of the amplifier by stabilizing the transconductance of M1 across different input levels. Third, it lowers the effective noise contribution of the input transistor by reducing the correlation between channel noise and gate-voltage noise. These combined benefits (better impedance matching, enhanced linearity, and reduced noise) make the inductive source degeneration technique especially suitable for low-power biomedical RF receivers, where maintaining signal integrity under tight power constraints is essential.

To further enhance frequency selectivity and noise suppression, the circuit includes an LC resonant tank comprising an inductor L1, a capacitor C1, and two resistors R1 and R2. Here, L1 has an inherent series resistance R1, and C1 is placed in parallel with R2. In the ideal case, if $R1 = 0$ and $R2 \rightarrow \infty$, the tank circuit behaves as a lossless resonator with a resonant frequency given by

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (2)$$

This resonant network helps shape the amplifier's frequency response, suppress out-of-band noise, and maintain stability across the desired bandwidth. The combination of BDPR feedback, self-cascode gain enhancement, and inductive degeneration makes the proposed LNA architecture highly effective for wideband, low-power biomedical and wearable RF applications.

The proposed LNA employs an input matching network, as shown in Fig. 1A(A), consisting of a source resistance (R_s), a gate inductor (L_g), a gate capacitance (C_2), and a biasing resistor (R_b), where

- R_s represents the source or antenna impedance typically of 50 Ω . Proper matching between R_s and the LNA input minimizes signal reflection and maximizes power transfer.
- L_g resonates with the gate-source intrinsic capacitances (C_{gs}) of the LNA MOSFETs to improve input matching and frequency tuning.
- C_2 creates a stable 50 Ω match across a broad frequency range and enhances the tradeoff between low power consumption, low noise, and high linearity in modern, high-performance LNA design.
- R_b , typically of high value, establishes DC bias while isolating the RF signal from the biasing network.

The mathematical expression of the input impedance, output impedance, transconductance, gain and noise figure of the proposed LNA are derived in Section S2 of the Supplementary Material.

Since hardware-level implementation of devices and projects incurs material and fabrication costs, as well as stress and processing time, a simulation approach is preferable for thorough investigation and analysis. Widely used simulation tools include MATLAB and Cadence. MATLAB can model, analyze, and characterize at the device level^{36,37}. On the other hand, Cadence has the ability of both device and circuit level modeling and characterization using Verilog-A models³⁸, SPICE models³⁹ and built-in TSMC models^{40,41}. Therefore, the proposed tunable BDPR-feedback based compact 1.8–4.0 GHz LNA has been designed and simulated using the Cadence Spectre simulator in standard 45 nm CMOS technology. The design parameters need to be selected to achieve an optimal trade-off among noise performance, gain, impedance matching, and power consumption. However, for MOSFET design in 45 nm technology, this requirement poses severe challenges because of the dominant short-channel effects (SCEs)⁴² and non-idealities⁴³. To overcome these challenges, MOSFET dimensions have been designed based on the recently used g_m over I_D technique^{21,40}, where the channel dimensions of all MOSFETs are calculated for chosen values of $\frac{g_m}{I_D}$ and I_D , and the estimated operating regime of each MOSFET, thereby bypassing the use of conventional long-channel FET equations which are questionable in downscaled MOSFETs due to SCEs and non-idealities. Transistor dimensions were chosen to balance transconductance and parasitic capacitances, ensuring broadband response across 1.8–4.0 GHz range. Table 3 lists the values of aspect ratios ($\frac{W}{L}$) of all four MOSFETs and the values of the passive components used in the simulation.

Table 3. LNA Design Parameters

Parameter	Value	Parameter	Value	MOSFET Aspect Ratio	Value
L ₁	15 nH	L _S	1 nH	$(\frac{W}{L})_1$	$\frac{300 \mu m}{90 nm}$
C ₁	100 fF	L _g	2.4 nH	$(\frac{W}{L})_2$	$\frac{500 \mu m}{90 nm}$
R ₁	40 Ω	C ₂	10 pF	$(\frac{W}{L})_3$	$\frac{50 \mu m}{2 \mu m}$
R ₂	400 K Ω	R _b	20 k Ω	$(\frac{W}{L})_4$	$\frac{50 \mu m}{2 \mu m}$

References

1. Ibrahim, A. A., Mohamed, H. A., Abdelghany, M. A. & Tammam, E. Flexible and frequency reconfigurable cpw-fed monopole antenna with frequency selective surface for iot applications. *Sci. Reports* **13**, 8409, DOI: [10.1038/s41598-023-34917-y](https://doi.org/10.1038/s41598-023-34917-y) (2023).

2. Liu, L. W. Y., Kandwal, A., Oster, T., Hofmann, K. & Chan, C. K. Wireless power transfer by spoof surface plasmon polaritons at ultrasonic frequencies. *Prog. In Electromagn. Res. M* **137**, 79–86, DOI: [10.2528/PIERM25121707](https://doi.org/10.2528/PIERM25121707) (2026).
3. Patel, S. K., Surve, J., Katkar, V. & Parmar, J. Machine learning assisted metamaterial-based reconfigurable antenna for low-cost portable electronic devices. *Sci. Reports* **12**, 12354, DOI: [10.1038/s41598-022-16678-2](https://doi.org/10.1038/s41598-022-16678-2) (2022).
4. Pu, Y. *et al.* A tri-mode reconfigurable receiver for gnss/nb-iot/ble with 68-db hr3 and 60-db imrr in 28-nm cmos. *IEEE Transactions on Very Large Scale Integration (VLSI) Syst.* **31**, 1140–1152, DOI: [10.1109/TVLSI.2023.3278859](https://doi.org/10.1109/TVLSI.2023.3278859) (2023).
5. Bajpai, N. & Chauhan, Y. S. A multi-variable double impedance matching network design algorithm with design example of a low noise amplifier. *Int. J. RF Microw. Comput. Eng.* **32**, e23462, DOI: <https://doi.org/10.1002/mmce.23462> (2022).
6. Bajpai, N., Maity, P., Shah, M., Das, A. & Chauhan, Y. S. An ultra-low noise figure and multi-band re-configurable low noise amplifier. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **70**, 1006–1016, DOI: [10.1109/TCSI.2022.3229135](https://doi.org/10.1109/TCSI.2022.3229135) (2023).
7. Snehiha Reddy, T. & Nath, V. A 180 nm cmos dual-mode lna with current reuse and double-resonance load for 2.4 ghz and 3.1–10.6 ghz wireless communication. *Sci. Reports* **15**, 93530, DOI: [10.1038/s41598-025-93530-3](https://doi.org/10.1038/s41598-025-93530-3) (2025).
8. Kim, D. & Im, D. A reconfigurable balun-lna and tunable filter with frequency-optimized harmonic rejection for sub-ghz and 2.4 ghz iot receivers. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **69**, 3164–3176, DOI: [10.1109/TCSI.2022.3169364](https://doi.org/10.1109/TCSI.2022.3169364) (2022).
9. Kumar, A. & Sharma, R. Design of 45nm CMOS front-end LNA for RF receiver. *VLSI J.* **12**, 115–124, DOI: <http://dx.doi.org/10.31838/jvcs/08.01.06> (2024).
10. Lourenço, N., Martins, R., Póvoa, R. & Horta, N. Review: Machine learning techniques in analog/RF integrated circuit modeling. *Integration, VLSI J.* **75**, 120–134, DOI: <https://doi.org/10.1016/j.vlsi.2020.11.006> (2020).
11. Kinget, P. R. Device mismatch and tradeoffs in the design of analog circuits. *IEEE J. Solid-State Circuits* **40**, 1212–1224, DOI: [10.1109/JSSC.2005.848021](https://doi.org/10.1109/JSSC.2005.848021) (2005).
12. Gómez, D., Sroka, M. & Gonzalez, J. Process and temperature compensation for RF low-noise amplifiers and mixers. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **56**, 2532–2545, DOI: [10.1109/TCSI.2009.2031707](https://doi.org/10.1109/TCSI.2009.2031707) (2009).
13. Pelgrom, M. J. M. & Welbers, H. P. T. The influence and modeling of process variation and device mismatch for analog/RF circuit design. In *Proceedings of the IEEE Custom Integrated Circuits Conference*, 165–172, DOI: [10.1109/CICC.2002.1004068](https://doi.org/10.1109/CICC.2002.1004068) (IEEE, 2002).
14. Prashar, R. & Kapur, G. Design of an inductive source degenerated non-volatile on-chip tunable low noise amplifier. *S@MACRONACCENT@adhan@MACRONACCENT@a* **51**, 76 (2026).
15. Aneja, A. & Li, X. J. Design and analysis of a continuously tunable low noise amplifier for software defined radio. *Sensors* **19**, 1273 (2019).
16. Parvizi, M., Allidina, K. & El-Gamal, M. N. An ultra-low-power wideband inductorless cmos lna with tunable active shunt-feedback. *IEEE Transactions on Microw. Theory Techniques* **64**, 1843–1853 (2016).
17. Kim, J. & Kwon, Y. High performance millimeter-wave image reject low-noise amplifier using inter-stage tunable resonators. *ETRI J.* **36**, 510–513 (2014).
18. Almonaier, A. M., Barakat, A. & Areed, N. F. Two gm/id design approaches for high-performance dual-resistive feedback noise-cancelling lna. *Int. J. Electron.* **112**, 1438–1456 (2025).
19. Belostotski, L. & Haslett, J. W. Noise figure optimization of inductively degenerated cmos lnas with integrated gate inductors. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **53**, 1409–1422 (2006).
20. Benatti, L., Zanotti, T. & Puglisi, F. M. Design strategies for optimized bulk-linearized mos pseudo-resistor. *Micromachines* **16**, 941 (2025).
21. Emon, M. Z. A., Apu, R. & Elamien, M. B. A 0.9 v, ultra-low-power ota with low nef and high cmrr for batteryless biomedical front-ends. *Electronics* **14**, DOI: <https://doi.org/10.3390/electronics14224520> (2025).
22. Razavi, B. *Design of analog CMOS integrated circuits* (Mc Graw Hill, 2005).
23. Cadence Design Systems, Inc. Accelerating monte carlo analysis at advanced nodes. White Paper, Cadence Design Systems, Inc. (2019). Accessed: February 2026.
24. Hamdi, A. Design and performance analysis of w-band low noise amplifier for rfic-5g mobile systems. *Mob. Information Syst.* **2022**, 8323322 (2022).

25. Kim, M.-S. & Yoo, S.-S. Rf-soi low-noise amplifier using rc feedback and series inductive-peaking techniques for 5g new radio application. *Sensors* **23**, 5808 (2023).
26. Ben Hammadi, A., Doukkali, M. A., Descamps, P. & Niamien, C. A 26–28 ghz, two-stage, low-noise amplifier for fifth-generation radio frequency and millimeter-wave applications. *Sensors* **24**, 2237 (2024).
27. Zeng, H., Huang, Z., Tan, T., Li, Y. & Li, X. Parasitic-aware analysis and design of a wideband gm-boost low noise amplifier at k-band. *IEEE Transactions on Circuits Syst. II: Express Briefs* **72**, 138–142 (2024).
28. Lee, B.-C. *et al.* Development of an l-band low-noise amplifier for gps rf front-end receiver. *The J. Korean Inst. Electromagn. Eng. Sci.* **35**, 180–183 (2024).
29. Murad, S. A. Z., Abd Manaf, A., Rhaffor, N. A. & Zawawi, R. A. Design of a 24.5 ghz cmos low noise amplifier using 0.13- μm technology for 6g wireless applications. *Jurnal Teknologi (Sciences & Eng.* **87**, 53–61 (2025).
30. Ji, H., Li, Z., Zhang, H. & Wan, C. A 15–28 ghz low-noise amplifier with 0.75-db gain ripple across the full k-band. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **72**, 7671–7680 (2025).
31. Cui, Y., Ma, K. & Hu, K. An ultra-wideband low-noise amplifier with a new cross-coupling noise-canceling technique for 28 nm cmos technology. *Electronics* **14**, 1904 (2025).
32. Park, Y., Choe, K. & Jeon, S. A 6.1-to-41.5 ghz cmos low-noise amplifier for wideband and highly linear applications. *J. Electromagn. Eng. Sci.* **25**, 154–159 (2025).
33. Michailidis, A., Chatzis, A., Tsimpou, P., Gogolou, V. & Noulis, T. A unified design methodology for front-end rf/mmwave receivers. *Electronics* **14**, 235 (2025).
34. Lee, N., Kim, J., Hong, S. K., Oh, J. *et al.* A 9.2–18-ghz sub-3.5-db nf cmos low noise amplifier using current-reuse stacked inverter with inductive series peaking. *IEEE Access* **13**, 82421–82430 (2025).
35. Li, Z., Zhang, Y., Wei, Z., Tang, X. & Huang, F. An x-band cmos low noise amplifier with a three-coupled transformer based gm-boosting structure for phased array receivers. *IEICE Electron. Express* 23–20250644 (2026).
36. Islam, M. J. & Chowdhury, M. I. B. Analytical modeling of base transit time in sige-hbts considering recombination effects under intermediate injection levels. *Int. J. Numer. Model. Electron. Networks, Devices Fields* **39**, e70144, DOI: <https://doi.org/10.1002/jnm.70144> (2026).
37. Huqe, M. R., Reba, S. I., Uddin, M. S. & Chowdhury, M. I. B. Analytical modeling of the base dark saturation current of drift-field solar cells considering auger recombination. *Int. J. Renew. Energy Res.* **3**, 420–426 (2013).
38. Islam, M. J. & Bahar Chowdhury, M. I. A subpicowatt vertical tunnel fet ph sensor with near-nernstian sensitivity for point-of-care diagnostics. *ACS Appl. Electron. Mater.* **8**, 3530–3543 (2026).
39. Emon, M. Z. A., Paul, P. C., Mayeen, N., Alam, N. & Chowdhury, M. I. B. Switching power of cnfet based 6-transistor 1-bit fast adder implemented using cadence. *Adv. Math. Sci. J.* **9**, 3581–3592 (2020).
40. Emon, M. Z. A., Salim, K. M. & Chowdhury, M. I. B. Design and analysis of a high-gain, low-noise, and low-power analog front end for electrocardiogram acquisition in 45 nm technology using gm/id method. *Electronics* **13**, 2190 (2024).
41. Emon, M. Z. A. & Chowdhury, M. I. B. Low threshold voltage mosfet-a potential candidate for biomedical ic design. In *2024 International Conference on Advances in Computing, Communication, Electrical, and Smart Systems (iCACCESS)*, 1–6 (IEEE, 2024).
42. Chowdhury, M. I. B. Ion-sensitive vertical tunnel field-effect transistor for highly sensitive, low power, low ph-resolution ph sensing. *IEEE Sensors Lett.* **8**, 1–4 (2023).
43. Amina, M., Biswas, P., Ullah, A. & Chowdhury, I. B. Analysis of common-mode rejection ratio of a cmos differential amplifier considering all the non-idealities. In *2015 2nd International Conference on Electrical Information and Communication Technologies (EICT)*, 234–238 (IEEE, 2015).

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Author contributions statement

R.A. conducted the simulations, M.J.I. and R.A. prepared the figures and the draft of the manuscript, M.I.B.C and R.A. derived the mathematical expressions and analyzed the results, M.I.B.C supervised the whole project, H.S.M. assisted in manuscript editing and validation of results. M.I.B.C and H.S.M. provided for financial support in this work. All authors reviewed and approved the final manuscript.

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Data availability

The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Competing interests

The authors declare no competing interests.

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