

# Supplementary Information: A BDPR-Feedback-Based LNA with Programmable RF Metrics in Real-World Settings for Wideband Wireless Communication Systems

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## Supplementary Note 1

### Inductive Source Degeneration

Fig. S1 shows the inductive source degeneration topology, a common configuration used in conventional LNA designs, where Fig. S1(a) shows a simple inductive source degeneration circuit, and Fig. S1(b) shows its small-signal equivalent circuit. The real part ( $R_{in}$  of the input impedance ( $Z_{in}$ ) and the noise figure (NF) of this circuit can be expressed as [1]-

$$R_{in} = \frac{g_{m1}L_s}{C_{gs1}} = \omega_T L_s \quad (S1)$$

$$NF = 1 + g_{m1}R_s\gamma \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (S2)$$

where,  $C_{gs1}$  is the gate-source capacitance of M1 MOSFET,  $g_{m1}$  is its transconductance,  $\omega_0$  is the operating frequency, and  $\omega_T = \frac{g_{m1}}{C_{gs1}}$  is the transit frequency.

From Eqns. (S1) and (S2), it is clear that the input impedance and noise performance of an inductive source-degenerated LNA are highly dependent on the value of the source inductor,  $L_s$ . The inductor directly influences the real and imaginary components of the input impedance, allowing the designer to match the amplifier input to the source impedance (typically 50  $\Omega$ ). At the same time,  $L_s$  affects the noise figure, since it modifies the voltage and current noise correlation at the transistor input. By selecting an appropriate value of  $L_s$ , designers can achieve a balanced trade-off between impedance matching and noise optimization. A larger  $L_s$  improves matching and linearity but can reduce gain and increase chip area, while a smaller  $L_s$  minimizes area but may degrade noise performance. Careful tuning of this parameter is therefore essential to meet both bandwidth and low-noise requirements in wideband, low-power RF designs—particularly in biomedical and wearable receiver applications, where power efficiency and signal sensitivity are critical.

### Resistive Feedback

Figure S2 illustrates the resistive feedback topology. In this configuration, a feedback resistor  $R_F$  is connected between the output and input nodes of the M1 MOSFET. This resistor senses the output voltage and routes a portion of it back to the input, which stabilizes the gain and supports wideband input impedance matching.

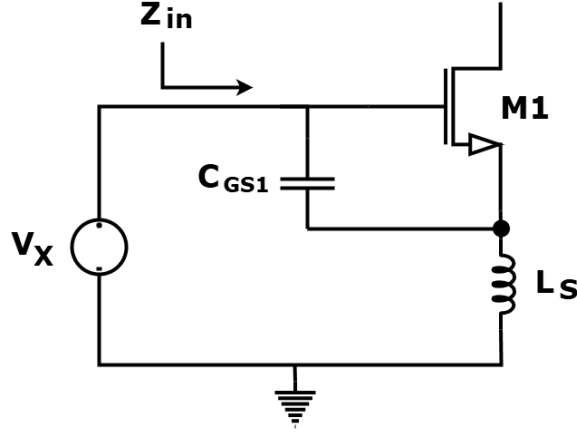


Figure S1: Inductive source degeneration

However, implementing large-valued resistors in standard CMOS technology is area-inefficient and introduces additional thermal noise, which can degrade the overall noise performance of the LNA [2]. To overcome these limitations, the conventional resistor  $R_F$  can be replaced with a bulk-driven pseudo-resistor (BDPR), realized using a pMOS transistor.

#### $R_F$ Calculation

The feedback resistance,  $R_F$  is the incremental drain-to-source resistance ( $r_o$ ) of the MOSFET illustrated in Figure S2, where  $r_o$  can be deduced from the drain-to-source conductance ( $g_o = \frac{1}{r_o}$ ) as-

$$\begin{aligned} g_o &= \frac{\partial I_D}{\partial V_{DS}} = I_{D0} \lambda \\ &= \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Th})^2 \times \lambda \end{aligned} \quad (S3)$$

$$\begin{aligned} r_o &= \frac{1}{I_{D0} \lambda} \\ &= \frac{1}{\frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Th})^2 \times \lambda} \end{aligned} \quad (S4)$$

where  $\lambda$  is the channel length modulation coefficient,  $I_{D0}$  is the drain current without channel length modulation,  $\mu_n$  is the electron mobility,  $C_{ox}$  is the oxide capacitance, and  $V_{Th}$  is the threshold voltage which can be expressed as [4]-

$$V_{Th} = V_{Th0} + \eta \left( \sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \quad (S5)$$

where,  $V_{Th0}$  is the threshold voltage when the bulk-to-source voltage ( $V_{SB} = V_S - V_{bulk}$ ) is zero,  $\phi_F$  is the Fermi potential, and  $\eta$  is the body-effect coefficient, typically ranging from 0.1 to 0.3 depending on the technology node and substrate doping profile [3], and can be expressed as [4]-

$$\eta = \frac{g_{mb}}{g_m} \quad (S6)$$

Therefore, when  $V_{bulk}$  [termed hereafter as bulk bias] increases (decreases) keeping  $V_S$  as constant,  $V_{Th}$  increases (decreases) [Eqn. (S5)],  $r_o$  increases (decreases) and hence, the effective resistance of the BDPR ( $R_F$ ) increases (decreases). In other words,  $R_F$  can be varied by tuning  $V_{bulk}$ . This tunability of  $R_F$  is the core idea of the LNA proposed in this work.

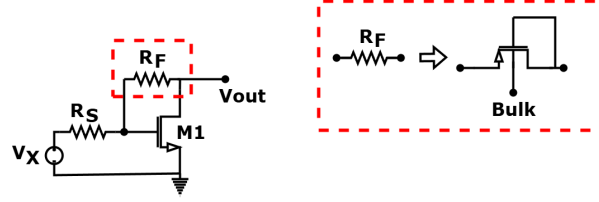


Figure S2: Resistor replaced by bulk-driven pseudo resistor (BDPR)

A bulk-driven pseudo-resistor (BDPR) composed of pMOS devices can be cascaded to increase its equivalent resistance. Fig. S3 shows the configuration for  $N = 2$  devices in series. Because of the series stacking  $R_F$  can be expressed as [4]-

$$R_F = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) \times r_{o1}r_{o2}$$

Assuming that the transistors (MR1 and MR2) are identical (i.e.  $g_{m1} = g_{m2} = g_m$  and  $r_{o1} = r_{o2} = r_o$ ) and employing the relation between  $g_{mb}$  and  $g_m$  [Eqn. (S6)] leads to the above expression as-

$$\begin{aligned} R_F &= 2r_o + g_m r_o^2 (1 + \eta) \\ &\approx g_m r_o^2 (1 + \eta) \end{aligned} \quad (S7)$$

where the approximation  $g_m r_o \gg 1$  holds making the gain-booster term dominant. Eqn. (S7) illustrates that the BDPR ( $R_F$ ) achieves extremely large resistances due to the intrinsic gain multiplication of each stacked MOSFET when operating in the subthreshold region. Moreover, increasing the number (N) of stacked devices further enhances  $R_F$  almost exponentially, enabling G $\Omega$ -level resistances in deep-submicron CMOS without excessive area consumption [5].

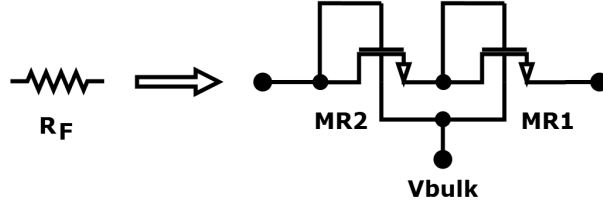


Figure S3: Bulk-driven pseudo-resistor (BDPR) with  $N = 2$  pMOS devices in series.

### Noise Calculation

The noise contribution of a BDPR with  $N = 2$  can be determined as follows. Because it is non-linear, its noise behavior depends on its operating region (zero-bias vs. non-zero-bias). The noise produced by the BDPR consists of two primary components:

- Thermal Noise (Nyquist Noise): Dominates at higher frequencies and zero-bias conditions.
- Bulk-Driven Flicker (1/f) Noise: Becomes significant at low frequencies (common in biomedical applications) and increases when a DC flows through the resistor.

When no DC is flowing, the BDPR acts like a passive component. Its thermal noise current spectral density is governed by the Nyquist-Johnson expression:

$$\overline{i_{n,th}^2} = \frac{4kT}{R_F} \quad (S8)$$

where  $R_F$  is extremely high for a PMOS in operating in the subthreshold regime, and varies exponentially with  $V_{BS}$ . For  $N = 2$ ,  $R_F$  increases further, which decreases the current noise spectral density, as  $\overline{i_n^2} \propto 1/R$ .

The bulk-driven flicker noise is typically modeled as a voltage source at the gate. For a bulk-driven device, the noise is referred to the input terminal (the bulk) by the ratio of transconductances ( $g_m/g_{mb}$ ) as -

$$\overline{v_{ni,F}^2} = \frac{4kT\gamma(g_{d0,MR}) + \frac{K_p g_{m,MR}^2}{C_{ox}WLf}}{(g_{mb,MR})^2} \quad (S9)$$

where  $g_{d0,MR}$  is the drain conductance,  $K_p = \mu_p C_{ox} (\frac{W}{L})$  is the process parameter,  $\mu_p$  is the hole mobility, and  $f$  is the frequency. Because the bulk transconductance ( $g_{mb}$ ) is smaller than the gate transconductance ( $g_m$ ), the input-referred flicker noise of a bulk-driven transistor is higher (typically by a factor of 3 to 10) than a standard gate-driven device. For an  $N = 2$  BDPR feedback network, where two identical PMOS transistors are connected in series, the total input-referred noise is derived by summing the noise contributions of each individual stage. Therefore, the total noise voltage for  $N = 2$  is:

$$\begin{aligned} \overline{v_{ni,F}^2} &= \overline{v_{ni,bulk1}^2} + \overline{v_{ni,bulk2}^2} \\ &= 2 \times \overline{v_{ni,bulk}^2} \\ &= 2 \left[ \frac{4kT\gamma(g_{d0,MR}) + \frac{K_p g_{m,MR}^2}{C_{ox}WLf}}{(g_{mb,MR})^2} \right] \end{aligned} \quad (S10)$$

Because the BDPR provides a very high resistance ( $R_F$  is in the  $G\Omega$  range), the thermal term  $4kT/R_F$  is usually negligible. However, the flicker noise term (scaled by  $2/\eta^2$ ) can become dominant at low frequencies, significantly impacting the Noise Figure, which is the penalty for stacking active devices in a bulk-driven configuration.

### Self Cascode Input Pair

Figure S4 shows the self-cascode input pair configuration, which uses two NMOS transistors, M1 and M2, connected in a stacked arrangement. The small-signal output resistance  $R_{out}$  and the overall transconductance  $G_m$  of the self-cascode stage is given by [4]

$$R_{out} = r_{o1} + r_{o2} + (g_{m2}r_{o2})r_{o1} \quad (S11)$$

$$\begin{aligned} G_m &= \frac{g_{m2}g_{m1}r_{o1} + g_{mb2}g_{m1}r_{o1} + g_{m1}\frac{r_{o1}}{r_{o2}} + g_{m2}}{1 + \frac{r_{o1}}{r_{o2}} + (g_{m2} + g_{mb2})r_{o1}} \\ &\approx g_{m1} \end{aligned} \quad (S12)$$

where  $g_{m1}$  ( $g_{m2}$ ) and  $r_{o1}$  ( $r_{o2}$ ) is the transconductance and output resistance of M1 (M2), respectively.

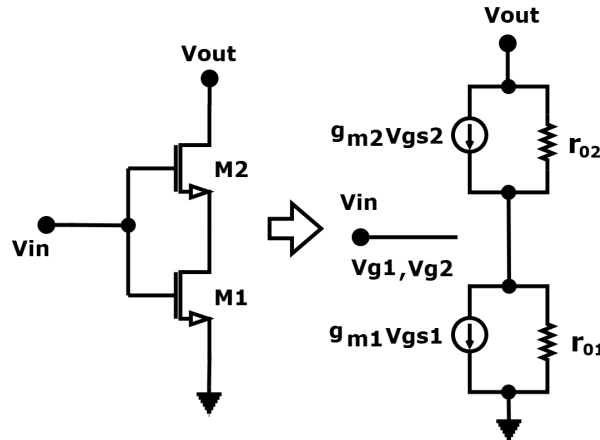


Figure S4: input pair small signal circuit

## Supplementary Note 2: Mathematical Analysis of the Proposed LNA

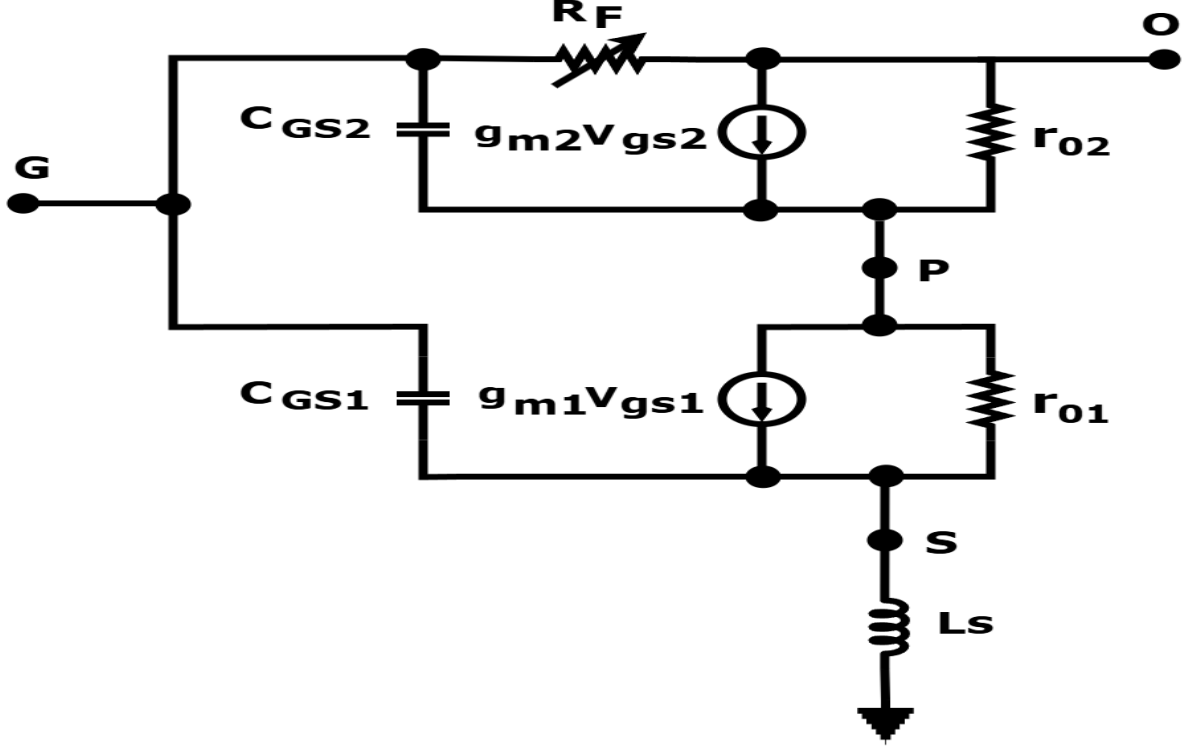


Figure S5: The small-signal equivalent circuit of the proposed LNA.

This section presents the mathematical analysis of the proposed LNA. The expressions of the input impedance ( $Z_{in}$ ), the output impedance ( $Z_{out}$ ), the effective conductance ( $G_m$ ), the voltage gain,  $A_v$ , and the impedance looking through the intermediate node have been derived from the analysis of the small-signal equivalent circuit of the proposed LNA, as shown in Fig. S5. The small-signal equivalent model of the proposed LNA represents the circuit behavior under linear operating conditions. It captures how the device parameters influence gain, input matching, and noise performance. In this model, the transistors are characterized by their transconductance ( $g_{m1}$ ,  $g_{m2}$ ) and gate-to-source capacitances ( $C_{gs1}$ ,  $C_{gs2}$ ). These parameters describe how the input voltage variations are converted into current and how capacitive effects influence high-frequency behavior.

The variable feedback resistor ( $R_F$ ), as shown in Fig. S5(B), models the bulk-driven pseudo-resistor (BDPR) network, which provides controlled negative feedback to stabilize the gain and improve linearity. This feedback path also helps to achieve wideband input matching by balancing the input impedance across the operating frequency range. The source degeneration inductor ( $L_S$ ), as shown in Fig. S5(B), introduces local feedback that further enhances input matching and reduces distortion. It improves noise performance by minimizing the noise contribution of the input transistors while maintaining a reasonable gain level. The biasing resistor  $R_b$  is omitted in the equivalent circuit model for convenience, as it solely affects the DC biasing.

### Expression of $Z_{in}$

To derive the expression of  $Z_{in}$ , a test voltage  $V_x$  is applied to the shorted-gate input node ('G') for which an input current  $I_x$  flows to the gate node. Under this condition, KCL has been applied at the output node ('O'), 'S' (source of M1) and 'P' (intermediate node), as follows:

1. KCL at the source node of M1 (node ‘S’) gives-

$$\begin{aligned}
\frac{V_s}{sL_s} &= (sC_{fgs1} + g_{m1})(V_{in} - V_s) + \frac{V_p - V_s}{r_{o1}} \\
\Rightarrow V_s &= \frac{(g_{m1} + sC_{gs1})V_{in} + \left(\frac{1}{r_{o1}}\right)V_p}{g_{m1} + \frac{1}{r_{o1}} + sC_{gs1} + \frac{1}{sL_s}} \\
&= a_1V_{in} + b_1V_p
\end{aligned} \tag{S13}$$

2. KCL at the intermediate node (node ‘P’) is-

$$\begin{aligned}
g_{m1}(V_{in} - V_s) + \frac{V_{in} - V_s}{r_{o1}} &= \frac{V_{out} - V_p}{r_{o2}} \\
&+ (g_{m2} + sC_{gs2})(V_{in} - V_p) \\
\Rightarrow V_s &= -\left(\frac{g_{m2} + sC_{gs2} - g_{m1} + \frac{A_v}{r_{o1}}}{g_{m1} + \frac{1}{r_{o1}}}\right)V_{in} \\
&+ \left(\frac{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + sC_{gs2}}{g_{m1} + \frac{1}{r_{o1}}}\right)V_p \\
&= -a_2V_{in} + b_2V_p
\end{aligned} \tag{S14}$$

where  $A_v = \frac{V_{out}}{V_{in}}$ .

3. KCL at the shorted gate input node (node ‘G’) is-

$$I_x = I_{Cgs1} + I_{Cgs2} + I_{Rf} \tag{S15}$$

with

$$\begin{aligned}
I_{Cgs1} &= sC_{gs1}(V_{in} - V_s) \\
&= sC_{gs1}V_{in}\left(1 - \frac{V_s}{V_{in}}\right) \\
&= sC_{gs1}\left[1 - a_1 - \frac{b_1(a_1 + a_2)}{b_2 - b_1}\right]V_{in}
\end{aligned} \tag{S16}$$

$$= Y_{M1}V_{in} \tag{S17}$$

$$\begin{aligned}
I_{Cgs2} &= sC_{gs2}(V_{in} - V_p) \\
&= sC_{gs2}V_{in}\left(1 - \frac{V_p}{V_{in}}\right) \\
&= sC_{gs2}\left(1 - \frac{a_1 + a_2}{b_2 - b_1}\right)V_{in}
\end{aligned} \tag{S18}$$

$$= Y_{M2}V_{in} \tag{S19}$$

$$\begin{aligned}
I_{Rf} &= \frac{V_{in} - V_{out}}{R_F} \\
&= \left(\frac{1 - A_v}{R_F}\right)V_{in}
\end{aligned} \tag{S20}$$

Solving Eqns. (S13) and (S14) gives-

$$V_p = \left(\frac{a_1 + a_2}{b_2 - b_1}\right)V_{in} = AV_{in} \tag{S21}$$

$$V_s = \left[a_1 + \frac{b_1(a_1 + a_2)}{b_2 - b_1}\right]V_{in} = BV_{in} \tag{S22}$$

Therefore, the input impedance,  $Z_{in}$  can be expressed as-

$$\begin{aligned} Z_{in} &= \frac{V_{in}}{I_x} \\ &= \frac{1}{Y_{M1} + Y_{M2} + \frac{1-A_v}{R_F}} \end{aligned} \quad (S23)$$

Neglecting the parasitic capacitance  $C_{gs2}$ , and assuming that  $r_{o1}$  and  $r_{o2}$  is assumed to be large, which is true for the MOSFETs with channel length greater than  $1 \mu\text{m}$ , the above expression can be simplified to -

$$Z_{in} \approx \frac{1}{Y_{M1} + \frac{1-A_v}{R_F}} \quad (S24)$$

with

$$Y_{M1} \approx sC_{gs1} \times \frac{\frac{1}{sL_s}}{g_{m1} + sC_{gs1} + \frac{1}{sL_s}} \quad (S25)$$

which leads to the real part of  $Z_{in}$  as-

$$R_{in} \approx \frac{1}{\frac{C_{gs1}}{g_{m1}L_s} + \frac{1-A_v}{R_F}} \quad (S26)$$

The above expression of  $R_{in}$  shunts the resistive term,  $\frac{g_{m1}L_s}{C_{gs1}}$  (the well-known expression of the input resistance for an LNA with inductive source degeneration) with the effects of BDPR-based tunable  $R_F$ , given by  $\frac{R_F}{1-A_v}$ . Therefore, the effects of bulk bias of the proposed LNA provides the tunability through  $R_F$  to match with  $R_{in}$ .

## Expression of $Z_{out}$

To derive the expression for  $Z_{out}$ , a test voltage  $V_x$  has been applied at the output node (node 'O') with input grounded ( $v_{in}=0$ ), for which a current  $I_x$  flows through the output node. Under this condition, KCL has been applied at the nodes 'O', 'S', and 'P', as follows:

1. At the output node 'O'

$$\begin{aligned} I_x &= \frac{V_x - V_p}{r_{o2}} + g_{m2}(0 - V_p) + \frac{V_x - 0}{R_F} \\ &= \left( \frac{1}{R_F} + \frac{1}{r_{o2}} \right) V_x - \left( g_{m2} + \frac{1}{r_{o2}} \right) V_p \end{aligned} \quad (S27)$$

2. At the intermediate node 'P', the current coming out from M2 and flowing into M1 is  $I_p$ . Therefore, the impedance looking through this node is  $Z_p = \frac{V_p}{I_p}$ . KCL at this node for M1 MOSFET results in-

$$\begin{aligned} I_p &= g_{m1}(0 - V_s) + \frac{V_p - V_s}{r_{o1}} \\ &= \frac{V_p}{r_{o1}} - \left( g_{m1} + \frac{1}{r_{o1}} \right) V_s \end{aligned} \quad (S28)$$

Plugging the expression of  $V_s$ , given by Eqn. (S22) where  $V_{in} = 0$ , modifies the above equation as-

$$I_p = \frac{V_p}{r_{o1}} - \frac{\left( g_{m1} + \frac{1}{r_{o1}} \right) \times \frac{1}{r_{o1}}}{g_{m1} + \frac{1}{r_{o1}} + \frac{1}{sL_s} + sC_{gs1}} \times V_p \quad (S29)$$

Therefore, the impedance looking through the drain of M1 ( $Z_p$ ) can be obtained as-

$$\begin{aligned} Z_p &= \frac{V_p}{I_p} \\ &= \frac{r_{o1} + (1 + g_{m1}r_{o1})sL_s + s^2L_sC_{gs1}r_{o1}}{1 + s^2L_sC_{gs1}} \end{aligned} \quad (\text{S30})$$

3. KCL at node 'P' for M2 MOSFET results in -

$$\begin{aligned} I_p &= \frac{V_p}{Z_p} = \frac{V_x - V_p}{r_{o2}} + (g_{m2} + sC_{gs2})(0 - V_p) \\ \Rightarrow V_p &= \left[ \frac{\frac{Z_p}{r_{o2}}}{1 + \left( g_{m2} + \frac{1}{r_{o2} + sC_{gs2}} \right)} \right] \times V_x \end{aligned} \quad (\text{S31})$$

Finally, combining the above expression of  $V_p$  with Eqn. (S27) gives the expression of  $Z_{out}$  as -

$$\begin{aligned} Z_{out} &= \frac{1}{\frac{1}{R_F} + \frac{1 + sC_{gs2}Z_p}{r_{o2} + [1 + (g_{m2} + C_{gs2})r_{o2}]Z_p}} \\ &= R_F || Z_0 \end{aligned} \quad (\text{S32})$$

where  $Z_0$  in the above equation represents the impedance seen looking through the drain terminal of M2 MOSFET, given by

$$Z_0 = \frac{r_{o2} + [1 + (g_{m2} + C_{gs2})r_{o2}]Z_p}{1 + sC_{gs2}Z_p} \quad (\text{S33})$$

and the tunable BDPR feedback resistor ( $R_F$ ) shunts this  $Z_0$  resulting in a tunable  $Z_{out}$ .

When parasitic capacitances  $C_{gs1}$ ,  $C_{gs2} \rightarrow 0$  are neglected, the expressions of  $Z_p$  and  $Z_0$  reduces to -

$$\begin{aligned} Z_p &\approx r_{o1} + (1 + g_{m1}r_{o1})sL_s \\ &= r_{o1} + sL_s + (g_{m1}r_{o1})sL_s \\ Z_0 &\approx r_{o2} + (1 + g_{m2}r_{o2})Z_p \\ &= r_{o2} + Z_p + (g_{m2}r_{o2})Z_p \end{aligned}$$

At DC or low frequencies,  $Z_p$  and  $Z_0$  reduces to-

$$\begin{aligned} Z_p &\approx r_{o1} \\ Z_0 &\approx r_{o2} + (1 + g_{m2}r_{o2})r_{o1} \\ &= r_{o1} + r_{o2} + (g_{m2}r_{o2})r_{o1} \end{aligned}$$

Therefore,  $Z_0$  of the proposed LNA with inductive source degeneration and BDPR-based tunable feedback resistor exactly resembles with that of a simple cascoded NMOS input pair at low frequencies, as seen from Eqns. (S11) and (S34). However, at high frequencies, the inductive source degeneration increases  $Z_p$ , and hence, increases  $Z_0$  and  $Z_{out}$  dramatically owing to the cascoding effect. Although the feedback resistor ( $R_F$ ) reduces  $Z_{out}$  due to its shunt connection with  $Z_0$ , its tunability offers flexibility to smooth  $Z_{out}$  over a wider frequency range- an attractive and desirable feature for the proposed LNA.

## Expression of $G_m$ and $A_V$

To derive the expression for  $G_m$ , the output node (node 'O') is ac-grounded. This makes the feedback resistance  $R_F$  as a load from the gate (node 'G') to the ground. The current  $I_{out}$  flows from the output node. Under this condition, KCL has been applied at the nodes 'O', 'G' (input node), 'S' (source of M1) and 'P' (intermediate node).

1. At the output node ‘O’

$$\begin{aligned} I_{out} &= \frac{0 - V_p}{r_{o2}} + g_{m2}(V_{in} - V_p) + \frac{0 - V_{in}}{R_F} \\ &= \left(g_{m2} - \frac{1}{R_F}\right)V_{in} - \left(g_{m2} + \frac{1}{r_{o2}}\right)V_p \end{aligned} \quad (\text{S34})$$

2. At the intermediate node ‘P’

$$\begin{aligned} \frac{V_p - V_s}{r_{o1}} + g_{m1}(V_{in} - V_s) &= \frac{0 - V_p}{r_{o2}} \\ &+ (g_{m2} + sC_{gs2})(V_{in} - V_p) \\ \Rightarrow \left(g_{m1} + \frac{1}{r_{o1}}\right)V_s &= \left(g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + sC_{gs2}\right)V_p \\ &+ (g_{m1} - g_{m2} - sC_{gs2})V_{in} \end{aligned} \quad (\text{S35})$$

3. At the source node ‘S’

$$\begin{aligned} \frac{V_s}{sL_s} &= \frac{V_p - V_s}{r_{o1}} + (g_{m1} + sC_{gs1})(V_{in} - V_s) \\ \Rightarrow V_s &= \frac{(g_{m1} + sC_{gs1})V_{in} + \frac{V_p}{r_{o1}}}{g_{m1} + \frac{1}{r_{o1}} + sC_{gs1} + \frac{1}{sL_s}} \end{aligned} \quad (\text{S36})$$

Substituting the expression of  $V_s$  in Eqn. (S35) relates  $V_p$  with  $V_{in}$  as-

$$V_p = \left(\frac{num}{den}\right)V_{in} = EV_{in} \quad (\text{S37})$$

with

$$\begin{aligned} num &= (g_{m2} + sC_{gs2})\left(g_{m1} + \frac{1}{r_{o1}} + sC_{gs1} + \frac{1}{sL_s}\right) \\ &+ \frac{sC_{gs1}}{r_{o1}} - \frac{g_{m1}}{sL_s} \\ den &= \left(g_{m1} + \frac{1}{r_{o1}} + sC_{gs1} + \frac{1}{sL_s}\right) \\ &\times \left(\frac{1}{r_{o2}} + g_{m2} + sC_{gs2}\right) + \frac{\left(sC_{gs1} + \frac{1}{sL_s}\right)}{r_{o1}} \end{aligned}$$

Now, combining Eqns. (S34) and (S37), gives the expression of  $G_m$  as-

$$\begin{aligned} G_m &= \frac{I_{out}}{G_m} \\ &= g_{m2}(1 - E) - \frac{E}{r_{o2}} - \frac{1}{R_F} \end{aligned} \quad (\text{S38})$$

If the effects of parasitic capacitances ( $C_{gs1}$ ,  $C_{gs2}$ ) and the output resistances ( $r_{o1}$ ,  $r_{o2}$ ) of the M1, M2 are neglected, the expression of  $G_m$  is reduced to-

$$G_m = \frac{1}{\frac{1}{g_{m1}} + sL_s} - \frac{1}{R_F} \quad (\text{S39})$$

At low frequencies, the above expression is simplified to-

$$G_m = g_{m1} - \frac{1}{R_F} \quad (\text{S40})$$

which is similar to the expression of  $G_m$  obtained for a simple cascoded input pair [Eqn. (S12)], except for the presence of the BDPR-based feedback resistor,  $R_F$ . Therefore, the overall transconductance is dominated by the M1 MOSFET. However, the roll-off of  $G_m$  occurs at high frequencies due to the presence of the degeneration inductance,  $L_s$ . On the other hand, the BDPR-based feedback resistor ( $R_F$ ) reduces  $G_m$  at the cost of gain stabilization. Since  $R_F$  is BDPR-based, these effects can be tunable by adjusting the bulk bias voltage ( $V_{bulk}$ ) over a wider frequency range. Finally, the overall gain,  $A_v$  can be deduced from the relation [4]-

$$A_v = -G_m \times (Z_{out} || Z_L) \quad (\text{S41})$$

where  $Z_L$  is the load impedance.

## Expression of Noise Figure (NF)

The primary noise sources are:

- Source Resistance ( $R_{in}$ ) Thermal Noise:

$$\overline{v_{n,Rin}^2} = 4kTR_{in} \quad (\text{S42})$$

- Bottom NMOS (M1) Channel Thermal Noise:

$$\begin{aligned} \overline{i_{n,M1}^2} &= 4kT\gamma(g_{d01}) \\ &= 4kT\left(\frac{\gamma}{\alpha}\right)g_{m1} \end{aligned} \quad (\text{S43})$$

- Top NMOS (M2) Channel Thermal Noise:

$$\begin{aligned} \overline{i_{n,M2}^2} &= 4kT\gamma(g_{d02}) \\ &= 4kT\left(\frac{\gamma}{\alpha}\right)g_{m2} \end{aligned} \quad (\text{S44})$$

- BDPR-based Feedback Resistor Noise:

$$\overline{i_{n,FB}^2} = \frac{4kT}{R_F} + \left(g_{mb,MR}^2 \times \overline{v_{ni,BDPR}^2}\right) \quad (\text{S45})$$

where  $\gamma$  is channel thermal noise coefficient, and  $g_{d01}$  ( $g_{d02}$ ) is the drain conductance of M1 (M2) which is related to its transconductance,  $g_{m1}$  ( $g_{m2}$ ) as-

$$g_{m1,2} = \alpha g_{d01,2} \quad (\text{S46})$$

The total output noise voltage spectral density  $\overline{v_{n,out}^2}$  is the sum of these independent sources:

$$\begin{aligned} \overline{v_{n,tot,out}^2} &= \overline{v_{n,Rin,out}^2} + \overline{v_{n,M1,out}^2} + \overline{v_{n,M2,out}^2} + \overline{v_{n,FB}^2} \\ &= \overline{v_{n,Rin}^2} \times |A_v|^2 + \overline{i_{n,M1}^2} \times |Z_p|^2 \\ &\quad + \overline{i_{n,M2}^2} \times |Z_{out}|^2 + \overline{i_{n,FB}^2} \times |Z_{out}|^2 \end{aligned} \quad (\text{S47})$$

Finally, the noise factor (NF) can be determined as-

$$\begin{aligned}
NF &= 1 + \frac{\text{Total output noise power, } v_{n,tot,out}^2}{\text{Total noise power due to } R_{in}, v_{n,Rin,out}^2} \\
&= 1 + \frac{\left( \frac{4kT}{R_F} + g_{mb,MR}^2 \times \overline{v_{ni,BDPR}^2} \right) |Z_{out}|^2}{4kTR_{in}|A_v|^2} \\
&+ \frac{4kT \left( \frac{\gamma}{\alpha} \right) g_{m1} |Z_p|^2}{4kTR_{in}|A_v|^2} + \frac{4kT \left( \frac{\gamma}{\alpha} \right) g_{m2} |Z_{out}|^2}{4kTR_{in}|A_v|^2} \\
&= 1 + \left[ \frac{1}{R_F} + 2 \left( \frac{\gamma g_{m,MR}}{\alpha} + \frac{k_p g_{m,MR}^2}{C_{ox} W L f} \right) \right] \\
&\times \left( \frac{1}{R_{in} G_m^2} \right) + \left( \frac{\gamma g_{m1}}{\alpha} \right) \left( \frac{|Z_p|^2}{R_{in} |A_v|^2} \right) \\
&+ \left( \frac{\gamma g_{m2}}{\alpha} \right) \left( \frac{1}{R_{in} G_m^2} \right) \tag{S48}
\end{aligned}$$

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