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Research Article

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Resilience of Sub-10 nm $MoSi_2N_4$ and WSi_2N_4 TFETs Against Surface Roughness: Device and Digital Applications

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Abstract

Monolayers of the $\mathbf{MA_2Z_4}$ family, particularly $\mathbf{MoSi_2N_4}$ and $\mathbf{WSi_2N_4}$, are promising channel materials for steep-slope tunnel field-effect transistors (TFETs) in beyond-CMOS electronics. However, interface imperfections introduce critical device variability. Here, we investigate the impact of substrate surface roughness on sub-10 nm $\mathbf{MoSi_2N_4}$ and $\mathbf{WSi_2N_4}$ TFETs using a tight-binding model within the non-equilibrium Green's function (NEGF) formalism. The surface corrugation induces localized midgap states, triggering parasitic trap-assisted tunneling that elevates the OFF-current and degrades the sub-threshold swing. Although both 2D channels show strong resilience up to an RMS roughness of $\boldsymbol{\delta h \approx 150}$pm-maintaining intrinsic delays as fast as $\boldsymbol{\tau \approx 0.20}$–$\mathbf{0.25}$ ps at $\boldsymbol{L_{ch} = 3}$ nm-higher roughness severely suppresses the ON-current and compresses the ON-OFF current ratio by four orders of magnitude. Monolayer $\mathbf{WSi_2N_4}$ consistently demonstrates superior electrostatic robustness compared to $\mathbf{MoSi_2N_4}$. Furthermore, inverter simulations reveal degraded transition slope with surface roughness. These results emphasize the need for atomically smooth substrates or planarization techniques to preserve steep-slope switching in scaled 2D nanoelectronics.

Keywords: Two-dimensional (2D) materials, $\mathbf{MA_2Z_4}$ family, Tunnel Field-Effect Transistor (TFET), NEGF formalism, Quantum transport, Surface roughness.

1 Introduction

The continuous scaling of complementary metal-oxide-semiconductor (CMOS) technology has enabled remarkable improvements in integration density and computational performance. However, as device dimensions approach the nanometer regime, conventional MOSFETs encounter fundamental limitations, including severe short-channel effects, increasing leakage current, and the thermionic limit of the sub-threshold swing (SS), which is restricted to 60 mV/dec at room temperature [1]. These challenges have motivated the exploration of alternative device architectures capable of achieving ultra-low-power operation while maintaining acceptable switching performance [2].

Among the emerging candidates, tunnel field-effect transistors (TFETs) have attracted considerable attention because their operation relies on band-to-band tunneling (BTBT) rather than thermionic carrier injection. Owing to this transport mechanism, TFETs can achieve a sub-threshold swing below the Boltzmann limit, making them promising devices for low-power electronics [2, 3]. Nevertheless, practical TFETs often suffer from limited ON-current due to the inherently low tunneling probability, thereby necessitating the search for channel materials with favorable electronic and transport properties.

In recent years, two-dimensional (2D) semiconductors have emerged as promising channel materials for next-generation TFETs. Their atomically thin body enables superior electrostatic gate control, excellent scalability, and suppression of short-channel effects [4]. Extensive research has been conducted on transition-metal dichalcogenides (TMDs), including MoS_2, WS_2, and WSe_2, for TFET applications. However, many TMD-based TFETs still exhibit relatively low ON-current due to unfavorable band alignments [5].

The recent discovery of the MA_2Z_4 family of 2D materials has opened a new avenue for nanoelectronic device engineering. In particular, monolayer $MoSi_2N_4$, experimentally synthesized by Hong *et al.* [6], exhibits a unique septuple-layer structure consisting of a MoN_2 layer sandwiched between two Si–N bilayers. This material demonstrates excellent environmental stability, mechanical robustness, and desirable electronic properties. First-principles studies have reported a bandgap in the range of approximately 1.9–2.3 eV, high carrier mobility, and strong electrostatic controllability, making it a promising candidate for advanced electronic applications [7]. Subsequently, WSi_2N_4 was proposed and synthesized as another stable member of the MA_2Z_4 family, exhibiting comparable structural stability and favorable carrier transport characteristics suitable for low-power transistor technologies [8, 9].

Recent investigations have demonstrated the potential of $MoSi_2N_4$- and WSi_2N_4-based transistors for achieving excellent switching characteristics, high ON-current and low leakage currents. Device simulations have suggested that these materials can provide improved electrostatic integrity and enhanced energy efficiency compared with several conventional 2D semiconductor channels [10–12]. Consequently, MA_2Z_4 monolayers have emerged as promising candidates for future TFET technologies [9, 13, 14].

Despite these encouraging developments, the influence of fabrication-induced imperfections on the performance of MA_2Z_4-based TFETs remains largely unexplored.

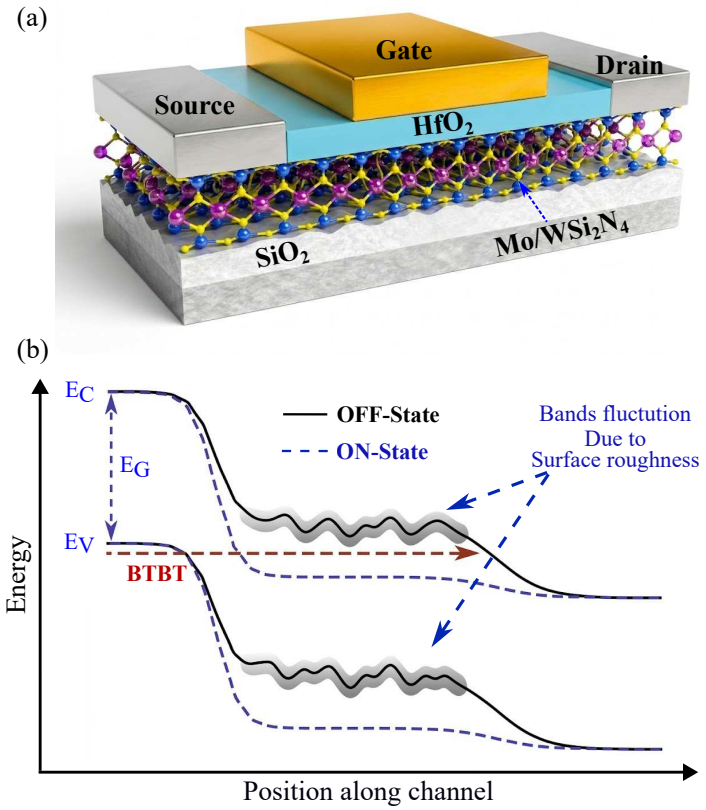


Fig. 1 (a) Three-dimensional schematic of the monolayer Mo/WSi_2N_4 tunnel field-effect transistor resting on a rough SiO_2 substrate with an HfO_2 top-gate dielectric. (b) Energy band diagrams along the channel in the OFF and ON states, illustrating the band-edge fluctuations and the band-to-band tunneling (BTBT) window induced by surface roughness.

In practical manufacturing processes, roughness at interfaces of materials and substrates is unavoidable. Such structural irregularities can perturb the local electrostatic potential, modify carrier confinement, and introduce additional scattering mechanisms that degrade transport characteristics. Since the current in a TFET is highly sensitive to the tunneling barrier profile and electric-field distribution at the source–channel junction, even minor roughness-induced variations may significantly affect the ON-current (I_{ON}), OFF-current (I_{OFF}), sub-threshold swing, and overall device variability [15, 16].

Interface roughness has been studied in FETs and various nanoscale devices, where it is identified as one of the main sources of performance degradation [17, 18]. Furthermore, recent studies have shown that defects and structural disorders in MA_2Z_4 materials can substantially alter their electronic properties by introducing localized states and modifying carrier transport pathways [7, 19]. These findings suggest that roughness-induced disorder may play a critical role in determining the ultimate performance limits of $MoSi_2N_4$- and WSi_2N_4-based TFETs.

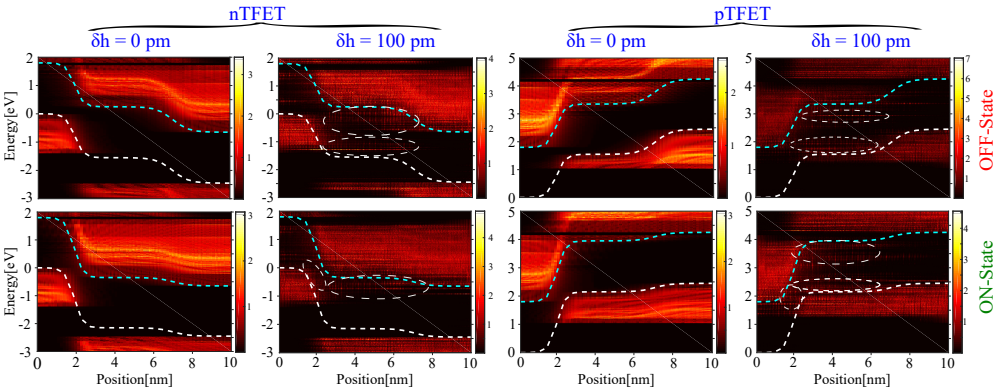


Fig. 2 The local density of states and corresponding energy band edges along the transport direction for monolayer n- and p-type TFETs in the OFF and ON states, comparing the pristine flat substrate (δh = 0 pm) with the corrugated substrate (δh = 100 pm). The dashed ellipses denote roughness-induced localized midgap states within the forbidden bandgap.

This study presents a thorough investigation into the influence of surface roughness on the monolayer $MoSi_2N_4$ and WSi_2N_4 TFETs, utilizing quantum transport simulations. By integrating realistic roughness profiles into the device architecture, we evaluate the resulting effects on transfer characteristics, tunneling probability, sub-threshold behavior, ON-OFF current ratio, and device variability. Additionally, a comparative analysis of $MoSi_2N_4$ and WSi_2N_4 channels is performed to determine their respective resilience to imperfections introduced during fabrication. These findings offer significant insights regarding the reliability and scalability of MA_2Z_4-based TFETs for upcoming low-power nanoelectronic applications.

2 Methods

The electronic band structures of monolayer $MoSi_2N_4$ and WSi_2N_4 are described via a parameterized tight-binding (TB) Hamiltonian [20]:

$$\hat{H}_0 = \sum_{\langle i,j\rangle;l,m} t_{i,j;l,m}\, \hat{c}^{\dagger}_{i;l}\hat{c}_{j;m}, \tag{1}$$

where $\hat{c}^{\dagger}_{i;l}$ and $\hat{c}_{j;m}$ correspond to the standard creation and annihilation operators for electrons occupying localized atomic orbital l at lattice position i and orbital m at site j, respectively. The intersite hopping matrix elements, designated by $t_{i,j;l,m}$, are parameterized based on density functional theory (DFT) band-structure fittings reported in Ref. [20].

To capture the topological disorder originating from substrate corrugation and interfacial imperfections, local lattice strain is incorporated by adjusting the transfer integrals. The strain-modulated hopping parameters in the perturbed crystal geometry

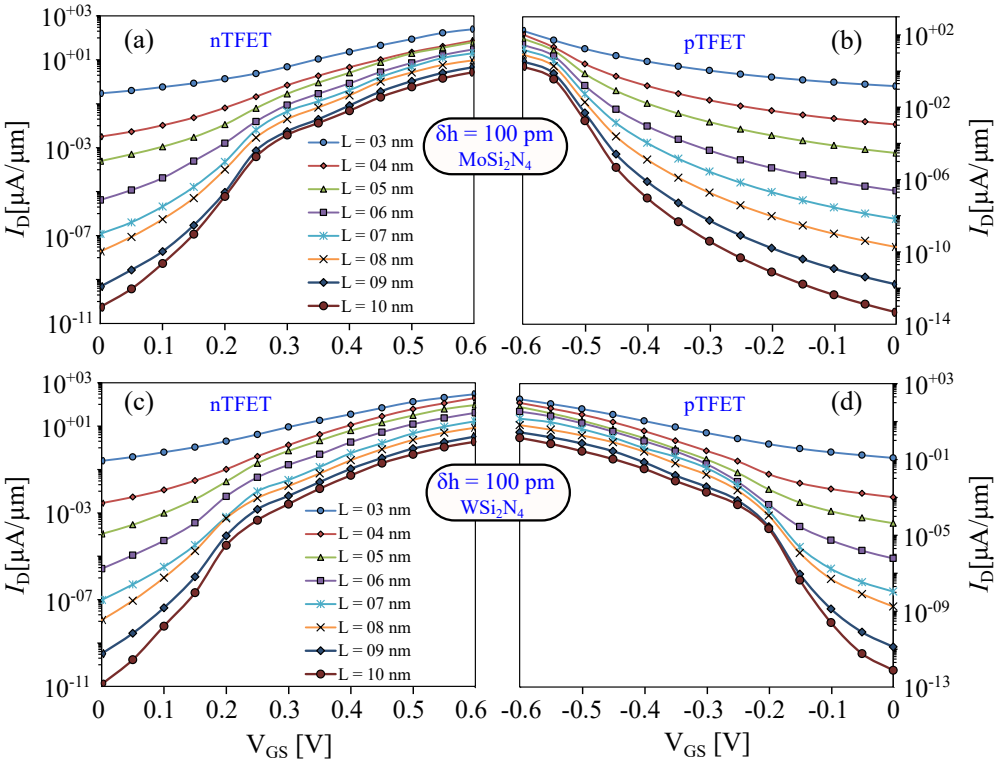


Fig. 3 Transfer characteristics (I_D–V_{GS}) across various channel lengths (L_{ch} = 3–10 nm) under an RMS surface roughness of δh = 100 pm at $|V_{DS}|$ = 0.6 V for: (a) $MoSi_2N_4$ *n*-TFET, (b) $MoSi_2N_4$ *p*-TFET, (c) WSi_2N_4 *n*-TFET, and (d) WSi_2N_4 *p*-TFET.

are formulated as:

$$t_{i,j;l,m}(\mathbf{r}_{ij}) = t_{i,j;l,m}(\mathbf{r}^0_{ij}) \left[1 - \beta_{i,j;l,m} \frac{|\mathbf{r}_{ij}| - |\mathbf{r}^0_{ij}|}{|\mathbf{r}^0_{ij}|} \right], \tag{2}$$

in which $|\mathbf{r}^0_{ij}|$ and $|\mathbf{r}_{ij}|$ denote the unstrained (equilibrium) and distorted interatomic bond lengths, respectively. The dimensionless electron-lattice coupling coefficient is defined by the radial logarithmic derivative of the hopping potential:

$$\beta_{i,j;l,m} = - \left. \frac{d \ln V_{i,j;l,m}(r)}{d \ln r} \right|_{r=|\mathbf{r}^0_{ij}|}. \tag{3}$$

Under the generalized Harrison and Wills-Harrison scaling principles, the decay rate $\beta_{i,j;l,m}$ is governed primarily by orbital angular momentum rather than magnetic quantum indices. In this work, the canonical value of $\beta_{d\text{–}d} = 5$ is assigned to nearest-neighbor *d*-orbital hopping terms, a strategy extensively validated for evaluating strain effects and surface roughness scattering in two-dimensional materials [21–23].

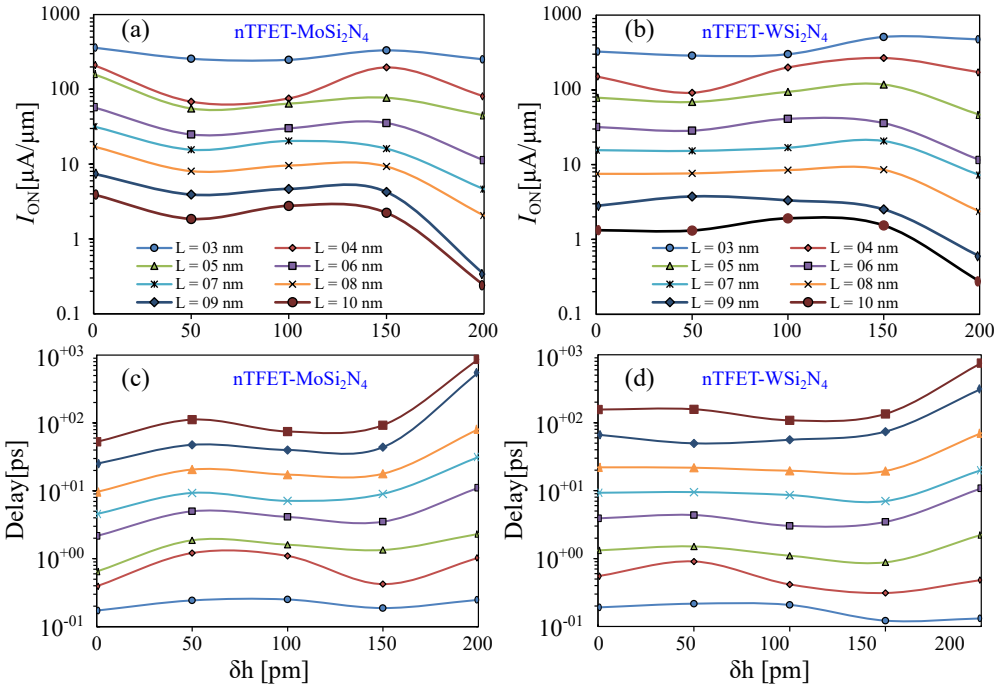


Fig. 4 The evaluation of ON-current and speed metrics as a function of RMS surface roughness (δh = 0–200 pm) for channel lengths from 3 to 10 nm: (a) ON-current (I_{ON}) for $MoSi_2N_4$ n-TFET, (b) I_{ON} for WSi_2N_4 n-TFET, (c) intrinsic gate delay (τ) for $MoSi_2N_4$ n-TFET, and (d) intrinsic gate delay for WSi_2N_4 n-TFET.

The spatial fluctuations of the substrate surface roughness are treated statistically through a two-dimensional Gaussian autocorrelation function:

$$R(x,y) = \delta h^2 \exp\left(-\frac{x^2}{L_x^2} - \frac{y^2}{L_y^2}\right), \tag{4}$$

where δh represents the root-mean-square (RMS) roughness amplitude, while L_x and L_y denote the spatial correlation lengths along the longitudinal (transport) and transverse directions, respectively.

Carrier transport in the perturbed device active region is evaluated within the non-equilibrium Green's function (NEGF) formalism, which accounts for quantum interference, local electrostatic potential distortions, and boundary conditions in nanoscale conduits [24]. Comprehensive descriptions of the model are detailed in our prior publication [12].

3 Results and Discussion

Fig. 1(a) schematically illustrates the simulated TFET structure. The device's channel, source, and drain regions are constructed from the two-dimensional material

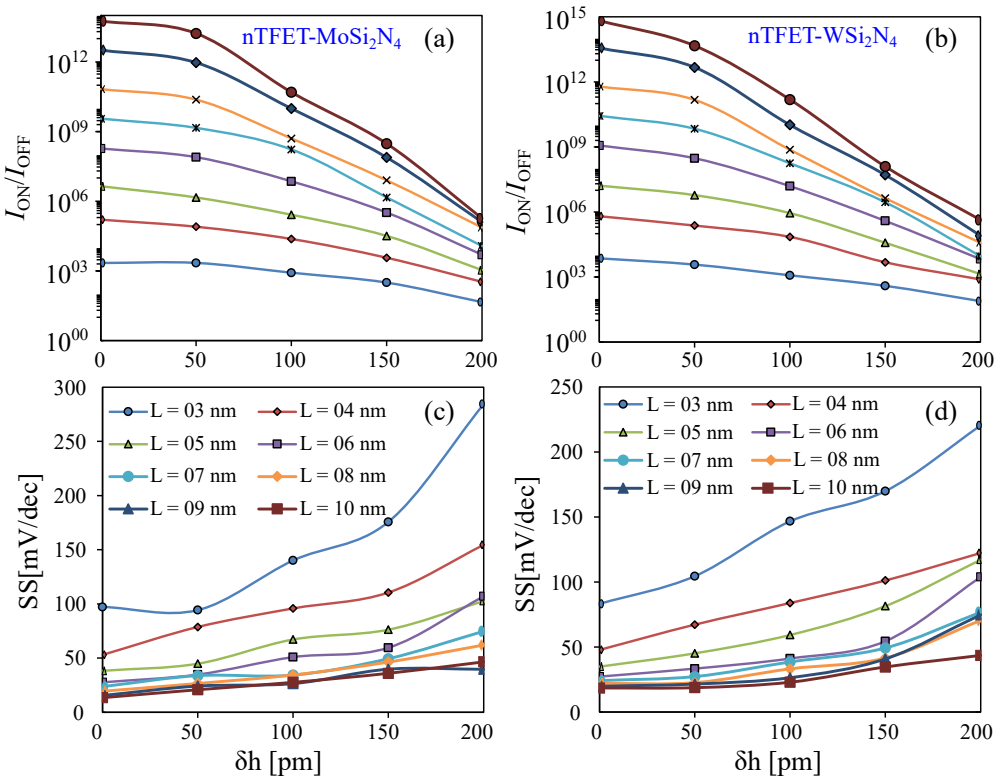


Fig. 5 Switching performance figures of merit versus RMS surface roughness (δh = 0–200 pm) across various channel lengths (L_{ch} = 3–10 nm): (a) the ON-OFF current ratio (I_{ON}/I_{OFF}) for $MoSi_2N_4$ n-TFET, (b) I_{ON}/I_{OFF} for WSi_2N_4 n-TFET, (c) sub-threshold swing (SS) for $MoSi_2N_4$ n-TFET, and (d) SS for WSi_2N_4 n-TFET.

Mo/WSi_2N_4. We have analyzed channel lengths ranging from 3 nm to 10 nm, maintaining a constant supply voltage of 0.6 V. Hafnium dioxide (HfO_2) serves as the gate oxide, featuring a dielectric constant of 25 and an Equivalent Oxide Thickness (EOT) of 1 nm, which equates to a physical thickness of 6.41 nm. For the substrate, we have utilized silicon dioxide (SiO_2), a standard material, with a thickness of 50 nm and a surface roughness expressed as a Root Mean Square (RMS) value between 0 and 200 pm. Additionally, the roughness of alternative substrate materials is included for comparative purposes. Fig. 1(b) illustrates the modifications in the energy band structure throughout the entirety of the device during both the on and off states. Within this figure, the implications of surface roughness regarding the energy bands, particularly within the channel region, are schematically delineated.

Fig. 2 depicts the spatially resolved local density of states (LDOS) of the n-type and p-type TFETs in both the OFF and ON states, comparing the ideal substrate condition (δh = 0 pm) with the case of substrate surface roughness characterized by δh = 100 pm. The superimposed energy-band profiles provide a direct visualization of the influence of substrate corrugation on the electronic structure and band-to-band

Table 1 Performance comparison of the proposed $MoSi_2N_4$- and WSi_2N_4-based TFETs under different surface-roughness conditions.

2D material	L	δh	I_{ON}		I_{OFF}		I_{ON}/I_{OFF}		SS		Delay	
	(nm)	(pm)	(μA/μm)		(μA/μm)				(mV/dec)		(ps)	
			MoSiN	WSiN	MoSiN	WSiN	MoSiN	WSiN	MoSiN	WSiN	MoSiN	WSiN
This Work	3	50	256	287	1.16×10^{-1}	7.70×10^{-2}	2.21×10^{3}	3.73×10^{3}	94.3	104	0.24	0.21
	3	100	248	299	2.97×10^{-1}	2.51×10^{-1}	8.37×10^{2}	1.20×10^{3}	140	146	0.25	0.20
	3	200	251	473	5.54×10^{0}	6.16×10^{0}	4.53×10^{1}	7.69×10^{1}	284	220	0.24	0.13
This Work	5	50	55.5	68.8	3.82×10^{-5}	2.22×10^{-9}	1.45×10^{6}	5.96×10^{6}	44.8	45.1	1.87	1.50
	5	100	64.4	94.2	2.45×10^{-4}	9.63×10^{-8}	2.63×10^{5}	8.83×10^{5}	67.2	59.2	1.61	1.10
	5	200	44.7	46.5	4.14×10^{-2}	8.04×10^{-4}	1.08×10^{3}	1.37×10^{3}	102	117	2.32	2.22
This Work	10	50	1.85	1.31	1.09×10^{-13}	2.83×10^{-14}	1.69×10^{13}	4.65×10^{13}	20.8	18.7	112	157
	10	100	2.77	1.91	5.60×10^{-11}	1.25×10^{-11}	4.94×10^{10}	1.53×10^{11}	27.6	22.9	74.9	108
	10	200	0.24	0.27	1.31×10^{-6}	6.38×10^{-7}	1.83×10^{5}	4.31×10^{5}	46.5	43.5	865	753
$MoSi_2N_4$ (n, p) [25]	7	—	77	378	—	—	1.54×10^{6}	87.56×10^{6}	69	52	1.45	0.24
WSi_2N_4 (n, p) [8]	7	—	700	350	—	—	1.40×10^{7}	7.56×10^{6}	69	59	0.13	0.28
$MoSi_2N_4$ [14]	7	—	42.6	—	8.84×10^{-9}	—	4.83×10^{9}	—	23.7	—	3.69	—
WSi_2N_4 [9]	5	—	358	—	2.58×10^{-4}	—	1.39×10^{6}	—	67.3	—	0.23	—
MoS_2 [26]	10	—	0.06	—	6.15×10^{-13}	—	9.76×10^{10}	—	13.1	—	—	—
ITRS 2028 (HP)	5.9	—	900	—	0.10×10^{0}	—	9.00×10^{3}	—	—	—	0.42	—
ITRS 2028 (LP)	5.9	—	295	—	5.00×10^{-5}	—	5.90×10^{6}	—	—	—	1.49	—
IRDS 2037 (HP)	12	—	753	—	—	—	—	—	65–70	—	0.88	—
IRDS 2037 (LP)	12	—	547	—	—	—	—	—	65–70	—	1.22	—

tunneling dynamics. In the ideal pristine case, the OFF-state band alignment provides an adequately wide tunneling barrier that suppresses the energetic overlap between source and channel states, thereby minimizing unwanted leakage. Under ON-state conditions, gate-induced electrostatic band bending establishes an efficient alignment between the source valence-band states and channel conduction-band states, significantly narrowing the tunneling barrier to facilitate strong carrier injection. When substrate-induced roughness is introduced, local topography variations transfer structural deformations to the two-dimensional channel, altering the hopping integrals. As observed for $\delta h = 100$ pm, these perturbations not only distort the band edges but also induce localized midgap states within the forbidden bandgap along the channel, as demarcated by the dashed ellipses. In the OFF state, these localized states act as intermediate stepping stones that promote parasitic trap-assisted tunneling, markedly degrading the sub-threshold swing and elevating I_{OFF}. Conversely, in the ON state, they induce destructive carrier scattering and blunt the abruptness of the tunneling barrier, which attenuates the coherent BTBT probability and lowers I_{ON}. While the core switching mechanism is preserved, the generation of these roughness-induced midgap states is the primary physical origin of the severe compression observed in the I_{ON}/I_{OFF} current ratio.

To evaluate device scalability and gate controllability under interfacial disorder, Fig. 3 illustrates the transfer characteristics (I_D–V_{GS}) across channel lengths ranging from $L_{ch} = 3$ to 10 nm at an RMS surface roughness of $\delta h = 100$ pm. Figures 3(a) and (b) depict the transfer curves for $MoSi_2N_4$-based n- and p-type TFETs, while Figs. 3(c) and (d) present the corresponding characteristics for monolayer WSi_2N_4 devices under a supply bias of $|V_{DS}| = 0.6$ V. As the channel length is scaled down, short-channel effects coupled with surface roughness lead to a pronounced rise in the OFF-state leakage current (I_{OFF}). For the $MoSi_2N_4$ devices, I_{OFF} varies from

2.97×10^{-1} μA/μm at $L_{ch} = 3$ nm down to 5.60×10^{-11} μA/μm at $L_{ch} = 10$ nm for the n-TFET, and from 1.46×10^{-1} μA/μm to 4.57×10^{-14} μA/μm for the p-TFET. A comparison between the two materials reveals that while both exhibit a degraded sub-threshold swing and suppressed ON-current relative to pristine counterparts [9, 14]. The WSi_2N_4 TFETs maintain steeper sub-threshold slopes and superior gate control down to shorter channel lengths. This contrast highlights the higher resilience of WSi_2N_4 against roughness-induced electrostatic degradation during extreme device downscaling.

Fig. 4 presents a systematic evaluation of the ON-current (I_{ON}) and intrinsic gate delay (τ) as functions of RMS surface roughness (δh = 0–200 pm) across channel lengths ranging from $L_{ch} = 3$ to 10 nm. Fig. 4(a) and (b) illustrate the I_{ON} characteristics for monolayer $MoSi_2N_4$ and WSi_2N_4 n-TFETs, respectively. Remarkably, both channel materials exhibit substantial resilience against interfacial disorder up to $\delta h \approx 150$ pm, maintaining nearly constant ON-currents with only minor fluctuations. However, exceeding this threshold ($\delta h > 150$ pm) triggers a decrement in I_{ON}, particularly at longer channel lengths where the current drops by nearly an order of magnitude. Correspondingly, the intrinsic switching delay ($\tau \approx C_g V_{DD}/I_{ON}$), shown in Figs. 4(c) and (d), remains well-preserved within the low-to-moderate roughness regime ($\delta h \leq 150$ pm) but increases beyond 150 pm due to the ON-current. A comparative inspection between the two monolayers highlights that WSi_2N_4 demonstrates superior electrostatic stability and higher current resilience than $MoSi_2N_4$, evidenced by flatter I_{ON}. This enhanced immunity establishes monolayer WSi_2N_4 as a more robust channel candidate for ultra-scaled, variation-tolerant TFET architectures.

Figure 5 evaluates two quintessential switching figures of merit: the ON-OFF current ratio (I_{ON}/I_{OFF}) and the sub-threshold swing (SS), as functions of RMS roughness amplitude across various channel lengths. As depicted in Figs. 5(a) and (b), the I_{ON}/I_{OFF} ratio degrades monotonically with increasing surface roughness, driven primarily by the sharp escalation in OFF-state leakage current. For example, in a 5 nm $MoSi_2N_4$ n-TFET, scaling the roughness from $\delta h = 0$ to 200 pm severely compresses the ON-OFF current ratio from 4.43×10^6 down to 1.08×10^3. Concurrently, the gate control over the channel electrostatics deteriorates, as evidenced by the sub-threshold swing characteristics in Figs. 5(c) and (d). While the pristine sub-10 nm TFETs operate comfortably below the thermionic Boltzmann limit (60 mV/dec at room temperature), heightened interfacial roughness causes SS to surpass this threshold; for instance, increasing δh from 0 to 100 pm in a 5 nm $MoSi_2N_4$ channel inflates SS from 38 to 67 mV/dec. Notably, this roughness-induced SS degradation is strongly channel-length dependent. The adverse impact is most acute at $L_{ch} = 3$ nm due to severe coupling with short-channel effects, but markedly attenuates for $L_{ch} \geq 4$ nm where enhanced gate electrostatic integrity buffers against local potential fluctuations. Across both metrics, monolayer WSi_2N_4 exhibits superior immunity compared to $MoSi_2N_4$, maintaining steeper sub-threshold slopes. These findings highlight that integrating atomically smooth substrates, such as hexagonal boron nitride (h-BN), or deploying advanced planarization techniques is essential to eliminate roughness-induced variability and fully preserve the steep-slope switching advantages of 2D MA_2Z_4 TFETs.

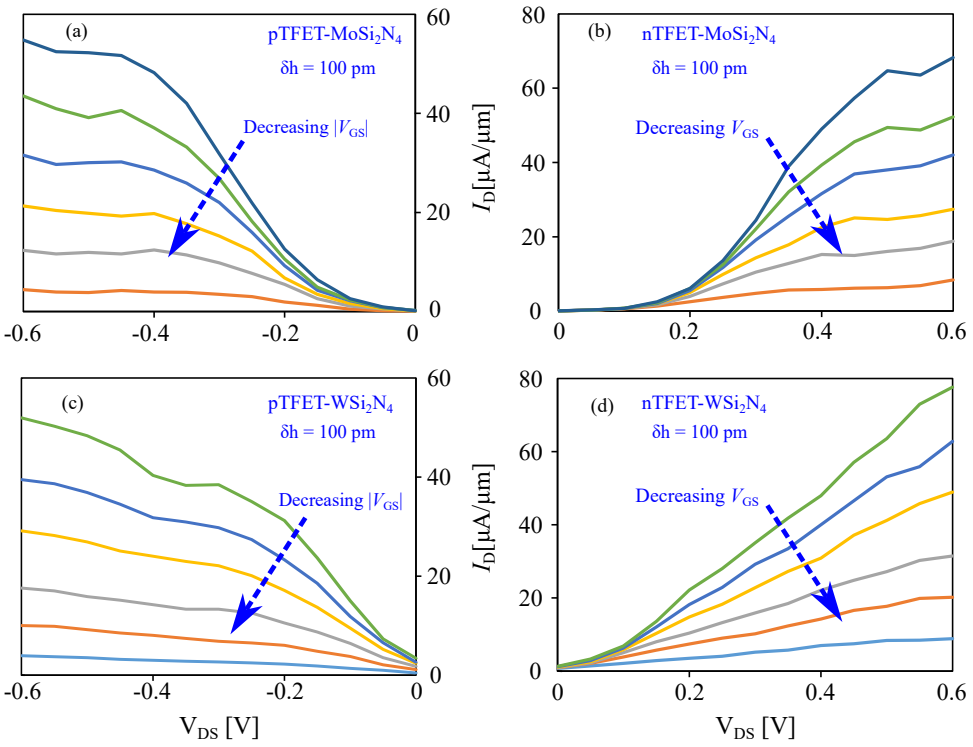


Fig. 6 Output characteristics (I_D–V_{DS}) of the 5 nm TFETs under an effective RMS surface roughness of $\delta h = 100$ pm for: (a) $MoSi_2N_4$ p-TFET, (b) $MoSi_2N_4$ n-TFET, (c) WSi_2N_4 p-TFET, and (d) WSi_2N_4 n-TFET. Gate voltage steps span from 0 to ±0.6 V.

Table 1 summarizes the key performance metrics of the studied $MoSi_2N_4$ and WSi_2N_4 TFETs at channel lengths of 3, 5, and 10 nm under various roughness conditions, benchmarked against previous 2D-based devices and future technological projections (ITRS 2028 and IRDS 2037) [8, 25]. The comparison reveals that under low-to-moderate roughness ($\delta h \leq 100$ pm), the 5 nm and 10 nm devices deliver excellent sub-threshold swings (SS < 60 mV/dec) and remarkable ON-OFF current ratios exceeding 10^5 and 10^{10}, respectively, thereby fulfilling the rigorous OFF-state leakage requirements for low-power (LP) logic technology. In particular, for the 3 nm channel at $\delta h \leq 100$ pm, the intrinsic gate delays of both monolayers remain exceptionally fast ($\tau \approx 0.20$–0.25 ps), outperforming the ITRS high-performance (HP) target of 0.42 ps. Across all channel lengths, WSi_2N_4 consistently demonstrates higher ON-currents and better switching ratios under equivalent roughness compared to $MoSi_2N_4$. However, scaling the roughness to $\delta h = 200$ pm drastically degrades the sub-threshold swing (e.g., reaching 284 mV/dec at $L_{ch} = 3$ nm). It expands the switching delay up to hundreds of picoseconds at $L_{ch} = 10$ nm, causing deviations from both ITRS and IRDS benchmarks. These benchmarking outcomes quantitatively demonstrate that maintaining interfacial roughness below 100 pm is critical for MA_2Z_4-based TFETs to compete with or surpass future commercial nanoscale standards.

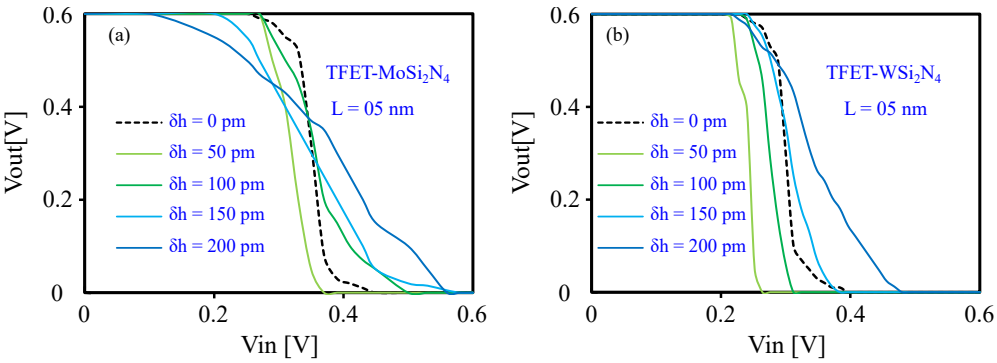


Fig. 7 Static inverter performance at $L_{\mathrm{ch}} = 5$ nm under different surface roughness amplitudes ($\delta h = 0$–200 pm): voltage transfer characteristics (V_{out}–V_{in}) for complementary inverters based on (a) monolayer $MoSi_2N_4$ and (b) monolayer WSi_2N_4 TFETs.

Figure 6 illustrates the output characteristics (I_{D}–V_{DS}) of the 5 nm n- and p-type TFETs based on monolayer $MoSi_2N_4$ and WSi_2N_4 across the cut-off, linear, and saturation operational regimes under an effective RMS surface roughness of $\delta h = 100$ pm. The gate-source voltage is stepped from 0 to 0.6 V for the n-TFETs and from 0 to -0.6 V for the p-TFETs, corresponding to $|V_{\mathrm{DS}}|$ sweeps up to 0.6 V. As demonstrated, surface roughness influences the carrier transmission along the channel, manifesting as noticeable current distortions and ON-current attenuation predominantly in the high-bias saturation regime. In contrast, the sub-threshold and low-$|V_{\mathrm{DS}}|$ linear regimes exhibit negligible sensitivity to roughness-induced disorder, showing only modest current roll-off. Crucially, a comparative evaluation between the two channel materials indicates that WSi_2N_4 delivers smoother, more stable I–V trajectories and higher saturation current levels than $MoSi_2N_4$ under equivalent roughness. This superior electrostatic resilience confirms that monolayer WSi_2N_4 provides enhanced robustness against fabrication-induced substrate imperfections, rendering it a highly reliable candidate for low-power digital logic applications.

Fig. 7 (a) and (b) illustrate the voltage transfer characteristics (VTCs) of static inverters based on monolayer $MoSi_2N_4$ and WSi_2N_4 TFETs, respectively, for different surface-roughness amplitudes. In the ideal case of $\delta h = 0$ pm, both inverters exhibit a steep transition between the logic-high and logic-low states, reflecting a well-defined switching point and strong voltage-transfer capability. The introduction of surface roughness progressively impacts the VTC and the carrier transmission through the channel, altering the balance between the pull-up and pull-down currents of the complementary TFETs. For the $MoSi_2N_4$-based inverter, the increase in δh from 50 to 200 pm results in a pronounced broadening and displacement of the transition region, accompanied by a substantial reduction in the local VTC slope, particularly for $\delta h \geq 150$ pm. This behavior indicates a degradation of the intrinsic voltage gain and a corresponding reduction in the sharpness of the digital switching transition. A similar trend is observed for the WSi_2N_4-based inverter, where increasing surface roughness progressively shifts and broadens the transition region and significantly distorts the

ideal VTC profile at large δh. Notably, the sensitivity of the switching characteristics to surface roughness is material dependent, as evidenced by the different transition shifts and VTC distortions observed for $MoSi_2N_4$ and WSi_2N_4. Nevertheless, the preservation of distinct logic-high and logic-low output states demonstrates that the inverter operation remains functional even in the presence of considerable surface irregularities. These findings underscore the proposition that surface roughness represents a significant reliability concern for two-dimensional TFET-based digital circuits, insofar as roughness-induced fluctuations in the switching voltage and transition slope may exert a direct influence upon noise margins and voltage gain.

4 Conclusion

In this work, we comprehensively investigated the quantum transport behavior and variability of sub-10 nm tunnel field-effect transistors based on monolayer $MoSi_2N_4$ and WSi_2N_4 in the presence of substrate surface roughness using an atomistic tight-binding model self-consistently coupled with the NEGF formalism. Our quantum simulations reveal that surface corrugations perturb the monolayer structure and induce localized midgap states across the channel, which severely deteriorate the abruptness of the tunneling barrier. In the OFF state, these midgap states promote the trap-assisted tunneling, driving an exponential surge in leakage current and inflating the sub-threshold swing beyond the Boltzmann limit (60 mV/dec) at large roughness amplitudes. Conversely, in the ON state, roughness-induced scattering blunts carrier injection, leading to ON-current attenuation and gate-delay degradation.

Crucially, both 2D material systems demonstrate remarkable resilience against moderate interfacial disorder up to an RMS threshold of $\delta h \approx 150$ pm, sustaining near-ideal ON-currents and fast switching times ($\tau \approx 0.20$–0.25 ps at $L_{\mathrm{ch}} = 3$ nm) that comfortably meet the ITRS projections. However, exceeding this regime ($\delta h > 150$ pm) triggers acute performance roll-offs, with the ON-OFF current ratio compressed by up to four orders of magnitude. Across all evaluated geometric nodes and operating regimes, monolayer WSi_2N_4 consistently demonstrates superior electrostatic integrity, flatter transfer characteristics, and greater resistance to surface disorder than its $MoSi_2N_4$ counterpart. At the circuit level, complementary inverter simulations indicate that while fundamental rail-to-rail logic transitions are preserved, severe interfacial roughness induces switching-point shifts and degrades the transition slope. These quantitative insights emphasize that controlling substrate morphology below 100 pm-via advanced surface planarization techniques or van der Waals encapsulation with atomically smooth dielectric substrates such as hexagonal boron nitride-is imperative to preserve the steep-slope switching advantages of 2D MA_2Z_4 TFETs in next-generation, energy-efficient Beyond-CMOS logic platforms.

Declarations

The authors declare that no funds were received during the preparation of this manuscript.

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