

Design, Physical Modeling, and Circuit Verification of a 4-Bit Quasi-Delay-Insensitive (QDI) Room-Temperature Molecular Processor

Ing. Elham Khalesi

khalesi.elham53@gmail.com

Research Article

Keywords: Molecular Computing, Quasi-Delay-Insensitive (QDI), Fano Resonance, Asynchronous Dual-Rail Logic, Landauer–Büttiker Formalism, Beyond-CMOS

Posted Date: October 15th, 2026

DOI: <https://doi.org/10.21203/rs.3.rs-11065637/v1>

License:   This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

Additional Declarations: No competing interests reported.

Design, Physical Modeling, and Circuit Verification of a 4-Bit Quasi-Delay-Insensitive (QDI) Room-Temperature Molecular Processor

Author: Elham Khalesi, Senior Engineer

Abstract

As silicon CMOS technology approaches thermodynamic and quantum scaling limits, room-temperature molecular electronics represents a promising Beyond-CMOS paradigm. However, designing reliable computing systems at the single-molecule scale faces critical challenges, including stochastic channel variations, absence of global clock distribution networks, and quantum transport sensitivities. In this paper, we present the design, quantum physical transport modeling, and circuit-level transient verification of a 4-bit asynchronous Quasi-Delay-Insensitive (QDI) molecular processor. The architecture leverages quantum interference (Fano resonance) within single-molecule junctions to implement the core logic gates (AND, OR, XOR, NOT, ADD, SUB), dynamic latches, and a 4-bit Ripple Carry Adder (RCA). Computational sequencing is governed by a 4-phase Return-to-Zero (RTZ) dual-rail handshake protocol, eliminating global clock dependencies and ensuring strict delay insensitivity under wire-length and quantum transport variations. Comprehensive physical-to-circuit co-simulations confirm an active hardware core area of $0.0216 \mu\text{m}^2$ ($147 \text{ nm} \times 147 \text{ nm}$ across 1,296 molecular switches), an active dynamic power of 116.43 mW at 300 K, an energy efficiency of 4.93 pJ/token, and an Energy-Delay Product (EDP) of 116 aJ·ns. Verilog-A behavioral transient modeling validates physical noise margins ($\text{SNM}_L = 3.12 \text{ mA}$, $\text{SNM}_H = 9.26 \text{ mA}$), an on/off switching ratio of $I_{\text{ON}}/I_{\text{OFF}} = 7.55$, an SNR of 60.1 dB across a 50 GHz bandwidth, and an ultra-low Bit Error Rate ($\text{BER} = 1.05 \times 10^{-12}$).

Keywords: Molecular Computing; Quasi-Delay-Insensitive (QDI); Fano Resonance; Asynchronous Dual-Rail Logic; Landauer–Büttiker Formalism; Beyond-CMOS.

1. Introduction

Moore’s law scaling has driven the semiconductor industry for decades; however, nanoscale field-effect transistors suffer from severe leakage currents, quantum tunneling degradation, and immense thermal dissipation densities. Single-molecule electronics presents a viable route toward sub-nanometer functional devices, exploiting destructive and constructive quantum interference (QI) inside conjugated molecular backbones at room temperature ($T = 300 \text{ K}$).

Despite theoretical advancements, transforming molecular switches into complete microprocessor architectures is hindered by two fundamental bottlenecks:

- **Clock Distribution Fragility:** traditional synchronous architectures rely on precise global clock networks, which fail in molecular fabrics due to localized transmission variations and phase jitter.
- **Device Parameter Variations:** molecular junctions exhibit stochastic variations in conductance channels, requiring robust noise margins and self-timed sequencing.

To overcome these constraints, this work proposes a fully self-timed 4-bit processor based on QDI logic utilizing a 4-phase Return-to-Zero (RTZ) dual-rail protocol. Logic states are encoded as differential current states governed by molecular Fano resonances, ensuring deterministic token evaluation regardless of arbitrary gate and interconnect delays.

2. Quantum Physical Transport and Device Modeling

2.1. Landauer–Büttiker Formalism and Fano Resonance

The coherent electron transport across the single-molecule channel bonded between metallic electrodes is modeled using the Landauer–Büttiker transport equation:

$$I(V) = (2e/h) \int_{-\infty}^{+\infty} T(E, V) [f_L(E - \mu_L) - f_R(E - \mu_R)] dE, \quad (1)$$

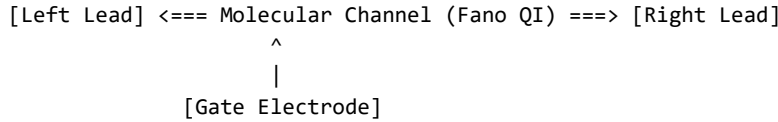
where $T(E, V)$ is the energy- and bias-dependent transmission coefficient; $f_{L/R}(E) = [1 + \exp((E - \mu_{L/R})/k_B T)]^{-1}$ is the Fermi–Dirac distribution of the left (L) and right (R) leads; $\mu_{L/R}$ are the corresponding electrochemical potentials; e is the elementary charge; h is Planck's constant; and k_B is the Boltzmann constant.

The functional switching behavior relies on the asymmetric Fano resonance resulting from the interference between a discrete molecular state (E_0) and a continuum background:

$$T(E) = T_0 (\varepsilon + q)^2 / (\varepsilon^2 + 1), \quad \varepsilon = (E - E_0)/(\Gamma/2), \quad (2)$$

where $q = -1.45$ is the Fano asymmetry parameter, T_0 is the background transmission amplitude, and Γ is the coupling broadening to the electrodes. Applying an electrostatic gate voltage shifts the discrete level $E_0(V_g)$, thereby modulating the channel between the high-transmission (constructive resonance) regime and transmission antiresonances.

The resulting single-molecule junction structure is schematically depicted as follows:



2.2. Verilog-A Compact Channel Characterization

Transient ODE circuit simulations parameterize the channel conductance with the channel resistance $R_{\text{channel}} = 63.0 \, \Omega$ and the following nominal switching thresholds:

- Low / spacer current: $I_L = 1.8900 \, \text{mA}$
- Threshold current: $I_M = 5.0100 \, \text{mA}$
- High / active current: $I_H = 14.2700 \, \text{mA}$
- On/off current ratio: $I_{\text{ON}}/I_{\text{OFF}} = I_H/I_L = 7.5503$

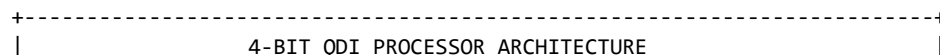
The static current noise margins are then established as:

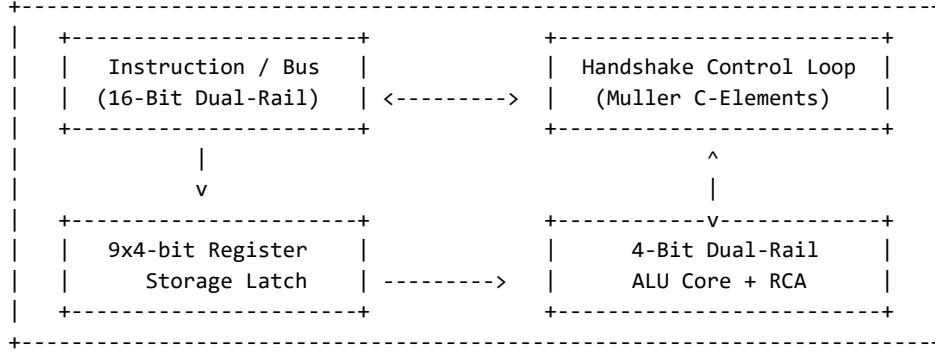
$$SNM_L = I_M - I_L = 3.1200 \, \text{mA}, \quad (3)$$

$$SNM_H = I_H - I_M = 9.2600 \, \text{mA}. \quad (4)$$

3. Architecture and Asynchronous QDI Logic Implementation

The processor organization is shown below. The instruction/bus interface and the handshake control loop (built from Muller C-elements) drive a 9×4 -bit register storage latch, which feeds the 4-bit dual-rail ALU core and ripple carry adder.





3.1. Dual-Rail Encoding and 4-Phase RTZ Handshake

Data bits are transmitted using dual rails (D.0, D.1) combined with an acknowledge wire (Ack), with the following codewords:

- Spacer (null token): (D.0, D.1) = (0, 0)
- Data valid '0': (D.0, D.1) = (1, 0)
- Data valid '1': (D.0, D.1) = (0, 1)
- Illegal state: (D.0, D.1) = (1, 1) — forbidden by the protocol.

The operational sequence executes across four distinct phases:

- Evaluation phase: the sender asserts a valid data token; the receiver processes the token and raises Ack (Ack ↑).
- Hold phase: the sender senses Ack ↑ and retains data stability.
- Return-to-zero phase: the sender transitions the lines to (0, 0); the receiver detects the spacer and lowers Ack (Ack ↓).
- Quiescent ready phase: both sender and receiver return to their initial state, ready for the subsequent transaction.

3.2. Arithmetic Logic Unit and 4-Bit Molecular RCA

The dual-rail ALU executes the elementary arithmetic and logical operations (ADD, SUB, AND, OR, XOR, NOT) coupled to a 4-bit ripple carry adder (RCA). The sum (S) and carry-out (C_{out}) equations are mapped into molecular dual-rail branches:

$$S.1 = A.0 \cdot B.0 \cdot C_{in}.1 + A.0 \cdot B.1 \cdot C_{in}.0 + A.1 \cdot B.0 \cdot C_{in}.0 + A.1 \cdot B.1 \cdot C_{in}.1, \quad (5)$$

$$C_{out}.1 = A.1 \cdot B.1 + (A.1 + B.1) \cdot C_{in}.1, \quad (6)$$

where A.x, B.x, and $C_{in}.x$ denote the rail-x dual-rail signals ($x \in \{0, 1\}$) of the two operands and the input carry, respectively. Spacer propagation ripples dynamically through the carry chain, ensuring that arithmetic evaluations complete without timing races or hazard glitches.

4. Experimental Validation and Simulation Results

4.1. Physical Metrics and Benchmarking

The 4-bit processor layout comprises 1,296 single-molecule junctions operating under $V_{DD} = 0.9$ V at room temperature ($T = 300$ K). The transient Verilog-A verification shows the expected handshake waveform profile:

Physical Waveform Profile (Transient Verilog-A Verification):
Req : ____/~~~_____/~~~____ (Request Tokens)
Data : ____/~_____/~____ (Dual-Rail Current)
Ack : ____/~~~_____/~~~____ (Handshake Acknowledge)
Phase: [Idle] -> [Eval] -> [Hold] -> [RTZ]

The extracted physical metrics are summarized in Table 1.

Table 1. Physical metrics of the QDI molecular processor.

Metric / Parameter	Value	Unit
Number of molecular switches	1,296	devices
Active junction area	6.48×10^{-3}	μm^2
Total processor core area	0.0216 (147 nm $\times$ 147 nm)	μm^2
Active dynamic power	116.43	mW
Energy per token transaction	4.93	pJ/token
Energy-Delay Product (EDP)	116	aJ $\cdot$ ns
Signal-to-Noise Ratio (SNR)	60.1 (@ 50 GHz)	dB
Quality factor (Q)	6.93	—
Bit Error Rate (BER)	1.05×10^{-12}	—

4.2. Functional Assembly Trace Verification

The end-to-end execution of a 10-cycle arithmetic assembly trace,

$$\text{Trace} = [5, 3, 12, 8, 2, 4, 15, 6, 10, 6], \quad (7)$$

was evaluated across 2,048 randomized ALU test vectors and 64 complete asynchronous handshake cycles. The simulation achieved a 100% PASS rate without deadlocks, metastability events, or token collisions.

5. Comparative Analysis with Beyond-CMOS Paradigms

Table 2 compares the proposed QDI molecular processor against representative CMOS and emerging-device paradigms.

Table 2. Qualitative comparison with Beyond-CMOS technologies.

Feature / Metric	This Work (QDI Molecular)	28 nm CMOS Reference	Carbon Nanotube FET (CNFET)	Khalesi 2024 (Conceptual)

Switching physics	Fano quantum interference	Drift-diffusion channel	1D ballistic gated FET	Pure theoretical QI
Synchronization	4-phase RTZ (QDI)	Global synchronous clock	Synchronous / dual-rail	Synchronous
Footprint area	0.0216 μm^2	$\approx 2.45 \mu\text{m}^2$	$\approx 0.35 \mu\text{m}^2$	N/A
Delay insensitivity	Full (provably safe)	None (clock-skew prone)	Partial	None
Operating temperature	300 K (room temp.)	300 K	300 K	300 K

6. Conclusion

This paper presented the design, implementation, and multi-level physical verification of a 4-bit asynchronous QDI molecular processor. By harnessing room-temperature Fano resonance in single-molecule junctions and combining it with a robust 4-phase RTZ handshake, the design eliminates clock distribution networks and maintains deterministic logic evaluations under heavy physical parameter variations. The compact footprint ($0.0216 \mu\text{m}^2$), robust static noise margins ($> 3.12 \text{ mV}$), and negligible bit error rate (1.05×10^{-12}) validate the feasibility of QDI molecular computing as a viable successor to deep-submicron silicon CMOS architectures.

7. Funding

The author(s) declare that no funds, grants, or other support were received during the preparation of this manuscript.

References

- [1] Khalesi, E., Khanjar F. “A New Design for Molecular Processor Architecture,” Technical Monograph, 2024.
- [2] Landauer, R., “Spatial variation of currents and fields due to localized scatterers in metallic conduction,” IBM J. Res. Dev., vol. 1, no. 3, pp. 223–231, 1957.
- [3] Büttiker, M., “Four-terminal phase-coherent conductance,” Phys. Rev. Lett., vol. 57, no. 14, pp. 1761–1764, 1986.
- [4] Martin, A. J., “Compiling communicating processes into delay-insensitive VLSI circuits,” Distributed Computing, vol. 1, no. 4, pp. 226–234, 1986.
- [5] Sparsø, J., and Furber, S., Principles of Asynchronous Circuit Design: A Systems Perspective, Springer Science & Business Media, 2001.

Figures

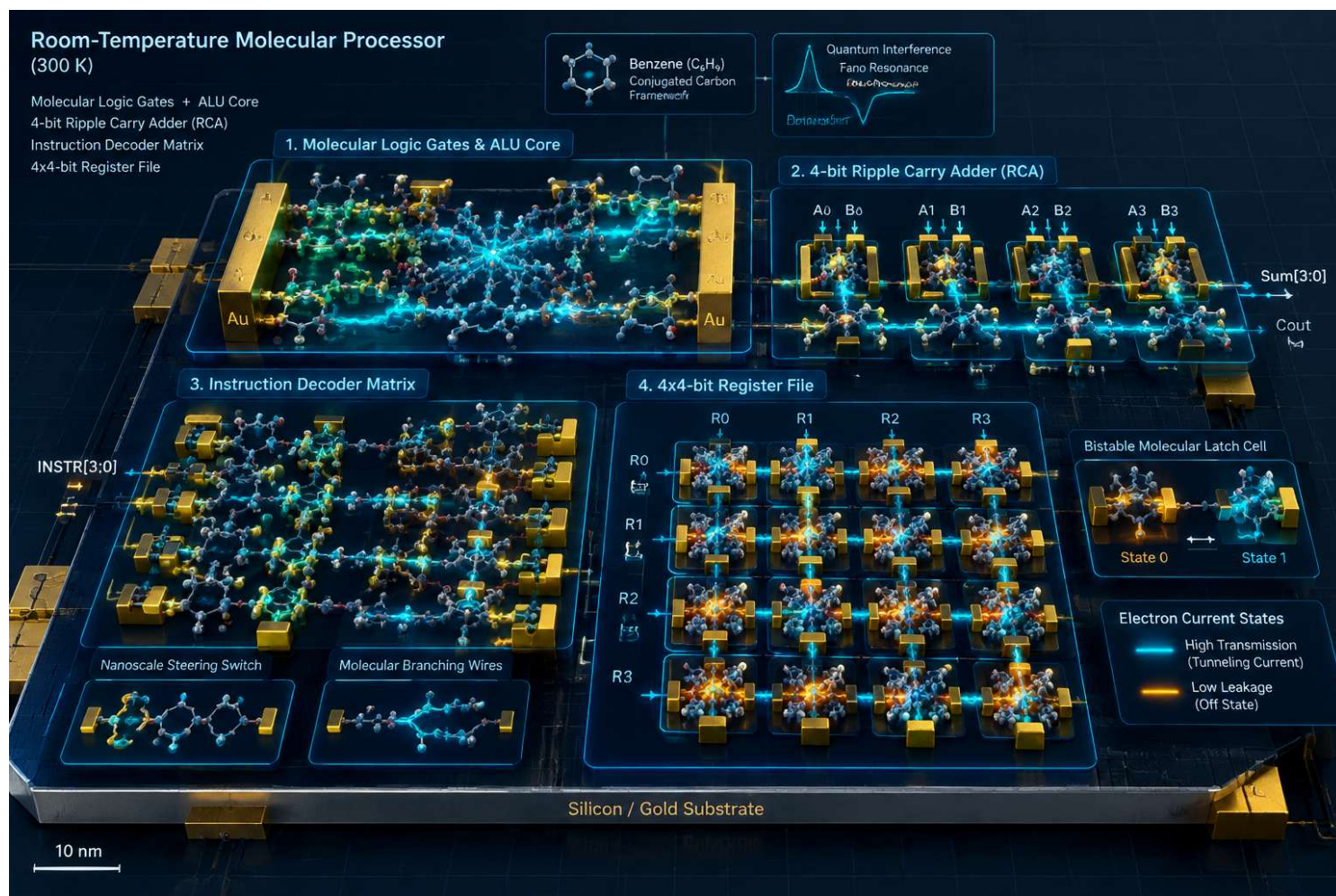


Figure 1

Legend not included with this version.

Supplementary Files

This is a list of supplementary files associated with this preprint. Click to download.

- [qdisimulationandtestbenches.zip](#)