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Research Article

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Structured abstract

Purpose: This study develops and empirically grounds a Digital Lean Six Sigma (D-LSS) architecture for Vietnam's electronics-semiconductor manufacturing ecosystem using longitudinal evidence from a contract manufacturer assembling high-mix semiconductor equipment. The research addresses a practical and methodological gap between increasingly sophisticated DMAIC 4.0 frameworks and the limited plant-level evidence available for high-mix, low-volume semiconductor-equipment assembly in emerging manufacturing locations.

Design/methodology/approach: The study reconstructs a longitudinal production event history from 128 production-tracking workbooks covering 111 observed snapshot days from 24 October 2024 to 29 March 2025. After deduplication, 53,860 snapshot-level observations were consolidated into 562 unique units across seven product families. Primary cycle-time inference uses 121 units from four families with exact Start Integration and Final QC dates; schedule-adherence inference uses 140 exact target/Final-QC pairs. Non-parametric tests, bootstrap confidence intervals, robust regression, logistic modeling, and event-history visualization are combined with Lean flow and Six Sigma measurement/control logic. Proprietary identifiers are excluded from the public analytical dataset.

Findings: Exact integration-to-Final-QC cycle times differ materially by product family (Kruskal-Wallis H=37.63, p=3.39×10^-8). Median cycle time was 4.0 days for Family A (95% bootstrap CI 3-5), 1.0 day for Family B, 1.0 day for Family C and 4.0 days for Family D. Family A and Family C also showed higher observed late-completion proportions (40.0% and 45.7%, respectively) than Family B (12.2%) and Family D (11.1%). Robust log-cycle modeling confirmed strong family effects after accounting for calendar trend and explicit shortage remarks. No monotonic learning trend was detected within the exact-date Family A subset, indicating that the observation window primarily captures post-ramp operational variability rather than a simple learning-curve effect.

Practical implications: The empirical results support a plant-ready D-LSS control system built around timestamp integrity, product-family stratification, WIP aging, schedule-risk triggers, material-readiness governance, and standardized milestone definitions. The paper specifies how the same evidence backbone can transfer to SMT and semiconductor back-end environments without treating the CM case as direct evidence for wafer fabrication or OSAT process capability.

Originality: The paper contributes a rare longitudinal, auditable dataset and analytical workflow for high-mix semiconductor-equipment contract manufacturing in Vietnam. It moves beyond generic LSS-Industry 4.0 mapping by reconstructing unit-level event histories from operational snapshots, explicitly separating exact from proxy milestone evidence, quantifying product-family heterogeneity, incorporating censoring logic, and linking empirical flow diagnosis to control-oriented D-LSS governance.

Keywords: Lean Six Sigma; semiconductor equipment; contract manufacturing; high-mix low-volume; Vietnam; cycle time; longitudinal manufacturing data; Digital DMAIC

1. Introduction

Vietnam's electronics sector has reached a scale at which small losses in yield, retest, downtime, queueing and process drift can translate into substantial economic effects. Official statistics report that exports of computers, electronic products and components increased from US$72.6 billion in 2024 to US$107.7 billion in 2025; the 2025 value represented 22.7% of national merchandise exports and grew 48.4% year on year (National Statistics Office of Vietnam, 2025, 2026). This growth is occurring alongside a deliberate semiconductor strategy rather than as an electronics-assembly story alone.

Decision No. 1018/QD-TTg sets a 2030 objective of more than US$25 billion in annual semiconductor revenue, at least 100 design firms, one small-scale fabrication facility, at least ten packaging and test plants, and more than 50,000 semiconductor engineers and graduates. The same strategy targets electronics revenue above US$225 billion (Government of Vietnam, 2024a). Existing industrial footprints illustrate the operational relevance of back-end manufacturing: Amkor's Bac Ninh campus is planned for 200,000 m² of cleanroom space with US$1.6 billion committed to the first two phases, while Intel describes its Vietnam site as the largest assembly-and-test facility in its network, with US$1.5 billion invested (Amkor Technology, 2023; Intel, 2025). These company facts are used only as scale/context indicators, not as evidence of LSS performance.

Lean Six Sigma (LSS) is attractive in this setting because electronics and semiconductor manufacturing simultaneously face flow loss and variation loss. Lean addresses waiting, WIP, changeovers, transport, motion, imbalance and non-value-added processing; Six Sigma contributes measurement-system analysis (MSA), statistical process control (SPC), capability analysis, design of experiments (DOE), regression and structured causal problem solving. Yet simply combining a Lean toolbox with DMAIC is no longer a sufficient academic contribution. Recent work already maps Industry 4.0 technologies into DMAIC and has developed an empirically evaluated DMAIC 4.0 framework (Pongboonchai-Empl et al., 2024, 2026). More recently, Ibrahim et al. (2026) proposed a unified LSS–Industry 4.0 framework specifically for electronics manufacturing services (EMS).

This creates a more demanding research gap. What remains underdeveloped is the control architecture required when the data-generating process is itself high-dimensional and hierarchical: board/pad/component within printer and product families in SMT, and lot/package/product within tool/head/chamber/recipe structures in semiconductor manufacturing. In these environments, pooled control limits, naive before/after comparisons and dashboard-centric digitalization can misidentify causes or create false alarms. Semiconductor process-control research instead emphasizes multivariate monitoring, fault detection and classification (FDC), high-mix run-to-run (R2R) control, state estimation and increasingly virtual metrology (VM) (Bode et al., 2007; Chang et al., 2011; Qin, 2012; Chen et al., 2023; Maitra et al., 2024; Chen and Chen, 2026).

Accordingly, this paper reframes Digital Lean Six Sigma as a control-oriented socio-technical system rather than a technology-enhanced project sequence. The proposed mechanism is: measurement integrity enables process observability; observability and correct stratification improve causal diagnosis; diagnosis must be matched to the dominant loss mechanism; the intervention must then be connected to a closed-loop control and governance mechanism. The paper develops this logic for both SMT and semiconductor back-end operations and translates it into a plant-ready validation protocol for Vietnam.

Unlike the earlier conceptual version of this framework, the present study adds a real industrial evidence base. The empirical setting is an anonymized Vietnamese contract manufacturer responsible for final assembly and production tracking of multiple semiconductor-equipment product families. This site is analytically distinct from a semiconductor wafer fab or OSAT plant; accordingly, the paper uses it as evidence for high-mix equipment-manufacturing flow and D-LSS governance, while SMT and semiconductor back-end applications remain transferability domains rather than claimed empirical outcomes.

1.1 Research questions and contributions

RQ1. How can fragmented daily production-tracking workbooks be reconstructed into an auditable longitudinal event history for high-mix semiconductor-equipment contract manufacturing?

RQ2. How strongly do integration cycle time and schedule adherence vary across product families after restricting inference to exact milestone dates?

RQ3. Do calendar progression, documented shortage remarks and product family explain observed cycle-time or late-completion variation in the available baseline data?

RQ4. How should the resulting empirical evidence be embedded into a control-oriented Digital Lean Six Sigma system that is transferable to SMT and semiconductor back-end operations without overstating domain equivalence?

The paper contributes six elements: (1) a reproducible longitudinal reconstruction method for spreadsheet-based production records; (2) a cleaned unit-level empirical baseline spanning 562 machines/assemblies and seven product families; (3) exact-date cycle-time and schedule-adherence analyses with uncertainty reporting; (4) a control-oriented D-LSS theory of change linking measurement integrity, observability, diagnosis, intervention and sustainment; (5) a high-mix event-history perspective that preserves incomplete/censored production states rather than silently deleting them; and (6) a transferability architecture connecting semiconductor-equipment CM learning to SMT and OSAT control requirements. The study deliberately distinguishes observed plant evidence, operational planning standards, literature evidence and analytical derivations.

2. Vietnam industrial context and why operational excellence matters

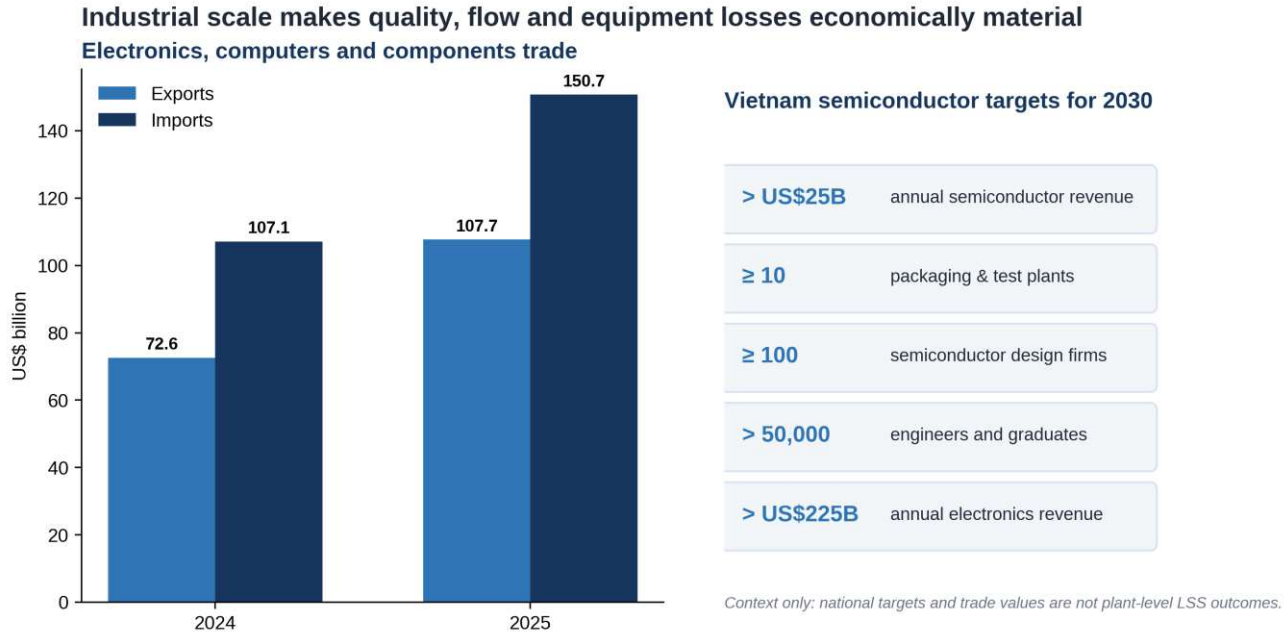


Figure 1. Vietnam electronics trade and 2030 semiconductor targets. Sources: National Statistics Office of Vietnam (2025, 2026) and Government of Vietnam (2024a).

Indicator	Verified public evidence	Why it matters for LSS research
Electronics/computer/component exports, 2025	US$107.7B; 22.7% of national exports; +48.4% YoY	Large scale magnifies the cost of scrap, retest, waiting and instability.
Electronics/computer/component imports, 2025	US$150.7B	Imported-input exposure increases the value of material-yield protection and inventory control.
Semiconductor target, 2030	>US$25B/year; ≥10 packaging/test plants; ≥100 design firms	Packaging/test quality, equipment productivity and engineering learning become strategic capabilities.
Semiconductor workforce target, 2030	>50,000 engineers/graduates	Statistical thinking and structured problem solving must scale faster than individual expert knowledge.
Amkor Bac Ninh footprint	US$1.6B committed to first two phases; 200,000 m² planned cleanroom	Shows advanced packaging/test scale and the relevance of back-end process control.
Intel Vietnam footprint	US$1.5B invested; described by Intel as its largest assembly/test facility	Shows established back-end manufacturing depth; not used as an LSS outcome.

The key analytical point is not that national export growth proves manufacturing productivity. It does not. Export and import values are macroeconomic measures and are influenced by product mix, prices, FDI structures and supply-chain flows. Their role here is to establish the scale and strategic direction of the manufacturing system in which process-improvement capability will be deployed. The plant-level causal unit remains the process, line, tool, product family, lot or package—not the national trade series.

3. Literature foundation and novelty boundary

3.1 From LSS to DMAIC 4.0: what is already known

The LSS literature already establishes the complementarity of flow and variation reduction. In high-mix electronics assembly, Raghavan et al. (2014) reported a 40% reduction in pilot-line cycle time and 10–30% defect reductions after Lean transformation. In SMT solder printing, Li et al. (2008) applied DMAIC with Taguchi design and control charts, reducing the standard deviation of solder thickness from 13.69 to 6.04 and increasing Cpk from 0.487 to 1.432. These cases show why an electronics-specific LSS approach must preserve both flow and statistical-control logic.

Digital integration is also well developed conceptually. Pongboonchai-Empl et al. (2024) quantitatively screened 692 papers and performed deeper analysis of 41 studies, finding that the Analyze phase receives disproportionate digital support. Their subsequent DMAIC 4.0 study used design science, expert interviews, action research and Delphi evaluation to build an empirically evaluated roadmap containing technology-enhanced DMAIC tasks (Pongboonchai-Empl et al., 2026). Ibrahim et al. (2026) then developed a unified framework tailored to EMS, explicitly addressing deployment sequencing, organizational readiness and phase balance. Therefore, a paper that merely maps IoT, AI, analytics or MES tools onto DMAIC would have weak novelty in 2026.

The remaining opportunity lies at the boundary between continuous-improvement governance and control engineering. Semiconductor manufacturing is not only data-rich; it is characterized by high mix, interacting upstream/downstream effects, tool-to-tool and chamber-to-chamber differences, sparse metrology for some CTQs, drift, maintenance events and recursive recipe changes. Bode et al. (2007) show that high-mix R2R control needs state-estimation logic when product-specific data are sparse. Chang et al. (2011) use group/product EWMA to share information across similar low-frequency products without destabilizing high-frequency product control. Chen et al. (2023) further address instability in tool-based EWMA under diverse product-model mismatch. VM extends this architecture by predicting quality from equipment and process variables between physical metrology observations (Maitra et al., 2024).

3.2 Novelty positioning relative to the 2024–2026 frontier

Capability	Pongboonchai-Empl et al. 2024	Pongboonchai-Empl et al. 2026	Ibrahim et al. 2026 EMS	This study
DMAIC + Industry 4.0 mapping	Strong	Strong	Strong	Used as baseline, not novelty
Empirical framework evaluation	Review synthesis	Action research + Delphi	Conceptual/review synthesis	Future plant protocol; no fabricated validation
EMS/electronics specificity	General manufacturing	General manufacturing	Strong	SMT process physics + control logic
Semiconductor back-end specificity	Limited	Limited	Limited	Die attach, wire bond, mold, final test/OQA
FDC / APC / R2R / VM layer	Limited	Technology-level	Limited	Explicit control layer and decision rules
Hierarchical high-mix statistics	Limited	Limited	Limited	Product/tool/recipe/shift random-effects and stratified SPC
Capability-to-risk / flow-to-WIP translation	Not central	Not central	Not central	Explicit analytical translation with assumptions
Causal plant validation design	Not sector-specific	Framework evaluated, not SMT/OSAT causal protocol	Not plant-causal	Matched control/DiD or ITS + mixed models
Vietnam industrial context	No	No	No	Official data + deployment design

Table 2 defines the novelty boundary conservatively. The present study does not compete with DMAIC 4.0 on the breadth of digital technologies or claim a first generic framework. Its narrower contribution is a control-oriented architecture for two physically different but strategically connected manufacturing domains, together with statistical and causal mechanisms that make the proposed artifact testable.

3.3 Process-control theory: why hierarchy and feedback change LSS

Traditional univariate SPC is valuable but can be misleading when heterogeneous populations are pooled. Semiconductor datasets are commonly nested by factory, area, tool, module/chamber, recipe, product, lot and unit; SMT data are similarly nested by product family, panel/board, pad/component, printer, stencil, paste lot, shift and environmental condition. Modern semiconductor statistical practice therefore combines conventional SPC with multivariate monitoring, PCA/PLS, change-point logic, Bayesian/hierarchical models, FDC and APC (Qin, 2012; Chen and Chen, 2026). The practical implication for LSS is that Measure and Analyze must preserve the data-generating hierarchy rather than flatten it into a single Pareto chart.

Feedback changes the Control phase as well. In a conventional LSS project, the control plan is often a chart plus operator reaction instructions. In advanced semiconductor manufacturing, Control may include automated equipment-state classification, predictive excursion detection, VM, or a R2R controller that updates a recipe after each relevant run. These systems require guardrails: validated sensors and metrology, bounded control variables, drift detection, model-version control, fail-safe fallback recipes, and engineering ownership. The D-LSS architecture therefore treats control automation as a governed extension of DMAIC rather than an independent AI project.

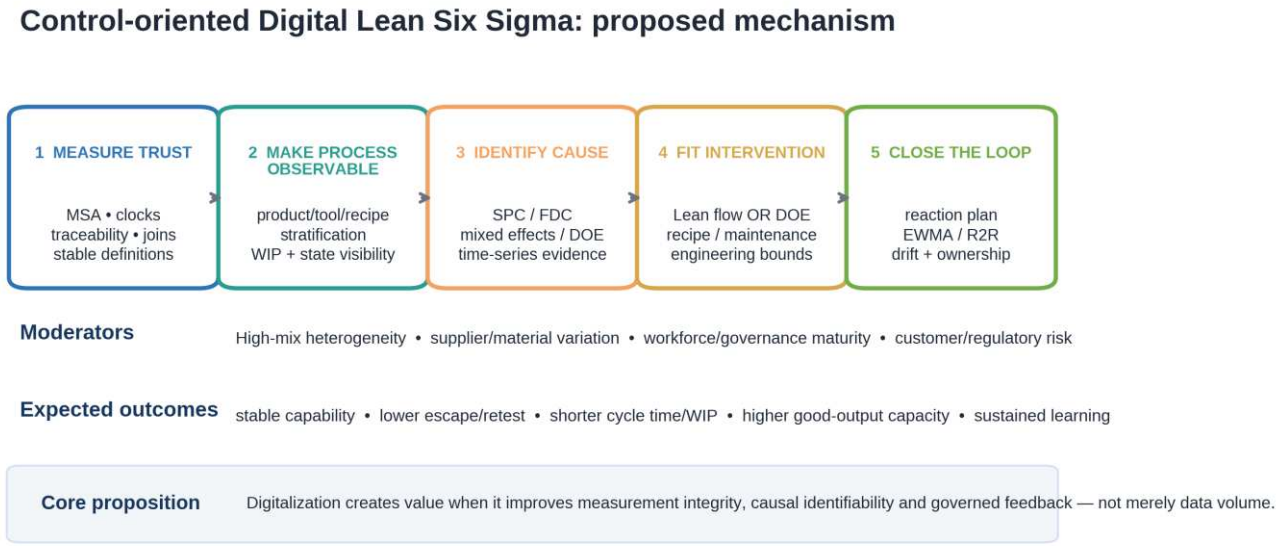


Figure 2. Proposed causal mechanism linking digital data to sustainable operational performance.

4. Research design and longitudinal industrial study

4.1 Study logic and empirical boundary

The research combines explanatory longitudinal case analysis with design-science logic. The empirical unit is a machine/equipment assembly tracked through production milestones at an anonymized Vietnamese contract manufacturer. The site assembles semiconductor production/inspection equipment; it does not fabricate wafers or package semiconductor devices. This distinction is maintained throughout the analysis. The design-science artifact is the D-LSS control architecture; the longitudinal case supplies plant-level evidence about data quality, product heterogeneity, flow variation and schedule risk that directly informs the artifact's measurement and control requirements.

4.2 Data sources and longitudinal reconstruction

The empirical archive contained 139 files, including 128 daily/periodic production-tracking workbooks plus monthly schedules and supporting capacity/UPH records. Tracking workbooks were dated from file names and covered 111 unique snapshot days between 24 October 2024 and 29 March 2025. Product-sheet names were normalized to seven families: Family A, Family B, Family C, Family D, Family E, Family F and Family G. For each workbook, the parser located the Product ID header and extracted available milestone fields such as frame arrival, material issue/full receipt, Start Integration, target completion, Final QC, packaging and shipment, together with source workbook and sheet provenance.

Because many later snapshots replace completed milestone dates with the text 'Done', the analysis did not treat the final workbook as the sole truth source. Instead, every unit was reconstructed across all available

snapshots. Direct calendar dates observed anywhere in the longitudinal history were retained; conflicting direct dates were flagged, and the modal date with the latest supporting observation was selected under a pre-specified rule. 'Done' states were recorded only as proxy completion evidence when no direct date existed. Primary statistical inference in this paper excludes such proxy dates and therefore uses exact-date pairs only. This conservative evidence hierarchy reduces sample size but improves reproducibility and protects against false precision.

Reconstruction stage	Count	Interpretation
Tracking workbooks parsed	128	Daily/periodic operational snapshots
Unique snapshot days	111	24-Oct-2024 to 29-Mar-2025
Deduplicated snapshot observations	53,860	Family × Product ID × snapshot after richness-based duplicate resolution
Unique reconstructed units	562	Seven product families
Exact Start Integration → Final QC pairs	125	Five families; Family E n=4 retained descriptively only
Primary exact cycle-time sample	121	Four families with n≥9
Exact target completion → Final QC pairs	140	Primary schedule-adherence sample

4.3 Outcomes and statistical analysis

The primary flow outcome is integration cycle time, CT_i = FinalQC_i - StartIntegration_i, expressed in calendar days. The primary delivery outcome is schedule deviation, SD_i = FinalQC_i - TargetComplete_i; SD>0 is classified as late completion. Additional reconstructed intervals include full-receipt-to-integration, receipt-to-QC, QC-to-packaging and frame-arrival-to-QC where exact dates exist. The primary cycle-time comparison uses medians, 95% bootstrap confidence intervals, Kruskal-Wallis omnibus testing and Holm-adjusted pairwise Mann-Whitney tests with Cliff's delta effect sizes. A heteroskedasticity-robust OLS model of log(1+CT) evaluates product-family, start-month trend and explicit shortage-remark associations. A robust binomial GLM models late-completion odds using the same covariates. These models are associational because treatment assignment and intervention timing were not controlled.

For incomplete units, event-history logic is used as a sensitivity analysis. Units with an exact Start Integration date and no observed Final QC date are retained as right-censored at their final available snapshot, rather than being deleted. The paper visualizes Kaplan-Meier-style remaining-before-Final-QC curves; formal causal claims are not drawn from this sensitivity analysis. This choice follows the broader manufacturing precedent that survival methods can represent stochastic duration processes and incomplete observations rather than forcing deterministic averages (Ruppert et al., 2021).

4.4 Structured evidence synthesis and source hierarchy

Evidence was assembled through a structured, non-exhaustive synthesis completed through 2 September 2026. Search terms combined Lean Six Sigma/DMAIC with SMT, solder paste printing, PCBA, electronics manufacturing, semiconductor manufacturing, assembly/test, OSAT, outgoing quality assurance, statistical process control, FDC, run-to-run control, virtual metrology and Industry 4.0. Priority was given to original peer-reviewed studies, official standards or government data, and first-party industrial disclosures when they were used only for context. The review is intentionally not labeled a PRISMA systematic review because a complete database-export screening corpus was not constructed; no invented screening counts are reported.

Evidence class	Purpose in this paper	Allowed inference	Safeguard
Official Vietnam statistics/policy	Scale, trajectory and national targets	Context only	No attribution of national growth to LSS
Peer-reviewed SMT/PCBA cases	Mechanism and observed improvement evidence	Process-specific evidence envelope	No transfer of effect size to Vietnam
Peer-reviewed semiconductor control studies	Statistical/control architecture	Method selection and boundary conditions	Distinguish simulation, industrial case and review evidence
Standards (IPC/SEMI)	Operational definitions and acceptance/equipment metrics	Implementation alignment	Standards are not evidence of causal benefit
Author analytical derivation	Risk/capacity/economic translation	Transparent scenario mathematics	Assumptions stated; values not called empirical
Proposed plant protocol	Future evaluation design	Testable research plan	No claim of completed Vietnamese plant validation

4.5 Analytical derivations and assumptions

Three derived relationships are used to translate engineering metrics into decision-relevant quantities. First, Cpk is converted to a centered-normal reference tail probability solely to illustrate order-of-magnitude risk. Because capability indices assume a stable process and conventional Cpk interpretation depends on distributional validity, the result is not an observed DPMO value (Montgomery, 2020; NIST, 2012). For a centered normal process:

$$Referenceppm(Cpk) = 2 \times [1 - \Phi(3Cpk)] \times 10^6$$

Second, flow is translated with Little's Law, WIP = Throughput × Cycle Time, under stable long-run flow conditions (Hopp and Spearman, 2011). Thus, if average throughput is held constant, a 40% cycle-time reduction implies approximately a 40% reduction in average WIP. The statement is an analytical implication, not a claim that the Raghavan et al. (2014) factory measured a 40% WIP reduction.

Third, economic translation separates engineering evidence from accounting assumptions. A proposed cost-of-poor-quality (COPQ) identity is:

$$COPQ = C_s N_s + C_r N_r + C_t N_t + C_e N_e + C_d T_d + C_h \int WIP_h old(t) dt$$

where the terms represent unit costs and quantities for scrap, rework, retest and escapes, plus downtime cost and time-integrated WIP holding cost. For capacity, a non-standard but transparent good-output potential metric can be expressed as scheduled hours × ideal rate × availability × performance × rolled throughput yield. If SEMI E79 OEE is used, quality must not be double counted. These equations are proposed analytical bridges for plant business cases; they are not substitutes for site finance validation.

5. Cross-domain CTQ, data and control architecture

Domain / step	Critical-to-quality or flow variables	Dominant mechanisms	Minimum digital evidence	Preferred analytical/control methods
SMT — solder paste printing	Paste volume/height, offset, transfer efficiency, bridging/insufficient risk	Stencil/paste aging, support, speed/pressure, separation, cleaning, environment	SPI + printer recipe/log + stencil/paste lot + product/pad ID	MSA; family/pad stratification; DOE; capability; EWMA/SPC; causal closed-loop after validation
SMT — placement	Placement offset, missing/wrong/polarity, feeder/nozzle errors, micro-stops	Feeder/nozzle wear, component presentation, vision/setup, product mix	Machine events + feeder/nozzle ID + AOI feedback + MES	Pareto by product/feeder; OEE loss tree; SMED; mistake-proofing; event-rate control
SMT — reflow	Peak temperature, TAL, ramp/soak, solder-joint/void defects	Recipe/load drift, oven zone variation, board thermal mass, contamination	Profiler + oven zone data + product recipe + AOI/X-ray	DOE; profile window; SPC; FMEA; change-control
SMT — AOI/X-ray	Escape, false call, review agreement, defect class	Algorithm threshold, image quality, reviewer inconsistency	Image/result + review disposition + downstream confirmation	Attribute MSA; precision/recall by defect class; risk-based thresholding
SMT — ICT/FCT/repair	FPY, retest, diagnosis/repair cycle time, fixture loss	Fixture/contact wear, software/recipe mismatch, fault isolation queues	Tester logs + failure code + fixture cycles + repair history	VSM; retest Pareto; survival/wear analysis; product-family SPC
OSAT — die attach/flip-chip	Placement, bond-line thickness, void, cure response	Material aging, placement/force/temperature drift, vision offset	Tool/recipe + material lot + vision/X-ray + metrology	Nested capability; DOE; FDC; material controls
OSAT — wire bond/interconnect	Pull/shear, ball geometry, loop height, NSOP/weak bond risk	Capillary wear, force/time/ultrasonic energy, surface/material variation	Bonder trace + tool/head + capillary cycles + pull/shear	Mixed-effects models; EWMA/CUSUM; DOE; PM optimization; stratified control
OSAT — mold/encapsulation	Warpage, void, flash, dimension, cure response	Compound lot, pressure/temp profile, tooling wear, changeover	Press curve + material lot + metrology/vision + recipe	DOE; capability; SMED; FMEA; FDC
OSAT — final test/handler	FPY, bin distribution, retest, test time, contact resistance, handler downtime	Socket/contact wear, temperature, program revision, product/tool mix	ATE results + site/bin + socket cycles + handler event + MES	Bin-shift monitoring; GLMM; EWMA; Weibull/survival; R2R where controllable
OSAT — OQA/shipment	Hold rate, escape risk, queue/cycle time, sampling load	Manual handling, batching, information latency, sampling policy	OQA + MES/AMHS + customer quality + hold timestamps	VSM; risk-based sampling; ITS/DiD for automation changes

The shared spine is therefore not a shared statistical model. Both domains need CTQ ownership, traceability, MSA, causal reasoning and control plans. However, SMT tends to require strong board/component/pad and product-family logic, whereas back-end semiconductor processes more often require tool/head/chamber/recipe and lot/package hierarchy, equipment-state definitions and high-mix adaptive control. This distinction is a central design requirement.

6. Control-oriented Digital DMAIC

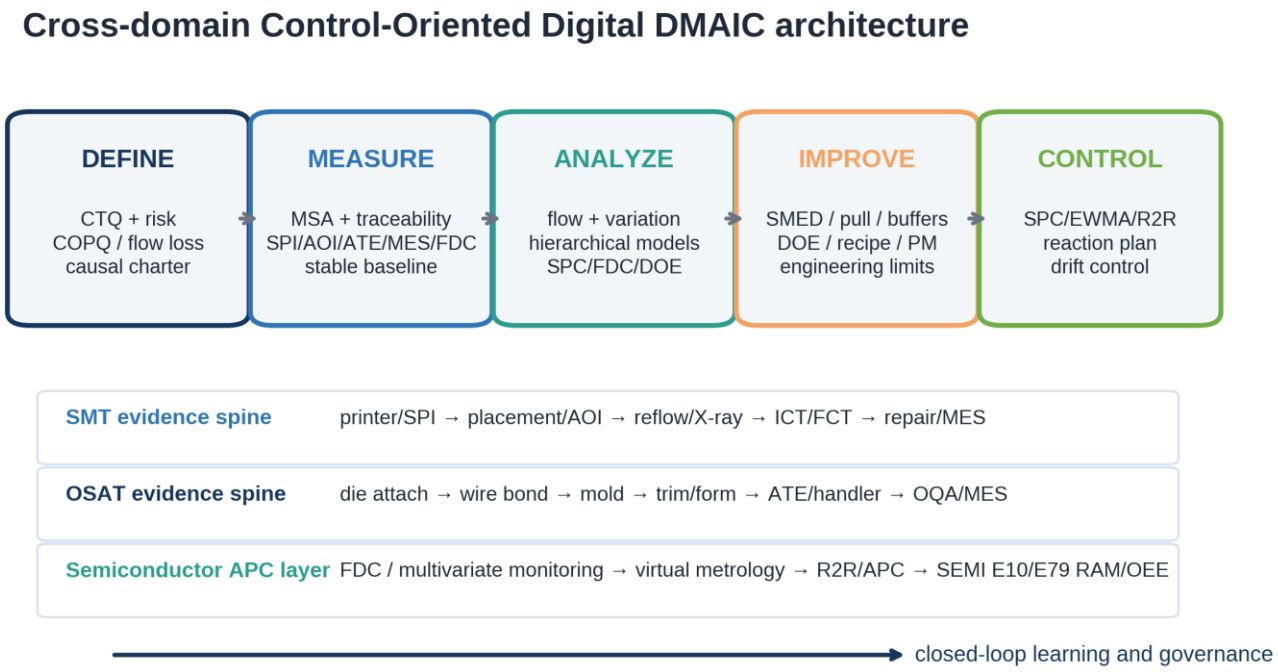


Figure 3. Cross-domain Control-Oriented Digital DMAIC architecture.

6.1 Define — formulate an engineering causal question

A project should start with a customer/business loss and a CTQ, not with an available AI model. The charter must define the unit of analysis, defect/opportunity definition, product/route scope, financial-loss mechanism, owner and expected control mechanism. A useful charter question has the form: 'Which controllable process, equipment or flow mechanism is causing the CTQ distribution or queue behavior to depart from the required state, and how will the intervention be verified against a counterfactual?' This formulation forces a causal hypothesis before data mining begins.

6.2 Measure — establish the measurement and traceability spine

Measure should prove that the data are fit for inference. For variable CTQs, gauge repeatability/reproducibility or an equivalent metrology study should be performed before capability analysis. For AOI/X-ray or classification data, attribute agreement and false-call/escape behavior should be quantified against an accepted reference. Timestamp studies should test missing events, clock synchronization and rework-loop semantics before cycle time is calculated. Finally, product, recipe, machine, tool/head/chamber, material lot, operator/shift and maintenance identifiers should be joinable without post-hoc guesswork. A factory with many sensors but weak identity resolution has low statistical observability.

6.3 Analyze — model hierarchy, flow and variation explicitly

The analysis stage uses two interacting lenses. The flow lens decomposes queue time, WIP aging, batch policy, changeovers, micro-stops, rework loops and constraint utilization. The variation lens analyzes location, dispersion, drift, excursions and covariate effects. High-mix data should not be pooled unless equivalence is demonstrated. A mixed-effects model can represent shared effects while allowing product/tool/shift heterogeneity; multivariate monitoring can detect correlated sensor excursions that univariate charts miss; EWMA/CUSUM can increase sensitivity to small persistent shifts. For semiconductor processes, FDC should be interpreted as a detection and diagnosis layer, not automatically as causal proof (Qin, 2012; Chen and Chen, 2026).

6.4 Improve — choose an intervention matched to the loss mechanism

If the dominant mechanism is flow, interventions include SMED, pull/Kanban, buffer policy, line balancing, route simplification, dispatching or automated material handling. If it is process variation, interventions include DOE, robust parameter windows, material controls, error-proofing, maintenance or calibration. DOE remains preferable when controllable factors can be deliberately varied because it separates main effects and interactions under known assignment logic (Montgomery, 2019). Machine-learning optimization should be

constrained by engineering limits and should not replace experiments when extrapolation risk is high. Herchenbach et al. (2025) illustrates an advanced extension: solder-printing control can combine surrogate optimization, causal knowledge and model-predictive closed-loop adjustment, with reported production spread reduction of 11.3% in open-loop optimization and simulated volume-range reduction of 16.7% for the predictive controller.

6.5 Control — move from charts to governed feedback

Control must specify who reacts, what action is permitted, how quickly, and how the process returns to a validated state. SMT may use product-family/pad-class EWMA, stencil-cleaning triggers and bounded printer adjustments. Semiconductor back-end may combine SEMI E10 equipment-state logic, SEMI E79 productivity/OEE definitions, tool/product EWMA, FDC, maintenance triggers and R2R controllers. VM should initially be advisory unless prediction error, drift, coverage and fallback behavior are validated; it can then support selective metrology or APC where risk permits (Maitra et al., 2024). Model versions, feature definitions and thresholds should be controlled like recipes because an ungoverned model change is effectively a process change.

DMAIC gate	Required evidence before gate closure	Typical reviewer/auditor question
Define	CTQ + customer/business loss; unit/opportunity definition; scope; owner; causal question	Is the project solving customer/factory loss or optimizing a convenient proxy?
Measure	MSA/attribute agreement; stable extraction logic; traceability joins; baseline distribution and product/tool mix	Can the observed change be distinguished from measurement or data-pipeline change?
Analyze	Stratified flow/variation diagnosis; explicit causal hypothesis; confounder list; model diagnostics	Was heterogeneity pooled away? Is the proposed cause identifiable?
Improve	DOE or quasi-experimental change logic; engineering limits; FMEA/risk review; rollback plan	What evidence shows the intervention—not concurrent changes—drove the outcome?
Control	Control limits/monitoring logic; reaction plan; ownership; drift/change-control; sustainment window	How is regression detected, and who has authority to react?

7. Empirical results: high-mix semiconductor-equipment contract manufacturing

To protect commercial confidentiality, the seven product families are labeled Family A through Family G in the public manuscript and reproducibility dataset. The mapping to internal product names is intentionally withheld and is not required to reproduce the reported statistical results.

7.1 Evidence reconstruction and data quality

Across the 128 tracking workbooks, the reconstruction produced 53,860 deduplicated snapshot observations and 562 unique units. Data completeness differed strongly by product family because legacy templates used different milestone conventions and sometimes replaced dates with status words. The primary analysis therefore prioritizes evidentiary quality over maximum sample size. Family E, Family F and Family G contribute to the reconstructed operational population and event-history context but are excluded from the principal four-family cycle-time comparison when exact paired dates are insufficient.

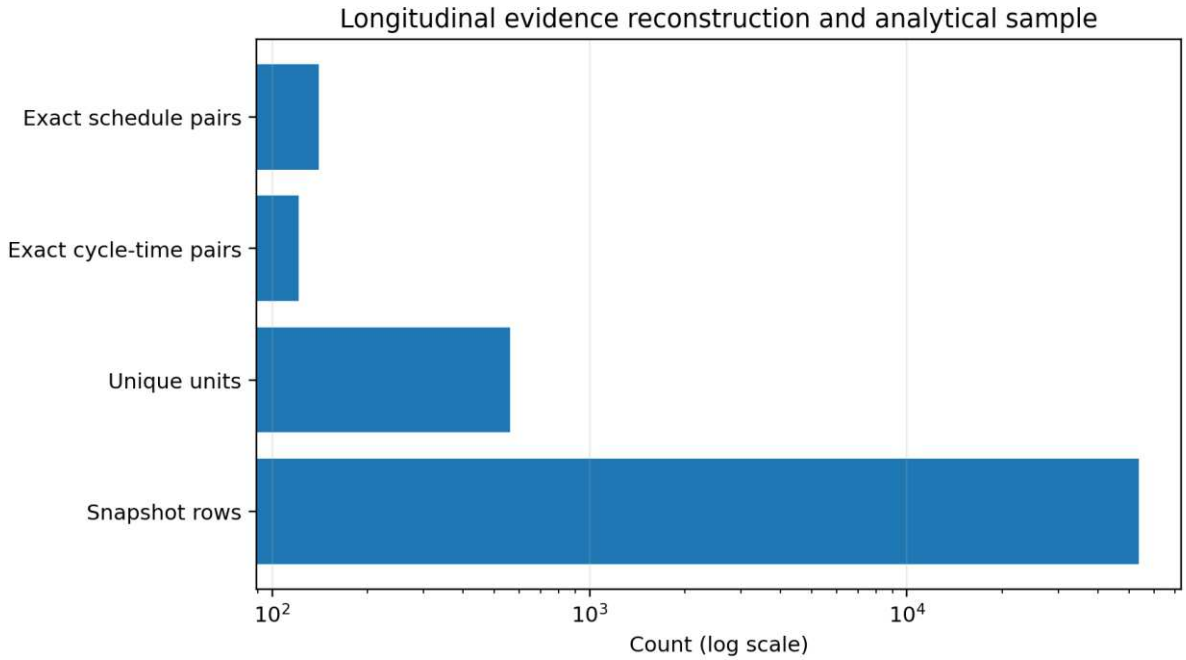


Figure 4. Longitudinal evidence reconstruction and analytical sample. Counts are derived from the submitted CM production-tracking archive.

Product family	Reconstructed units	Exact cycle-time pairs	Exact schedule pairs	Units with date conflicts
Family E	90	4	4	49
Family A	150	36	55	15
Family G	40	0	0	0
Family C	45	35	35	9
Family D	15	9	9	8
Family B	193	41	41	43
Family F	29	0	0	10

Date conflicts are not interpreted automatically as operator error. In an operational workbook they can reflect rescheduling, late data entry, target-date revision or corrected timestamps. For this reason, conflict flags are retained in the analytical lineage and should become a Control-phase data-quality KPI in any deployed D-LSS system. The public reproducibility file excludes customer/order/serial identifiers and exposes only de-identified analytical variables.

7.2 Product-family heterogeneity in integration cycle time

The four-family exact-date sample contains 121 units. The distributions are non-normal, discrete and strongly family-dependent; therefore, median-based and rank-based inference is more defensible than a pooled mean/Cpk interpretation. The omnibus Kruskal-Wallis test rejects equality of the four distributions (H=37.63, p=3.39×10^-8). This result is operationally important: a single plant-wide cycle-time target or pooled control limit would combine fundamentally different product processes and obscure the dominant sources of variation.

Family	n	Median days	95% bootstrap CI	Mean days	P90 days
Family A	36	4.0	3.0–5.0	4.83	9.5
Family B	41	1.0	1.0–5.0	3.00	6.0
Family C	35	1.0	1.0–2.0	1.49	2.6
Family D	9	4.0	3.0–8.0	5.11	8.0

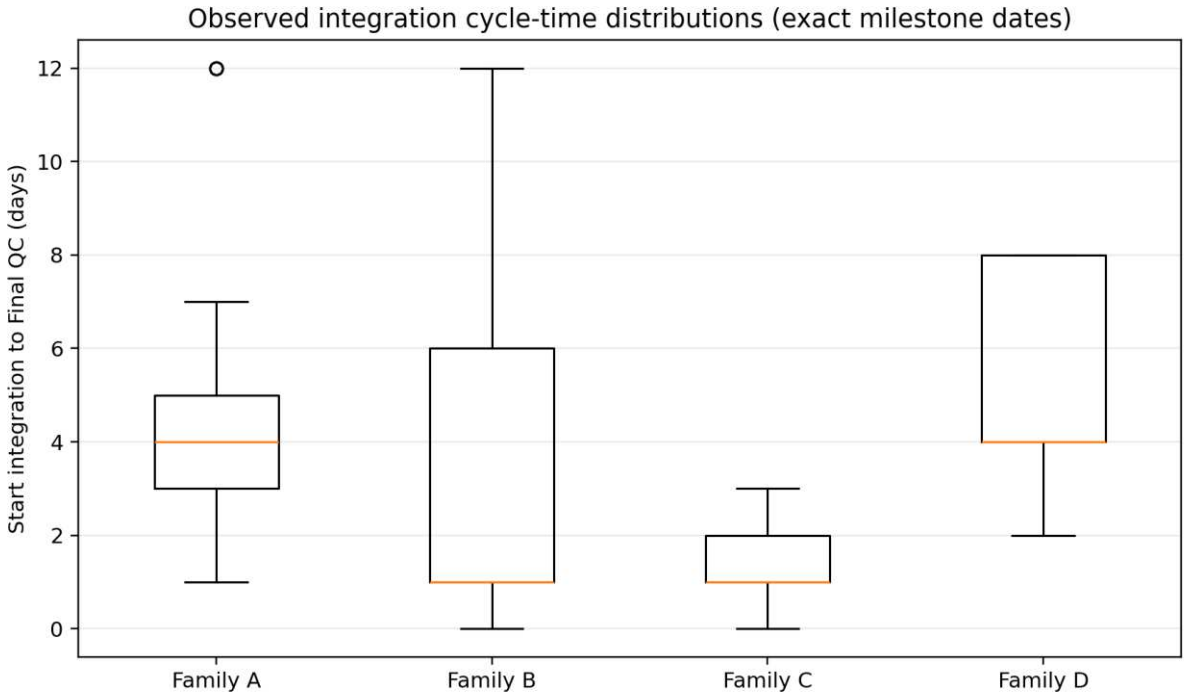


Figure 5. Exact-date Start Integration to Final QC cycle-time distributions by product family.

Pairwise effect sizes reinforce the engineering significance of the family structure. Family A cycle times exceed Family C with a very large Cliff's delta (δ=0.892; Holm-adjusted p=2.97×10^-10) and exceed Family B with a moderate positive effect (δ=0.360; adjusted p=0.024). Family C is also materially shorter than Family D (δ=-0.924; adjusted p=5.71×10^-5). Family A and Family D are not statistically separable in the available exact sample. These results should be interpreted as product-family flow differences, not as quality rankings: more complex equipment may legitimately require longer integration and verification sequences.

7.3 Schedule adherence is not equivalent to cycle time

Exact target-completion and Final-QC pairs were available for 140 units. The late-completion pattern does not mirror median cycle time. Family C has a short median integration cycle but the highest observed late proportion (45.7%), while Family D combines a longer median cycle with a low late proportion (11.1%). This divergence demonstrates a central Lean planning principle: schedule performance depends on the relationship between promised/target time and realized flow, not on raw cycle time alone. It also warns against using a single speed KPI as a proxy for delivery reliability.

Family	n schedule pairs	Late units	Late proportion	Median deviation (days)
Family A	55	22	40.0%	0.0
Family B	41	5	12.2%	0.0
Family C	35	16	45.7%	0.0
Family D	9	1	11.1%	0.0

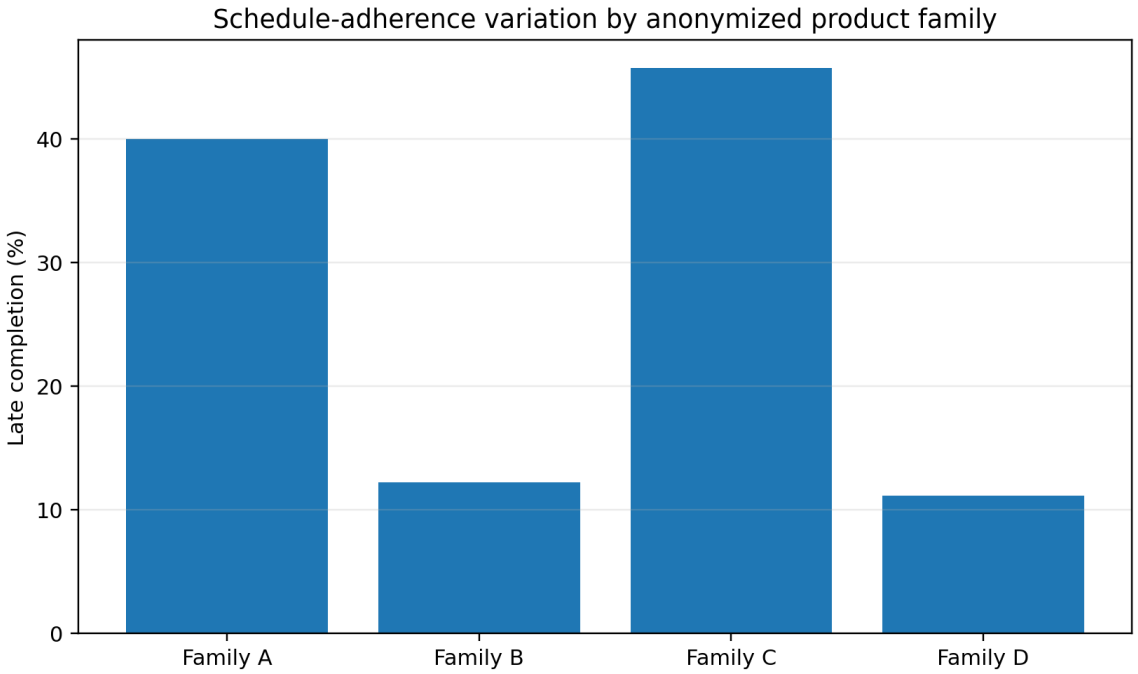


Figure 6. Observed late-completion proportions from exact target/Final-QC date pairs.

7.4 Robust adjusted associations

A heteroskedasticity-robust model of log(1+cycle time), using Family A as the reference family, confirms that the family effect is not an artifact of simple rank comparisons. Family B has a lower adjusted log-cycle coefficient (β=-0.543, robust p=0.00011) and Family C is lower still (β=-0.812, p=2.06×10^-10). Family D is not distinguishable from Family A (p=0.444). The calendar start-month term is positive (β=0.152 per month, p=0.0057), indicating that later cohorts in the exact-date sample tended to have longer log-cycle values after controlling for family. Because the dataset is observational, this trend may reflect product mix, changing work content, capacity pressure or data-capture effects and should not be interpreted as deterioration caused by time itself.

An explicit shortage remark is positively associated with cycle time in the robust model (β=0.196; exp(β)=1.22), but the 95% interval crosses zero and p=0.166. The unit-level shortage sheets are organized partly by PR ranges and current shortage status, which makes causal attribution to a specific unit interval uncertain. Accordingly, the paper does not claim a statistically established shortage effect. Instead, this non-result directly motivates a D-LSS data-design requirement: shortage events must be joined to unit IDs with open/close timestamps and quantity-at-risk before material delay can be estimated causally.

Predictor	β on log(1+CT)	Robust SE	p	exp(β)
Family B	-0.543	0.140	0.0001113	0.58
Family C	-0.812	0.128	2.056e-10	0.44
Family D	0.136	0.178	0.4436	1.15
Start month trend	0.152	0.055	0.005692	1.16
Explicit shortage remark	0.196	0.142	0.1663	1.22

7.5 Event-history sensitivity and incomplete production states

The exact-start event-history sensitivity dataset contains 185 units, of which 121 have observed exact Final-QC events and the remainder are right-censored at the last available snapshot. Retaining censored units is preferable to deleting all unfinished work because deletion would systematically favor faster jobs. The resulting curves are descriptive rather than causal, but they provide a natural Control-phase representation of WIP aging: at any day since integration start, management can estimate what proportion of the cohort remains before Final QC and stratify the curve by product family.

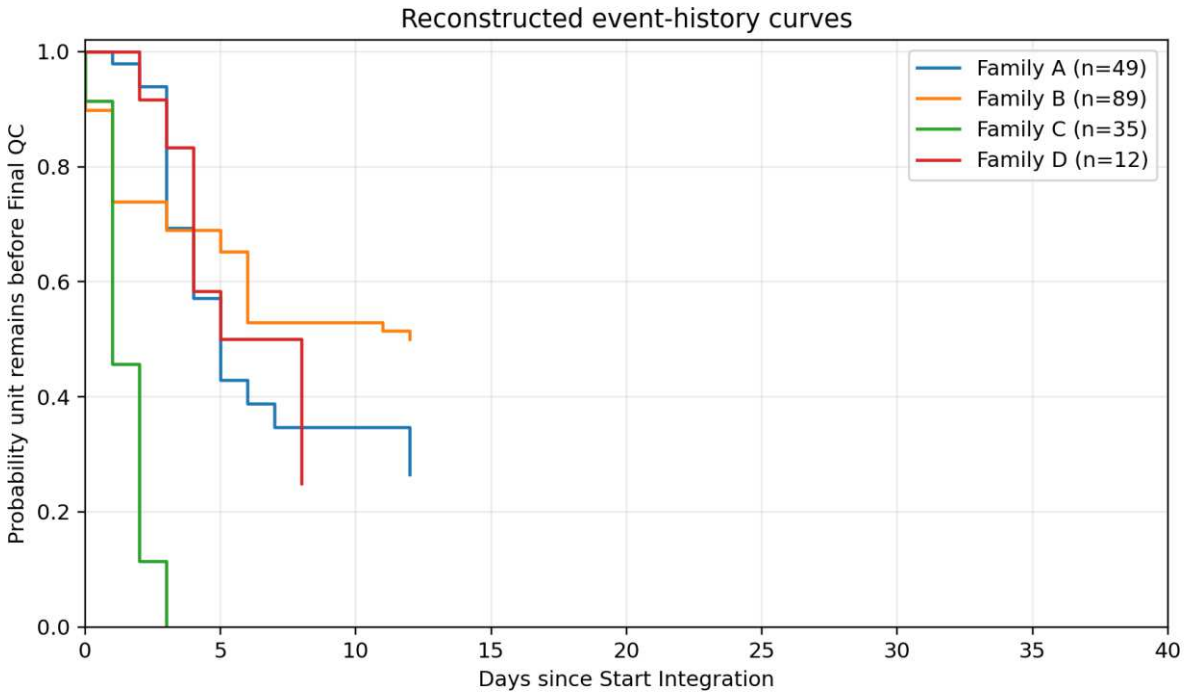


Figure 7. Event-history sensitivity analysis: probability that a unit remains before Final QC after Start Integration. Exact completion dates are used; incomplete units are right-censored at the last observed snapshot.

7.6 Family A: post-ramp stability rather than a simple learning curve

The supporting capacity workbook documents a Family A ramp program involving assembler training, tool preparation, collection of build findings, material preparation, golden-sample planning and targets that progressed from two to five units per week. The same planning file lists standard top-level build assumptions declining from 64 h/unit earlier in 2024 to 55 h and then 48 h. These values are planning/standard-work inputs, not independently measured output data, so they are not treated as empirical improvement effects.

Within the exact-date Family A subset observed from late October 2024 onward, chronological build sequence is not associated with integration-to-QC cycle time (Spearman ρ=0.047, p=0.786). This null result is informative. It suggests that the sampled period follows the major early learning phase or that learning gains are masked by changing product configuration, material readiness and scheduling conditions. A Q1-quality improvement study should therefore avoid attributing later performance to training alone unless an intervention date and pre-ramp comparable units are available.

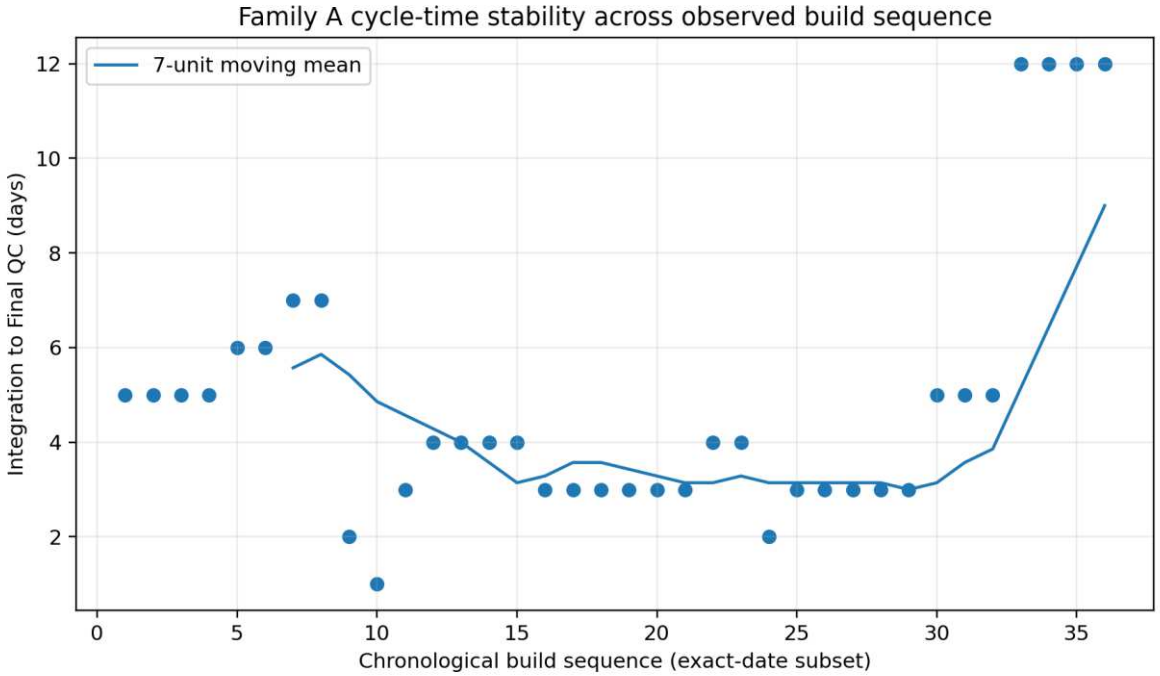


Figure 8. Family A exact-date cycle time across chronological build sequence. The moving mean is descriptive; no monotonic learning association was detected.

7.7 Empirically driven D-LSS control design

The empirical diagnosis changes the recommended improvement architecture. First, product family must be a mandatory stratification variable; pooled cycle-time limits are invalid for this HMLV environment. Second, milestone data quality is itself a CTQ: direct dates, status words and target revisions must be governed through one timestamp dictionary and immutable event logging. Third, schedule risk should be monitored separately from cycle time. A short-cycle product can still be late if target setting or release timing is unstable. Fourth, WIP aging should use event-history logic rather than a fixed red/green threshold across all families. Fifth, material readiness requires unit-level shortage open/close timestamps rather than range-based shortage lists if the plant wants to quantify causal material-delay effects.

A practical Control dashboard can therefore use five linked indicators: (i) family-specific median and P90 integration-to-QC time; (ii) on-time completion probability; (iii) days-since-integration aging percentile relative to the family-specific event-history curve; (iv) unresolved material-shortage exposure with unit-level timestamps; and (v) data-quality exception rate for conflicting or proxy milestones. The reaction plan should trigger root-cause review when a unit crosses a family-specific aging percentile or when the rolling late-completion probability exceeds its baseline confidence band. This architecture converts the reconstructed historical evidence into an executable D-LSS operating routine.

8. Literature-derived benchmarking and analytical translation

Published study	Observed result reported by source	Author-derived interpretation in this study	Boundary
Li et al. (2008), SMT solder printing	σ: 13.69 → 6.04; Cpk: 0.487 → 1.432; mean moved near 150 μm target	Dispersion fell 55.9%; Cpk rose ~194%. Centered-normal reference ppm changes ~144,015 → 17.4	Reference ppm is analytical only; actual defect/escape depends on distribution, stability and defect physics
Raghavan et al. (2014), HMLV PCBA	Cycle time −40%; defects −10–30%	At unchanged average throughput, Little's Law implies ~40% lower average WIP as a steady-state analytical consequence	Study did not establish a universal effect for Vietnam
Lyu et al. (2021), semiconductor OQA	Lots/month 3,106 → 3,719; customer cycle times −43.67%, −57.91%, −58.39%; operators 10 → 7; utilization 61% → 87.26%	Throughput +19.7%; utilization +26.26 percentage points; illustrates flow + automation leverage	Foundry OQA context; not OSAT and not Vietnam
Herchenbach et al. (2025), solder printing	Production spread −11.3% in open-loop optimization; simulated volume range −16.7% in closed-loop predictive control	Shows a path from static parameter optimization toward causal/adaptive control	Closed-loop result reported in simulation; data confidential
Bode et al. (2007); Chang et al. (2011); Chen et al. (2023)	High-mix R2R/EWMA methods address sparse product observations and product/tool mismatch	Supports product/tool-aware feedback rather than pooled generic control	Method evidence; effect sizes are context-dependent

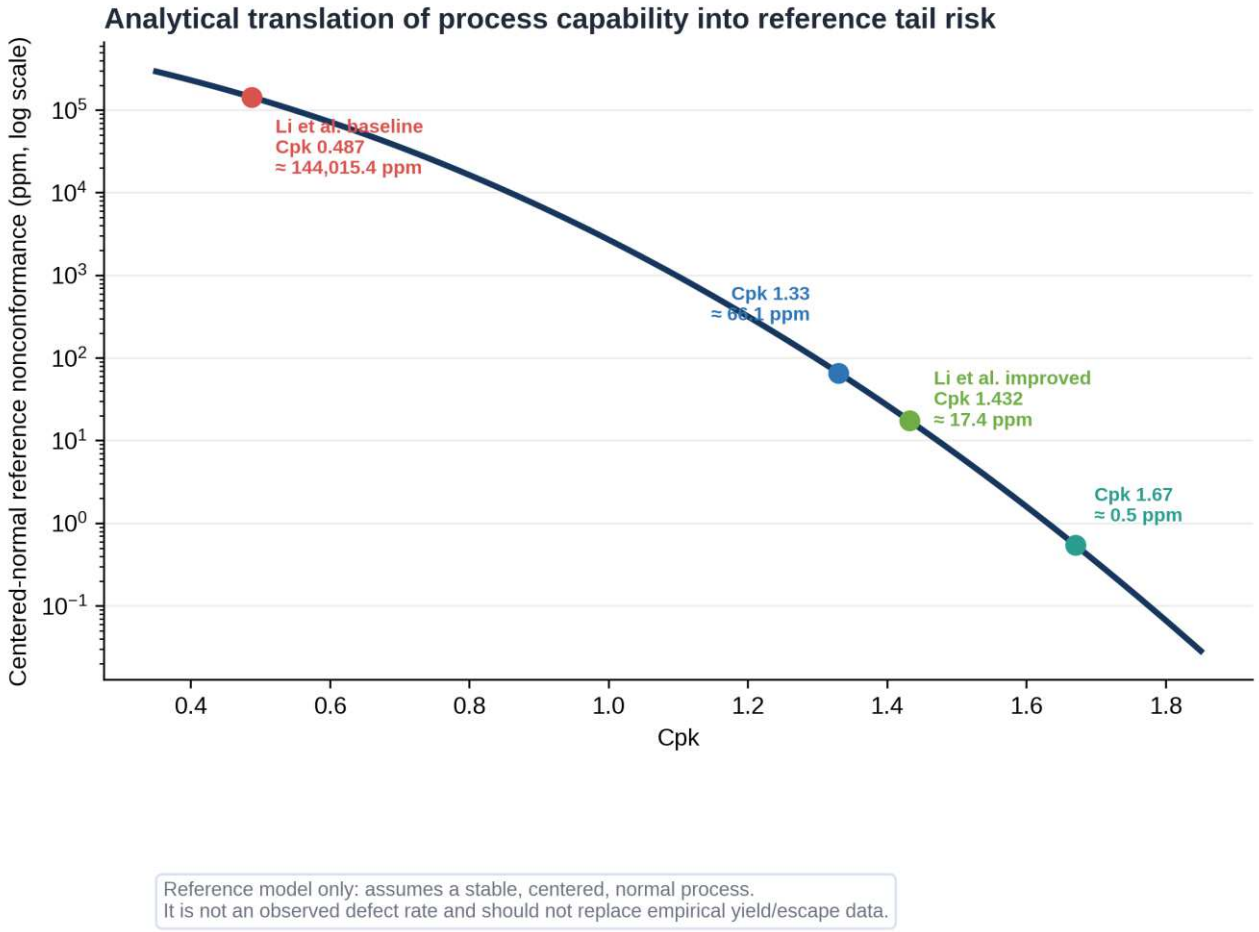


Figure 4. Centered-normal reference translation of Cpk to tail probability. This is an analytical sensitivity view, not an observed DPMO estimate.

Figure 4 makes the risk nonlinearity visible. Moving from Cpk 0.487 to 1.432 is more than a 55.9% reduction in standard deviation: Li et al. (2008) also moved the mean close to the nominal target, so both dispersion and centering improved. Under the reference normal model, capability gains near common industrial thresholds produce orders-of-magnitude differences in tail probability. This is why a factory should report the full distribution, stability evidence and actual FPY/escape data together with Cpk rather than treating Cpk as a self-sufficient quality result.

The same principle applies to flow. Mean cycle time should be accompanied by median and upper-tail measures (for example P90/P95) because high-mix production often contains a long tail of held, reworked or low-frequency products. WIP should be analyzed by age and route state, not only total quantity. In final test, retest consumes capacity without necessarily appearing as a classical defect, so quality-adjusted throughput and retest-adjusted test time can be more decision-relevant than raw tester UPH.

9. Transferability protocols for SMT and semiconductor back-end operations

8.1 Pilot A — SMT solder-paste printing as a closed-loop D-LSS project

Problem definition. Select one product family or a deliberately stratified family set in which printing contributes materially to downstream defects, rework or inspection load. Define CTQs at pad/component/board level (e.g., paste volume, height, offset and insufficient/excess/bridging classes), together with customer-relevant downstream confirmations. Do not use SPI pass rate alone as the business outcome because thresholds can change without changing solder-joint risk.

Measurement design. The minimum key structure is board/panel ID → product family → pad/component location → printer/recipe → stencil ID/age and cleaning history → paste lot/age → environmental condition → SPI measurement → downstream AOI/X-ray/ICT/FCT disposition. Confirm SPI repeatability/reproducibility or an equivalent metrology study and audit timestamp/ID completeness. If different pad geometries have different expected transfer behavior, control/model by pad class rather than pooling.

Analyze and improve. Build a flow map of printer waiting, cleaning, changeover and rework loops in parallel with a variation model. Candidate factors include print speed, squeegee pressure, separation, cleaning frequency, board support, stencil condition, paste age/temperature and interactions. Use engineering knowledge to narrow the factor space, then a blocked or split-plot DOE when some factors are hard to change. Include product/stencil/shift effects where appropriate. The confirmation run must be separated from the factor-screening data.

Control. Establish family/pad-class control logic, bounded parameter windows, stencil-cleaning and material-expiry triggers, and an explicit response to sustained EWMA or capability deterioration. A closed-loop printer adjustment should be introduced only after the measurement system and causal relationship are stable. IPC J-STD-001J provides soldering process/material requirements and IPC-A-610J provides post-assembly acceptance criteria; these standards define acceptance/process context but do not replace the project's statistically validated CTQs (IPC, 2024).

8.2 Pilot B — OSAT final test and retest-capacity loss

Problem definition. Final test is a strong D-LSS pilot because quality and capacity losses are coupled. Define FPY, bin distribution, retest rate, test time, handler downtime, contact-related failures and socket life. Separate true device failures from contact/handling/test-system phenomena; otherwise the project may reduce retest by relaxing diagnostic rules rather than improving manufacturing performance.

Measurement design. The minimum hierarchy is device/product family → lot/package → tester → handler → test head/site → program/revision → socket/contactor and cycle count → temperature condition → initial bin/result → retest sequence/result → equipment alarm/state → timestamps. Link maintenance and contactor changes. Align equipment time-state definitions to SEMI E10 and equipment-productivity/OEE calculations to SEMI E79 where available so that capacity claims are comparable and not based on ad hoc downtime definitions (SEMI, 2021, 2022).

Analyze and improve. Use bin-shift and retest Pareto by product/tool/site, then model the probability of first-pass failure with a binomial mixed model or equivalent hierarchical method. Positive skew in test time may require log-normal/gamma modeling or robust quantile analysis. Socket/contact wear can be treated with survival/reliability methods. If a process input can be adjusted run-to-run, use product/tool-aware EWMA or R2R logic rather than one pooled offset. Where upstream process trace is available, incorporate it as covariates instead of treating final test as an isolated inspection station.

Control. Monitor product/tool/site residuals and bin-distribution shifts, define socket-maintenance triggers, freeze approved program versions, and couple repeated anomalies to FDC/maintenance investigation. If VM or predictive classification is introduced, manage prediction error, drift, confidence/coverage and fallback to physical tests. Financial validation should convert avoided retest time and downtime into released good-output capacity, while avoiding double counting improvements already reflected in OEE or FPY.

10. Causal validation protocol for Vietnamese plants

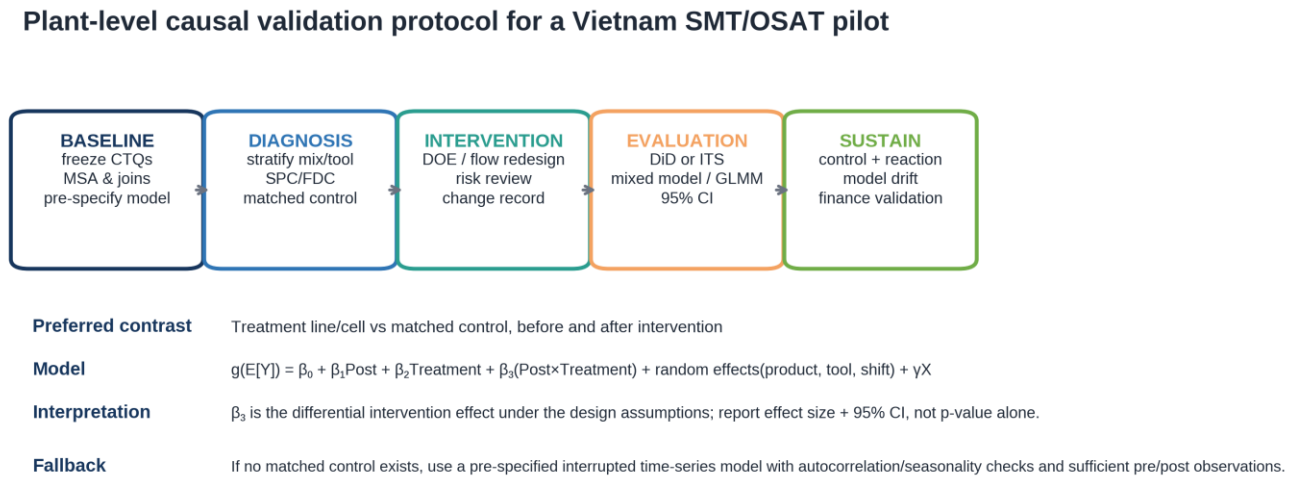


Figure 5. Recommended causal validation sequence for plant-level SMT/OSAT studies.

A Q1-quality empirical extension should not use a simple before/after mean comparison. Production performance changes with mix, learning, engineering revisions, maintenance, seasonality, staffing and demand. The preferred design is a treated line/cell/tool group with a matched control observed over pre- and post-intervention periods. Where treatment assignment cannot be randomized, difference-in-differences (DiD) can estimate the differential change if the control provides a credible counterfactual. If no control exists, interrupted time series (ITS) with an a priori impact model, autocorrelation checks and time-varying covariates is stronger than two snapshots (Bernal et al., 2017).

$$g(E[Y_{ipst}]) = \beta_0 + \beta_1 Post_t + \beta_2 Treat_i + \beta_3 (Post_t \times Treat_i) + u_product + u_tool + u_shift + \gamma X + \varepsilon$$

In the model above, β3 is the differential intervention effect under the design assumptions, while random effects represent repeated observations nested within product, tool and shift. X contains pre-specified covariates such as product mix, volume, material lot, recipe revision or environmental condition. The link function g and outcome distribution should match the data. Continuous approximately normal CTQs may use a linear mixed model; binary pass/fail or escape outcomes a binomial generalized mixed model; overdispersed defect/retest counts a negative-binomial model; positive-skew cycle time a log-normal/gamma model or quantile regression; and time-to-failure/socket life a survival model. Report effect sizes and 95% confidence intervals, not p-values alone.

Outcome	Recommended primary analysis	Key diagnostic / design concern
Variable CTQ (paste volume, pull/shear, dimension)	Linear mixed model or robust/hierarchical alternative; capability after stability check	Normality/transform, nested product/tool effects, MSA
Pass/fail, escape, FPY	Binomial GLMM / risk difference or odds ratio	Changing inspection threshold; dependence/repeated units
Defect/retest counts	Poisson or negative-binomial mixed model	Overdispersion and exposure/opportunities
Cycle time / queue time	Log-normal/gamma mixed model; median/P90/P95; ITS for intervention	Long tails, holds, censoring, volume/mix
Bin distribution	Multinomial/Dirichlet-multinomial or monitored category proportions	Multiple testing, rare bins, program revisions
Equipment failure / socket wear	Survival/Weibull or recurrent-event model	Maintenance censoring and replacement policy
Multi-sensor FDC	PCA/PLS/other multivariate monitoring + fault diagnosis	Concept drift, false alarm rate, explainability
Plant intervention effect	DiD with matched control; ITS if control unavailable	Parallel-trend/impact-model assumptions, autocorrelation, concurrent changes

Sample size should be determined by the planned estimand and data hierarchy, not by a universal number of boards or lots. The analysis plan should be written before Improvement: primary CTQ, effect metric, product/tool strata, exclusion rules, baseline/post windows, multiple-testing method and treatment of rework/retest observations. For many simultaneous CTQs or bins, false-discovery-rate control or a pre-specified primary/secondary hierarchy reduces selective reporting. Engineering significance should be assessed against specification margin, customer risk and economic impact in addition to statistical significance.

11. Vietnam deployment model: from pilot to operating system

The practical deployment sequence should begin with measurement and traceability rather than AI. Large multinational sites may already have mature MES/FDC infrastructures, while local suppliers may have partial traceability and manual inspection. A common national or supplier-development playbook therefore needs maturity gates. The proposed D-LSS Readiness Rubric below is a design artifact for assessment and prioritization; it has not yet been psychometrically validated.

Maturity level	Measurement & traceability	Analytics & causal discipline	Control & governance	Recommended next move
0 — Reactive	Manual records; inconsistent IDs; limited MSA	Defect firefighting / anecdotal root cause	Operator-dependent reaction	Standard definitions, MSA, traceability and loss Pareto
1 — Visible	Basic digital inspection/MES; partial joins	SPC/VSM on isolated datasets	Static control plans	Create joined quality-flow-equipment data and CTQ ownership
2 — Integrated	Reliable product/tool/material joins	DOE, stratification, mixed models; flow/variation separation	Automated alerts with defined reaction	Pilot causal evaluation and family/tool-specific controls
3 — Closed-loop	High-frequency sensor/equipment trace with validated metrology	FDC, predictive models, causal monitoring	Bounded automated feedback; change/model governance	Expand R2R/VM selectively and validate sustainment/economics
4 — Learning system	Cross-line/supplier traceability and governed data models	Transfer learning/causal learning with drift monitoring	Portfolio governance tied to NPI, supplier and finance systems	Scale only models/interventions that remain stable across products/sites

For supplier development, the architecture should be simplified without being diluted. A supplier does not need a data lake before it can perform MSA, stable SPC, DOE and changeover reduction; conversely, a sophisticated dashboard cannot compensate for an unstable gauge or ambiguous defect definition. The first capability target should therefore be reliable measurement and reaction ownership. Digital depth should increase only when it reduces decision latency or makes previously hidden variation observable.

For workforce development, belt training should be attached to verified projects rather than classroom completion. A Green/Black Belt project should demonstrate a valid measurement system, reproducible extraction logic, a causal analysis consistent with the data hierarchy, an engineering-approved intervention and evidence of sustained control. This links Vietnam's semiconductor workforce expansion to operational capability rather than certificate count.

For governance, LSS portfolios should be integrated with NPI, equipment engineering, customer quality and finance. NPI projects can use the same CTQ/data architecture before mass production; equipment teams can own SEMI-aligned RAM and productivity loss trees; customer-quality teams can connect escapes and complaints to process genealogy; finance can independently validate COPQ and capacity release. This prevents local optimization in which one function reports a gain while another absorbs hidden rework or inventory cost.

12. Research propositions and theoretical implications

P1. Measurement integrity positively mediates the relationship between manufacturing digitalization and LSS performance; without adequate MSA and traceability, additional data volume will not reliably improve outcomes.

P2. Product/tool heterogeneity negatively moderates the effectiveness of pooled LSS analysis; hierarchical stratification or mixed-effects modeling strengthens diagnostic accuracy in high-mix SMT and OSAT.

P3. Mechanism–intervention fit mediates project performance: flow interventions dominate when queue/changeover/batching losses are primary, whereas DOE/process-control interventions dominate when variation/drift is primary.

P4. Closed-loop monitoring and explicit reaction ownership positively mediate the sustainability of LSS gains after project closure.

P5. FDC, VM and R2R control create incremental value only after measurement validity, model drift and bounded-action governance are established.

P6. In Vietnam, supplier data maturity and workforce statistical capability positively moderate the transfer of multinational manufacturing standards into sustained domestic operational capability.

11.1 Theoretical contribution

The framework extends LSS theory by specifying an intermediate causal mechanism between digital technology and performance. Existing LSS 4.0 research often focuses on which technologies enhance which DMAIC tasks. This paper argues that the missing construct is process observability: the degree to which relevant variation, flow states and equipment states can be measured, joined and correctly stratified at the level at which causes operate. Digital technology affects performance indirectly by improving observability; observability improves causal identifiability; and identifiability supports mechanism-fit interventions. This formulation creates testable mediation and moderation hypotheses rather than a technology checklist.

The second contribution is to Control theory within LSS. Control is redefined as a graduated feedback architecture: human reaction plans → statistically triggered actions → equipment-aware FDC → predictive/virtual metrology → bounded R2R/APC. This continuum provides a common language between operational-excellence teams and control/process engineers. It also clarifies why an AI model with high predictive accuracy may still have low operational value if no safe action, owner or feedback path exists.

11.2 Managerial and policy implications

For plant managers, the framework changes project selection. The highest-value opportunities are often interfaces: SPI false calls generating rework queues, tester retest loops consuming invisible capacity, tool drift that only affects a subset of products, or maintenance events that reset a process offset. Projects should therefore be prioritized by customer risk × COPQ × flow leverage × learning value rather than defect count alone.

For Vietnam’s semiconductor policy, the implication is that talent and factory count are necessary but insufficient indicators of industrial upgrading. A packaging/test ecosystem needs reproducible process knowledge: MSA, SPC/FDC, DOE, equipment-state standards, causal validation and change-control. These capabilities are portable across products and suppliers and therefore contribute to domestic learning even when product IP and capital equipment remain multinational.

The empirical study is observational and single-site. It does not contain a randomized or matched intervention, so product-family coefficients and calendar trends are associations rather than causal treatment effects. Exact milestone availability is incomplete and differs by legacy workbook template; the analysis responds by separating exact from proxy evidence and by publishing the reconstruction rules. Material-shortage records are sufficiently rich for operational tracking but not yet normalized into unit-level open/close event histories. These limitations define the next empirical step: prospectively instrument one product family with immutable milestone events, unit-linked shortage timestamps, labor-hour exposure and a pre-specified intervention/control design.

13. Limitations and research agenda

The principal limitation is intentional: the paper does not contain proprietary Vietnamese factory observations. Consequently, it cannot estimate a Vietnam-specific causal effect of LSS on yield, Cpk, cycle time, WIP or cost. The analytical translations are transparent scenario calculations, not empirical results. A Q1 empirical follow-up should execute the protocol in Section 9 and disclose baseline/post distributions, MSA, product mix, treatment timing, concurrent changes and model diagnostics.

Second, the structured evidence synthesis is not an exhaustive systematic review. It prioritizes mechanism-relevant and high-authority sources, including recent 2026 publications that materially change the novelty boundary, but it does not claim complete database coverage. A separate systematic review could quantify effect heterogeneity by electronics/semiconductor process, intervention class and digital maturity.

Third, the paper bridges wafer/fab control literature and back-end/OSAT deployment where direct back-end evidence is thinner. Methods such as R2R and VM should therefore be transferred only when the control variable, metrology latency and product/tool context support the underlying assumptions. Final test, wire bond and mold each have distinct physics that require process-specific validation.

Fourth, the proposed readiness rubric and propositions have not been validated psychometrically or across multiple Vietnamese sites. Future research should test inter-rater reliability, construct validity and predictive validity, and should examine whether supplier maturity and workforce capability explain variation in sustained project performance.

Finally, sustainability outcomes are outside the primary scope. A subsequent Green LSS extension should add energy per good unit, nitrogen/compressed-air use, scrap material, chemical consumption and carbon cost to the same causal and measurement architecture rather than adding environmental KPIs as a parallel scorecard.

14. Conclusion

Vietnam's electronics and semiconductor expansion makes operational excellence a strategic capability, but the 2026 research frontier means that a generic Digital DMAIC framework is no longer sufficiently novel. This study therefore advances a narrower and deeper contribution: a control-oriented D-LSS architecture that connects SMT process physics, semiconductor high-mix control, Lean flow, statistical inference and plant-level causal validation.

The central mechanism is that digitalization has no automatic quality effect. Data must first be trustworthy and traceable; the process must then be observable at the correct product/tool/recipe hierarchy; analysis must distinguish flow from variation and correlation from plausible cause; the intervention must fit the mechanism; and Control must create a governed feedback loop. In SMT, this may progress from SPI MSA and DOE to family-level EWMA and bounded printing adjustment. In semiconductor back-end, it may progress from ATE/equipment genealogy and stratified SPC to FDC, VM and R2R logic. IPC and SEMI standards provide practical process/equipment definitions around this architecture.

The public evidence shows that substantial gains are technically plausible: published cases report major improvements in solder-printing capability, PCBA cycle time and defects, and semiconductor OQA flow. The paper does not treat these results as Vietnam forecasts. Instead, it translates them analytically and provides the experimental/quasi-experimental design needed to determine what a Vietnamese plant actually achieves. This boundary between evidence, derivation and future validation is the feature that makes the proposed framework scientifically testable and practically deployable.

Declarations

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Conflict of interest: The author declares no conflict of interest.

Human participants / ethics: Not applicable. This study uses public secondary data and published literature and does not involve human-subject research.

Data availability: All national statistics and policy documents are publicly available from the cited official sources. Literature-derived process outcomes are traceable to the cited publications. No proprietary Vietnamese factory dataset is claimed.

Author contributions (CRediT): Ngoc Huy Mai — Conceptualization, Methodology, Investigation, Formal analysis, Visualization, Writing – original draft, Writing – review & editing.

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Appendix A. Minimum plant data dictionary for reproducible validation

Domain	Required identifiers	Primary response variables	Key covariates / events
SMT printing	board/panel, product family, pad/component, printer, recipe, stencil	SPI volume/height/offset; downstream defect/escape	paste lot/age, cleaning history, support, speed/pressure/separation, temperature/RH, shift
SMT placement/reflow	board, product, placement machine/feeder/nozzle, oven/recipe	AOI/X-ray class, placement offset, reflow defect, cycle time	feeder/nozzle cycles, micro-stops, zone temperatures, profile revision, changeover
SMT test/repair	board, tester/fixture, program revision, repair record	FPY, retest, repair disposition, diagnostic cycle time	fixture cycles, failure code, program version, technician/shift
OSAT assembly	lot/package, product, tool/head/chamber, recipe, material lot	placement/void, pull/shear, loop/ball geometry, warpage/flash	tool consumable cycles, maintenance, material age, environment, shift
OSAT final test	device/lot/product, tester, handler, head/site, program, socket	initial bin, FPY, retest, test time, contact-related fail	socket cycles, temperature, handler alarm/state, maintenance, upstream route
Flow/equipment	lot/board, route step, equipment ID, event timestamps	cycle time, queue time, WIP age, availability, downtime	SEMI E10 state, setup/changeover, hold reason, volume/product mix

Reproducibility rule: freeze field definitions and extraction logic before the intervention. Any post-hoc change to defect coding, timestamp logic, product grouping or exclusion rules should be versioned and sensitivity-tested. For a double-anonymous submission, plant/customer identifiers should be pseudonymized and external repositories reviewed to avoid revealing author/site identity.

Appendix B. Research-integrity boundary

Empirical cycle-time and schedule-adherence values in this manuscript are reconstructed from the author's submitted CM production-tracking archive and are reported only after de-identification and evidence-quality filtering. Customer, order, serial and part identifiers are not included in the public analytical dataset. The site is described generically as a Vietnamese contract manufacturer assembling semiconductor equipment. The study does not claim that CM assembly results are direct measures of SMT process capability, wafer-fabrication performance or OSAT yield. Literature-derived numbers, planning/standard-hour assumptions and analytical derivations remain explicitly distinguished from observed plant outcomes.