Supplementary

Supplementary Note S1. Bipolar Leaky Integrate and Fire (BiLIF) Neuron

The bipolar leaky integrate and fire neuron (BiLIF) is adapted from the standard LIF neuron model, which update the membrane potential $U(t)$ according to Equation (S1). To determine whether an output spike is to be generated, $U(t)$ is compared against predetermined firing threshold U_{th} (Equation (S2)). Thus, this model is only capable of handling unipolar input and emitting unipolar spikes. In our work, the BiLIF is able to overcome this limitation by using bipolar U_{th} and emit spikes of both positive and negative polarity (Equation (S3)).

$$\tau \frac{dU(t)}{dt} = -U(t) + I_{in}(t)R \tag{S1}$$

$$S(t) = \begin{cases} 1, & U(t) > U_{th} \\ 0, & \text{otherwise} \end{cases} \tag{S2}$$

$$S(t) = \begin{cases} 1, & U(t) > U_{th} \\ -1, & U(t) < -U_{th} \\ 0, & \text{otherwise} \end{cases} \tag{S3}$$

In our experiments, the BiLIF neuron used the following setting: $\tau = \frac{1}{f_s}$, $R = 5$, $U_{th} = 0.8$ and $dt = \frac{1}{f_s}$, where f_s is the sampling frequency of the dataset used. τ, U_{th} and R were swept to find the optimal point where the BIC is similar to DM.

Supplementary Note S2. Izhikevich Neuron Model

The Izhikevich neuron model is a well established neuron model that is capable of reproducing spiking and bursting behavior of known types of cortical neurons[1]. The Izhikevich neuron model is defined according to Equation (S4), and where v is the membrane potential and u is the membrane recovery variable. Upon v reaching the predefined threshold of 30 mV, v and u are reset according to Equation (S5).

$$\begin{aligned} v' &= 0.04v^2 + 5v + 140 - u + I \\ u' &= a(bv - u) \end{aligned} \tag{S4}$$

$$\text{if } v \geq 30mV, \text{ then } \begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases} \tag{S5}$$

In the Izhikevich neuron model, parameters a, b, c and d are set according to the type of spiking/bursting behavior the user seeks to model. In Fig. 3a of the main text, the parameters used to simulate the bursting dynamic are $a = 0.2$, $b = 0.2$, $c = -50$ and $d = 2.0$, while the input current is set to 10 mA.

Supplementary Note S3. Delta Modulation (DM)

Delta Modulation (DM) is a well established technology with a wide range of application. In essence, DM aims to compress the original signal into sparse pulses via step size thresholding, where a spike or event is generated if the change in voltage at the current time exceeds the step size threshold. Many variants of this technique have been developed in the hope of overcoming the shortcomings inherent to DM, such as loss of information through quantization and granular noise from the step size used. In the context of this paper, where we investigate the strengths and weaknesses of different encoding techniques, DM is an extremely simple and effective option. The DM variant used in this paper is Pulse-Count Modulation (PCM).

We define the input voltage signal as $V_{in}(t)$, the reference voltage used to compare if a spike is generated as $V_{ref}(t)$, and the ON/OFF threshold as $V_{th_{on/off}}$.

The input signal is first filtered with a second-order band-pass elliptical filter. With the filtered signal, the median peak-to-peak voltage, $\overline{V_{pp}}$, can be calculated and be used to determine the threshold according to Equation (S6). The k_{DM} parameter is the variable swept to determine the optimal threshold for DM.

$$\begin{aligned} V_{th_{on}} &= k_{DM} \cdot \overline{V_{pp}} \\ V_{th_{off}} &= -V_{th_{on}} \end{aligned} \tag{S6}$$

At each timestep Δ the difference between V_{in} and V_{ref} is compared with $V_{th_{on/off}}$ to determine whether a spike event is generated or not (as seen in Equation (S7)). V_{ref} is incremented or decremented whenever a spike is generated by the corresponding threshold value according to Equation (S8).

$$S(t) = \begin{cases} 1, & V_{in}(t) - V_{ref}(t) \geq V_{th_{on}} \\ -1, & V_{in}(t) - V_{ref}(t) \leq V_{th_{off}} \\ 0, & \text{otherwise} \end{cases} \tag{S7}$$

$$V_{ref}(t+\Delta) = V_{ref}(t) + V_{th_{on/off}} \cdot S(t) \tag{S8}$$

Since k_{DM} is the variable that controls the size of the threshold, it is imperative that an ideal value is chosen to generate a spike train that balances data compression and loss of information. Fig. S1 illustrates how k_{DM} affects the spike generation process on two different datasets. In Fig. S1a and Fig. S1e, it can be seen that at small k_{DM}, a large number of spikes are generated, allowing for accurate reconstruction of the original signal, while at large k_{DM} outputs sparse spikes, leading to very rough approximation of the original signal, as seen with Fig. S1d and Fig. S1h. This phenomena matches our expectation, where small k_{DM} leads to small threshold, which reduces the amount of data compressed and high information retention, while large k_{DM} leads to large threshold, which increases the amount of data compressed and high information loss. In real world application, finding the optimal spot where the balance of high data compression and retaining large amount of information is very challenging.

To this end, we have designed experiments to determine the optimal k_{DM} using the intracortical dataset[2]. For this dataset, we swept k_{DM} and compared the performance of the reconstruction that uses the DM's spike train as input in terms of data compression rate, reconstruction error rate and Bayesian Information Criteria (BIC). The result is summarized in Fig. S2. From Fig. S2a-d, it can be observed that as the compression ratio increases, the RMSE of the reconstruction increases and the BIC increases. With Fig. S2a and b, it can be observed there exists an optimal point where data compression is increased while data loss is minimized.

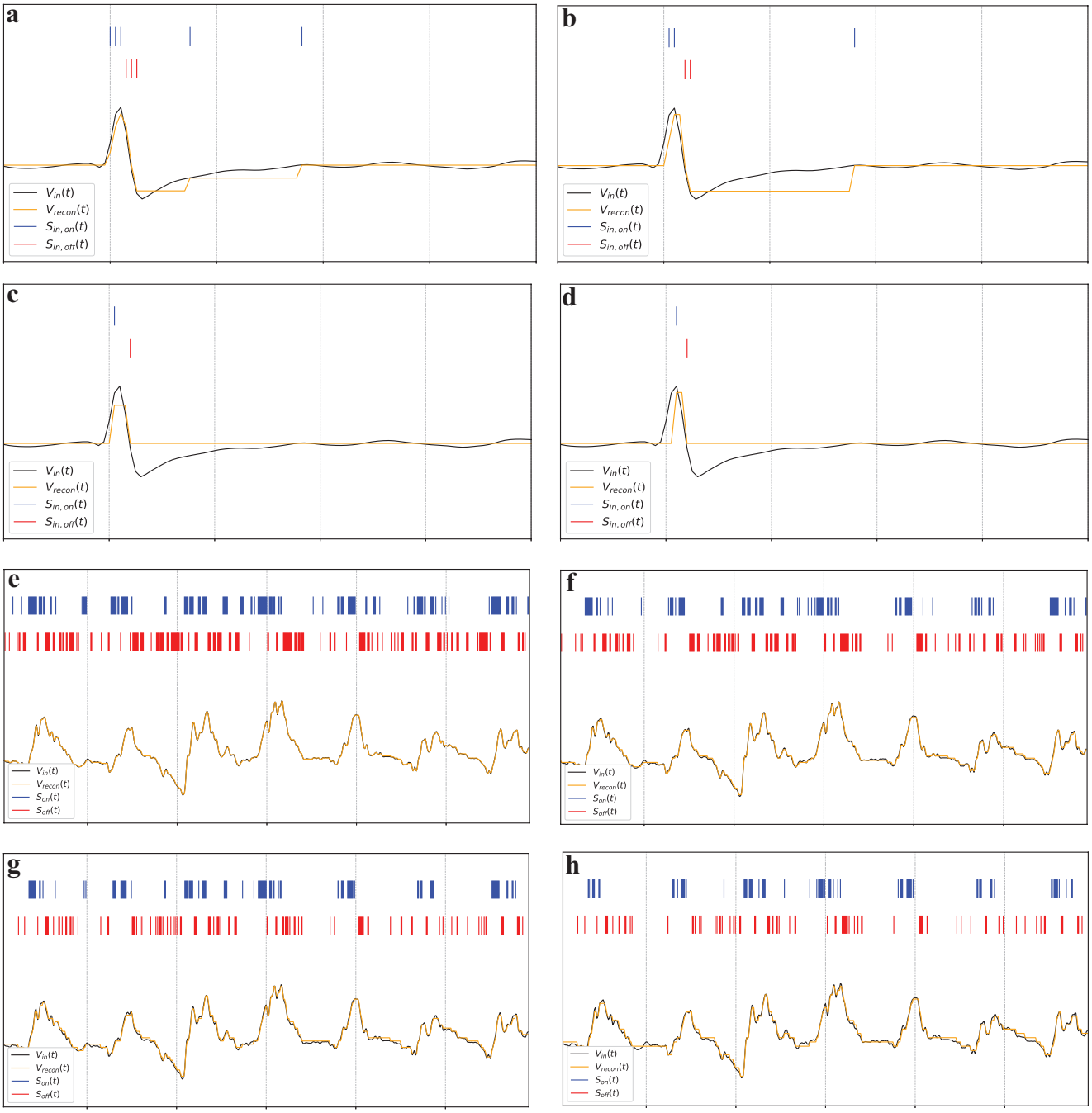

Figure S1. $S(t)$ generated by Delta Modulation under different k for the intracortical dataset (**a** $\sim$ **d**) and iEEG dataset (**e** $\sim$ **h**), along with the corresponding reconstructed signal. **a** $k = 0.2$. **b** $k = 0.4$. **c** $k = 0.6$. **d** $k = 0.8$. **e** $k = 0.1$. **f** $k = 0.2$. **g** $k = 0.3$. **h** $k = 0.4$.

Supplementary Note S4. Burst Delta Modulation (BDM)

Burst Delta Modulation (BDM) is proposed as an extension of conventional Delta Modulation (DM) to improve the trade-off between data compression and information preservation. The key idea is to use two operating modes: a high-threshold mode for suppressing false or noise-induced spike generation, and a low-threshold burst mode for capturing salient signal transitions with higher temporal precision. This mechanism is inspired by bursting neurons in the hippocampus, where both high-threshold late-bursting neurons[3] and low-threshold early-bursting neurons[4] have been observed.

In conventional DM, a fixed threshold is used throughout the encoding process. As discussed in Supplementary Note S3., a

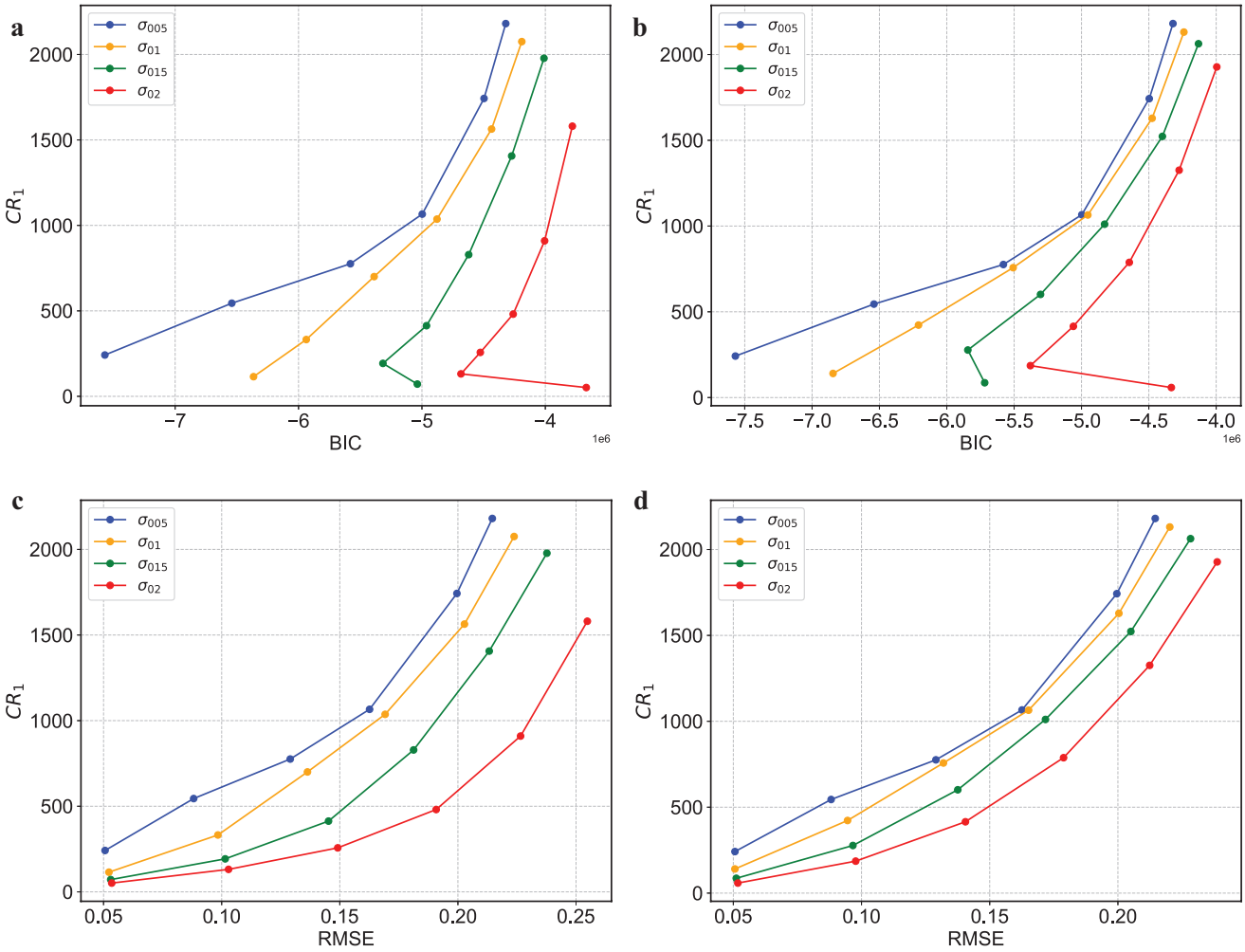

Figure S2. Analysis of how k_{DM} can effect data compression and loss of information using **Delta Modulation** as the ASC encoder. From the four plots, it can be observed there exists a k_{DM} where data compression can be optimized where data loss is minimized. **a** BIC vs CR for intracortical dataset. **b** BIC vs CR for pink noise intracortical dataset. **c** RMSE vs CR for intracortical dataset. **d** RMSE vs CR for pink noise intracortical dataset.

small threshold improves reconstruction accuracy but produces a large number of events, while a large threshold improves compression but may discard important signal details. BDM addresses this limitation by first using a large threshold, θ_1, to detect significant voltage changes. Once such a change is detected, the encoder temporarily switches to a smaller threshold, θ_2, for a fixed burst duration, allowing the local waveform around the event to be represented in more detail. We define $\theta_1 > \theta_2 > 0$.

Similar to DM, the input voltage signal is denoted as $V_{in}(t)$, the reference voltage as $V_{ref}(t)$, and the output spike event as $S(t)$. At each timestep, the difference between $V_{in}(t)$ and $V_{ref}(t)$ is compared with the instantaneous threshold $V_{th}(t)$:

$$S(t) = \begin{cases} 1, & V_{in}(t) - V_{ref}(t) \geq V_{th}(t) \\ -1, & V_{in}(t) - V_{ref}(t) \leq -V_{th}(t) \\ 0, & \text{otherwise} \end{cases} \tag{S9}$$

Whenever an ON or OFF event is generated, the reference voltage is updated by the current threshold step size:

$$V_{ref}(t+\Delta) = V_{ref}(t) + V_{th}(t) \cdot S(t) \tag{S10}$$

The threshold switching is controlled by a slow variable $x(t)$. In the resting state, $x(t) < 0$, and the encoder operates with

the large threshold θ_1. When the voltage difference exceeds the current threshold and $x(t) < 0$, the slow variable is reset to 1, which activates the burst mode:

$$\tau \frac{dx}{dt} + x = -\varepsilon, \quad \text{if } |V_{in}(t) - V_{ref}(t)| > V_{th}(t) \text{ and } x(t) < 0, \text{ then } x(t^+) = 1 \tag{S11}$$

The instantaneous threshold is then defined as

$$V_{th}(t) = (1 - u(x))\,\theta_1 + u(x)\theta_2 \tag{S12}$$

where $u(x)$ is the unit step function:

$$u(x) = \begin{cases} 1, & x > 0 \\ 0, & x \leq 0 \end{cases} \tag{S13}$$

Therefore, when $x(t) \leq 0$, $V_{th}(t) = \theta_1$, and BDM behaves as a high-threshold encoder. Once a significant input transition triggers the burst state, $x(t)$ is reset to 1 and $V_{th}(t)$ switches to θ_2. The encoder remains in this low-threshold state until $x(t)$ decays below zero according to Equation (S11). The effective burst duration is therefore determined by τ and ε. For example, choosing these parameters to produce a burst window of approximately 1 ms allows BDM to capture fast action-potential-like events while suppressing isolated noise fluctuations outside the burst window.

In practice, θ_1 controls the event detection sensitivity, while θ_2 controls the reconstruction fidelity during the burst. A larger θ_1 reduces false spike generation and improves data compression, whereas a smaller θ_2 increases the number of spikes around salient events and reduces reconstruction error. This two-threshold mechanism allows BDM to achieve a better balance between compression ratio and signal fidelity than conventional single-threshold DM, especially when the input contains both low-amplitude noise and sharp transient events. The effect θ_2 have on spike rate can be visualized via Fig. S3a $\sim$ d, where smaller θ_2 generates more events compared to large θ_2.

The observation made in Supplementary Note S3. can also be made for BDM. Fig. S4 sees a similar trend in Fig. S2 where there is an optimal point where data compression is maximized while BIC is minimized.

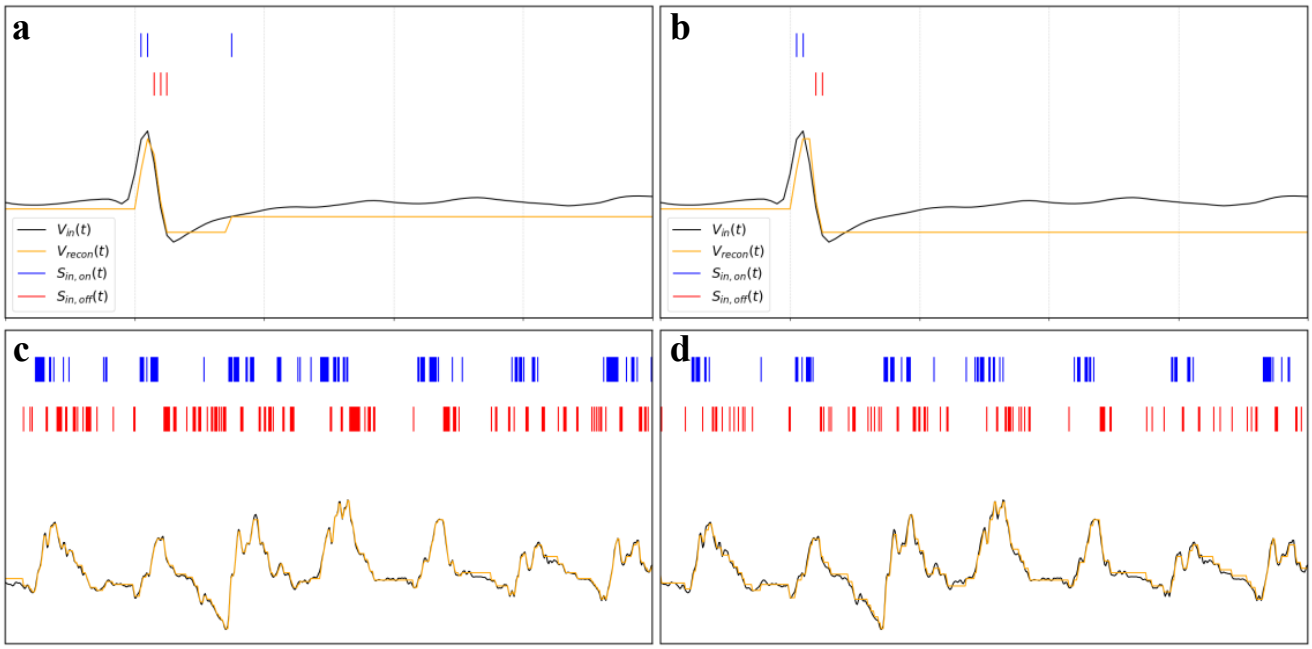

Figure S3. Burst Delta Modulation.$S(t)$ generated by Burst Delta Modulation under different k_2 for the intracortical dataset (**a** **b**) and iEEG dataset (**c** **d**), along with the corresponding reconstructed signal. **a** $k_2 = 0.2$. **b** $k_2 = 0.4$. **c** $k = 0.2$. **d** $k = 0.4$.

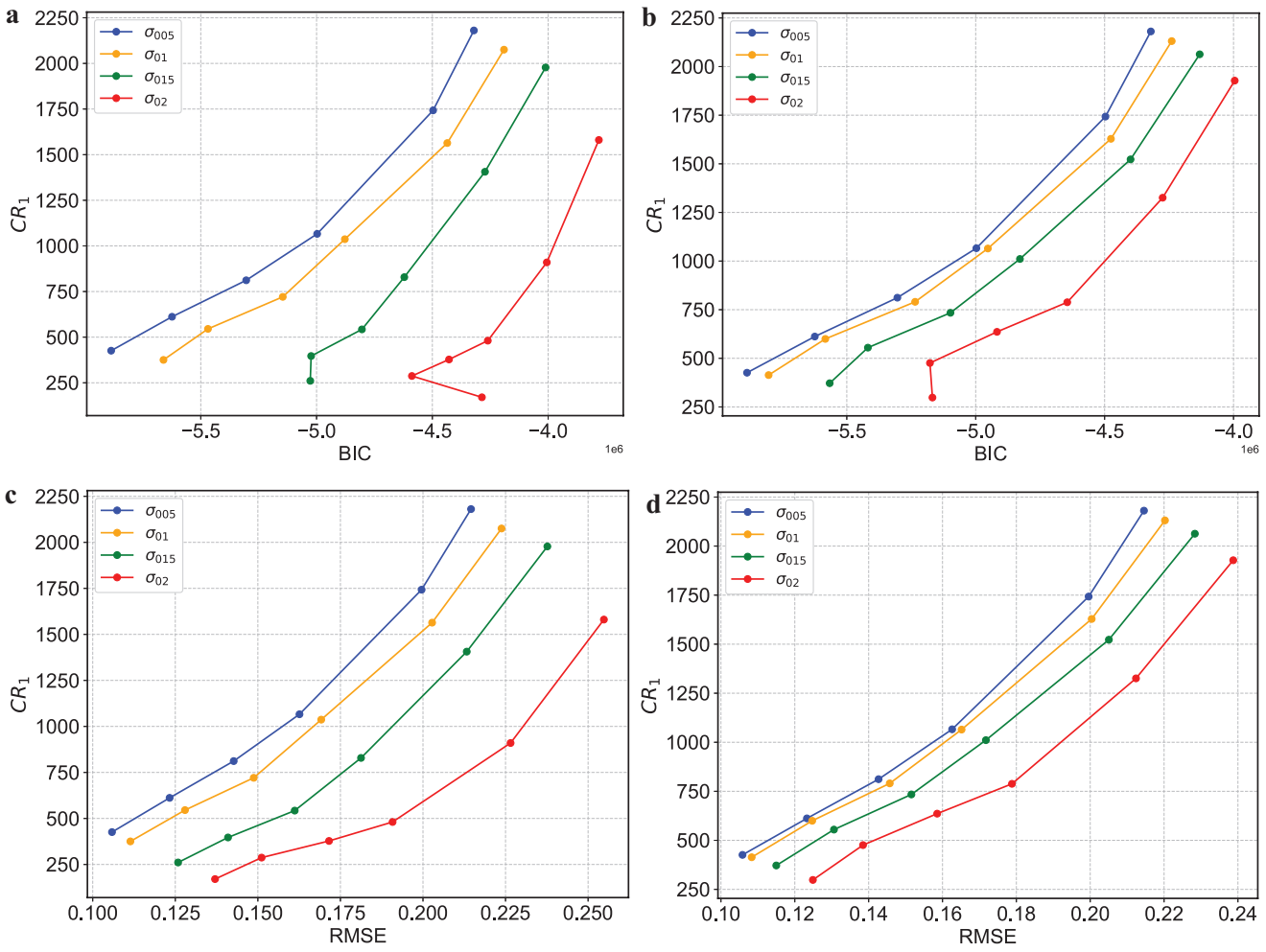

Figure S4. Analysis of how k_2 can effect data compression and loss of information using **Burst Delta Modulation** as the ASC encoder. From the four plots, it can be observed there exists a k_2 where data compression can be optimized where data loss is minimized. **a** BIC vs CR for intracortical dataset. **b** BIC vs CR for pink noise intracortical dataset. **c** RMSE vs CR for intracortical dataset. **d** RMSE vs CR for pink noise intracortical dataset.

Supplementary Note S5. BDM Circuit Design

The burst-delta modulation integrated circuit consists of a two-stage neural frontend circuit, a delta modulator and a BDM threshold control circuit. The circuit schematic and layout are presented in Fig. S5 and transistor sizes are shown in Table S1. The metadata of BDM hardware compression ratio and RMSE are provided in Table S2.

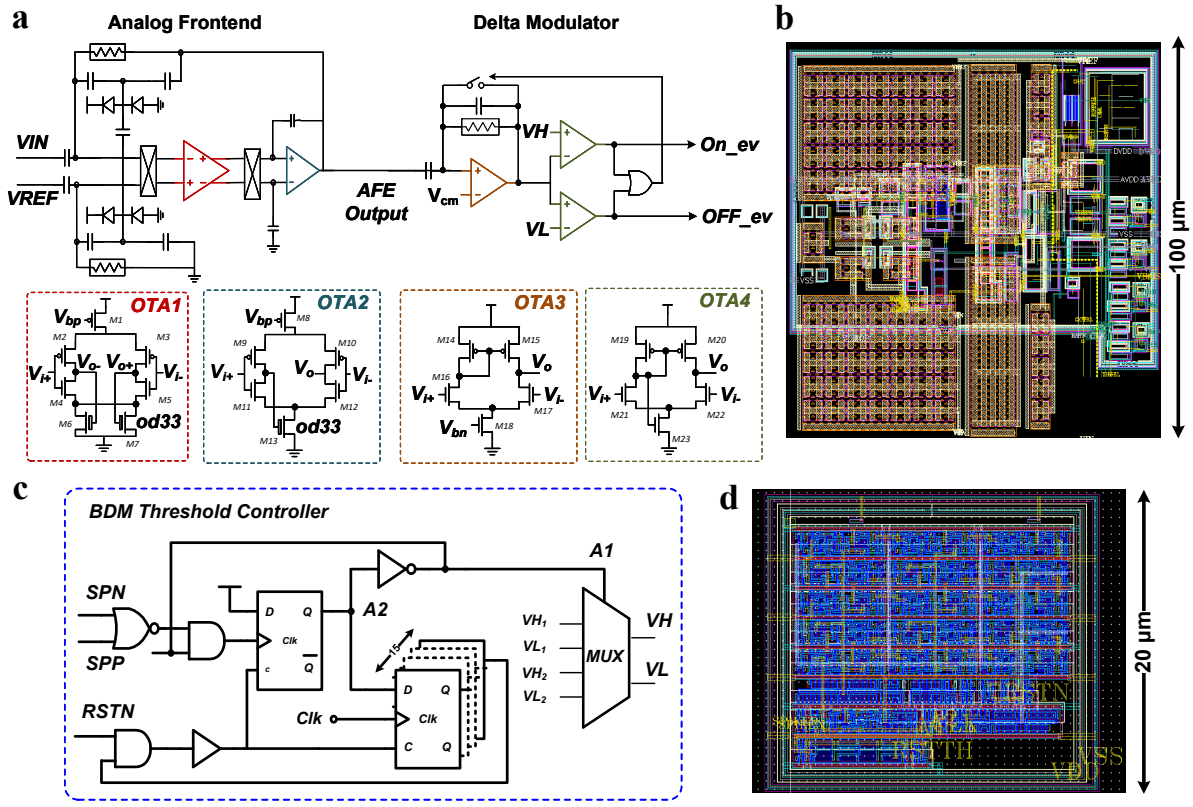

Figure S5. Burst Delta Modulation Integrated Circuit Design. **a** Neural analog frontend and delta modulator circuit schematic. **b** Circuit layout of the AFE and delta modulator. **c** Burst delta modulation threshold controller circuit schematic. **d** BDM control logic layout.

Table S1. Sizing of transistors

Transistor	Size W/L (in μm)
M1-M5	2/2
M6-M7	2.5/5
M8-M13	2/2
M14-M15	1/4
M16-M17	2/1
M18	1/4
M19-M20	0.2/5
M21-M22	0.5/0.06
M23	0.5/5

Supplementary Note S6. SNN Architecture

The SNN model used in this work takes inspiration from Hwang et al[5], where the model expects an input of N time steps, with a single hidden layer and an output layer of 2 neurons. For our experiments, we set $N = 24$, with 16 LIF neurons in the hidden layer. The spiking neuron used in this model is the Leaky Integrate-and-Fire (LIF) neuron.

The SNN model operates in two modes, streaming and window mode, which is illustrated in Fig. S6. In streaming mode, the model continuously takes in N consecutive time steps for inference, and the N time steps moves forward in time by stride size S, which is set to 1 in our work. In window mode, the model extracts L consecutive time steps and breaks the window into smaller sub-window of size N. The sub-window steps through the window with a step size of S_{win}. In this work, $L = 47$, $N = 24$ and $S_{win} = 1$. The key difference between the two modes is the state of the spiking neurons. While operating in streaming mode, the spiking neurons retains past information to make predictions, while in window mode, the at the start of each inference, the

Table S2. Metadata of Hardware Measurement on Intracortical Dataset

Scheme	θ_1	θ_2	Dataset	Low-freq. interference	RMSE	CR_1
DM	0.05	0.05	σ_{005}	No	0.191278	166.714906
DM	0.05	0.05	σ_{02}	No	0.209085	109.121221
DM	0.05	0.05	σ_{005}	Yes	0.156418	129.945330
DM	0.05	0.05	σ_{02}	Yes	0.174650	95.059440
DM	0.10	0.10	σ_{005}	No	0.215028	1201.251303
DM	0.10	0.10	σ_{02}	No	0.230499	732.420633
DM	0.10	0.10	σ_{005}	Yes	0.205195	605.635777
DM	0.10	0.10	σ_{02}	Yes	0.190372	448.551552
DM	0.15	0.15	σ_{005}	No	0.241871	4611.689351
DM	0.15	0.15	σ_{02}	No	0.277057	2598.496241
DM	0.15	0.15	σ_{005}	Yes	0.195750	1535.726982
DM	0.15	0.15	σ_{02}	Yes	0.247783	1134.379308
BDM	0.20	0.10	σ_{005}	No	0.202741	7448.275862
BDM	0.20	0.10	σ_{02}	No	0.216843	6301.969365
BDM	0.20	0.10	σ_{005}	Yes	0.175032	1560.411775
BDM	0.20	0.10	σ_{02}	Yes	0.222273	1212.801797

SNN resets the membrane potential of the LIF neurons, as the model makes prediction within a given context.

For both modes, temporal voting is applied to make the final classification, where the spiking neuron that fires the most within a fixed duration determines whether AP is generated. In window mode, the duration is $L-N+1$ while in streaming mode, the during is set to a fixed 1ms interval.

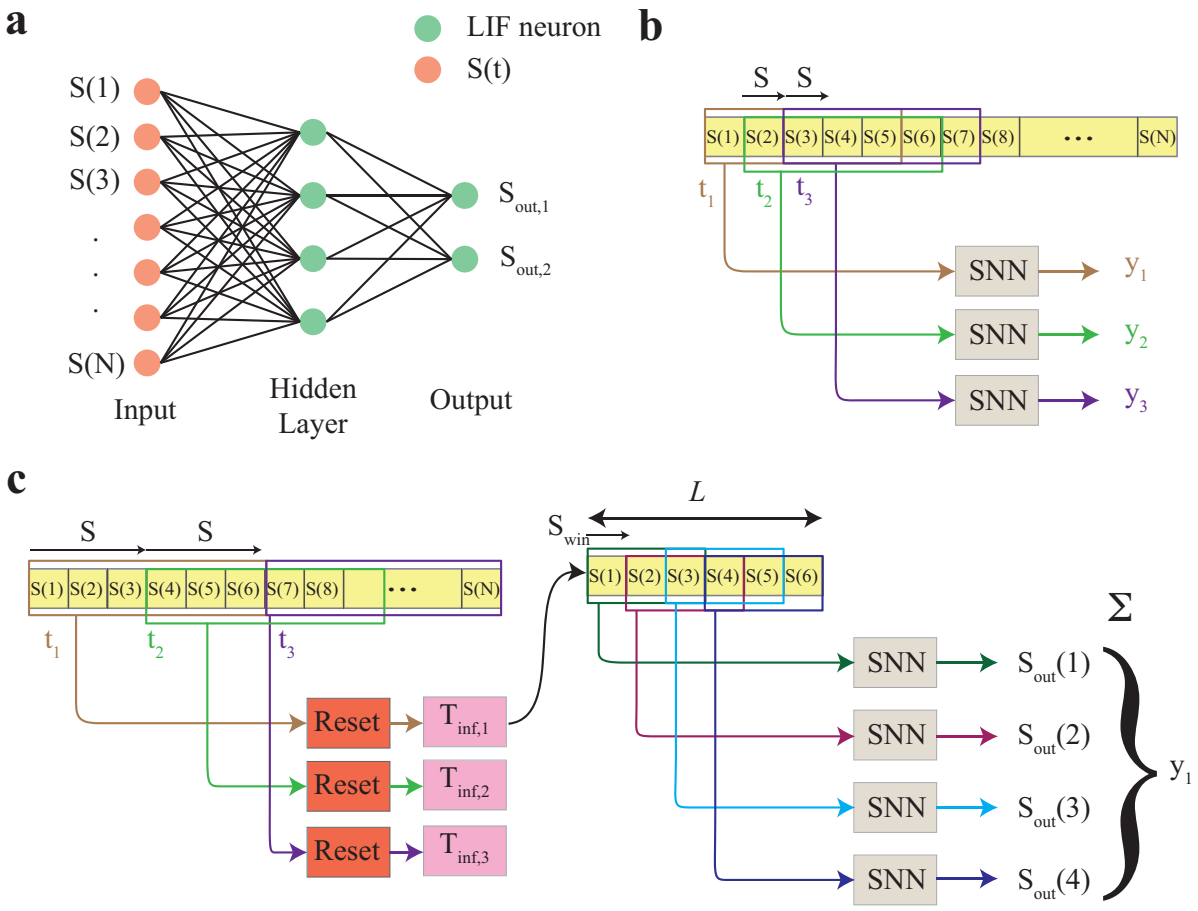

Figure S6. SNN model architecture used in this paper and the two operating modes. **a)** SNN model architecture used in this paper. The SNN model expects input of N consecutive time steps of the input spike train S(t). **b)** When the SNN is operating in streaming mode, the SNN accepts N time steps and passes it through the model, and the input spike train have a stride of size S. **c)** In window mode, the SNN model extracts a window of L consecutive time steps from the spike train $S(t)$, and resets the model's LIF neurons before each inference. During inference, the model extracts N time steps from the window, and the model steps through the window with a step size of S_{win}. During the window mode operation, the SNN model will operates for $L-N+1$ times, and the output spikes over $L-N+1$ time steps is summed and classify based on which neuron fires the most spike during that period.

Supplementary Note S7. BDM Circuit Measurement

The BDM integrated circuit is tested with the setup in Fig. S7. The chip is mounted on a custom PCB board and connected to a waveform generator and an FPGA for intracortical recording measurements.

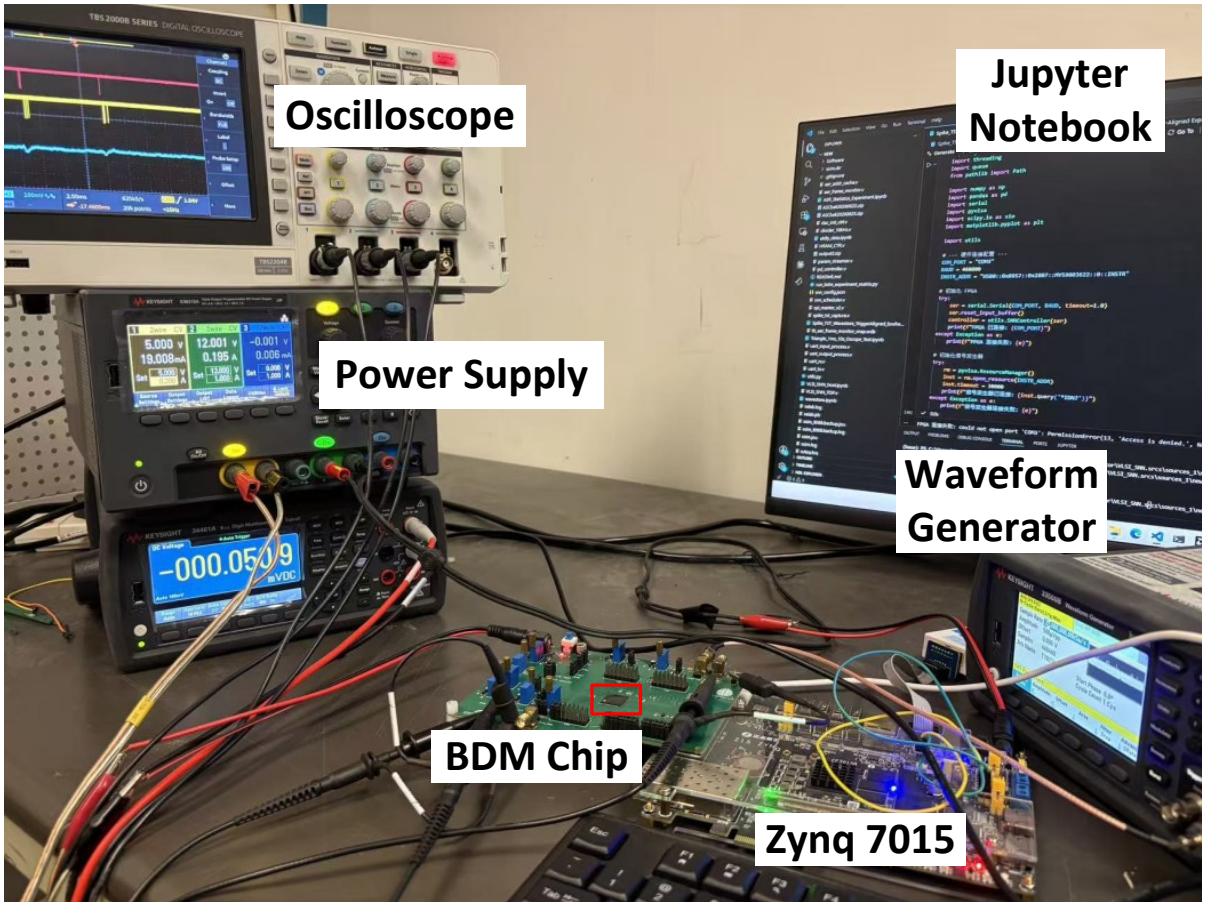

Figure S7. Burst Delta Modulation Circuit Testing Setup.

Supplementary Note S8. List of Papers Surveyed in Fig 2a

1. Yeager, D., Biederman, W., Narevsky, N., Alon, E. & Rabaey, J. A fully-integrated 10.5μw miniaturized (0.125mm2) wireless neural sensor. In *2012 Symposium on VLSI Circuits (VLSIC)*, 72–73, DOI: 10.1109/VLSIC.2012.6243795 (2012).
2. Han, D., Zheng, Y., Rajkumar, R., Dawe, G. & Je, M. A 0.45v 100-channel neural-recording ic with sub-μw/channel consumption in 0.18μm cmos. In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 290–291, DOI: 10.1109/ISSCC.2013.6487739 (2013).
3. Lopez, C. M. *et al.* An implantable 455-active-electrode 52-channel cmos neural probe. *IEEE J. Solid-State Circuits* **49**, 248–261, DOI: 10.1109/JSSC.2013.2284347 (2014).
4. Shulyzki, R. *et al.* 320-channel active probe for high-resolution neuromonitoring and responsive neurostimulation. *IEEE Transactions on Biomed. Circuits Syst.* **9**, 34–49, DOI: 10.1109/TBCAS.2014.2312552 (2015).
5. Corradi, F. & Indiveri, G. A neuromorphic event-based neural recording system for smart brain-machine-interfaces. *IEEE Transactions on Biomed. Circuits Syst.* **9**, 699–709, DOI: 10.1109/TBCAS.2015.2479256 (2015).
6. Mora Lopez, C. *et al.* A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13 μm soi cmos. *IEEE Transactions on Biomed. Circuits Syst.* **11**, 510–522, DOI: 10.1109/TBCAS.2016.2646901 (2017).
7. Bagheri, A., Salam, M. T., Perez Velazquez, J. L. & Genov, R. Low-frequency noise and offset rejection in dc-coupled neural amplifiers: A review and digitally-assisted design tutorial. *IEEE Transactions on Biomed. Circuits Syst.* **11**, 161–176, DOI: 10.1109/TBCAS.2016.2539518 (2017).
8. Tu, C.-C., Wang, Y.-K. & Lin, T.-H. A low-noise area-efficient chopped vco-based ctdsm for sensor applications in 40-nm cmos. *IEEE J. Solid-State Circuits* **52**, 2523–2532, DOI: 10.1109/JSSC.2017.2724025 (2017).
9. Gagnon-Turcotte, G., Khiarak, M. N., Ethier, C., De Koninck, Y. & Gosselin, B. A 0.13- μm cmos soc for simultaneous multichannel optogenetics and neural recording. *IEEE J. Solid-State Circuits* **53**, 3087–3100, DOI: 10.1109/JSSC.2018.2865474 (2018).

10. De Dorigo, D. *et al.* Fully immersible subcortical neural probes with modular architecture and a delta-sigma adc integrated under each electrode for parallel readout of 144 recording sites. *IEEE J. Solid-State Circuits* **53**, 3111–3125, DOI: 10.1109/JSSC.2018.2873180 (2018).

11. Chandrakumar, H. & Marković, D. A 15.2-enob 5-khz bw 4.5- μ w chopped ct $\delta\sigma$ -adc for artifact-tolerant neural recording front ends. *IEEE J. Solid-State Circuits* **53**, 3470–3483, DOI: 10.1109/JSSC.2018.2876468 (2018).

12. Park, S.-Y., Cho, J., Na, K. & Yoon, E. Modular 128-channel δ - $\delta\sigma$ analog front-end architecture using spectrum equalization scheme for 1024-channel 3-d neural recording microsystems. *IEEE J. Solid-State Circuits* **53**, 501–514, DOI: 10.1109/JSSC.2017.2764053 (2018).

13. Kim, C. *et al.* Sub- μ vrms-noise sub- μ w/channel adc-direct neural recording with 200-mv/ms transient recovery through predictive digital autoranging. *IEEE J. Solid-State Circuits* **53**, 3101–3110, DOI: 10.1109/JSSC.2018.2870555 (2018).

14. Wang, S. *et al.* A compact quad-shank cmos neural probe with 5,120 addressable recording sites and 384 fully differential parallel channels. *IEEE Transactions on Biomed. Circuits Syst.* **13**, 1625–1634, DOI: 10.1109/TBCAS.2019.2942450 (2019).

15. Nikas, A., Jambunathan, S., Klein, L., Voelker, M. & Ortmanns, M. A continuous-time delta-sigma modulator using a modified instrumentation amplifier and current reuse dac for neural recording. *IEEE J. Solid-State Circuits* **54**, 2879–2891, DOI: 10.1109/JSSC.2019.2931811 (2019).

16. Wang, J. *et al.* 1024-electrode hybrid voltage/current-clamp neural interface system-on-chip with dynamic incremental-sar acquisition. In *2020 IEEE Symposium on VLSI Circuits*, 1–2, DOI: 10.1109/VLSICircuits18222.2020.9162837 (2020).

17. Yoon, D.-Y. *et al.* A 1024-channel simultaneous recording neural soc with stimulation and real-time spike detection. In *2021 Symposium on VLSI Circuits*, 1–2, DOI: 10.23919/VLSICircuits52068.2021.9492480 (2021).

18. Jung, Y. *et al.* A wide-dynamic-range neural-recording ic with automatic-gain-controlled afe and ct dynamic-zoom adc for saturation-free closed-loop neural interfaces. *IEEE J. Solid-State Circuits* **57**, 3071–3082, DOI: 10.1109/JSSC.2022.3188626 (2022).

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20. Yang, X. *et al.* An ac-coupled 1st-order - readout ic for area-efficient neural signal acquisition. *IEEE J. Solid-State Circuits* **58**, 949–960, DOI: 10.1109/JSSC.2023.3234612 (2023).

21. Cartiglia, M. *et al.* A 4096 channel event-based multielectrode array with asynchronous outputs compatible with neuromorphic processors. *Nat. Commun.* **15**, 7163 (2024).

22. Wendler, D. *et al.* A 0.0046-mm2 two-step incremental delta–sigma analog-to-digital converter neuronal recording front end with 120-mvpp offset compensation. *IEEE J. Solid-State Circuits* **58**, 439–450, DOI: 10.1109/JSSC.2022.3190446 (2023).

23. Wu, H. *et al.* An energy-efficient small-area configurable analog front-end interface for diverse biosignals recording. *IEEE Transactions on Biomed. Circuits Syst.* **17**, 818–830, DOI: 10.1109/TBCAS.2023.3293492 (2023).

24. Shaeri, M. *et al.* A 2.46-mm2 miniaturized brain-machine interface (mibmi) enabling 31-class brain-to-text decoding. *IEEE J. Solid-State Circuits* **59**, 3566–3579, DOI: 10.1109/JSSC.2024.3443254 (2024).

25. Wu, J. *et al.* A low-noise low-power 0.001hz–1khz neural recording system-on-chip with sample-level duty-cycling. *IEEE Transactions on Biomed. Circuits Syst.* **18**, 263–273, DOI: 10.1109/TBCAS.2024.3368068 (2024).

26. Jang, M. *et al.* A 1024-channel 268-nw/pixel 36×36 μm2/channel data-compressive neural recording ic for high-bandwidth brain–computer interfaces. *IEEE J. Solid-State Circuits* **59**, 1123–1136, DOI: 10.1109/JSSC.2023.3344798 (2024).

27. Dorigo, D. D. *et al.* A 0.00175 mm2/channel direct-digitization frontend with automatic edo/drift compensation for floating subcortical neural probes. In *2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*, 416–419, DOI: 10.1109/ESSERC62670.2024.10719430 (2024).

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