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A Fault Current Limiter Coordinated with a Hybrid DC Circuit Breaker for HVDC Applications

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Abstract

This paper presents proposed Fault Current Limiter (FCL) aims to reduce the transient overvoltage stress on the IGBT used in its circuit and enhance the protection performance by limiting the fault current and reducing the stress on the DC circuit breaker during fault condition. In addition, a control system is proposed to coordinate the operation of the FCL and the hybrid DCCB. The proposed system is modeled and simulated using MATLAB/Simulink. The results demonstrate that the proposed FCL significantly reduces the transient overvoltage across its IGBT by 86.96%, while maintaining the same level of reduction in the fault current magnitude. The results also show that the proposed control system effectively detects and isolates faults occurring at different time instants. Overall, the proposed approach provides a reliable and effective solution for enhancing the protection performance of HVDC interconnection networks, making it suitable for practical applications. The paper investigated the integration of the proposed FCL with hybrid DC circuit breaker in the interconnection ± 500 kV DC line. The main advantages of the proposed FCL is to decrease the transient over voltage on power electronic switches during the switching operation at the fault initiation, it is characterized by a simple structure and low implementation cost and its operation does not rely on charging and discharging capacitors, which increases its lifespan.

Keywords: HVDC, Fault Current Limiter (FCL), Hybrid DC Circuit Breaker (DCCB), Transient Overvoltage, IGBT, Control System.

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1. Introduction

Energy plays a crucial role in shaping modern society. However, reliance on fossil fuels and other non-renewable energy sources has led to environmental pollution, power supply instability and climate change. In response to these challenges, recent advancements in renewable energy technologies, along with the inherent technical advantages of direct current (DC) systems over AC systems [1], have significantly increased the adoption of DC power technology in transmission networks. DC transmission provides multiple technical advantages especially when transmitting electrical power over long distances [2, 3]. A key challenge in the protection of DC systems arises from the absence of a natural current zero crossing, making fault interruption significantly more complex compared to AC systems [4]. The lack of a natural current zero crossing results in the interruption of high fault currents, which represents a major challenge for fault interruption and circuit breaker operation. To isolate a fault in DC systems, several protection techniques can be employed, including fuses, system de-energization, and DC circuit breakers [5].

DC circuit breakers are generally classified into mechanical, solid state, and hybrid types. Mechanical DC circuit breakers offer low conduction losses but suffer from slow operating speeds and severe arcing phenomena during fault interruption [6-10]. Solid state DC circuit breakers provide ultra-fast current interruption at the expense of higher conduction losses [11-13]. Due to the increased current in DC networks during faults, which causes network components to break down and voltages to increase on the contacts of the circuit breakers if protection systems fail to operate, it is necessary to use a fault current limiter. Multiple current limiters are used in FCLs design. Such these are superconducting FCLs, Solid-State FCLs, Bridge-Type FCLs, Resonant FCLs, Inductive FCLs and Hybrid FCLs.

The ideal performance criteria for FCLs in HVDC networks include minimal impedance during normal operation, a rapid transition to high impedance under fault conditions, fast and automatic recovery, suitability for high DC voltage applications, and cost effectiveness [14]. The superconducting SFCL is one of the techniques employed to limit the magnitude of fault current in power systems [15]. Superconducting and air core SFCLs are capable of responding naturally and extremely rapidly to restrain the rise of fault currents, thereby reducing DC fault levels to more manageable values [16-19]. Superconducting fault current limiters can be divided into resistive and inductive types [16-18]. In 2019, a fault current limiting circuit was proposed, utilizing multiple inductors connected in parallel under normal operating conditions and reconfigured into a series configuration during the fault current limiting mode [20].

In 2025, a new fault current limiting circuit was introduced, relying on a number of inductors together with a fixed-value resistor [21]. This circuit was compared with the circuits reported in [22] and [23], and its effectiveness in reducing fault current magnitudes as well as alleviating the stress on the hybrid circuit breaker was clearly demonstrated.

The present paper proposed FCL aims to reduce the transient overvoltage stress on the IGBT used in its circuit and enhance the protection performance by limiting the fault current and reducing the stress on the DC circuit breaker during fault condition. In addition, a control system is proposed to coordinate the operation of the FCL and the hybrid DCCB. The article is organized as following: Section 2, details about Hybrid DC circuit breaker is presented. In Section 3, the proposed FCL circuit, operating principle is explained. Design of the control system of the proposed FCL is given in Section 4. Simulated Results of

the FCL with Hybrid DCCB in HVDC system is given in section 5. Parameters affecting the FCL operation are presented in section 6. Finally, the conclusions of the present work are illustrated in section 7.

2. Hybrid DC circuit breaker

Hybrid DC circuit breaker represents a combination of mechanical and solid-state circuit breaker technologies. Through the integration of solid-state and mechanical switching paths, the hybrid DC circuit breaker achieves fast fault isolation while ensuring low-loss conduction under normal conditions [24-26]. In ABB's hybrid DCCB design, the current normally flows through a mechanical switch called the ultra-fast disconnector (UFD) and a power electronic switch called the load commutation switch (LCS) as shown in Fig.1 [27-29]. This path has very low losses.

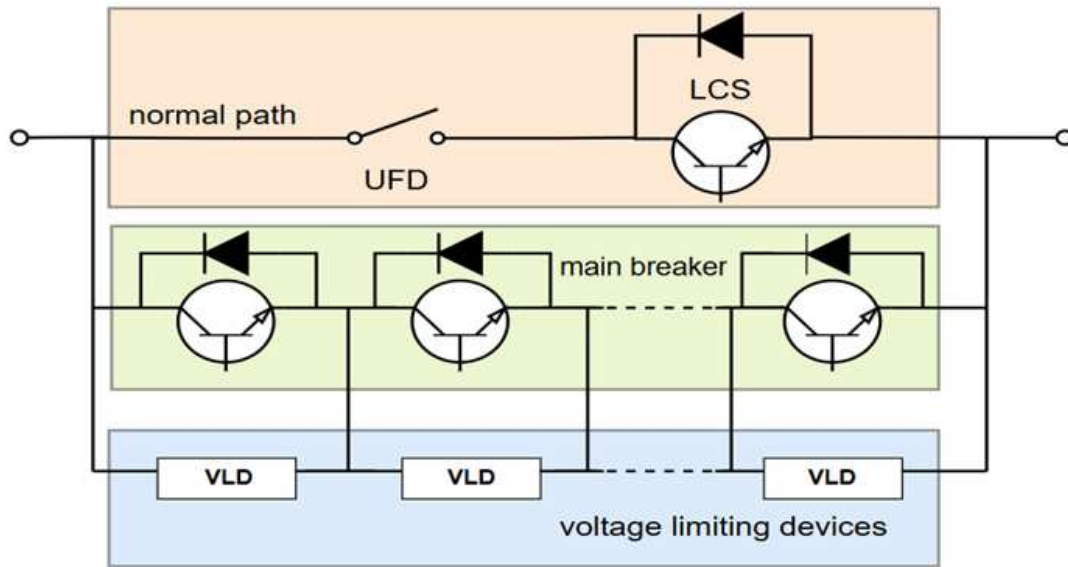


Figure 1: Hybrid DCCB

In parallel with this normal path, there is a main breaker branch made from many series connected IGBTs with anti-parallel diodes. Another parallel branch contains a voltage-limiting devices, typically a metal oxide varistor (MOV), is used to clamp over-voltages. Due to the high stress experienced by the hybrid DC circuit breaker during operation, resulting from the absence of a natural current zero-crossing in direct current systems, additional circuits have been implemented to limit the fault current magnitude before the opening of the hybrid circuit breaker for network isolation. These circuits are commonly referred to as Fault Current Limiters (FCLs).

3. The Power Circuit of the Proposed Fault Current Limiter

3.1. Network Description

Fig. 2 shows the power circuit of the proposed FCL. It consists of two inductors ($L1$ and $L2$), a resistor (R_d), and power electronic devices, including an IGBT ($T1$) and two diodes ($D1$ and $D2$). The inductors $L1$ and $L2$ are used to reduce the rate of rise of the fault current at the instant of fault occurrence [30, 31]. Due to their inherent property of opposing rapid changes in current, inductors restrict the instantaneous

increase of current when a fault occurs. As a result, the fault current does not rise abruptly, which provides sufficient time for the protection system and the fault current limiter to operate effectively. The resistor (R_d) acts as a damping element that limits the fault current magnitude, in addition it is used to dissipate the energy stored in the inductors ($L1$ and $L2$) after the complete isolation of the DC system. The IGBT ($T1$) operates as an on/off switch. Under normal operating conditions, it remains in the ON state, while under fault conditions; it transitions to the OFF state to redirect the fault current into the damping resistance path. The anti-parallel diode ($D1$) provides a path for reverse current when the IGBT is turned OFF, thereby preventing reverse current conduction through the IGBT and protecting it from excessive voltage stress. The diode ($D2$) provides a path for dissipating the energy stored in the inductors ($L1$ and $L2$) after the complete isolation of the DC system.

The proposed FCL circuit has been provided by highlighting the improvement achieved in reducing the voltage stress across the IGBT in the FCL circuit. One advantage of the proposed FCL is eliminating the potential failure of its electronic components, such as IGBT ($T1$). The peak voltage across $T1$, for example, is reduced from 3.5919 MV in some previously reported designs [21] to 0.4682 MV in the proposed FCL design.

3.2. Operating principle of the proposed FCL

3.2.1. Operation under normal conditions

Under normal operating condition of the network, the line current flows through the $L1$, $L2$, $T1$, and HDCCB path as shown in fig. 2. In this case the magnitude of the line current is calculated by equation (1). In this equation V_{DC} is the terminal voltage, R_{Line} is the line resistance, and R_L is the load resistance.

$$I_{Line} = \frac{V_{DC}}{R_{Line} + R_L} \quad (1)$$

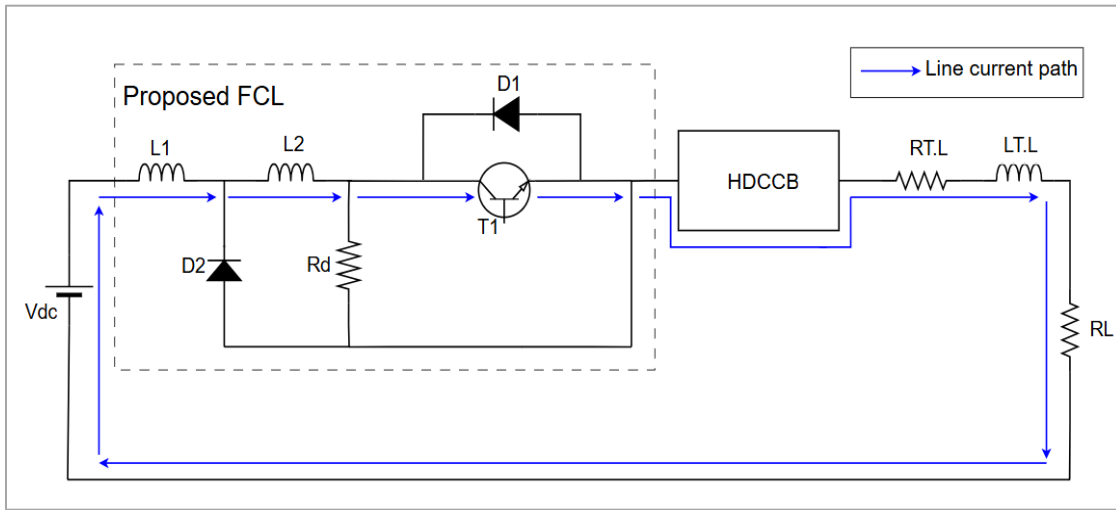


Figure 2: proposed circuit of the FCL

3.2.2. At the instant of fault occurrence

The fault current flows from the DC source (converter station), travels through the line resistance to the fault location, ionizes the air to create an arc, and completes its circuit via the earth or return path. In

this part of study, the fault resistance is ignored to investigate the worst case, the impact of the fault resistance on the FCL performance is investigated in section 6. At the instant of fault occurrence, the effect of the current rate of change in inductors L_1 , L_2 , the line inductance L_{Line} and the line resistance R_{Line} are considered, as given in time-domain expression of the fault current illustrated in equation (2). In this equation L_{eq} represents the summation of L_1 , L_2 , and L_{Line} .

$$i_f(t) = \frac{V_{DC}}{R_{Line}} * \left(1 - e^{-\frac{R_{Line}t}{L_{eq}}}\right) + I_{Line} * e^{-\frac{R_{Line}t}{L_{eq}}} \quad (2)$$

3.2.3. Fault current limiting stage

At fault current limiting stage, the controller system for the FCL opening the IGBT (T1), conducting the fault current along the L1, L2, Rd, and HDCCB path as shown in Fig. 3. The time domain expression of the fault current in this stage considering the damping resistance is as illustrated in equation (3).

$$i_{fwith FCL}(t) = \frac{V_{DC}}{R_{Line}+R_d} * \left(1 - e^{-\frac{(R_{Line}+R_d)t}{L_{eq}}}\right) + I_{Line} * e^{-\frac{(R_{Line}+R_d)t}{L_{eq}}} \quad (3)$$

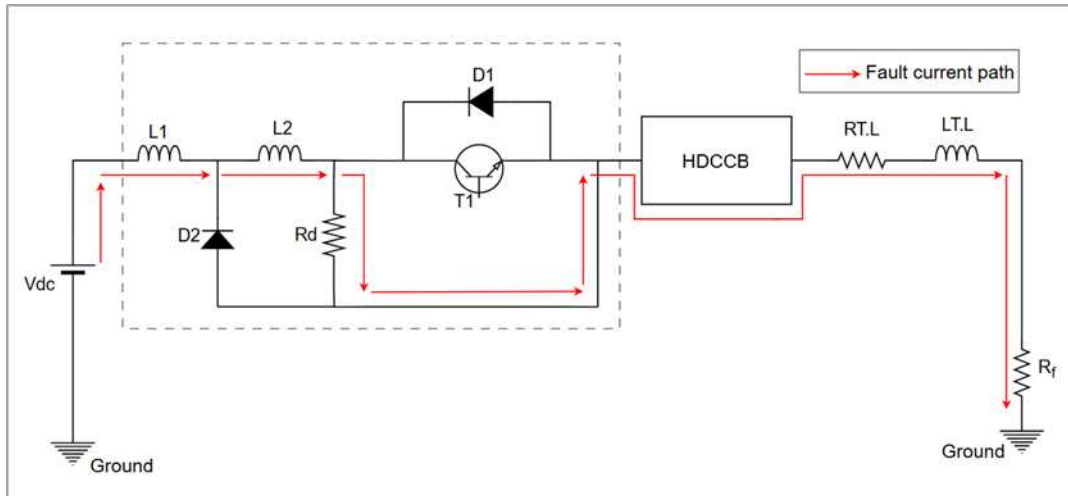


Figure 3: The line current path after activation of the proposed FCL circuit

One advantage of the proposed FCL is the eliminating the potential collapse of its electronic elements such as IGBT (T1). The peak value of the voltage across T1 as example is reduced from 3.5919 MV in some designs [21] to 0.4682 MV in the present FCL design. The clipping ratio (CR) can be calculated by the relation

$$\text{The clipping ratio (CR)} = \frac{\text{peak value } i_{fwith FCL}(t)}{\text{peak value } i_f(t)} \quad (4)$$

4. Design of the Control System of the Proposed FCL

The design of the control system for fault detection and the subsequent generation of control signals for both the FCL circuit and the hybrid circuit breaker are initiated by comparing the line current magnitude with a predefined constant threshold. This constant value is referred to as the critical current value. In selecting this current, the worst case scenario of a transient current increase must be taken into consideration, in which the line current experiences a temporary rise before returning to its nominal value. The worst case scenario is referred to the starting condition. The operating principle of the proposed control system can be represented in the form of a flowchart, as illustrated in Fig. 4. In Fig. 4, t_1 denotes the operating time of the hybrid DCCB, after which complete fault isolation is achieved, t_2 denotes the instant at which the Load Commutation Switch (LCS) is opened to facilitate the opening of the Mechanical Switch (MS) under zero-current conditions, and t_3 denotes the instant at which the Mechanical Switch (MS) is opened. The proposed control system is designed to issue coordinated control signals to both the fault current limiter (FCL) circuit and the hybrid circuit breaker.

4.1. First Stage of the Proposed Control System Design

The first stage in designing the proposed control system involves generating the control signal for the IGBT (T1) employed in the fault current limiter (FCL) circuit. The key characteristic of the FCL circuit is its ability to reduce the fault current to values lower than the rated current.

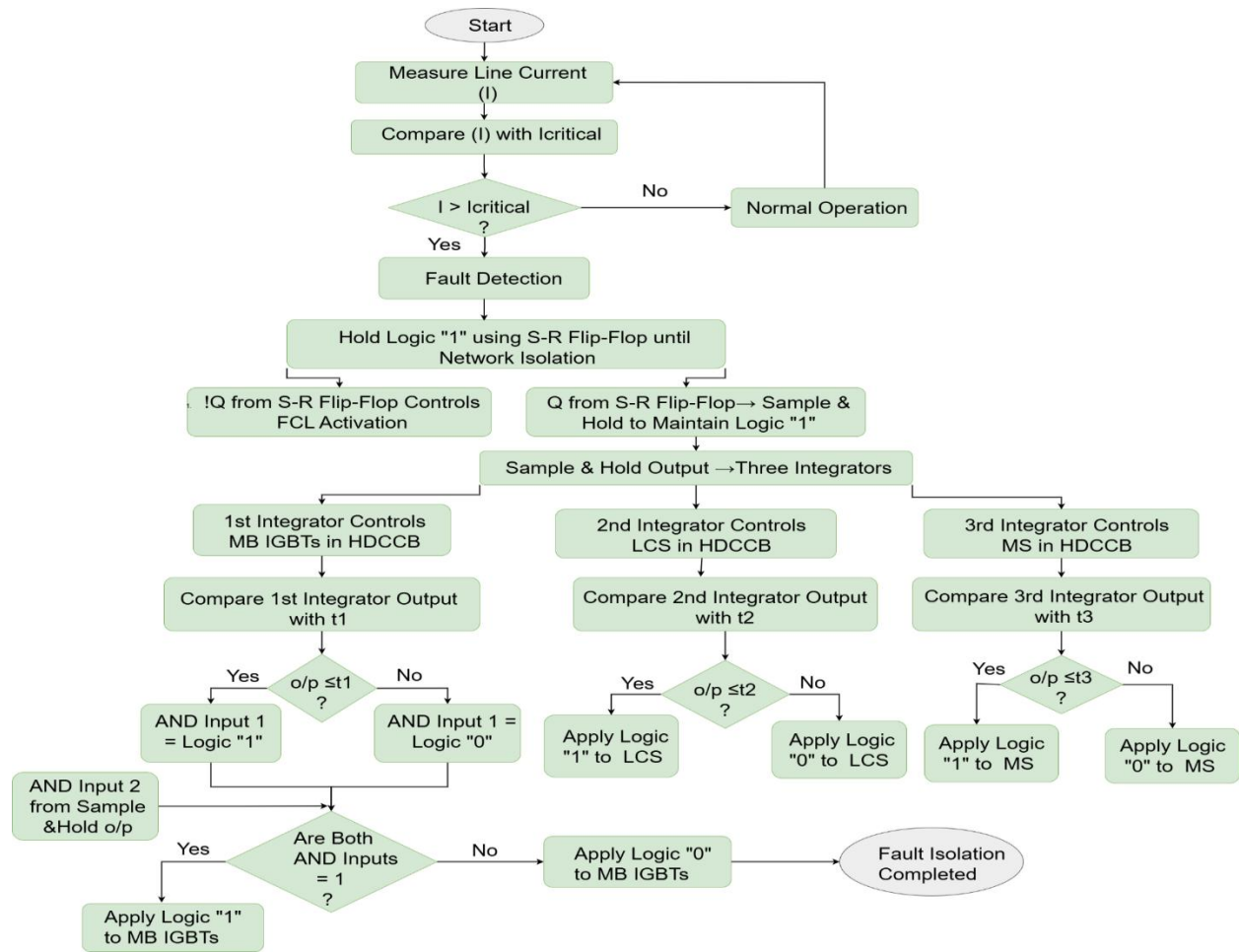


Figure 4: Flowchart illustrates the operating principle of the proposed control system

Consequently, if a single comparator is used to compare the line current with a fixed threshold value, the activation of the FCL will cause the line current to drop below the rated value. As a result, the comparator may falsely interpret this condition as fault clearance, thereby preventing the generation of a tripping signal for the hybrid circuit breaker.

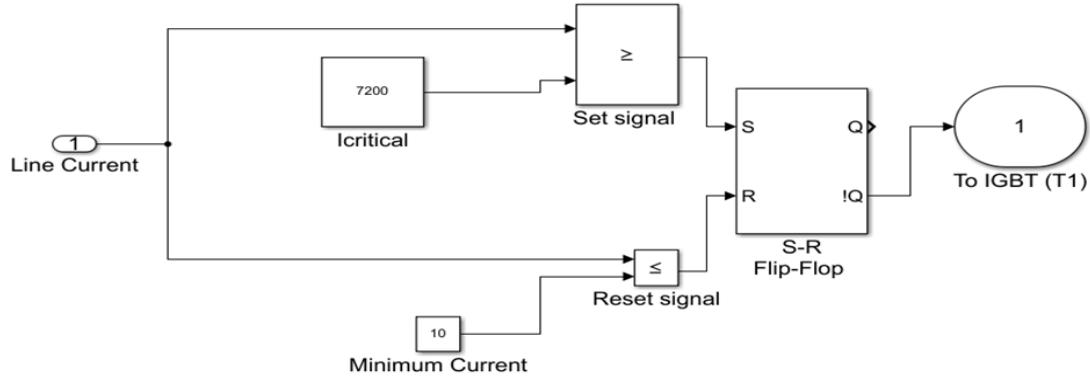


Figure 5: Controller Design for the IGBT (T1) in the FCL Circuit

To overcome this limitation, two current comparators are used in the proposed control scheme, as shown in Fig. 5. The proposed control signal for the IGBT (T1) is designed and implemented using the MATLAB/Simulink environment. In Fig. 5, an SR flip-flop block is employed [32]. This block operates in a manner similar to an alarm latch; once the SET input is activated, the output remains at a logic high state until the RESET input is triggered.

Table 1: Operating States of the SR Flip-Flop in the HVDC Fault Detection System with FCL.

State	Line current	S (Set)	R (Reset)	Q (Fault)	Description
1	≈ 3000 A	0	0	0	Normal operation– no fault
2	> 7200 A	1	0	1	Fault occurrence – fault is latched (Set)
3	< 3000 A and > 10 A	0	0	1	Fault current limited by FCL – fault remains latched
4	≤ 10 A	0	1	0	Circuit isolation – fault is cleared (Reset)

In the fault detection circuit, the SR flip-flop operates as follows: when a logic high signal is applied to the SET input, which indicates that the line current has exceeded the critical current value, the output Q is latched at a logic high state, representing that the fault condition is still present. This latched state is maintained even if the line current decreases due to the activation of the FCL circuit.

The output Q is only reset to a logic low state when a logic high signal is applied to the RESET input. It can be observed from Table (1) that the output Q is equal to zero under normal operating conditions and becomes equal to one when a fault occurs. However, this behavior is opposite to the required switching logic of the IGBT (T1), which must be turned off during fault conditions. To ensure that the IGBT (T1) operates during normal conditions and turns off under fault conditions, the complementary

output Q^- of the SR flip-flop is connected to the gate input of the IGBT (T1). The resulting Q^- output waveform is shown in Fig. 6. Before the fault occurrence, the output Q^- remains at a logic high level, indicating that the IGBT (T1) is in the ON state. After the fault occurs, and until complete network isolation is achieved using the hybrid circuit breaker, the output Q^- switches to a logic low level, which corresponds to turning off the IGBT (T1). The fault is assumed to occur at the third second from the start of the simulation.

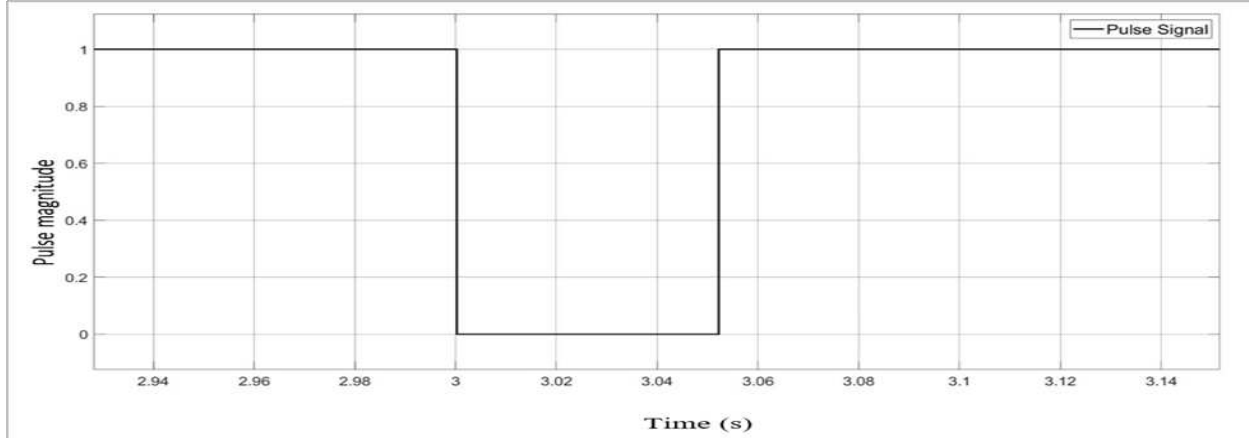


Figure 6: The control signal applied to the IGBT (T1).

4.2. Second Stage of the Proposed Control System Design

The second stage of the proposed control system design involves developing a controller for the hybrid circuit breaker and coordinating this controller with the previously designed controller responsible for controlling the IGBT (T1) in the FCL circuit.

Fig.7 illustrates the internal structure of the proposed control system after the integration of the two controller systems. It can be observed from this figure that the controller system designed for operating the hybrid circuit breaker is based on the use of a Sample-and-Hold block in combination with an Integrator blocks. The Sample-and-Hold block is used to latch the output signal at a logic high level. The control system designed for the hybrid circuit breaker is divided into three control signals. The first control signal is responsible for activating the IGBTs in the main breaker branch, the second control signal responsible for controlling the LCS, and the third control signal is responsible for controlling the mechanical switch. The circuit used to generate the first control signal relies on an AND gate [33] to activate the main breaker branch from the instant a fault occurs until the expected time required to achieve complete network isolation. It is assumed that the hybrid circuit breaker requires 50 ms from the instant of fault occurrence to achieve complete isolation of the network. Accordingly, the constant block is set to a value of 0.05 s. In this stage, the integrator receives a unit input signal from the Sample and Hold block and operates as a timer, where its output increases from zero according to Eq. (5). Table (2) illustrates the operating principle of the AND gate. In this table, it is assumed that the fault occurs at the third second in order to clarify the operating principle of the AND gate. It can be concluded from Table (2) that the output of the AND gate is equal to zero before the occurrence of the fault, and becomes equal to one from the instant of fault occurrence until the time specified in the Constant block. After that, the output returns to zero again, as illustrated in Figure 8.

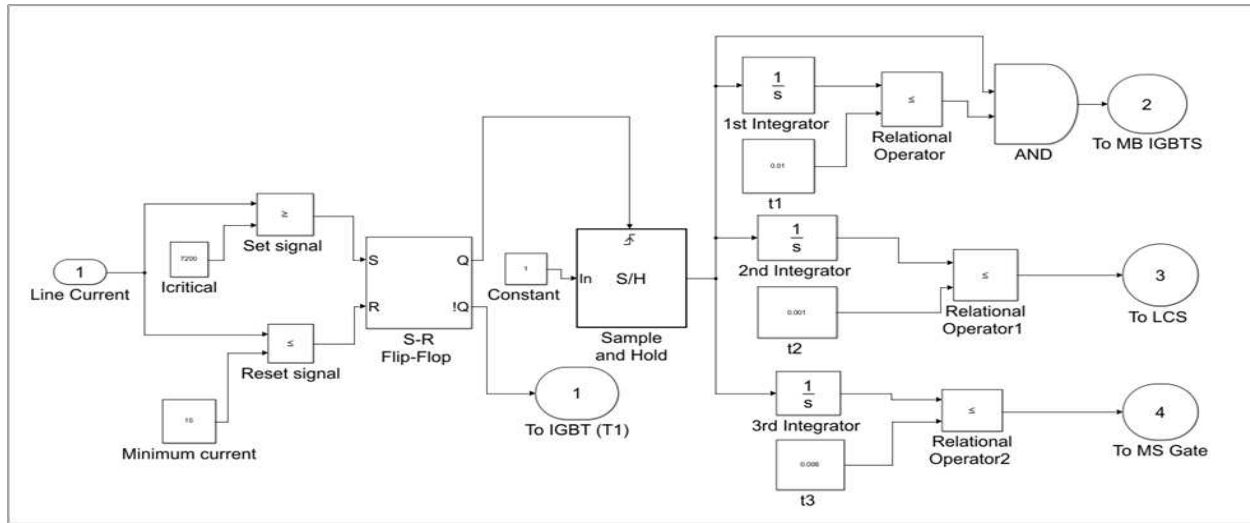


Figure 7: The internal structure of the proposed control system

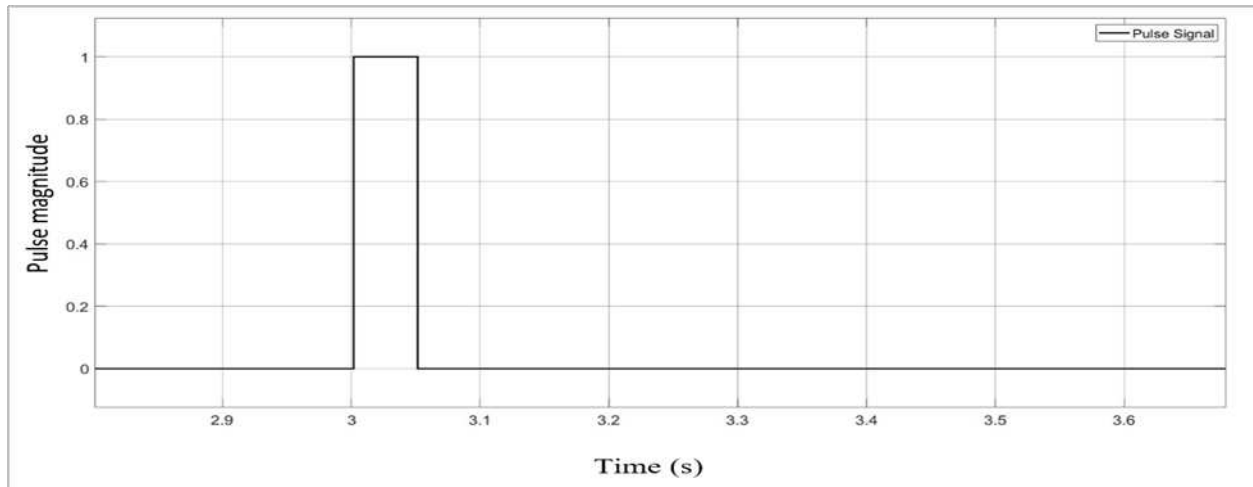


Figure 8: The control signal output from AND gate.

Table 2: Logic Operation of the AND Gate in the circuit used to generate the first control signal.

Time (s)	The first input of AND gate	Output of the integrator	Constant block	The second input of AND gate	The o/p of AND gate
0	0	0	0.05	1	0
1	0	0	0.05	1	0
2	0	0	0.05	1	0
3	1	0	0.05	1	1
3.01	1	0.01	0.05	1	1
3.02	1	0.02	0.05	1	1
3.03	1	0.03	0.05	1	1
3.04	1	0.04	0.05	1	1
3.05	1	0.05	0.05	1	1
3.06	1	0.06	0.05	0	0

In the circuit used to generate the second control signal, the integrator is utilized as a timer that starts counting from the instant of fault occurrence. The output of the integrator can be represented by Eq. (5). When the input to the integrator is zero, the output remains zero. However, when the input is equal to one, the integrator output start counting with zero and increases with time.

$$T = \int U(t)dt \quad (5)$$

As seen in Eq. (5), T represents the output of the integrator, and $U(t)$ represents the input to the integrator.

When the integrator output exceeds the value set in the Constant block, the output of the relational operator becomes equal to zero. Accordingly, the value of the Constant block represents the time after which the load commutation switch (LCS) is opened to isolate the main current path. The operating principle of the circuit used to generate the third control signal is based on the same concept adopted for the circuit used to generate the second control signal. The only difference lies in the value of the constant block used in this circuit, which is selected to be greater than that used in the circuit designed for generating the second control signal. This ensures that the mechanical switch is opened under zero current conditions, thereby avoiding the high arcing phenomenon associated with mechanical switch operation.

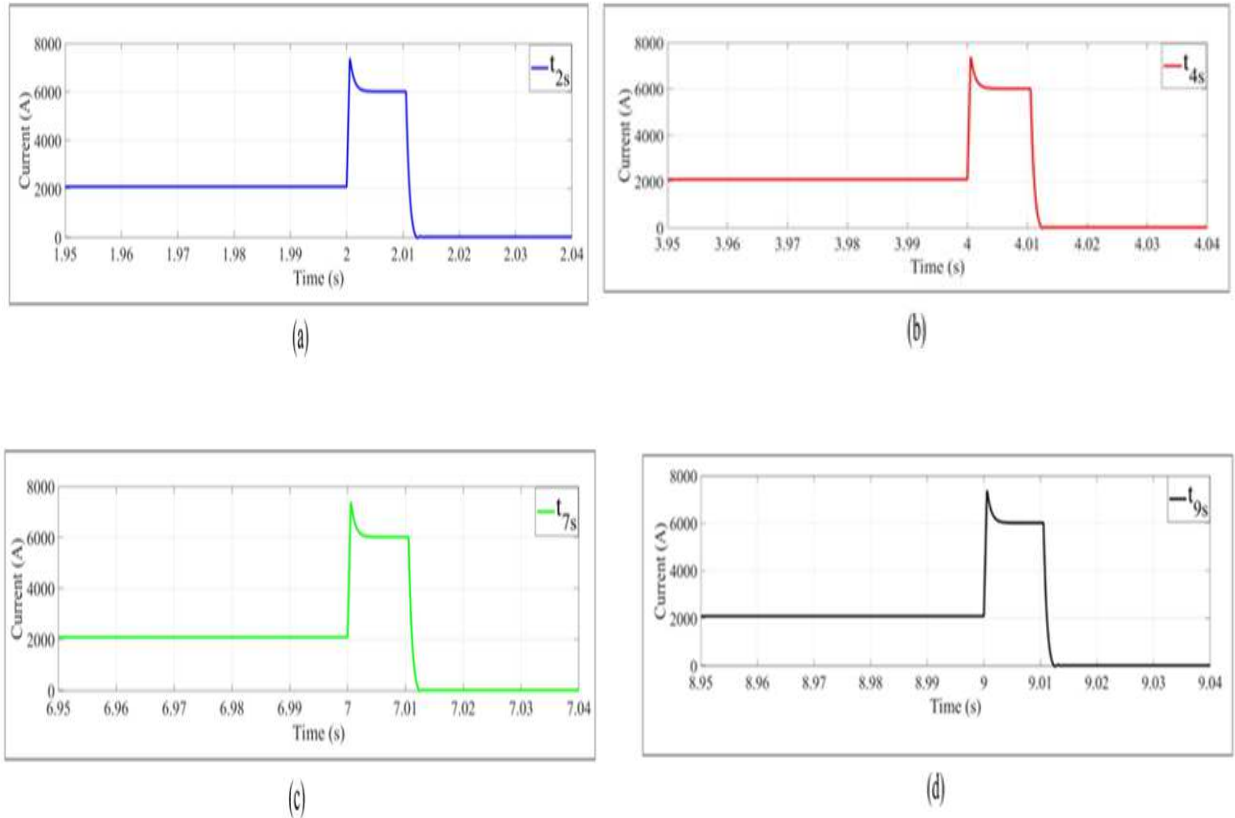


Figure 9: Line current waveforms under a fault occurring at: (a) 2s, (b) 4s, (c) 7s, and (d) 9s

Fig. 9 presents the results of testing the proposed control system under fault conditions introduced at different time instants from the beginning of the simulation. The simulation results demonstrate the successful performance of the proposed control system in detecting fault conditions at different occurrence times. Moreover, the results confirm the effective activation of the FCL circuit to limit the fault current magnitude, followed by the successful operation of the hybrid circuit breaker to efficiently isolate the network.

5. Simulated Results of the proposed FCL with Hybrid DCCB in HVDC system

5.1. Description of the Studied HVDC System

A hybrid DC circuit breaker is implemented, and the effect of the proposed fault current limiter is tested on the Egypt–Saudi Arabia DC interconnection project [34]. The project aims to interconnect the Egyptian and Saudi power grids through a ± 500 kV DC transmission system. Table (3) illustrates the parameters of the transmission line used in the simulation. In table (3), it is assumed that the fault occurs at a distance of 300 km from the converter station in Egypt.

Table 3: The parameters of the transmission line used in the simulation

Supply terminal voltage (kV)	± 500
Rated power (MW)	1500
Line Current (KA)	3
Line length (km)	1350
Location of fault (km)	300, from supply (conversion station)
Line Resistance (Ω/km)	0.054
Inductance (mH/km)	0.1
Capacitance ($\mu\text{f}/\text{km}$)	0.012

5.2. Integration of Hybrid DCCB with the proposed FCL in the HVDC System

The transmission line was simulated with the integration of a hybrid DC circuit breaker and the proposed fault current limiter (FCL) using MATLAB/Simulink, as shown in Fig. 10. Figures 11 and 12 illustrate the internal configurations of the hybrid DCCB and the proposed FCL, respectively.

The voltage limiting devices (VLDs) illustrated in Fig. 11 are internally composed of a surge arrester connected in parallel with a series RC snubber circuit. The capacitor in the RC snubber circuit plays a crucial role in mitigating transient overvoltage across the hybrid DC circuit breaker [35]. The IGBT is selected to withstand a rated current of 3 kA under normal operating conditions of the DC network [36].

The number of IGBTs employed in the hybrid DCCB and the proposed FCL to withstand the DC source voltage and the transient over voltage during the switching-off process of the IGBTs is calculated using Eq. (6).

$$N = \frac{V}{V_{Max-IGBT}} \quad (6)$$

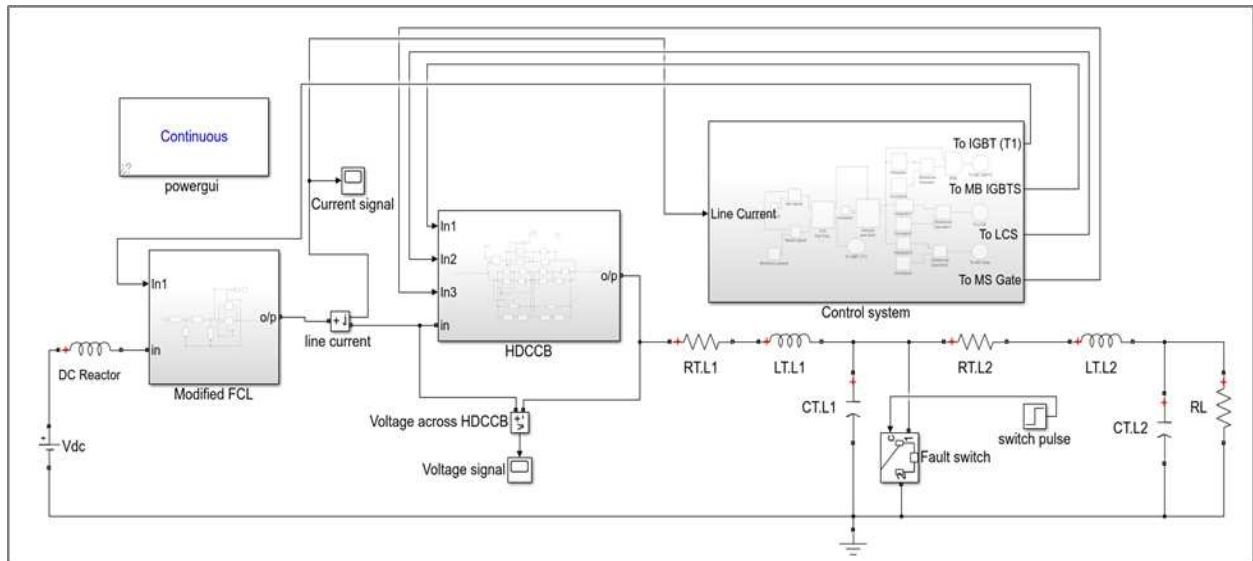


Figure 10: The overall Simulink model of the HVDC system with the proposed FCL

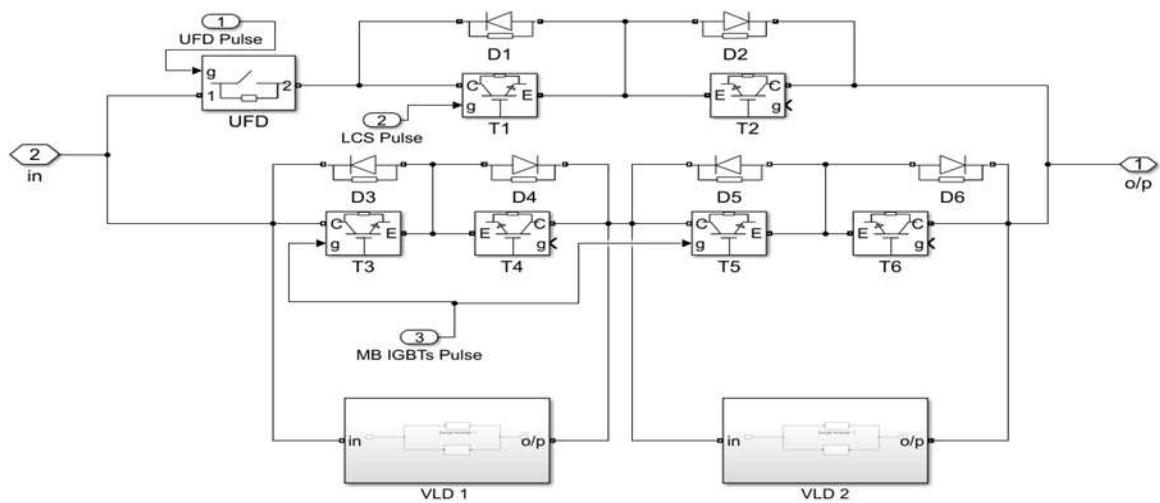


Figure 11: Internal structure of the Hybrid DCCB

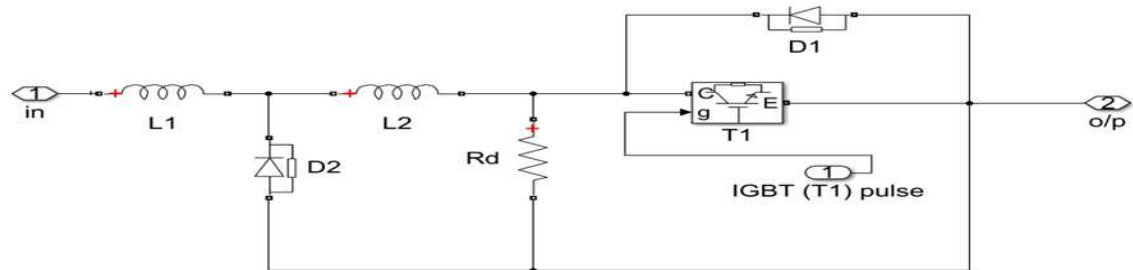


Figure 12: Internal structure of the proposed FCL

In Eq. (6), N is the required number of series-connected IGBTs; V is the maximum voltage applied across the series-connected IGBTs, and $V_{Max-IGBT}$ is the maximum voltage that a single IGBT can withstand. IGBT type 5SMA 5000L450300 is considered the most suitable for this purpose, as presented in the reference [36].

5.3. Selection of the Damping Resistance Value (R_d)

Fig. 13 illustrates the effect of increasing the damping resistance (R_d) on the fault current magnitude at the instant of hybrid DCCB opening, the peak voltage across the hybrid DCCB during the interruption process, and the peak voltage across the IGBT in the FCL during the opening process. It can be observed from Fig. 13(a) that increasing the damping resistance (R_d) reduces the fault current magnitude.

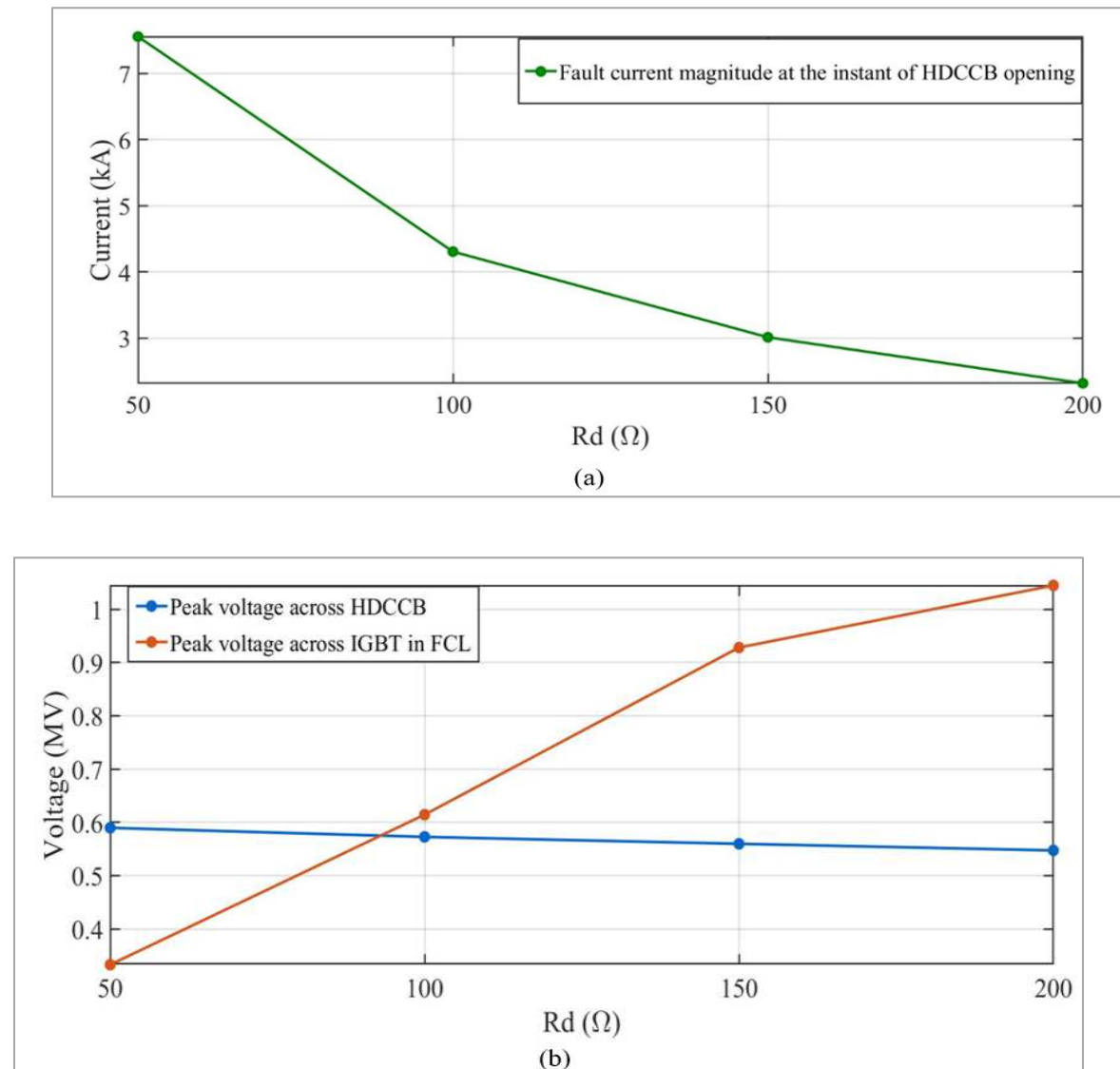


Figure 13: Effect of increasing the damping resistance (R_d) on: (a) the magnitude of the fault current, (b) the transient overvoltage across the hybrid DCCB, and the peak voltage across the IGBT (T1) in the proposed FCL.

Fig. 13(b) illustrates the trade-off between the positive and negative effects of increasing the damping resistance (R_d). As shown in this figure, increasing the damping resistance results in a lower peak voltage across the hybrid circuit breaker during the opening instant, consequently mitigating the electrical stress imposed on the hybrid DCCB. On the other hand, this increase in the damping resistance leads to an increase in the peak voltage across the IGBT used in the FCL. The damping resistance is selected to be 67Ω in order to prevent the maximum voltage across IGBT (T1) from reaching 500 kV. This selection is intended to reduce the number of IGBTs required in the main current path, thereby minimizing conduction losses at the rated current during normal network operation.

5.4. Breaking Capacity, and oscillation frequency with and without the proposed FCL

The rapid rate of rise and high peak value of short-circuit currents in high-voltage direct current (HVDC) systems directly determine the required response time, impedance transfer rate, and power dissipation capacity of the fault current limiter (FCL). It is observed from Table (4) that the proposed FCL significantly reduces the fault current by 78.3%, as shown in Fig.14, while reducing the peak voltage across the hybrid DCCB by 8.5%. The oscillation frequency before and after the FCL is calculated using Eqs. (7) and (8), respectively. The calculation proved that the oscillation frequency is reduced by approximately 14.67% after applying the FCL. The proposed FCL significantly increases the damping effect, leading to a faster decay of oscillations and improved system stability, as shown in Fig. 15.

$$f_{before FCL} = \frac{1}{2\pi * \sqrt{L_{Line}C}} \quad (7)$$

$$f_{after FCL} = \frac{1}{2\pi} * \sqrt{\frac{1}{L_{eq}C} - \left(\frac{R_d}{2L_{eq}}\right)^2} \quad (8)$$

In Eq. (7) L_{Line} is the total line inductance and C is the total line capacitance of the transmission line.

Table 4: Fault Current Magnitude, Breaker Voltage, and oscillation frequency with and without the proposed FCL

Fault location from the source (km)	300
Fault Current Magnitude (without FCL) (kA)	27.7
Fault Current Magnitude (with FCL) (kA)	6.01
Voltage across HDCCB (without FCL) (MV)	0.6325
Voltage across HDCCB (with FCL) (MV)	0.5787
Frequency (without FCL) (HZ)	107.62
Frequency (with FCL) (HZ)	91.83

Table 5 presents the breaking capacity values that should be considered in the design of the hybrid DCCB with and without the proposed FCL. This table indicates that the proposed FCL achieves a reduction of 86.61% in the breaking capacity. The breaking capacity values before and after the FCL are determined using Equations (9) and (10), respectively. The breaking capacity is calculated at the supply bus bar to design the hybrid DCCB according to the worst-case scenario. In Eq. (9) and (10), t_{delay} is the interval between fault occurrence and its detection, and t_{op} is the duration required by the hybrid DC circuit breaker to complete the fault interruption after receiving the trip command. It can be observed from Fig. 16 that increasing the snubber capacitance reduces the peak voltage across the hybrid DCCB

during the interruption process. However, this increase in capacitance results in a longer settling time, indicating a trade-off between voltage suppression and transient response.

$$I_{break\ before\ FCL} = \frac{V_{DC}}{L_{Line}} * (t_{delay} + t_{op}) + I_{Line} \quad (9)$$

$$I_{break\ after\ FCL} = \frac{V_{DC}}{R_d} * \left(1 - e^{-\frac{R_d}{L_{eq}} * (t_{delay} + t_{op})}\right) + I_{Line} * e^{-\frac{R_d}{L_{eq}} * (t_{delay} + t_{op})} \quad (10)$$

Table 5: Breaking capacity with and without the proposed FCL.

Fault location from the source (km)	0.005
Breaking Capacity (Before FCL) (kA)	55.587
Breaking Capacity (After FCL) (kA)	7.441

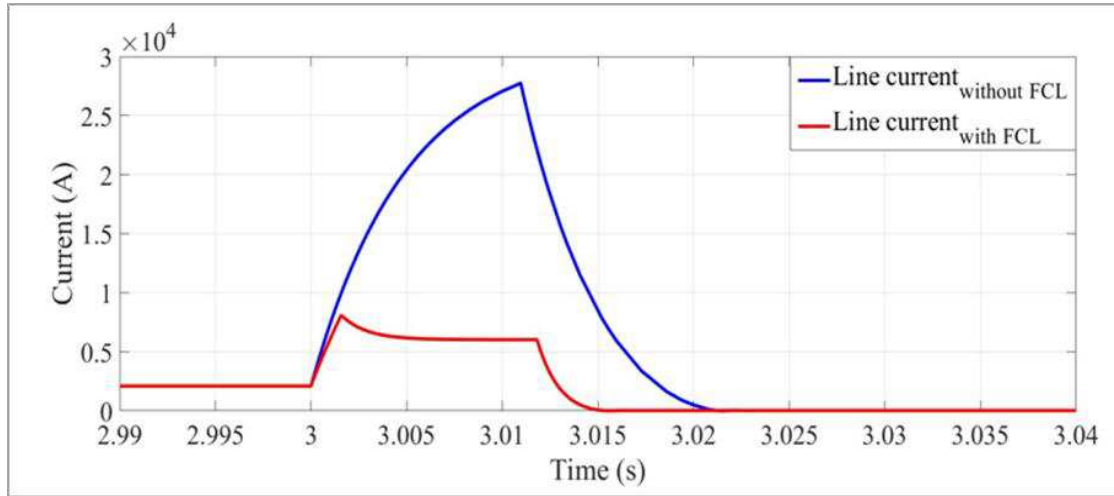


Figure 14: Line current waveform with and without the proposed FCL

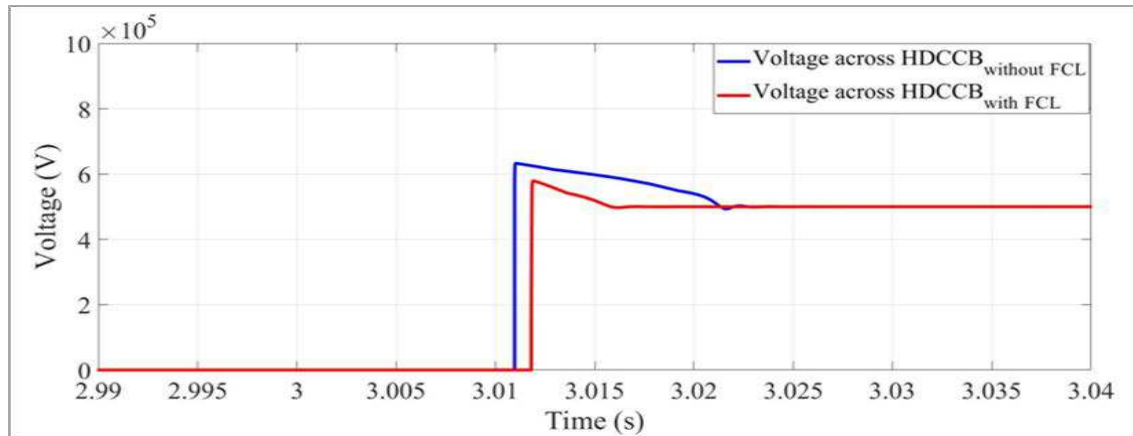


Figure 15: Voltage across the hybrid DCCB with and without the proposed FCL

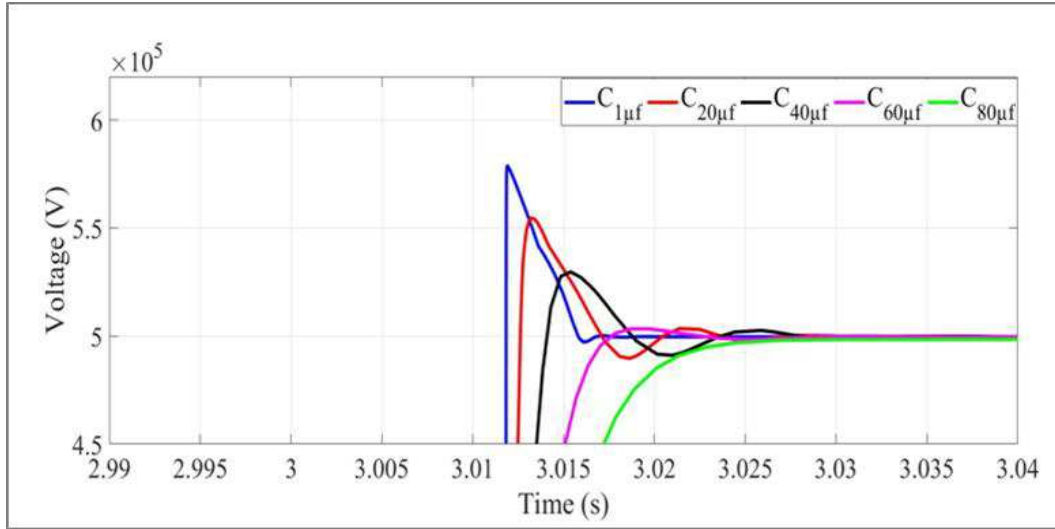


Figure 16: Effect of increasing the snubber capacitance on the peak voltage and settling time of the hybrid DCCB

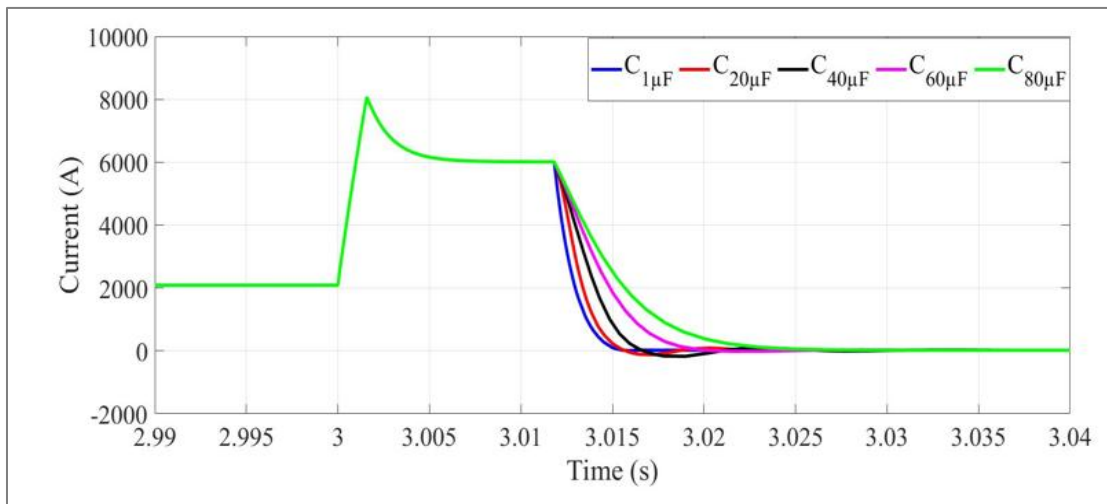


Figure 17: Effect of increasing the snubber capacitance on the fault current magnitude and its settling time

It can be observed from Fig. 17 that increasing the snubber capacitance has no effect on the magnitude of the fault current. However, the settling time of the current increases as the capacitance increases, indicating a slower transient response.

6. Parameters Affecting the FCL operation

6.1. Impact of the Fault Resistance on the FCL Performance.

Fault resistance dictates the severity of a short circuit and directly dictates the burden placed on a Fault Current Limiter (FCL). As fault resistance increases, the overall prospective fault current decreases, lessening the thermal and mechanical stress on the FCL and surrounding power grid equipment. The

most commonly used, standardized approach for calculating DC arc resistance R_{arc} outlined in IEEE 1584 / NFPA 70E (Annex D) as given in equation (11) [37].

$$R_{arc} = \frac{(a + k \cdot G)}{I_f} \quad (11)$$

Where: $a = 100$, $k = 0.127$, and G is the conductor gap distance in millimeters which is considered 3800 mm according to the same standards [37].

Table 6: Effect of fault resistance on the fault current with and without the proposed FCL

R_{arc} in(Ω) without FCL	R_{arc} in(Ω) with FCL	R_g (Ω)	I_f without FCL without fault resistance (kA)	I_f without FCL with fault resistance) (kA)	% clipping ratio (CR) due to R_f Without FCL	I_f with FCL and without fault resistance (kA)	I_f with FCL and with fault resistance (kA)	% clipping ratio CR) due to R_f with FCL
0.021	0.097	1	27.7	26.485	4.386	6.01	5.935	1.248
		3		24.335	12.148		5.8	3.494
		5		22.494	18.794		5.672	5.624
		10		18.902	31.762		5.386	10.383

The magnitude of the fault resistance R_f is the summation of arc resistance and the ground resistance R_g . By calculating the arc resistance; it was found to be around 0.021 Ω , which can be neglected compared to the ground resistance, which was considered to be between 1 Ω and 10 Ω depending on the quality of the grounding system and the soil resistivity. Table 6 gives the effect of fault resistance on the fault current with and without the proposed FCL

6.2. Effect of Increasing the Equivalent Inductance in the FCL Circuit

Fig. 18 illustrates the effect of increasing the equivalent inductance used in the FCL circuit on the fault current magnitude.

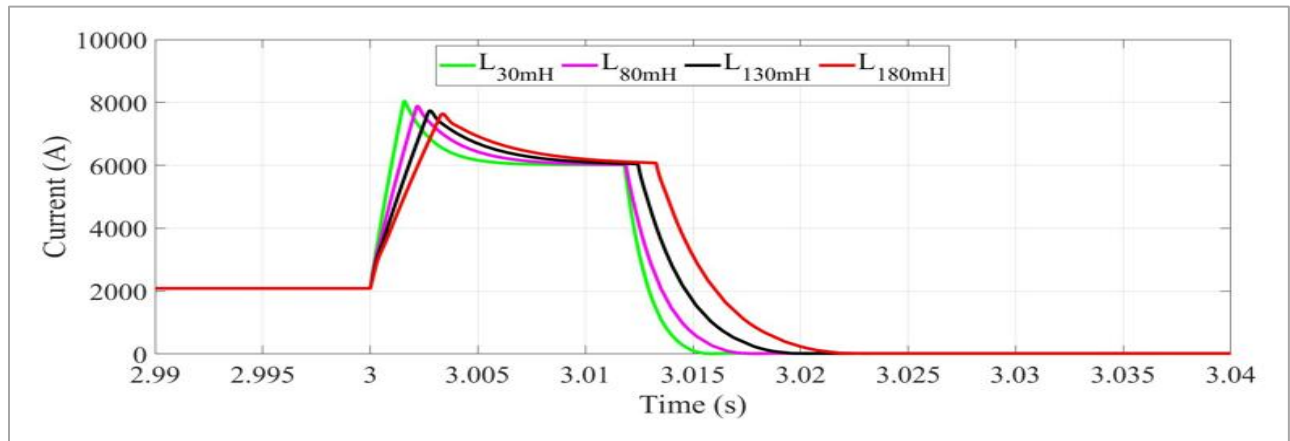


Figure 18: Effect of Increasing the Equivalent Inductance in the FCL on its operation

The figure shows that increasing the equivalent inductance delays the time required to reach the critical current value, beyond which the fault is confirmed and the FCL is activated to limit the fault current. Consequently, increasing the equivalent inductance delays the activation of the FCL. In this case, increasing the equivalent inductance does not significantly influence the fault current at the instant of hybrid circuit breaker opening, as the damping resistance (R_d) plays the dominant role in limiting the fault current at that instant.

6.3 Effect of the fault location on the magnitude of the fault current

Table 7 shows the effect of changing the fault location on the fault current magnitude. Figure 19 illustrates the effect of fault location on the peak fault current. It can be observed from this figure that the peak fault current decreases as the fault location moves farther away from the converter station due to the increase in the equivalent line resistance between the source and the fault point.

It can be concluded that faults occurring closest to the voltage source represent the worst-case scenario in terms of fault current magnitude. Therefore, when designing a hybrid DC circuit breaker, this worst-case scenario should be taken into consideration to ensure reliable operation for under severe fault conditions.

Table7: The magnitude of the fault current at different distance from the supply

Location of fault from supply voltage (km)	100	300	500	700
Magnitude of fault current (kA)	6.91	6.01	5.32	4.77

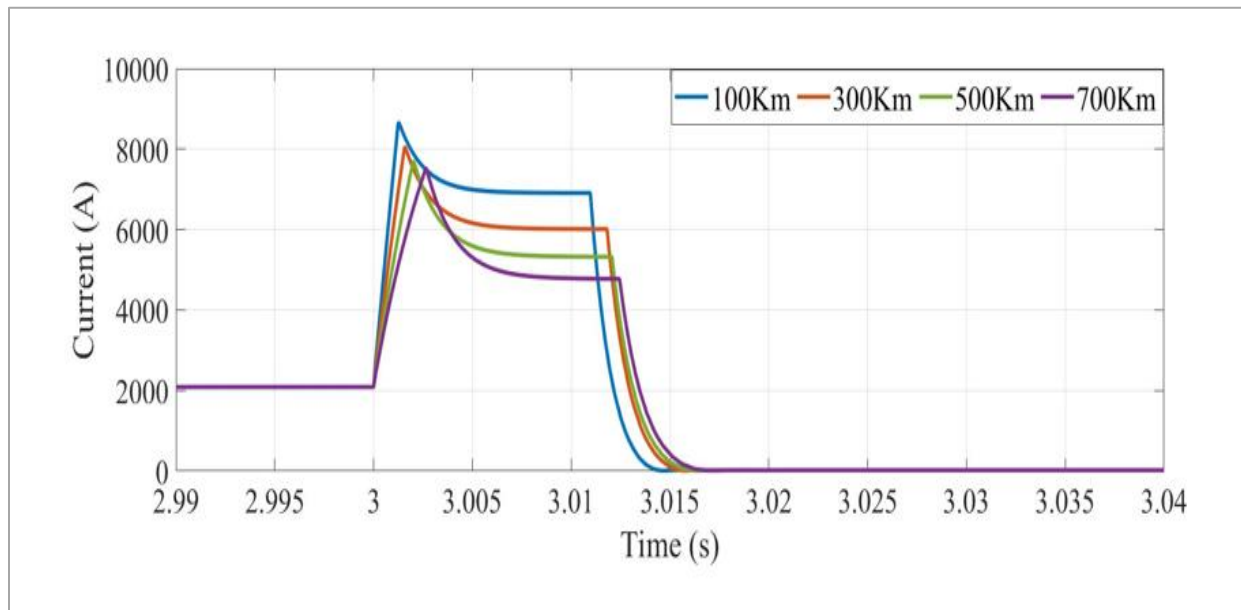


Figure19: Effect of Fault Location on the Fault Current

6.4. Damping resistance (R_d)

Using fixed resistance in the proposed FCL is a reliable way to suppress short-circuits currents, but it introduces several operational drawbacks. These primarily include constant power losses, adverse voltage drops, excessive heat generation, and potential limitations in overall current reduction

capabilities. It can be observed from figure 13(a) that increasing the damping resistance (R_d) reduces the value of the fault current by a non-linear relationship. On the other hand, it increases the voltage on the electronic current limiter components such as IGBT (T1) as illustrated in Fig. 13(b), The damping resistance value was specifically selected as $67\ \Omega$ to ensure that the voltage across the IGBT does not exceed 500 kV during the current commutation process from the normal path to the current-limiting path. This design criterion is important because the IGBT is designed to withstand a maximum voltage of 500 kV during the transfer instant. By limiting the voltage stress to this level, the required number of series-connected IGBTs in the normal path can be reduced, resulting in a more practical and cost-effective design.

An analysis of the effect of increasing the damping resistance on the power loss dissipated in the resistor during fault conditions has been conducted. This study was carried out to evaluate the impact of the damping resistance value on the energy dissipation and power loss during fault current limiting operation. It can be observed from Table 8 that increasing the damping resistance (R_d) reduces the power loss during fault conditions due to the reduction in the fault current magnitude.

Table 8: Effect of increasing the damping resistance (R_d) on fault current magnitude and power loss

Resistance (Ω)	Fault current (kA)	Power loss (MW)
50	7.554	2853.14
100	4.306	1854.16
150	3.012	1360.82
200	2.3167	1073.42

7. Comparative Analysis Overview

Coordinating the proposed Fault Current Limiter (FCL) consisting of two inductors L_1 , L_2 , discharging/limiting resistor R_d , a self-turn-off power switch like an IGBT, and two steering/freewheeling diodes D_1 , and D_2 with a Hybrid DC Circuit Breaker (HDCB) represents a highly effective method for protecting DC grids.

Evaluating the differences between MATLAB/Simulink simulations and experimental/real-time hardware validation (such as HIL/RTDS) reveals key operational gaps, design requirements, and performance characteristics. The comparison analysis overview can be carried out according to the proposed table 9

The root discrepancies between the experimental modeling done by others [38 and 39] and MATLAB/Simulink Simulation carried out in the present paper can be summarized in the following points

1. Standard power electronics modules in the Simulink software assume homogeneous distributions of internal charge carriers. In reality, the reverse rectification of D_1 and D_2 leads to the formation of localized negative current tails that cause electromagnetic interference (EMI) in the control circuits of adjacent devices.
2. Inductor saturation: The FCL inductors (L_1 and L_2) are modeled with fixed inductance values in the basic simulation loops. In the event of severe device failures, core saturation leads to a significant decrease in the nominal inductance value, allowing the fault current in practice to rise more rapidly than the simulation predicts.
3. The microcontrollers (DSP/FPGA) usually used in experimental verification require discrete sampling intervals and filtering algorithms, which add deterministic delays not present in Simulink's continuous-time blocks.

Table 9: Comparative Analysis Overview

Feature / Metric	Simulation by MATLAB/Simulink	Experimental / Real-Time Validation
Component-level modeling	Mathematical/ideal parameters. Physical anomalies are ignored unless manually entered	This includes inherent parasitic inductance, path resistance, and nonlinear component behaviors.
Fault Current Peak i_{fp}	Sharp drop due to perfect switching and instant control triggers	It is slightly delayed due to the gate-driver propagation delay and the mechanical response latency response time.
Transient Recovery Voltage (TRV)	The model was designed using clean and predictable mathematical damping curves	It is characterized by extreme voltage fluctuations, high stresses (dv/dt), and localized thermal fluctuations
Commutation Time	Near-instantaneous (typically calculated within micro-seconds based purely on ideal load curves).	It is extended by the binary reverse recovery times and the minority carrier storage times of the IGBT.
Thermal Energy Dissipation	Evaluated via simplified math models or ideal thermal network blocks.	High thermal buildup in (Rd) and metal oxide varistors (MOVs) of the DCCB.

8. Conclusion

The FCL configuration proposed in this article aims to reduce the transient overvoltage stress on the IGBT used in the FCL circuit and enhance protection performance by limiting the fault current and reducing the stress on the circuit breaker during the fault condition. The proposed FCL circuit significantly reduced the transient overvoltage across the IGBT by 86.96%, while maintaining the same level of reduction in the fault current magnitude. Furthermore, the impact of varying the damping resistance (R_d) was investigated. It was observed that increasing R_d contributes to a reduction in the fault current magnitude. However, this improvement comes at the expense of increased transient overvoltage across the IGBT used in the FCL during the turn-off process of the IGBT. In addition, the performance of the proposed control system was thoroughly evaluated under fault conditions at different time instants.

The results indicate that the proposed control strategy provides reliable and stable performance under varying the operating conditions. Overall, the proposed system offers an effective solution for improving HVDC system protection, with enhanced fault current limitation and reduced stress on system components. The integration of the proposed fault current limiter (FCL) with the hybrid DC circuit breaker (DCCB) in ± 500 kV DC line has been investigated in this study. Finally, the parameters affecting the FCL operation have been investigated

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