

Organic memory device with poly-L-lysine nanoparticles embedded as charge trapping layer

Hyeyeon Hur

Myongji University

Pilwoo Lee

Myongji University

Seungju Oh

Myongji University

Taejin Kim

Myongji University

Hyun Ho Lee

hyunho@mju.ac.kr

Myongji University

Research Article

Keywords: poly-L-lysine, indigo, charge trapping layer, TFT

Posted Date: September 14th, 2026

DOI: <https://doi.org/10.21203/rs.3.rs-10873902/v1>

License: © ⓘ This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

Additional Declarations: No competing interests reported.

Organic memory device with poly-L-lysine nanoparticles embedded as charge trapping layer

Hyeyeon Hur[#], Pilwoo Lee[#], Seungju Oh, Taejin Kim, Hyun Ho Lee^{*}

*School of Chemical Engineering and Material Science, Myongji University, 17058, Yongin-Si, Gyeonggi,
Republic of Korea*

[#]First authors.

^{*}Corresponding author.

Email address: hyunho@mju.ac.kr (Hyun Ho Lee)

Abstract

Recent bioelectronics has been rapidly evolved based on versatile biomolecules such as carbohydrate, amino acid, and nucleotide. In this study, polymeric amino acids of poly-L-lysine nanoparticles (PLL NPs) were synthesized and fabricated as charging elements for biosemiconductor of indigo memory devices. The PLL NPs as charge trapping layer (CTL) for non-volatile memory was self-assembled as floating gate (FG) layer by epoxy-amine bonds between 3-glycidylpropyl trimethoxysilane functionalized dielectrics and self-assembly monolayers (SAMs) of the PLL NPs. A memory window of +5.1 V (ΔV_{FB}) represented by capacitance-voltage hysteresis was obtained for metal-indigo-insulator-silicon (MIIS) capacitor. In addition, program/erase operations controlled by gate bias (± 30 V) were demonstrated in the PLL NPs embedded indigo thin film transistor (TFT) device with citric acid (CA) crosslinked polyvinylalcohol (PVA) dielectric on flexible substrate of poly ethylene terephthalate (PET). These results can be further extended to development of fully biomaterial-based memory device targeted to signal interface between biological logics and computer.

Keyword: poly-L-lysine, indigo, charge trapping layer, TFT

1 Introduction

Organic memory devices have been continuously developed owing to rapid evokedness of flexible and foldable electronics [1,2]. For example, field-effect transistor (FET) sensors based on organic semiconductors are sensitive devices that directly detect specific molecules. In addition, organic electronic components that change their conductivity using protein-protein interactions, DNA-protein bonds, DNA-DNA hybridization, and hormone-receptor binding have been intensively demonstrated to construct bioelectronics [3-8]. In this stage, direct and electronic analysis of these bioelectronics and biosemiconductor are scientifically, medically, and industrially important. Very recent remarkable examples of bioelectronics technology is information communication between biosystem's logic and computer such as brain computer interface (BCI). In addition, the performance of organic memory device varies greatly with the static charge and surface adsorption of various biomolecules [3-9].

In a normal format of electronic memory device, stored information is deleted when power is removed, while a non-volatile memory (NVM) device may retain stored information or data even when power is removed. NVM device refers to storage of a semiconductor memory chip configured with a floating gate (FG) including flash memory storage [3-9]. ROM, EPROM, EEPROM, ferroelectric RAM, etc. are examples of NVM and are mostly used as computer data storage devices based on Si. NVM is generally used for secondary storage or long-term/permanent storage, for example, in computer storage devices such as USB and SSD. In addition, the NVM has a higher process cost and a slower read speed than the volatile memory, resulting in low performance or limited lifespan.

Charge trapping layer (CTL) is an essential component of NVMs such as NOR or NAND flash

memory. CTL is one of FG MOSFET memory technologies, but typically uses an insulator rather than the doped polysilicon that is FG structure to store electrons. Typically, a silicon nitride (Si_3N_4) film is used in Si semiconductor format, but now a multi-metal oxide film or a high-k dielectric is also used [8-10]. A memory device using CTL has an advantage in that process costs can be reduced. It is difficult to control trap density and distribution in silicon/oxide/nitride/oxide/silicon devices, which are widely used as CTLs [10]. In CTL based NVM devices, trap density and distribution control are very important in determining programming/erasing bit distribution and data retention. Due to stability and charge trapping efficiency of N atoms of Si_3N_4 , the Si_3N_4 has been widely adopted as discrete CTL dielectric layer particularly for silicon active device. In addition, a lot of research is currently focused on memory devices using NPs-based CTLs because they have advantages in controlling trap density and distribution by uniform and discrete location of charging nodes as individual NPs [3-7]. Mechanism how CTL acquires charge is called writing or program, which is similar to how FG NOR flash is programmed. The electrons or holes gain enough energy as they traverse the high field region near the drain, boil in channel, and inject into CTL to stop [3,4]. In the other hand, mechanism, how CTL removes charge, can be accomplished through hot electron or hole injection, which is called erasing or removing.

For the bioelectronic memory devices, proteins have been introduced for development FG memory device, which focus on the protein's role as self assembly monolayers (SAMs) formation for organic semiconductor device [3,8]. Mainly, iron (Fe) storage or capping proteins (e.g. ferritin) have been employed as the FG due to charging by change of redox state of Fe ions [1,2]. In addition to metal ions, gold nanoparticles (AuNPs) have been adopted due to uncomplicated process of surface modification by biomolecules' conjugations [3-7]. However, synthetic protein or peptides have not been employed as charging trapping centers, yet. PLL, moreover as form of NPs, is one

of rarely studied biomaterial polymers and often reported to be synthesized in polymerization process accompanying condensation. The PLL can be synthesized in NPs form with environmental stability by acid or base-catalyzed amide bond formation [11,12]. The simple polymerization method could produce 10 nm diameter of PLL NPs, of which amine groups could be completely protonated form of polymer. Another application of PLL has been specific metal ion adsorption agent for surface plasmonic biosensor and biomedical agent for adherence of cell and proteins to glass and plastic surface [11-13]. Basic mechanism of biosensor using PLL was based on surface enhanced Raman spectroscopy (SERS) for detection of Hg(II) ions through conformational change of C-N peak of ϵ NH_3^+ upon binding of Hg(II) ions at PLL [12]. Synthesis of PLL can have complicated molecular layouts to have multiple conformation due to two amine groups (α, ϵ) in lysine molecule. By acid or base catalyst with thermal energy, α -PLL and ϵ -PLL can be synthesized simply [11]. In this study, α -PLL, which was compensated by KOH catalyst, was used as FG layer [11]. Through optimization of lysine concentration, dendritic polymer can be obtained by raising ϵ branch proportion to α branch proportion. However, in this study, α branch proportion was maximized. Meanwhile, any report of application of the PLL NPs to organic electronics has not been unveiled. Moreover, biological applications of the PLL NPs other therapeutic purposes have been introduced due to surface charges [13].

Amine ($-\text{NH}_2$) group in various biomaterial molecules was reported to have a mild physical adsorption subsequently having a fast intramolecular covalent binding with epoxy group. Since the epoxy groups are very stable at neutral pH even in aqueous condition, the epoxy-activated surface seems to be ideal for anchoring or immobilization of amine containing biomaterial NPs [7]. Furthermore, epoxy functional groups can react with different nucleophile groups, such as hydroxyl ($-\text{OH}$) and thiol ($-\text{SH}$). Since the PLL NPs has amine groups in its nano-sized molecules,

the covalent bond, or epoxy-amine bond between the epoxy- functionalized surface and the PLL NPs, can be stably realized. Recently, chemical reagent of 3-glycidylpropyl trimethoxysilane (GPTMS) was reported to have a strong covalent epoxy-amine bond with amine group of polyaniline (PANI) NPs [4]. In addition, the covalent bonding was efficiently enhanced by substrate heating at 80 °C.

In the other hand, natural dyes of indigoids including melanin or its derivatives have been continuously introduced and demonstrated as active layer of thin film transistors (TFTs), which were produced by chemical synthesis or microorganism fermentation [14-18]. Particularly, indigo or indigo analogs or derivatives have shown ambipolar TFT behavior, which could be used as active material of p-channel and n-channel simultaneously [14-16]. Even though their electron or hole mobilities have been far below 1.0 cm²/Vs, their application such as biosensor can be extended further. Compared to chemically synthesized organic semiconductor such as pentacene, the indigoids have amine groups in their chemical structures, which can be sensitive to moisture or inborn water content [18]. However, the semiconductor based on the indigoids are biocompatible unlike the pentacene to be used for flexible electronic device as biosystem interface.

Meanwhile, among organic insulating materials for the flexible device, polyvinyl alcohol (PVA) has many advantages, such as low temperature processing, water-soluble, low-cost, high dielectric constant and good resistance to most organic solvents [19,20]. However, under humid circumstance, OFETs with PVA dielectric usually give rise to an obvious hysteresis and terrible degeneration. The PVA thin-films have often been cross-linked with ammonium dichromate (ADC) in electronic industry [3,21]. Several chromium free methods also have been reported for the cross-linking of PVA gate dielectrics to reduce their electrical leakage, recently [19,20]. However, efficient methods for crosslinking of PVA thin-films in a controlled manner and with high dielectric performances are still needed.

In this study, PLL NPs were synthesized and the PLL NPs were used as charging trapping layer (CTL) in capacitor memory device of metal-indigo-insulator-silicon (MIIS) device and indigo FG thin film transistors (TFTs) device on silicon and glass substrate, respectively. The PLL NPs were self-assembly monolayers (SAMs) in aqueous phase based on dielectric layer by the epoxy-amine conjugation chemistry realized by anchoring amine-terminated PLL NPs and epoxy-terminated GPTMS surface. In addition, a flexible substrate of poly ethylene terephthalate (PET) was also applied to metal-indigo-PLL NPs-insulator-silicon (MIPIS) transistor to accomplish successful memory writing and erasing by gate programming voltage of +30 V for Si common gate device and +30 V for PET flexible device, respectively. Further advances of the FG TFT can be integrated into biointerface electronic system with fully biomaterial-based materials.

2 Materials and Methods

2.1. Materials

To fabricate CTL memory devices in this study, three substrates were used: a 10 nm and 200 nm SiO₂ grown with thermal oxidation on the heavily doped p-type Si wafer (Wafer Market) and a transparent and flexible plastic substrate, polyethylene terephthalate (PET). DI water, isopropyl alcohol (IPA, 99.9%, Sigma-Aldrich), and acetone ($\geq 99.9\%$, Sigma-Aldrich) were used for the cleaning process. Polyvinyl alcohol (PVA, Mw 130,000, $\geq 99\%$, Sigma-Aldrich) was used for the insulator layer on the PET substrate, and citric acid ($\geq 99.5\%$, Sigma-Aldrich) was used as a crosslinking agent to crosslink PVA.

3-Glycidyloxypropyl trimethoxysilane (GPTMS, 98%, Sigma-Aldrich) was used to functionalize the insulator layers such as SiO₂ and CA crosslinked PVA (PVA-CA). Indigo (95%, Sigma-Aldrich) was used as the semiconductor layer with ethyl alcohol ($\geq 99.5\%$, Sigma-Aldrich). Finally, Au or Al (iTASCO, Korea) was used as gate or source/drain electrode.

2.2. Synthesis of PLL NPs

A simplified polymerization procedure for the synthesis of PLL NPs was adopted. Lysine powder were added with mechanical stirring in quartz reactor having a thermostated bath at 65 °C for 1.5 hrs. More detailed synthesis method is described in references [11,13]. The synthesized brown dispersion of PLL NPs was purified by dialyzing against ultrapure deionized (DI) water using dialysis membrane. After dialysis, the dispersion was centrifuged to obtain the supernatant containing nano-sized PLL.

2.3. Dip-coating with GPTMS & PLL NPs

Figure 1(a) shows schematic diagram for charge trapping layer of PLL NPs on GPTMS functionalized dielectric layer. Prior to the dip-coating process, all substrates are cleaned using DI water, acetone, and IPA. After cleaning the substrate with DI water, it was sonicated with acetone for 20 min. Then, steam cleaning is performed using isopropyl alcohol (IPA) at 95 °C for one day. Finally, to remove the solution remaining on substrates, air-blowing is performed using an air gun, and then annealed on a hot plate at 80 °C for 5 min.

Dip-coating process was performed to form PLL NPs SAMs on the substrate surface that has undergone the cleaning process. To functionalize the surface of the insulator, which is SiO₂ or PVA-CA, 5.0 vol.% solution of GPTMS in ethanol was used. After soaking for 1 h using a dip-coating device, PLL NPs layer was formed on the substrate surface using PLL dissolved in DI water at a concentration of 0.1 wt.%.

The GPTMS treated substrate has epoxy group, which supports capable of reacting with nucleophilic groups such as amino (-NH₂), hydroxyl (-OH) and thiol (-SH) moieties. In order to have a covalent bond between the epoxy group and the nucleophile group of PLL NPs, first, the substrate was immersed in PLL NPs solution to adsorb the molecule, and secondly, the covalent bond formation with the epoxy group was performed. Since PLL NPs had an amine group, it can be surface-treated with GPTMS to covalently bond with epoxy-rich substrates.

2.4. Capacitor and TFTs on Si substrate

Common gate TFT was fabricated using a 200 nm SiO₂ wafer. A schematic diagram for the fabrication of a common gate transistor is shown in Figure 1(b). For TFT using a common gate structure, Au was used for source/drain electrodes with shadow mask. For fabrication of MIIS memory capacitor device, 10 nm thick thermal grown SiO₂ is formed on p-type boron doped (100) silicon wafer having a resistivity of 10-15 W-cm. The SiO₂ surface was first functionalized with

GPTMS by immersing the substrate in 5.0 vol.%. GPTMS in ethanol for 1 hr. The PLL NPs were assembled on SiO₂ by immersing the substrates into the PLL NPs solution in DI water. After formation of the PLL NPs monolayer, the substrate was annealed at 80 °C and sonicated with DI water to remove non-covalently bound PLL NPs [4]. Indigo and top gold electrode are then deposited via sequential thermal evaporation. Also, indigo TFTs memory device was fabricated with 200 nm SiO₂ was formed on p-type boron doped silicon wafer with gold electrode.

To confirm the charge storage capacity of charge trapping layer (CTL) using PLL NPs, metal/indigo/insulator/silicon (MIIS) and metal/Indigo/PLL NPs/insulator/silicon (MIPIS) capacitors were fabricated. 10 nm SiO₂ wafer was used to fabricate the capacitor, and an indigo semiconductor layer was deposited for 5 min. using a thermal evaporator after cleaning and dip-coating processes. As the electrode of the capacitor, Au or Al was deposited using a thermal evaporator. To analyze whether PLL NPs have sufficient capability as CTL, capacitors were made and capacitance-voltage (C-V) was measured using Agilent LCR meter 4284A equipment.

2.5. PLL NPs CTL indigo TFTs using PET substrate

In Figure 1(c), PET substrate was used to fabricate a transparent and flexible memory device. Before coating dielectric layer, the PET substrate was cleaned and then treated with UV/Ozone for 20 min. Then, 5.0 wt.% of PVA was dissolved in DI water mixed with the same concentration of CA as a crosslinking agent. On the PET substrates patterned using Al gate electrode, PVA-CA was spin-coated at 500 rpm for 5 s and at 3500 rpm for 30 s. To activate the crosslinking process of PVA, it was annealed on hot plate at 110 °C for 1 h. After dip-coating PLL NPs and GPTMS such as common gate transistor, indigo was deposited with thermal evaporator and then Au was deposited as source/drain electrodes using shadow mask. Agilent semiconductor parameter analyzer 4156C equipment was used to measure the electrical transfer characteristics of MIPIS memory devices

fabricated with common gate.

2.6. Instrumental analysis of PLL NPs, PVA-CA, and indigo

To induce the crosslinking of PVA, which is the dielectric layer, a solution of 5.0 wt.% PVA solution and 5.0 wt.% PVA-CA were prepared on a bare glass that had undergone cleaning process and UV/Ozone treatment. The solution was spin-coated at 500 rpm, 5 s, and then 3000 rpm 30 s. Then, to activate the crosslinking of PVA-CA, annealing was performed at 110 °C for 1 h to produce a film. Crosslinking of the two components was confirmed using attenuated total reflection (ATR) mode Fourier transform infrared spectroscopy (FTIR). In order to accomplish the SAMs formation of PLL NPs, dip-coating process was performed on the cleaned Si wafer, and the NPs CTL was confirmed by checking field emission scanning electron microscope (FE-SEM, SU-70, Hitachi Co., Osaka, Japan). In addition, it was also confirmed whether NPs were well dispersed on the surface using atomic force microscope (AFM). In addition, from a bench-top SEM (COXEM, EM-30AX, Korea), PLL NPs dried on glass surface could be imaged with Au coating. Particle size analysis of PLL NPs was performed by dynamic light scattering (DLS) system (Zetasizer Nano, Malvern Co. USA) as shown in Figure 2(a). Conjugation of the PLL NPs was also analyzed by atomic force microscopy (AFM: Park systems XE-100, Korea).

3 Discussion

3.1 Analysis of ATR FTIR of PLL SAMs and PVA-CA dielectric layer

Fig. 2(a) also shows image of synthesized PLL NPs, which confirmed that the size are in ranges of 10~200 nm as identified by FE-SEM. In addition, Figure 2(b) represents proofs of PLL NPs conjugated on SiO₂ layer by surface modifier of GPTMS and comparison with physically adsorbed PLL NPs [3,4]. As identified in FTIR spectra of Fig. 2(b), broadened peak at 3200~3600 cm⁻¹ corresponds to hydroxyl group (-OH) stretching mode from epoxy ring opening of GPTMS. Figure 3(c) also shows two proofs of SAMs formation by FE-SEM and AFM. Since dip-coating process could remove heavy and large-sized PLL NPs by gravity, 10~100 nm sized PLL NPs were successfully aligned on dielectric surface as confirmed by FE-SEM and AFM.

Crosslinking of PVA using CA was carried out by annealing at 120°C for 1 hour. During the heat treatment, an esterification reaction occurs between hydroxyl group of PVA and carboxyl group of CA. The physical stability of PVA-CA through annealing also increased because the crystallinity increased and the structure was stabilized. The FTIR spectra of PVA and PVA-CA films spin-coated on bare glass could be compared as shown in Figure 2(d) [3,19-21].

The stability of PVA-CA could increase absorption peak at 1200 cm⁻¹. This peak is due to the C-C stretching mode, which is reported to be related to the crystallinity of the PVA structure. Therefore, it shows that the structure is physically stabilized due to increased crystallinity compared to pure PVA. An oscillation band for PVA-CA was observed at 1718 cm⁻¹. Since it is a peak indicating the formation of an ester, carbonyl (-C=O) group, it can be seen that the crosslinking of PVA using CA proceeds due to the formation of ester linkage. Finally, when the pure PVA film and the PVA-CA film were compared over 3000-3600 cm⁻¹ region, the O-H stretching vibration peak was relatively reduced due to ester bond formation between carboxyl group of CA and the hydroxyl group of PVA.

3.2. Capacitor using Si wafer

One of important feature of lysine out of many amino acids is that the lysine has two amine group in its structure. In fact, amine or amino group containing chemical compounds, especially when intervened between semiconductor and dielectric layer, were found to trigger large memory hysteresis for organic TFTs using pentacene as active channel [22]. As a consequence, the PLL NPs layer is expected to induce significantly wide memory hysteresis due to their plenty of amine groups [4,10,22]. Metal/indigo/insulator/Si (MIIS) capacitor and metal/indigo/PLL NPs/Si (MIPIS) capacitor devices were fabricated, and both devices used a Si wafer with an insulator layer of 10 nm SiO_2 as tunneling oxide. Electrode of two capacitors were made of gold (Au) and deposited using a shadow mask with a circular pattern having a diameter of 300 μm or 500 μm with thermal evaporator. In addition, voltages were sequentially applied to both devices in the order of -5 V $\sim$ +5 V $\sim$ -5 V (-5 V to +5 V sweep), -7 V $\sim$ +7 V $\sim$ -7 V, and -9 V $\sim$ +9 V $\sim$ -9 V, and measurements were made at a frequency of 1MHz. Figure 3(a) and 3(b) shows the C-V measurements of the two devices, shows the typical capacitance characteristics of a capacitor: accumulation, depletion, and inversion [3-7]. Also, all hysteresis loops were clockwise.

Comparing Fig. 3(a) and 3(b), it can be seen that there are differences in flatband voltage shift (ΔV_{FB}) of capacitance or the memory window depending on the presence or absence of PLL NPs. Looking at Fig. 3(a), the voltage shift of the device with only indigo without PLL NPs has values lower than 0.5 V, which is close to 0V. However, the device as CTL with PLL NPs in Fig. 3(b) has as little as 3.1 V at -5 V to +5 V sweep, at -9 V to +9 V sweep, the ΔV_{FB} increased to 5.8 V. Therefore, as the voltage sweep range increases, the charging effect of MIPIS capacitor device become significant. However, MIPIS capacitor device with PLL NPs has a more charging effect. However, in both devices, some leakage current occurred due to the thin 10 nm insulating layer of SiO_2 [6,7].

As a result, the MIIS capacitor has the characteristics of a non-memory device that cannot store charge, while the PLL NPs of MIPIS capacitor has sufficient charge trapping capability to be applied as a CTL having a sufficient memory window of ΔV_{FB} . It shows a potential ability of being applied as a NVM device for biocompatible electronic interface.

3.3. Electrical characteristics of MIPIS transistor

In the MIPIS memory device, which is a Si-based transistor, the gate voltage range was -10 V to +5 V at +0.5 V intervals, and the drain-source voltage was measured at -10 V. In addition, to measure the transfer sweep of the MIPIS device, the gate voltage was swept at -10 V to +10 V sweep, the drain voltage was fixed at -10 V, and the step was set at +0.5 V.

As shown in Figure 4(a), the MIPIS transistor with the active semiconductor layer of indigo having a p-type Si common gate structure was confirmed to have the property that the indigo behaves like an ambipolar semiconductor in the transfer curve.

As identified in Fig. 4(b), reversible shifts in V_{th} were obtained for the MIPIS transistor arising from charge trapping and detrapping in PLL NPs [4]. Measured with positive source drain voltage, V_{th} of the PLL NPs indigo memory TFT was in the range of -7.1 V to -9.6 V for hole [16]. As characterized in Fig. 4(b), sweep pattern of transfer curves showed typical ambipolar charge transport with large width of hysteresis of 14.4 V [4,14,16,22,25]. The high hysteresis of transfer curve sweeps in Fig. 4(b) is due to strong water content dependence of indigo semiconductor and PLL NPs [16,23,24,25]. For example, indigo analogues such as epindolidione semiconductor showed drastic changes of transfer hysteresis under various aqueous conditions (tens of μ L DI water and pH variant water on TFT active channel) [16]. The most drastic hysteresis changes were by pH changes rather than the existence of water in this case. Therefore, since PLL NPs can be easily

protonated (H^+) to ϵ amine ($-NH_2$) groups by aqueous condition, hydration, and H^+ concentration, the huge hysteresis behavior in Fig. 4(b) is assumed to be from humidity environment [11-13,25]. In fact, the measurement was performed under 20-60 relative humidity (RH) in this study. As consequence, it can be concluded that the PLL NPs indigo memory TFT is very RH sensitive [18,23,24,25]. In addition, off current of the MIPIS device was one order higher than MIIS device, there is a high chance of ionic conduction between source and drain apart from major current medium of electron and hole [23,24,25]. To summarize, the existence of PLL NPs as CTL layer could drive more dependence of humidity, hydration, and pH change as like as melanin-based electronic devices [18,23,24,25].

The programming-erasing process was measured to confirm the capability as a memory device. The Program and erase process also used the semiconductor parameter analyzer. Programming-erasing process was performed three steps in order to measure. First, the initial transfer properties were measured. The drain voltage was -10 V, and the gate voltage was measured from -10 V to 0V at +0.5 V intervals. Next, for programming, a -30 V bias is applied to the gate to store charges (memory) in the CTL made of PLL NPs, and then measure the transfer characteristics. In this case, the drain voltage and the gate voltage range for measuring the initial transfer characteristics were remained the same. Finally, to erase the stored charge again, a +30 V bias is applied to subtract the stored charge (memory), and then the transfer characteristic was measured.

Referring to Figure 4(c), it can be seen that threshold voltage shift (ΔV_{th}) was made in the negative direction (-1.8 V) after the program compared to the initial stage (+2.0 V). Therefore, programming window was 2.0 V as shown in Fig. 4(c).

It can be confirmed that holes are injected into the PLL NPs when a negative voltage was applied to the gate electrode. It demonstrates that it has a charge trapping effect from the indigo layer. Also, after erasing to remove the memory (applying a +30 V via to the gate), it can be identified that V_{th}

was restored to the same as the initial state, and it can be seen that the holes trapped in PLL NPs have escaped. Through this, the MIPIS device, which is a common gate structure using a Si substrate, demonstrated the behavior of a non-volatile memory device, and confirmed that PLL NPs have a charge trapping effect as a CTL [4].

3.4. Electrical characteristics of PLL NPs indigo memory transistor on PET substrate

To measure the electrical transfer characteristics of the PLL NPs indigo memory device fabricated with the bottom gate top contact (BGTC) structure. As like as the MIPIS device, both the transfer characteristics and the programming-erase process were measured in the same gate voltage range and drain voltage.

As shown in Figure 5(a), the PLL NPs indigo memory device with the BGTC structure using the PET substrate was also confirmed to have the property of indigo to behave like an ambipolar semiconductor in the transfer curve as like as the previous MIPIS device. As characterized in Fig. 5(a), sweep pattern of transfer curves showed typical ambipolar charge transport with large width of hysteresis of 7.2 V [16,22,25]. In this case, it was detected that a slight leakage current through PVA-CA dielectric layer occurred compared to the MIPIS device using the Si substrate.

Referring to Figure 5(b), it can be seen that ΔV_{th} was changed in the negative direction (-1.0 V) after the program compared to the initial stage. It can be confirmed that holes are injected into the PLL NPs when a negative voltage is applied to the gate electrode. This demonstrates that even on PET substrates, PLL NPs have a charge trapping effect from the indigo layer. In addition, after the erasing operation to remove the memory (applying a +30 V via to the gate), it can be seen that moves in a positive direction (+2.8 V) to restore than the initial state, which was shown in the transfer

characteristics. It can be seen that electrons are trapped behind. However, compared to Fig. 4(b) of the memory device on Si common gate, Fig. 5(c) could not show a desirable erase operation that passed through the initial V_{th} . It is believed that it is originated from dielectric layer of PVA-CA layer, which has another function of charge storage mechanism accompanied by PLL NPs' CTL function [19].

In summary, like the MIPIS devices, the PLL NPs indigo memory on PET has also proven to be a CTL-based non-volatile memory operation. It also confirmed that indigo behaves as a semiconductor material even on a transparent and flexible plastic PET substrate and that PLL NPs have charge trapping ability as a CTL. A memory device using a PET substrate has opened up the possibility of developing a transparent and flexible memory device as a next-generation bioelectronic device.

4 Conclusions

Indigo was used as a semiconductor material and PLL NPs were applied to CTL to fabricate memory devices. PLL NPs were functionalized with GPTMS to form SAMs on a dielectric surface such as SiO₂ or PVA-CA through an epoxy-amine reaction with the functionalized surface. In addition, flexible memory devices on PET substrates were fabricated by spin-coating the PVA-CA dielectric. Through FE-SEM image, PLL NPs SAMs were confirmed on the Si substrate. From AFM image, it was confirmed that the PLL NPs were present as CTL function. In addition, to confirm the crosslinking of PVA and PVA-CA films were made and FTIR peaks were confirmed that the carboxyl group of CA and the hydroxyl group of PVA were ester-bonded to form an ester carbonyl group. To confirm the charge trapping ability of PLL NPs, a capacitor was fabricated, and it could be demonstrated that PLL NPs could be applied as CTLs through memory window shifts of ΔV_{FB} . A MIPIS TFT device was fabricated using Si substrate, which was investigated whether it could be applied as a NVM device through a programming-erasing process. In addition, it was confirmed that the PLL NPs indigo TFT device using PET, which was a transparent and flexible substrate, could be applied as a next-generation bioelectronic memory. Based on the transfer curves of the two devices, the indigo showed bipolar semiconductor characteristics, which were sensitive to hydrated or protonated state of amine groups of PLL NPs. Based on this study, future development of fully biomolecular-based memory device can be facilitated.

Acknowledgements

This work was conducted with the support of the International Collaborative Research and Development Program (P0028061, Development of High-Speed RT-PCR Systems Utilizing Liquid Metal Composites) funded by the Ministry of Trade, Industry & Energy (MOTIE, Republic of Korea). This research was also supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (RS-2026-25485062).

5 References

1. Lim, B.J., Ko, Y., Cho, J.H., Cho, J.: Organic field-effect transistor memory devices using discrete ferritin nanoparticle-based gate dielectrics. *Small* **9**, 3784-3781 (2013). <https://doi.org/10.1002/sml.201300522>
2. San, B.H., Kim, J.A., Kulkarni, A., Moh, S.H., Dugasani, S.R., Subramani, V.K., Devappa, T.N., Lee, H.H., Park, S.H., Kim, T., Kim, K.K.: Combining protein-shelled platinum nanoparticles with graphene to build a bionanohybrid capacitor. *ACS Nano* **8**, 12120-12129 (2014). <https://doi.org/10.1021/nn503178t>
3. Kim, H.-J., Jung, S.M., Kim, Y.-H., Kim, B.-J., Ha, S., Kim, Y.-S., Yoon, T.-S., Lee, H.H.: Characterization of Au nanoparticle pentacene memory device with polymer dielectric layer. *Thin Sol. Films* **519**, 6140-6143 (2011). <https://doi.org/10.1016/j.tsf.2011.03.112>
4. Kim, Y.-H., Kim, M., Oh, S., Jung, H., Kim, Y., Yoon, T.-S., Kim, Y.-S., Lee, H.H.: Organic memory device with polyaniline nanoparticles embedded as charging elements. *Appl. Phys. Lett.* **100**, 163301 (2012). <http://dx.doi.org/10.1063/1.4704571>
5. Oh, S., Kim, M., Kim, Y., Jung, H., Yoon, T.-S., Choi, Y.-J., Kang, C.J., Moon, M.-J., Jeong, Y.-Y., Park, I.-K., Lee, H.H.: Organic memory device with self-assembly monolayered aptamer conjugated nanoparticles. *Appl. Phys. Lett.* **103**, 083702 (2013). <http://dx.doi.org/10.1063/1.4819336>
6. Kim, M., Lee, H.-J., Oh, S., Kim, Y., Jung, H., Oh, M.-K., Yoon, Y.J., Yoo, T.H., Yoon, T.-S., Lee, H.H.: Robust ZnO nanoparticle embedded memory device using vancomycin conjugate and its biorecognition for electrical charging node. *Biosens. Bioelect.* **56**, 33-38 (2014). <http://dx.doi.org/10.1016/j.bios.2013.12.049>
7. Kim, Y., Kim, M., Jung, H., Choi, Y.-J., Kang, C.J., Yoon, T.-S., Lee, H.H.: Electrical charging characteristics of Au NPs embedded by sequence specific complementary DNA hybridization in metal-pentacene-insulator-silicon device. *Biochip J.* **8**, 275-281 (2014). <http://dx.doi.org/10.1007/s13206-8405-7>
8. Sarkar, J., Tang, S., Shahrjerdi, D., Banerjee, S.K.: Vertical flash memory with protein-mediated assembly of nanocrystal floating gate. *Appl. Phys. Lett.* **90**, 103512 (2007). <https://doi.org/10.1063/1.2711528>
9. Tang, Z., Liu, Z., Zhu, X.: Progress of high-k dielectrics applicable to SONOS-type nonvolatile semiconductor memories. *Trans. Elect. Electro. Mater.* **11**, 155-165 (2010).

<http://www-riss-kr-ssl.openlink.mju.ac.kr/link?id=A101056188>

10. Choi, S., Yang, H., Chang, M., Baek, S., Hwang, H., Jeon, S., Kim, J., Kim, C.: Memory characteristics of silicon nitride with silicon nanocrystals as a charge trapping layer of nonvolatile memory devices. *Appl. Phys. Lett.* **86**, 251901 (2005). <https://doi.org/10.1063/1.1951060>
11. Scholl, M., Nguyen, T.Q., Bruchmann, B., Klok, H.-A.: The thermal polymerization of amino acids revisited; Synthesis and structural characterization of hyperbranched polymers from L-lysine. *J. Polym. Sci. A: Polym. Chem.* **45**, 5494-5508 (2007). <https://doi.org/10.1002/pola.22295>
12. Ly, N.H., Joo, S.-W.: Hg(II) Raman sensor of poly-L-lysine conformation change on gold nanoparticles. *Biochip J.* **8**, 303-309 (2014). <https://doi.org/10.1007/s13206-014-8409-3>
13. Roh, S., Jang, Y., Yoo, J., Seong, H.: Surface modification strategies for biomedical applications: enhancing cell-biomaterial interfaces and biochip performances. *Biochip J.* **17**, 174-191 (2023). <https://doi.org/10.1007/s13206-023-00104-4>
14. Irimia-Vladu, M., Głowacki, E.D., Troshin, P.A., Schwabegger, G., Leonat, L., Susarova, D.K., Krystal, O., Ullah, M., Kanbur, Y., Bodea, M.A., Razumov, V.F., Sitter, H., Bauer, S., Sariciftci, N.S.: Indigo-a natural pigment for high performance ambipolar organic field effect transistors and circuits. *Adv. Mater.* **24**, 375-380 (2012). <https://doi.org/10.1002/adma.201102619>
15. Han, J., Wang, W., Ying, J., Xie, W.: Ambipolar organic thin-film transistor-based nano-floating-gate nonvolatile memory. *Appl. Phys. Lett.* **104**, 013302 (2014). <https://doi.org/10.1063/1.4860990>
16. Głowacki, E.D., Romanazzi, G., Yumusak, C., Coskun, H., Monkowius, U., Voss, G., Burian, M., Lechner, R.T., Demitri, N., Redhammaer, G.J., Sunger, N., Suranna, G.P., Sariciftci, S.: Epindolidiones-versatile and stable hydrogen-bonded pigments for organic field-effect transistors and light-emitting diodes. *Adv. Funct. Mater.* **25**, 776-787 (2015). <https://doi.org/10.1002/adfm.201402539>
17. Pitayatanakul, O., Iijima, K., Kadoya, T., Ashizawa, M., Kawamoto, T., Matsumoto, H., Mori, T.: Ambipolar organic field-effect transistors based on indigo derivatives. *Eng. J.* **19**, 61-76 (2015). <https://doi.org/10.4186/ej.2015.19.2.61>
18. Kim, Y., Park, H., Lee, P., Woo, K., Choi, K.-Y., Lee, H.H.: Biosynthesis of tyrosine-derived i-melanin and its characteristics for organic thin film transistor device. *Mater. Today Adv.*

- 26**, 100582 (2025) <https://doi.org/10.1016/j.mtadv.2025.100582>
19. Tsai, T.-D., Chang, J.-W., Wen, T.-C., Guo, T.-F.: Manipulating the hysteresis in poly(vinyl alcohol)-dielectric organic field-effect transistors toward memory elements. *Adv. Funct. Mater.* **23**, 4206-4214 (2013). <https://doi.org/10.1002/adfm.201203694>
 20. Çay, A., Kumbasar, A., Keskin, E.P., Akduman, Z., Ürkmez, A.: Crosslinking of poly(vinyl alcohol) nanofibres with polycarboxylic acids: biocompatibility with human skin keratinocyte cells. *J. Mater. Sci.* **52**, 12098-12108 (2017). <https://dx.doi.org/10.1007/s10853-017-1370-5>
 21. Kim, B.-J., Kim, H.-J., Jung, S.-M., Kim, Y.-H., Ha, S., Yoon, T.-S., Lee, H.H.: Capacitance-voltage characteristics of metal-polymer-silicon device with inkjet-printed Ag electrode. *Thin Sol. Film* **519**, 4319-4323 (2011). <https://dx.doi.org/10.1016/j.tsf.2011.02.035>
 22. Zheng, C., Tong, T., Hu, Y., Gu, Y., Wu, H., Wu, D., Meng, H., Yi, M., Ma, J., Gao, D., Huang, W.: Charge-storage aromatic amino compounds for nonvolatile organic transistor memory devices. *Small* **14**, 1800756, (2018). <https://doi.org/10.1002/sml.201800756>
 23. Vahidzadeh, E., Kalra, A.P., Shankar, K.: Melanin-based electronics: From proton conductors to photovoltaics and beyond. *Biosens. Bioelect.* **122**, 127-139 (2018). <https://doi.org/10.1016/j.bios.2018.09.026>
 24. Sheliakina, M., Mostert, A.B., Meredith, P.: Decoupling ionic and electronic currents in melanin. *Adv. Funct. Mater.* **28**, 1805514 (2018). <https://doi.org/10.1002/adfm.201805514>
 25. Paulin, J.V., Coleone, A.P., Batagin-Neto, A., Burwell, G., Meredith, P., Graeffae, C.F.O., Mostert, A.B.: Melanin thin-films: a perspective on optical and electrical properties. *J. Mater Chem. C* **3**, 8612 (2021). <https://doi.org/10.1039/d1tc01440d>

Figure captions

Figure 1. schematic illustrations of (a) diagram for charge trapping layer of PLL NPs on GPTMS functionalized dielectric layer, (b) fabrication procedure of MIPIS device, and (c) fabrication procedure of flexible memory device using PVA-CA, indigo, and PLL NPs

Figure 2. (a) DLS analysis and FE-SEM image of synthesized PLL NPs, (b) ATR mode FTIR spectra of epoxy-amine tethered PLL NPs, (c) FE-SEM image of PLL NPs tethered on Si wafer and AFM image of PLL NPs on Si wafer, and (d) ATR mode FTIR spectra of PVA and PVA-CA films.

Figure 3. C-V characteristics of (a) MIIS capacitor, (b) MIPIS capacitor

Figure 4., (a) ambipolar transfer characteristics of MIPIS transistor, (b) sweep excursion of transfer curve, and (c) ΔV_{th} of program-erase process of MIPIS transistor

Figure 5. (a) sweep excursion of transfer characteristics of PLL NPs indigo memory transistor on PET and (b) ΔV_{th} of program-erase process of PLL NPs indigo memory transistor on PET

Figure 1.

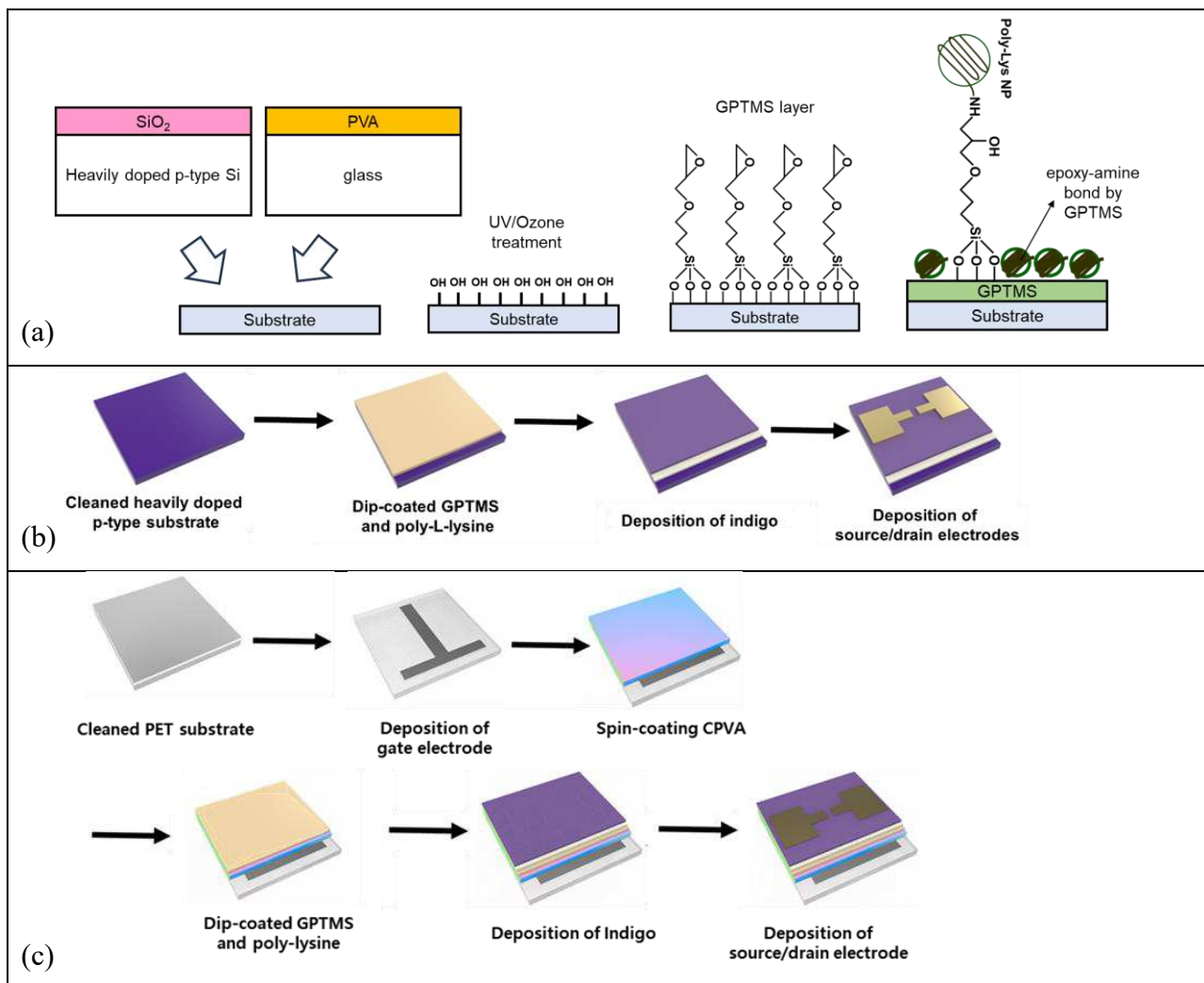


Figure 2.

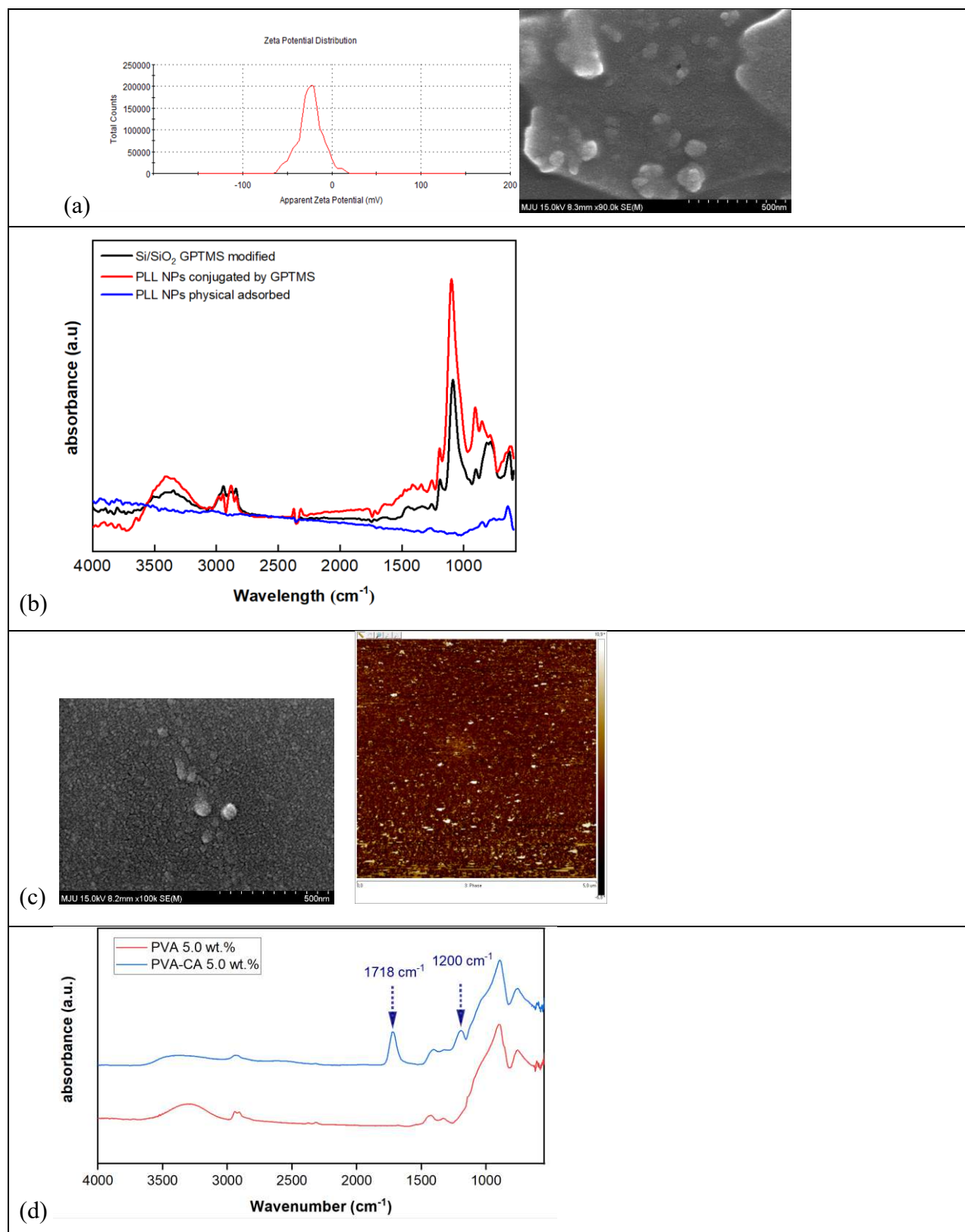


Figure 3.

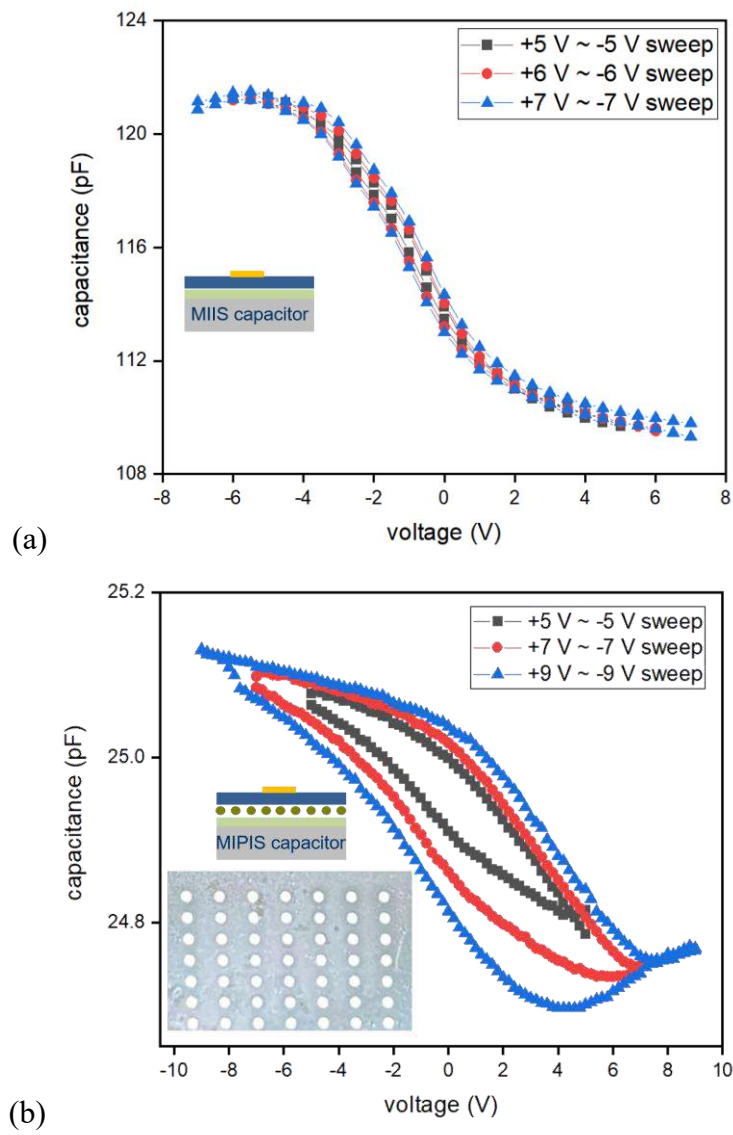


Figure 4.

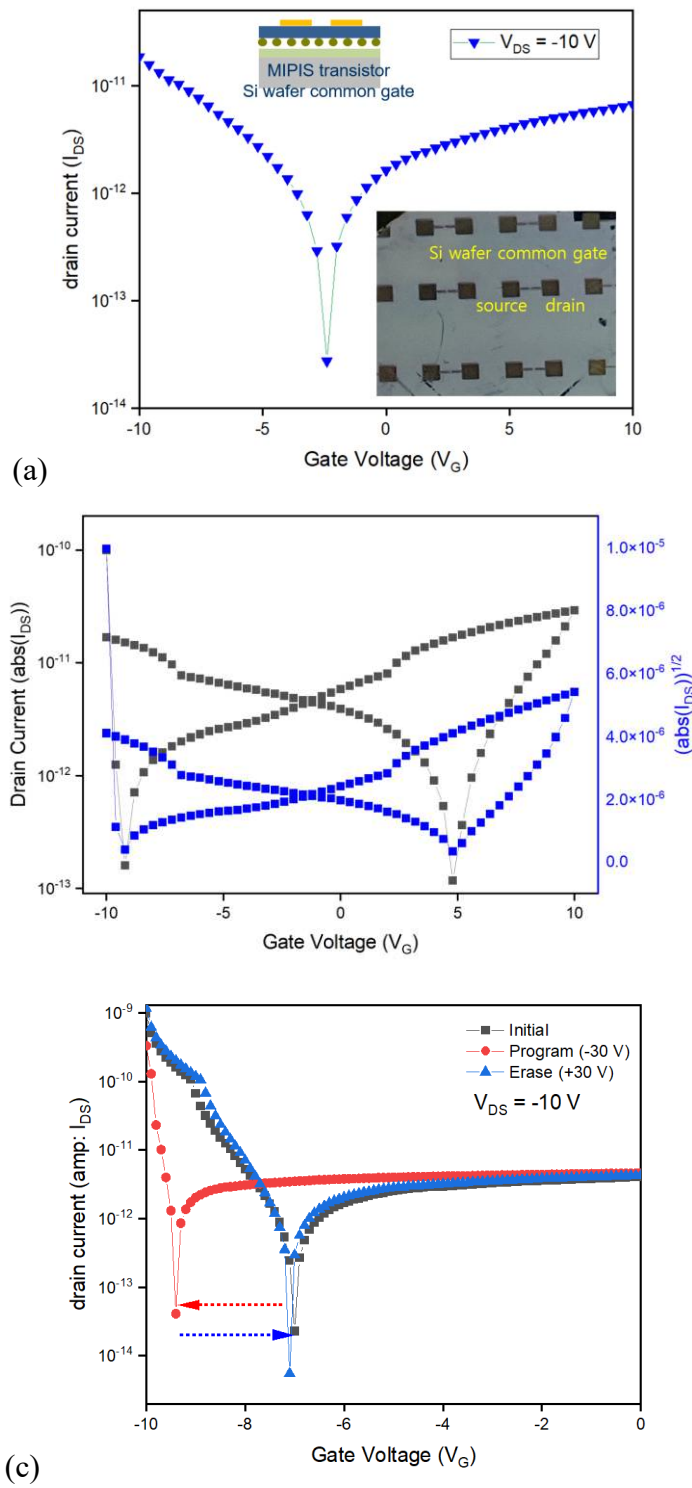


Figure 5.

