Research Square

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Unravelling the improvement in resistive switching characteristics of Cu/HfO 2 /AlN/Pt ReRAM devices

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Research Article

Keywords: Hafnium oxide, Aluminium nitride, Resistive switching, Conduction, Memory

Posted Date: September 12th, 2026

DOI: https://doi.org/10.21203/rs.3.rs-10863599/v1

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Additional Declarations: No competing interests reported.

Abstract

This work explores the resistive switching properties of sputter-deposited Cu/HfO_2/AlN/Pt memory device. The effect of an ultra-thin layer of AlN deposited between HfO_2 and the Pt interface was investigated in detail. We observed that the performance of the memory device improved in terms of endurance and retention. The stability of the device also improved due to the transformation of the AlN layer to an aluminium oxy-nitride (AlON) layer, which acts as a better heat sink, and the variation in SET/RESET voltages decreased. Formation/disruption of the oxygen vacancies related conducting channel (ionic filament) is accountable for the resistance state change in the device. In HRS, the current conduction mechanism is dominated by modified space charge limited current (SCLC), while Ohmic conduction is confirmed for charge transport in LRS. The device having AlN ultra-thin layer i.e. Cu/HfO_2/AlN/Pt, exhibits excellent endurance up to 4800 cycles and a long non-volatile retention (~ 10^4 s) along with a significant HRS to LRS ratio of ~ 10^2. This study suggests that addition of an ultra-thin layer of high thermal conductivity material (AlN) improve the resistive switching performance of HfO_2-based ReRAM devices, and could be a prominent technology in futuristic non-volatile memory applications.

1. Introduction

Nowadays, flash memories are silicon charge-based and the research is ongoing to scale down to fulfill the future memory storage demands, motivated by Moore's law [1–3]. Researchers faced restrictions during further miniaturization of the device dimensions due to physical limitations. In recent decades' researchers have explored different types of memory devices depending on the nature and properties of materials such as ferroelectric memories, ferromagnetic memories, etc. [4–6]. The phase change material (PCM) based resistive random access memory (PC-RAM) exhibits miniaturization problem below 40-nm node technology. Magnetic property-based random access memory (MRAM) operates at a higher current density. Nowadays, the resistive random access memory (ReRAM), which is based on resistive switching (RS) phenomenon, has attracted great attention for memory storage applications due to its high operating speed, low operating voltage, low power consumption, and excellent scalability along with a simple fabrication structure [7–10]. In ReRAM devices, the data is stored in distinct resistance states of the metal-insulator-metal (MIM) structure. The resistive switching is caused by cyclically and repeatedly changing from the high resistance state (HRS) to the low resistance state (LRS) by applying a biasing voltage between the top and bottom electrodes of the MIM structure [11–12].

The resistive switching property has been investigated for a number of materials such as metal nitrides (AlN, WN, CuN), transition metal oxides (TiO_2, ZnO, HfO_2), perovskite oxides ($BaTiO_3$, $SrTiO_3$), chalcogenides, etc. [13–20]. Transition metal oxides are the most promising candidate for ReRAM due to their excellent process compatibility with the conventional complementary metal oxide semiconductor (CMOS) technology [21]. Among the many transition metal oxides, hafnium oxide (HfO_2) has shown extraordinary electrical performance and is widely explored for ReRAM applications [22–23]. Hafnium

oxide, also known as hafnia, is a member of group IV-B metal oxides. In the last decade, it has emerged as a potential material due to its outstanding physical and chemical properties. It has a high potential barrier with respect to SiO_2 and is a highly stable material. HfO_2 is a wide band gap material with excellent features such as high dielectric constant, high melting point (-2700^oC), high chemical stability, good mechanical properties (hardness, elasticity) and high corrosion resistance, etc. [23–24]. These excellent features suggest that HfO_2 a suitable material for memory components sustaining high-temperature and harsh environment conditions such as nuclear power plants, chemical manufacturing industry, aerospace, oil refineries, etc. [25].

However, the HfO_2-based ReRAM devices face complications such as large reset current and slow reset time. Moreover, the TiN/HfO_x/Pt based device reported by Fang *et al.* faced problems of non-uniformity and decrease in ON/OFF ratio with temperature [16]. The performance of the non-volatile filamentary ReRAM device is widely affected by randomness in the formation and disruption of the conducting filament [26]. This can cause enormous variation in SET/REST voltages, hence degrading the performance of the memory device. The reason for the above-mentioned variation in SET/REST voltages is the low thermal conductivity of HfO_2. Many researchers overcome this issue by fabricating bi-layers structures such as TiO_2/ZnO, TiO_2/HfO_2, and that of $BiFeO_3$ composites [27–29]. Enhancement in the resistive switching properties of AlN-Al_2O_3 based bilayer structure were observed due to their high thermal conductivity [19]. Therefore, the RS properties of HfO_2 memory device might be improved further if we insert AlN layer below it.

In this study, we fabricated Cu/HfO_2/AlN/Pt structure and investigated the effect of additional layer of ultra-thin AlN on the resistive switching behaviour of HfO_2 thin film. The conduction mechanism responsible for resistive switching is also explained using a pictorial representation. Herein we proposed a capable and more convenient way to improve the bipolar RS performance of HfO_2-based ReRAMs.

2. Experimental details

The Cu/HfO_2/AlN/Pt MIM structure was fabricated using DC magnetron sputtering of 99.99% pure hafnium (Hf) and Aluminium (Al) targets (5 mm thick and a diameter of 50.6 mm). The left inset of Fig. 2 shows the pictorial representation of the Cu/HfO_2/AlN/Pt device. Ultrasonic bath containing a mixture of ethanol and acetone for 15 minutes was used to clean the Pt-coated silicon substrate. Before deposition, the hafnium (Hf) target was placed at a distance of 60 mm from the substrate inside the sputtering chamber. For the growth of high-quality HfO_2/AlN structure, the sputtering chamber was evacuated to a base pressure of $3x10^{-6}$ Torr using a turbo-molecular pump backed by a rotary pump. After it, the inert argon (Ar) gas was inserted into the deposition chamber through a mass flow controller (MKS) at a flow rate of 20 sccm for the development of the plasma, and thin film deposition started. The optimized sputtering parameters are illustrated in Table 1. To measure current-voltage (I-V) characteristics, the top

electrode (TE) of copper (Cu) with a 300 μm diameter was sputtered using a shadow mask at room temperature.

Table 1
The sputtering parameters used for the fabrication of HfO_2/AlN/Pt memory cell.

Sputtering Parameters		
Target	Aluminium	Hafnium
Substrates	Pt coated Si	AlN coated Pt
Base pressure	3×10^{-6} Torr	3×10^{-6} Torr
Working pressure	15 mTorr	10 mTorr
Deposition power	60 W	50 W
Deposition time	1 min	8 min
Substrate temperature	200 ºC	200 ºC
Target-substrate distance	6 cm	6 cm
Gas used	Ar:N_2(3:1)	Ar:O_2 (4:2)

An X-ray diffractometer (Bruker D8 advance) in θ-2θ geometry was performed to identify the phase formation of the as-grown HfO_2/AlN bilayer thin film. The cross-sectional image of the as-prepared HfO_2/AlN/Pt structure was examined by field-emission scanning electron microscopy (Carl-Zeiss Ultra plus, FESEM). Furthermore, the electrical characterization of the deposited device was determined using the Keithley 4200 SCS semiconductor characterization system. During electrical measurement, a biasing voltage was applied onto the top electrode, whereas the bottom electrode was connected to ground. To protect the device from the hard dielectric breakdown, a compliance current (CC) of 10 mA was also applied.

3. Result and discussion

Figure 1 reveals the XRD pattern of the as-prepared HfO_2/AlN/Pt structure at room temperature. The XRD pattern depicted an orthogonal structure of HfO_2 thin film with diffraction peaks at 30.15°, 69.10°, and 86.08° corresponding to (111), (231), and (402) planes, respectively (JCPDS ICDD No. 00-021-0904).

Moreover, diffraction peaks at 39.92 and 46.44° were also observed which are related the Pt substrate. Here, no diffraction peak for ultra-thin layer of AlN was detected. Inset of Fig. 1 depicts the cross-sectional FESEM image of as-deposited HfO_2/AlN/Pt/Ti/SiO_2/Si MIM structure. The cross-sectional image shows the formation of the good-quality interface between the active switching layer and the

bottom electrode. It can be seen that the thickness of the HfO_2 thin film and AlN ultra-thin film was measured approximately to be 90 nm and 10 nm, respectively.

Current-voltage (I-V) measurement was done as shown in Fig. 2 to study the bipolar resistive switching of the Cu/HfO_2/Pt and Cu/HfO_2/AlN/Pt memory devices. The fresh device founds almost electrically insulating (high resistance), therefore; a comparatively high biasing voltage was applied across the top and bottom electrodes.;

The right inset of Fig. 2 shows that at 3.5 V, the current is suddenly enhanced and the device resistance becomes, low; this is called the electroforming process. The biasing voltage sweeps in a sequence of 0 V → 1.5 V → 0 V → -1.5 V → 0 V. Positive bias voltage was used to achieve the SET condition, while negative voltage was applied to achieve the RESET state. In the case of Cu/HfO_2/AlN/Pt memory device, during the application of positive voltage sweep, at + 1.1 V the current is drastically increased, and the device transitions into a low resistance state from a high-resistance state. Thereafter, as the negative voltage sweep applied across the memory cell, at -0.9 V the current decreases very sharply and the low current state (RESET condition) occurs, as shown in Fig. 2. The SET and RESET processes for Cu/HfO_2/Pt structure were obtained at the voltages + 0.95 V and − 0.1.1 V, respectively. The above voltage-dependent resistance state arrangement approves the bipolar resistive switching behaviour of the HfO_2-based memory cell.

Now, to scrutinize the current conduction and resistive switching mechanism of the Cu/HfO_2/AlN/Pt memory device, the positive voltage region of I-V characteristics has been re-plotted with a double logarithmic scale as shown in Fig. 3 (a). The linear fitting for HRS and LRS was analysed and then compared with the power law relation ($I \propto V^n$). In HRS, on the basis of calculated slopes, the current conduction can be divided into three voltage regions. First, in the low voltage region ($V < 0.1$), the slope (S) is determined to be ~ 0.98 ($I \propto V$), which corresponds to the Ohmic regime in which the current conduction follows the equation ($J = qn_0\mu V/L$, where q is charge, and n_0 is density of thermally generated free electrons). In the voltage region ($0.1 < V < 0.4$), the slope is ~ 1.97 ($I \propto V^2$) which can be associated with Mott-Gurney law ($J = 9/8\varepsilon\mu V^2/L^3$, where ε is the free-space permittivity). In the high voltage region ($0.5 < V < 1.1$) slope is ~ 2.55, corresponding to the steep current increase region. The combination of these three charge transport behaviours may be explained by the modified space-charge limited conduction (SCLC) mechanism. Moreover, in LRS region the calculated slope was found to be ~ 1.03 ($I \propto V$) throughout the positive voltage, which corresponds to Ohm law. Further, to confirm the formation of an ionic conducting filament (due to oxygen vacancies) in the Cu/HfO_2/AlN/Pt memory device, the resistance vs. temperature (R-T) measurement was performed during LRS and HRS as shown in Fig. 3(b).

It reveals that resistance during LRS as well as HRS is decreasing with increasing temperature (250 K-450 K range), indicating the formation of ionic filament between TE and BE, and rules out the formation of Cu mettalic filament during LRS .

The bipolar resistive switching (RS) behaviour could be described by a localized conductive filamentary (CF) model. The previous reports on the resistive switching study of HfO_2-based devices suggested that a conducting filament formed across the top and bottom electrodes via grain boundaries or defects [30]. It is widely accepted that the conduction filament formed due to the alignment of oxide-related vacancies can act as charge traps. As we applied the positive voltage to the Cu top electrode of the device, the oxygen ions migrated towards TE, and leaving behind oxygen vacancies, which can be written as the following equation.

$HfO_2 \rightarrow HfO_{2-x} + x\,O^{2-} + xV_o^{2+}$ ..... (1)

These oxygen vacancies in the active switching medium (HfO_2 film) are filled by the trap-to-trap electron hopping process, and as a consequence, the conduction path is established between TE and BE. As a result, the resistance of the memory device is reduced (SET process) and the device comes to LRS from HRS. After it, as the negative bias voltage employed on the memory cell, the oxygen-related traps recombine with the oxygen ions, which break the filament due to joule-heating and the device comes back to HRS from LRS (RESET process) as shown in Fig. 4. During the creation and recombination of the oxygen vacancies, the AlN layer also plays a crucial role. When a positive bias voltage was imposed on the top Cu electrode, oxygen ions as well as oxygen vacancies were generated. Thus some oxygen ions of the switching layer react with the AlN layer, forms an ultra-thin aluminium oxy-nitride (AlON) layer between the HfO_2 film and ITO BE. The formation of the AlON layer can be written as follows [19, 31].

$AlN + ½\ O_2 \rightarrow AlON$ ..... (2)

Figure 4

Schematic diagram for conduction path formation/rupture of Cu/HfO_2/AlN/Pt memory cell

As a consequence, the formation of AlON ultra-thin film may increase the number of vacancies inside the switching layer and these vacancies serve as charge traps [32]. The AlON layer significantly influences the switching performance because of its high thermal conductivity. It provides an adequate heat sink during the RESET process [33].

Statistical distribution of SET and RESET voltages also carried out as shown in Fig. 5 [(a)-(b)]. It was observed that the SET voltage for Cu/HfO_2/Pt device [Fig. 5(a)] varies between 0.7 V to 1.4 V, whereas the RESET voltage ranges from − 0.6 V to -0.9 V. In the case of Cu/HfO_2/AlN/Pt device [Fig. 5(b)], SET and RESET voltages vary from 0.9 V to 1.2 V and − 0.75 V to -0.85 V, respectively. Variation in the SET/RESET voltages is narrow (in other words, better SET/RESET response) in Cu/HfO_2/AlN/Pt device as compared to Cu/HfO_2/Pt device. This can be considered that the RESET process occurs due to the breaking of filament from its weakest part at the highest temperature due to Joule-heating. In the case of Cu/HfO_2/Pt device, the weakest part of the conduction filament lies near the BE; therefore, during the

RESET process, the complete dissolution of the conducting filament would occur. When the highest temperature point inside the conductive filament reaches the critical temperature, the stability of the conductive filament becomes worse and is easily broken. It affects the next SET process because the subsequent filament formation occurs at different site, boosting the variation in switching voltage. However, insertion of the AlN layer maintains the point of highest temperature of the conducting filament, which may lie in the centre of the filament [34–35]. As a result, during the repeated SET process, the reformation of the filament is found to be more uniform, which leads to a smooth distribution of SET/RESET voltages compared to the memory devices without AlN layer. Hence, the addition of an ultra-thin layer of AlN over the BE serves a better reproducible, uniform and stable resistive switching performance. Figure 6: **(a)-(b)** Endurance and retention performance of the Cu/HfO_2/Pt memory cell, **(c)-(d)** Endurance and retention performance of the Cu/HfO_2/AlN/Pt ReRAM memory device.

The effect of AlN layer on the performance and reliability in terms of the endurance and retention properties was examined as shown in Fig. 6[(a)-(d)]. The DC pulses of + 1.5 V 100 ns and − 1.5 V 100 ns were applied to the HRS and LRS, respectively with 0.1 V read voltage. The memory device without AlN layer exhibits degradation after 2400 cycles as shown in Fig. 6(a), while Cu/HfO_2/AlN/Pt memory device [Fig. 6(b)] shows the endurance up to 4800 cycles.

It implies that the memory window becomes more stable after insertion of the AlN layer in HfO_2-based memory device. The non-volatile retention time of the device with the AlN layer (Cu/HfO_2/AlN/Pt) maintained up to 10^4 s as shown in Fig. 6(d), which is almost 100 times greater as compared to Cu/HfO_2/Pt memory device [Fig. 6(c)]. This improvement in endurance and retention may be due to the formation of a ceramic AlON layer beneath the HfO_2 active switching layer. AlON ultra-thin film gives better stability to the conducting channel formed and ruptured during the SET and RESET processes, respectively. The resistance ratio between HRS and LRS is found to be ~ 10^2, which is good enough to identify individual states.

4. Conclusion

In summary, the influence of aluminium nitride (AlN) ultra-thin layer on the resistive switching performance of hafnium oxide (HfO_2) has been thoroughly explored. The as-fabricated Cu/HfO_2/AlN/Pt device demonstrates the reproducible and bipolar resistive switching characteristics in very low voltage region. The binary resistance states i.e., high resistance state (HRS) and low resistance state (LRS) are facilitated by the formation and rupture of conducting path within HfO_2 active switching layer. Formation of a highly thermal conducting oxy-nitride (AlON) interfacial layer between the switching layer and bottom electrode plays a crucial role in enhancing the stable and reliable switching performance. The endurance (4800 cycles) and retention (10^4 s) analysis suggest that the Cu/HfO_2/AlN/Pt-based MIM structure has potential application in futuristic ReRAM device.

Declarations

Declaration of interest statement

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

The authors acknowledge the experimental support provided by Indian Institute of Technology Roorkee, India; Indian Institute of Technology Delhi, India; and C. C. S. Haryana Agriculture University, Hisar, Haryana, India.

Authorship contributions

Arvind Kumar: Writing original draft, Methodology, Formal analysis, Figure preparation. **Avinash Kumar:** Formal analysis, software, Data curation, **Mamta Rawat:** Figure preparation, Visualization, Formal analysis, **Mukesh Kumar:** Software, Data curation, Investigation, **Sanjeev Kumar:** Resources, Visualization, Investigation, **Narendra Singh:** Writing- review and editing, Conceptualization, Validation.

Funding

No funding was available for this work.

Data availability

All data that support the findings of this study are included in the article.

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Figures

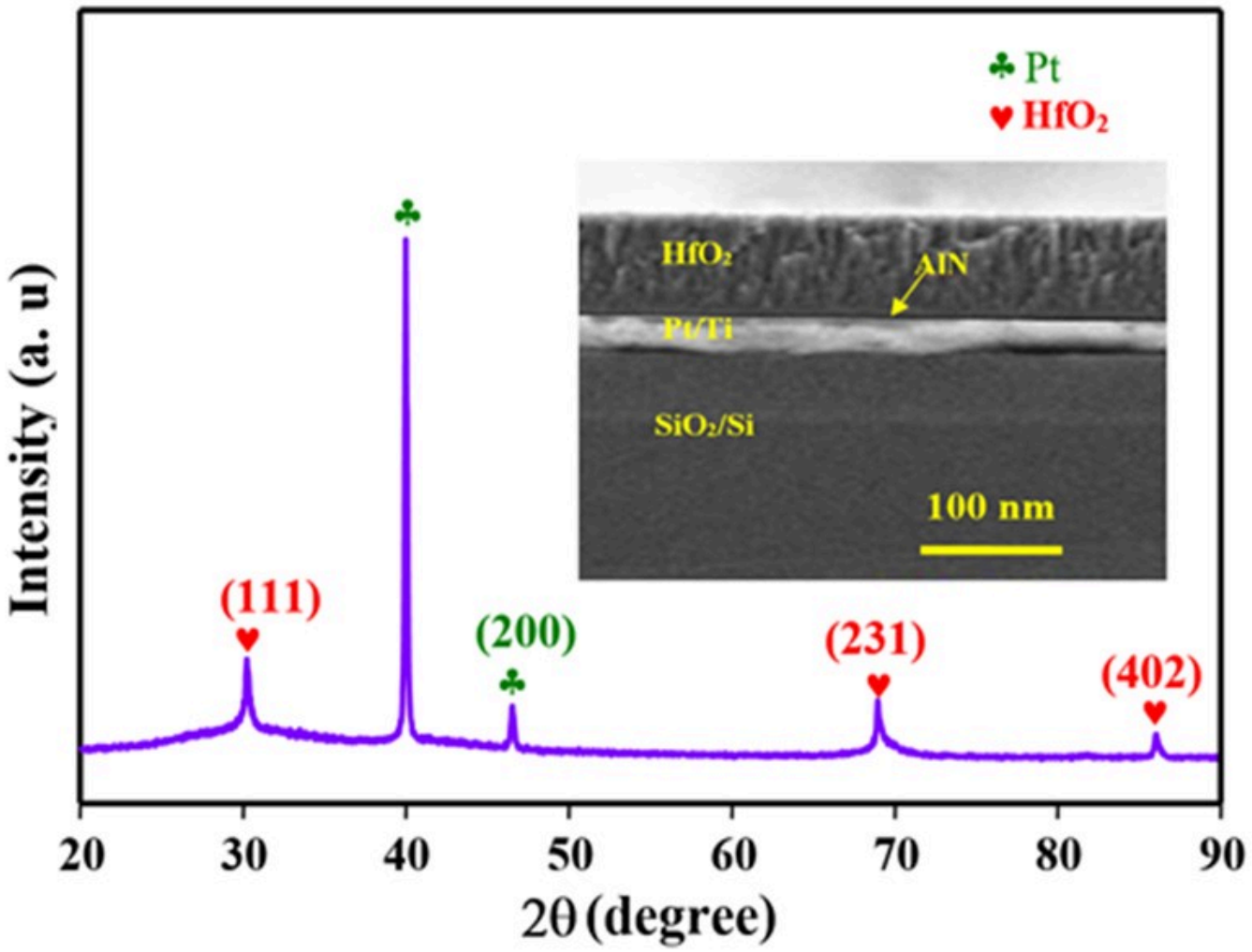


Figure 1

X-ray diffraction pattern of HfO_2/AlN/Pt structure, inset shows the cross-sectional Fe-SEM view of the HfO_2/AlN/Pt/Ti/SiO_2/Si Structure.

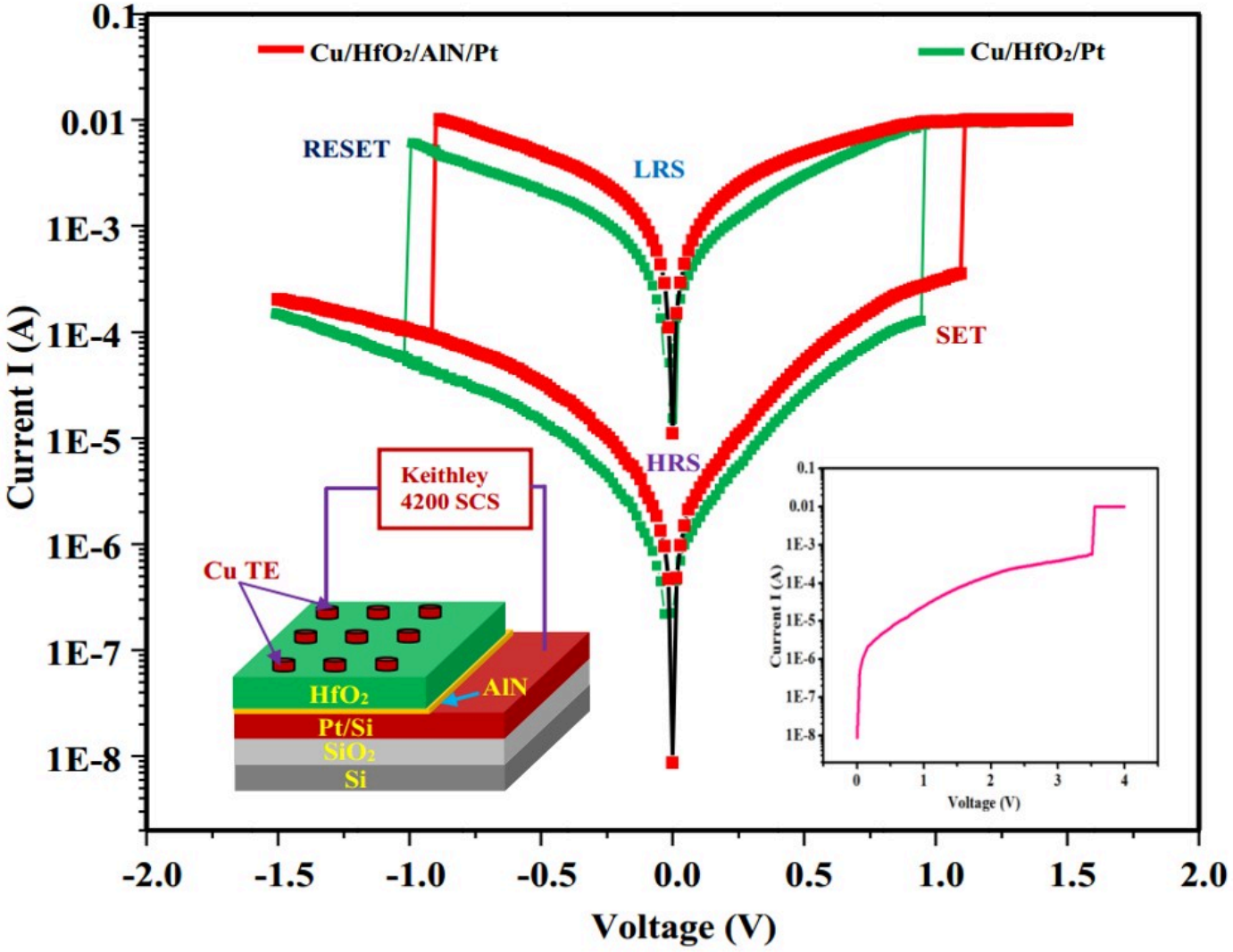


Figure 2

Current-voltage characteristics of Cu/HfO_2/AlN/Pt and Cu/HfO_2/Pt memory cells, the left inset shows the schematic view of ReRAM memory cell and the right inset shows irreversible electroforming process.

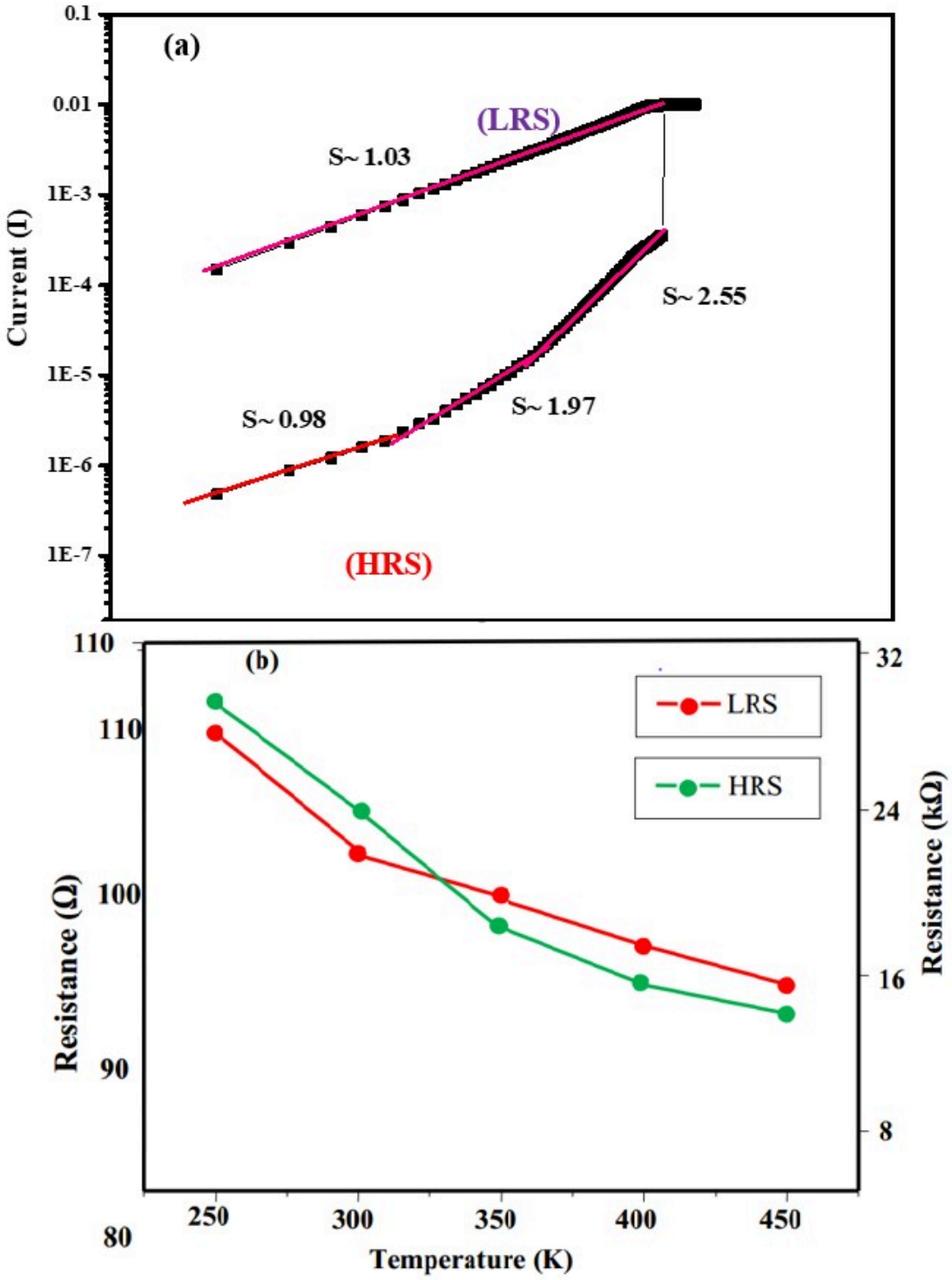


Figure 3

(a) The I-V characteristic curves on a double logarithmic scale and the linear fitting for HRS and LRS in the positive voltage region, **(b)** Resistance vs. Temperature curve for LRS and HRS.

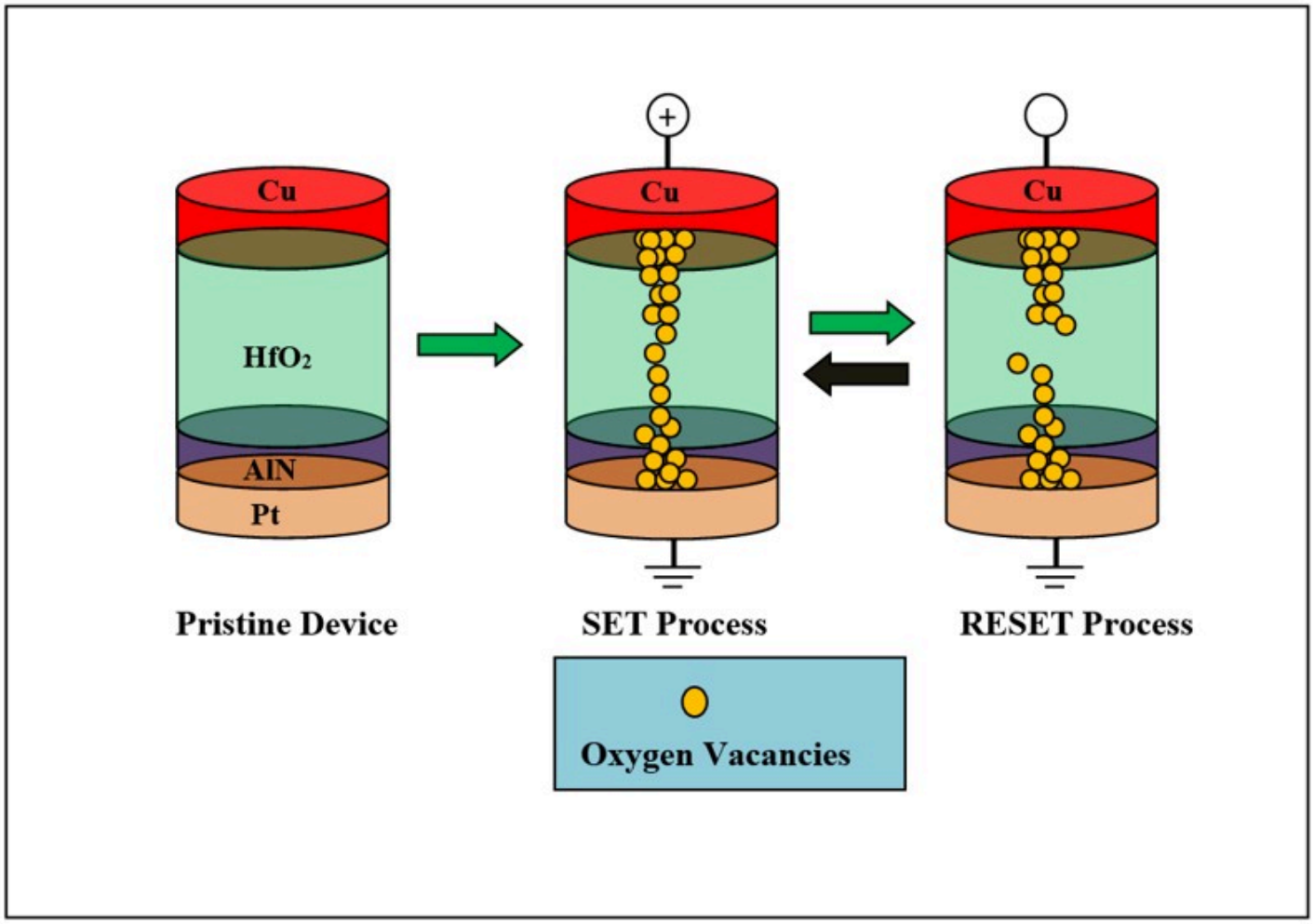


Figure 4

Schematic diagram for conduction path formation/rupture of Cu/HfO_2/AlN/Pt memory cell

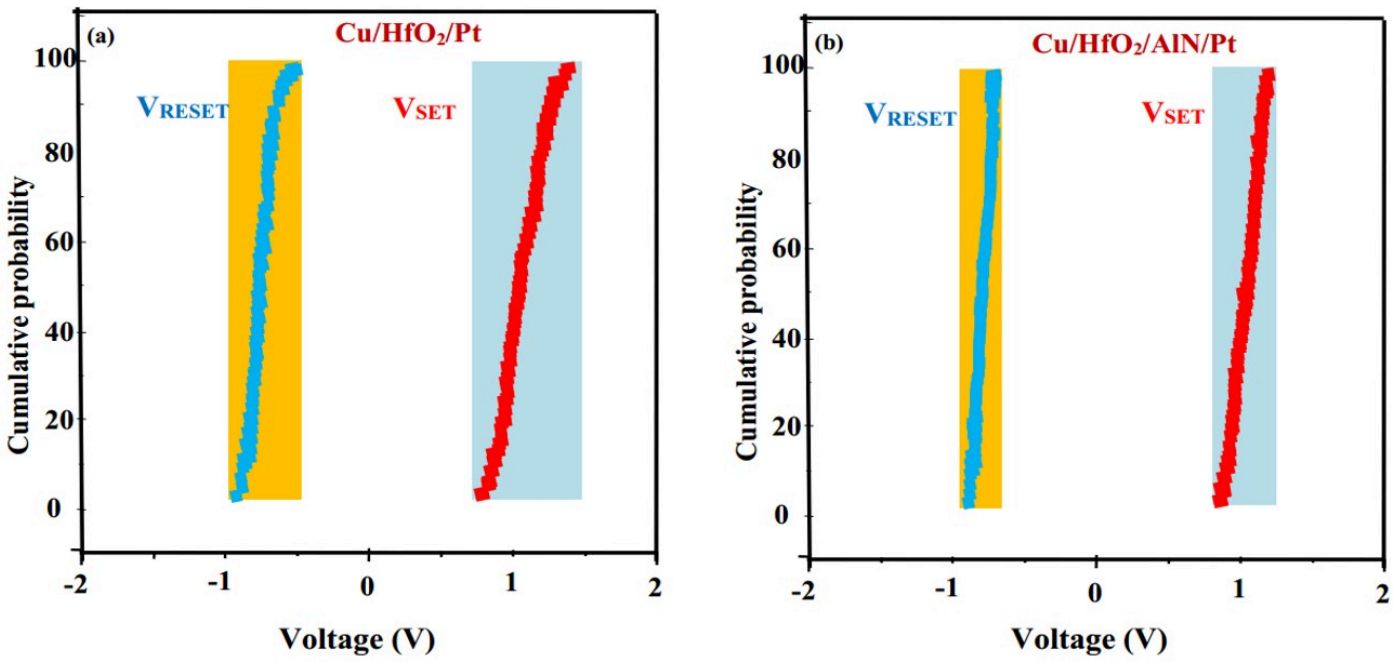


Figure 5

(**a)-(b)** Statistical distribution of SET voltage (V_{SET}) and RESET voltage (V_{RESET}) of Cu/HfO_2/Pt and Cu/HfO_2/AlN/Pt devices, respectively.

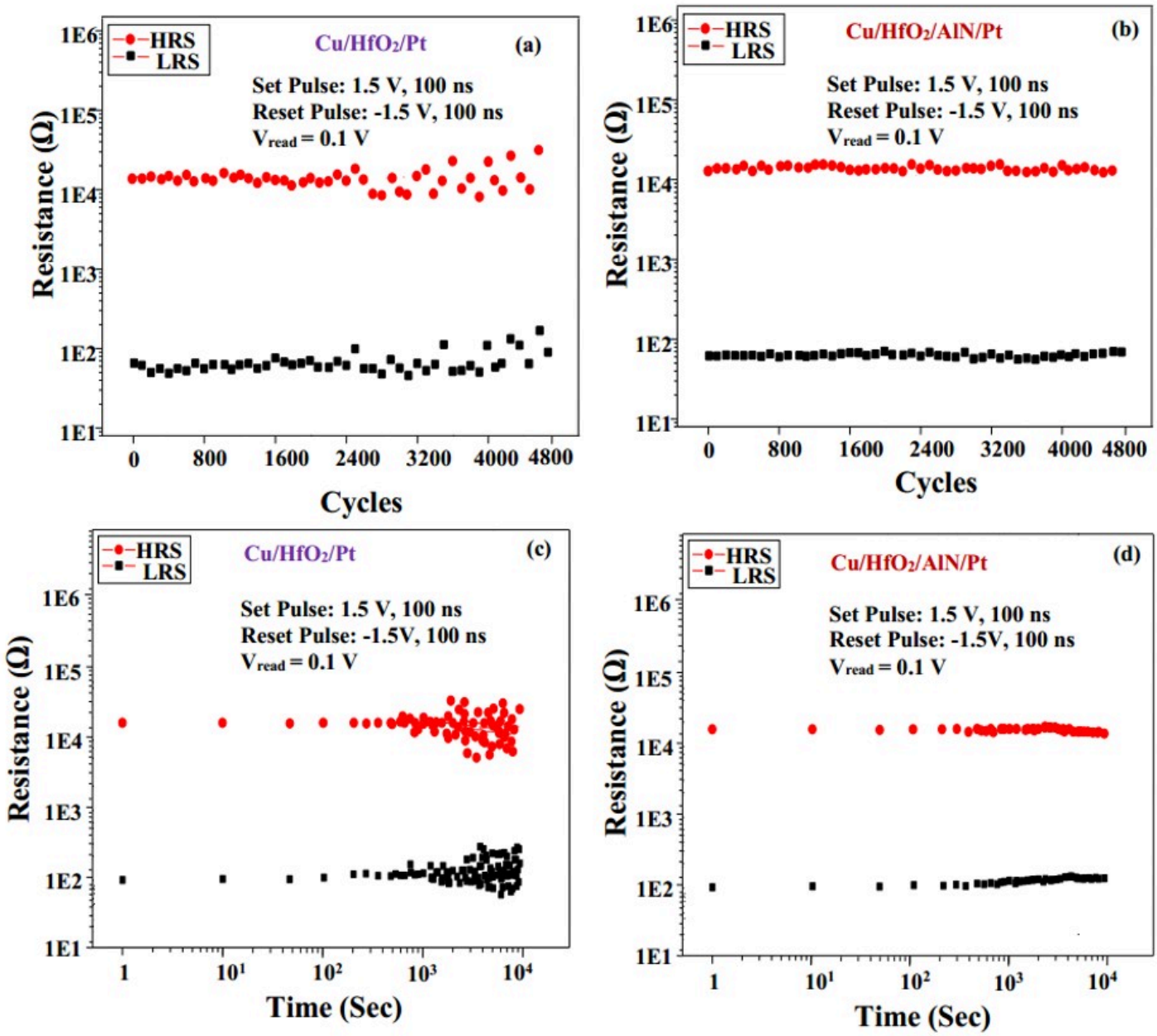


Figure 6

(a)-(b) Endurance and retention performance of the Cu/HfO_2/Pt memory cell, **(c)-(d)** Endurance and retention performance of the Cu/HfO_2/AlN/Pt ReRAM memory device.