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Analog/RF performance of Hexagonal Gate All Around Nanosheet FET with Spacer Engineering

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Abstract

The analog/RF performance of gate-all-around nanosheet field-effect transistor (GAA NSFET) with spacer dielectric engineering is investigated using three-dimensional TCAD tool. The analog/RF figures of merit of the GAA NSFET, including the intrinsic gain, transconductance generation factor, unity-current gain frequency ($\boldsymbol{f_T}$), transconductance-frequency product (TFP), gain-frequency product (GFP), and gain-transconductance-frequency product (GTFP), are evaluated for different single layer spacers and dual layer spacers. Employing single-layer $\mathbf{SiO_2}$ spacer as the reference baseline, which inherently exhibit favourable RF metrics with $\boldsymbol{f_T}$ of 540.19 GHz, TFP of 5,120 GHz/V, GFP of 32 THz, GTFP = 137 THz/V, and intrinsic voltage gain of 59.3 V/V owing to low dielectric permittivity and consequent parasitic capacitance minimization, this work demonstrates that strategic dual-layer heterostructure implementation enables application domain specific performance optimization transcending single-dielectric limitations. For RF and analog-centric applications, the proposed GAA NSFET with $\mathbf{SiO_2}$+$\mathbf{Si_3N_4}$ dual-spacer architecture manifests unprecedented enhancements: 31.25 % TFP elevation to 6720 GHz/V, 29.38 % GFP amplification to $\mathbf{4.14 \times 10^4}$ GHz, 19.71 % GTFP augmentation to $\mathbf{1.64 \times 10^5}$ GHz/V, and 7.55 % $\boldsymbol{f_T}$ improvement to 580.96 GHz, compared to single-layer $\mathbf{SiO_2}$. This performance superiority emanates from synergistic exploitation of the outer low-$\boldsymbol{k}$ $\mathbf{SiO_2}$ layer for fringing capacitance suppression and the inner moderate-$\boldsymbol{k}$ $\mathbf{Si_3N_4}$ layer for enhanced gate-channel electrostatic coupling, yielding optimized transconductance-to-capacitance ratios.

Keywords: Nanosheet FET, Spacer materials, Short channel effects, Unity gain frequency, Voltage gain

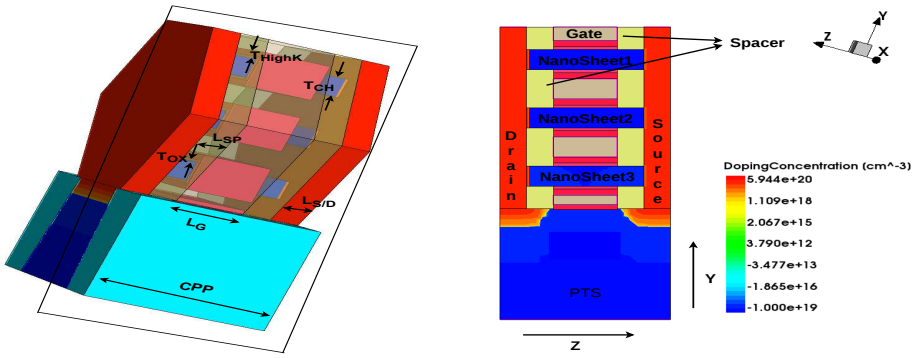
1 Introduction

The continuous scaling of devices has played an important role in the development of integrated circuit technology, resulting in important enhancements in power efficiency, speed, and device density. However, as MOSFET sizes shrink underneath the sub-5 nm regime, conventional structures such as double-gate MOSFETs (DG MOSFETs), planar MOSFETs, and FinFETs encounter fundamental electrostatic and fabrication related challenges that progressively reduce their behaviour [1, 5]. The scaling induced reduction in gate control exacerbates short channel effects (SCEs), including drain induced barrier lowering (DIBL), threshold voltage instability, and increased OFF currents, thereby adversely affecting power dissipation and switching characteristics [2, 3]. Although DG MOSFETs provide enhanced electrostatic control over MOSFETs, their effectiveness reduces at extreme scaling limits owing to insufficient gate control [4, 6]. Among these unconventional designs, FinFETs have developed as the leading technology for sub-10 nm nodes. As FinFET dimensions approach the 5 nm regime, electrostatic scaling laws that hold at larger geometries begin to break down, leading to severe SCEs, including DIBL and reduced subthreshold swing (SS) [7]. Besides, parasitic capacitances and resistances increasingly dominate MOSFET performance, resulting in decreased ON current and diminished switching efficiency [8].

Nanosheet FET (NSFET), based on a gate all around (GAA) structure, offer superior gate to channel coupling by fully enclosing the channel, thereby offering enhanced control over SCEs compared to planar and Fin-based FETs [9, 10]. In addition to the benefits of the GAA architecture, spacer engineering plays an important role in MOSFET optimization [11, 12]. The spacer region governs gate to source/drain parasitic capacitances, fringing fields, and the trade-off between leakage current (I_{OFF}) and drive current (I_{ON}) [15, 16]. Consequently, NSFETs with spacer engineering, offer a scalable pathway beyond FinFETs, provide an improved electrostatic control and enhanced characteristics for next generation CMOS technologies [13, 14]. This leakage degrades long term device reliability and power efficiency, thereby necessitating careful co-optimization of material characteristics and MOSFET structure [17, 18]. Effective architecture process integration is therefore important to reduce OFF currents without compromising RF performance or drive capability [19, 20].

The analog/RF behaviour optimization has become equally critical in deeply scaled GAA NSFETs. High frequency behaviour is strongly governed by gate capacitance (C_{gg}), transconductance (g_m) and parasitic components, which directly influence important figures-of-merit such as gain bandwidth metrics and cut-off frequency (f_T) [21]. Performance improvement schemes include low-k, high-k, metal gate stacks for reduced equivalent oxide thickness (EOT), or dual-layer spacers for fringing capacitance suppression, and nanosheet dimension optimization to maximize the g_m/C_{gg} ratio.

Motivated by the essential to optimize analog/RF behaviour, this work demonstrates an exhaustive analysis of analog/RF characteristics in the GAA NSFET employing single and dual layer spacer structures. A range of hybrid dielectric combinations in the GAA NSFET, including HfO_2/SiO_2, HfO_2/Si_3N_4, Si_3N_4/SiO_2, Si_3N_4/HfO_2, SiO_2/Si_3N_4, and SiO_2/HfO_2, is systematically assessed to exploit



(a) (b)

Fig. 1: (a) Three-dimensional schematic of the GAA NSFET with spacer engineering (b) Cross-sectional view in the Z-direction with T_{BO} = 5 nm.

complementary dielectric characteristics for optimal trade-offs among parasitic capacitance, electrostatic control, drive capability, and mechanical stability [22].

The GAA NSFET performance is evaluated using key analog metrics, including output conductance (g_d), g_m, transconductance generation factor (TGF = g_m/I_D), intrinsic gain (g_m/g_d), and early voltage ($V_E = I_D/g_d$). RF performance is characterized through transconductance frequency product (TFP = $(g_m/I_D)f_T$), f_T, gain transconductance frequency product (GTFP = $(g_m/g_d)(g_m/I_D)f_T$), and gain frequency product (GFP = $(g_m/g_d)f_T$), providing a unified framework to assess the impact of spacer engineering on RF frequency operation.

2 Device Architecture and Simulation Setup

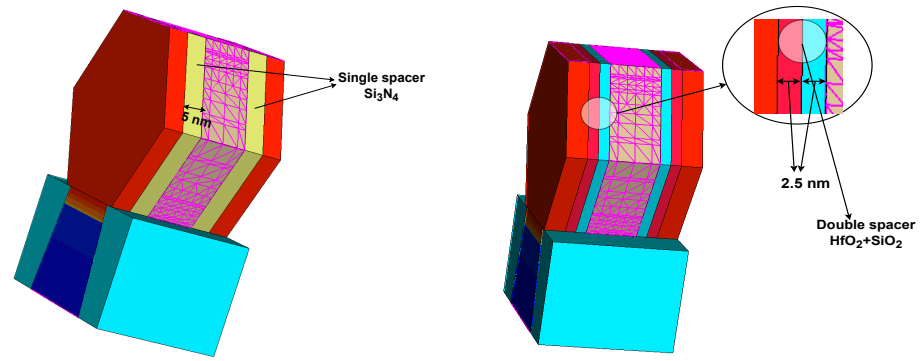
2.1 Device Structure

A three channel hexagonal GAA NSFET is designed and analysed using the Sentaurus Technology Computer Aided Design (TCAD) platform [23], as demonstrated in Fig. 1. The device architecture contains key geometrical parameters, including metal gate, source/drain regions, stacked nanosheets, dielectric spacers, high-k gate dielectric, interfacial oxide, a bottom isolation layer, and punch-through stopper. The material parameters and geometrical dimensions are illustrated in Table 1. The effective channel width is assessed to be approximately 58 nm, calculated as $2(T_{CH} + W_{CH})$. The gate stack contains of a dual layer dielectric comprising 1.5 nm HfO_2 (high-k layer) and 0.7 nm SiO_2 (interfacial layer), resulting an equivalent EOT of 2.2 nm.

The analysis begins with a systematic evaluation of single spacer structures employing dielectric materials spanning high (HfO_2) permittivity, moderate (Si_3N_4), and low (SiO_2), as demonstrated in Fig. 2a. Each dielectric is evaluated to quantify its effect on MOSFET behaviour. Dual spacer structures, as demonstrated in Fig. 2b, wherein

Table 1: Key parameters are used in the GAA NSFET simulations

S.No.	Quantity	Symbol	Value
1	Channel Thickness	T_{CH}	5 nm
2	Gate Length	L_{G}	12 nm
3	Nanosheet Width	W_{CH}	24 nm
4	Interfacial Oxide Thickness	T_{IOX}	0.7 nm
5	High-k Thickness	T_{highk}	1.5 nm
6	Inner Spacer Length	L_{IS}	5 nm
7	Source Doping	N_{S}	3×10^{20} cm^{-3}
8	Drain Doping	N_{D}	3×10^{20} cm^{-3}
9	Punchthrough Stopper Doping	N_{PTS}	1×10^{19} cm^{-3}
10	Contacted Poly Pitch	CPP	32 nm
11	Source/Drain Length	$L_{\mathrm{S/D}}$	5 nm
12	Spacer Length	L_{SP}	5 nm
13	Gate Workfunction	WF	4.8 eV



(a) (b)

Fig. 2: (a) GAA NSFET with single spacer material Si_3N_4. (b) GAA NSFET with double spacer material HfO_2+SiO_2.

two dielectric materials are strategically joined to exploit complementary electrical characteristics.

2.2 Simulation Setup

Electrical behaviour of the NSFET is simulated using Synopsys Sentaurus TCAD to predict MOSFET performance [25]. Carrier recombination effects are included via Shockley Read Hall and direct band to band recombination models. High field transport is estimated using the HighFieldSaturation (GradQuasiFermi) model. Carrier mobility degradation owing to surface and bulk scattering is modeled using the Lombardi (Enormal) models and Philips Unified Mobility (PhuMob). Band structure

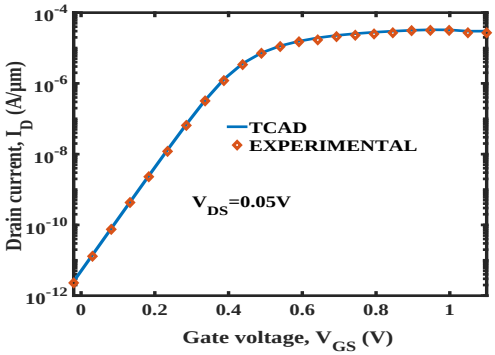


Fig. 3: Calibration of NSFET against the experimental data from [24].

modifications in heavily doped regions are captures using the BandGapNarrowing (OldSlotboom) model. Inversion layer mobility refinement is attained using the Enormal (IALMob) model. Nonlocal carrier transport phenomena are modeled using the nonlocal band to band tunneling model with the NonlocalPath option. Quantum confinement effects are considered through the Density Gradient model. The resulting simulated data show strong agreement with experimental results [24], thereby validating the simulation methodology, as illustarted in Fig. 3.

3 Results and Discussion

3.1 Performance analysis of GAA NSFET with single layer spacer

Fig. 4 shows the transfer characteristics (I_D-V_{GS}) along with the g_m at associated $V_{\mathrm{DS}} = 0.7$ V, whereas Fig. 5 shows the output characteristics (I_D-V_{DS}) and the corresponding g_d at $V_{\mathrm{GS}} = 0.7$ V. The GAA NSFET with high-k dielectric HfO_2 shows the strongest gate to channel electrostatic coupling, enabling enhanced MOSFET control and enhanced channel modulation.GAA NSFET employing SiO_2 and Si_3N_4 spacers show intermediate behaviour, where their moderate dielectric constants offer a balanced trade-off between reduced fringing parasitic capacitance and effective gate modulation. The GAA NSFET with spacer materials exhibit a strong dependence of gate capacitance, as illustrated in Fig. 6. The device with HfO_2 spacer demonstrates the largest C_{GG}. This behaviour is primarily governed by parasitic fringing capacitances between the gate and drain/source regions, which increase with spacer permittivity.

The device employing SiO_2 spacer achieves the highest f_T, exceeding 540.19 GHz at $V_{\mathrm{GS}} = 0.7$ V, owing to minimal parasitic coupling that reduces total gate capacitance and enhances carrier transport speed. As demonstrated in Fig. 7, the GAA NSFET with intermediate-k Si_3N_4 spacer illustrates moderate RF performance, attaining an f_T of 478.6 GHz, which reflects a balanced trade-off between increased capacitive loading and enhanced electrostatic modulation. In contrast, device with HfO_2 spacer shows the lowest cut-off frequency 368.13 GHz, despite provide higher drive current

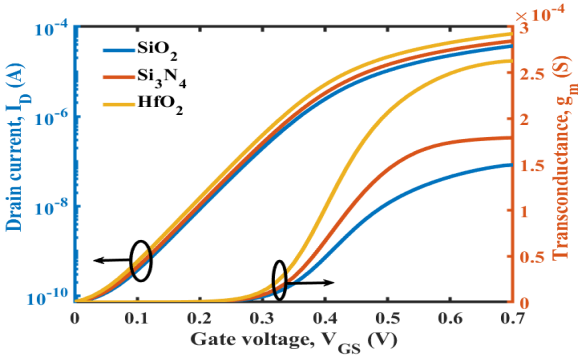


Fig. 4: Transfer characteristics and g_m of the GAA NSFET with various spacer materials at $V_{\mathrm{DS}} = 0.7$ V.

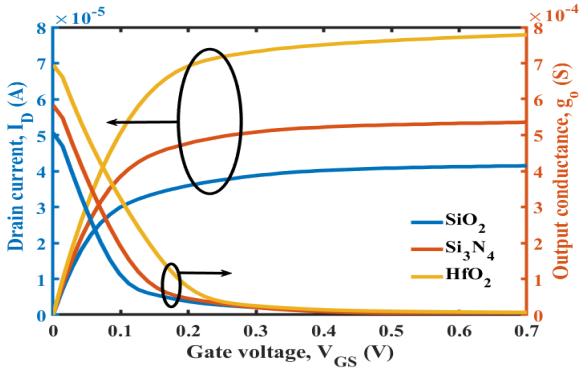


Fig. 5: Drain characteristics and g_d of the GAA NSFET with various spacer materials at $V_{\mathrm{GS}} = 0.7$ V.

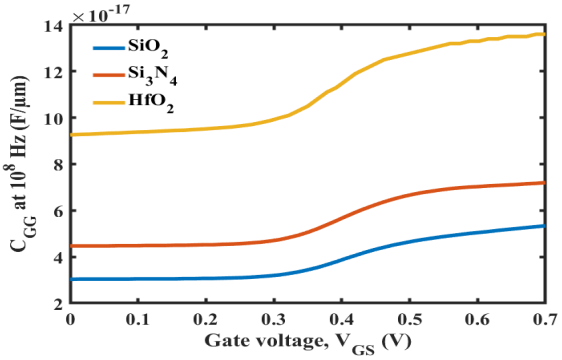


Fig. 6: Gate capacitance at 10^8 Hz of the GAA NSFET with different spacer materials at $V_{\mathrm{GS}} = 0.7$ V.

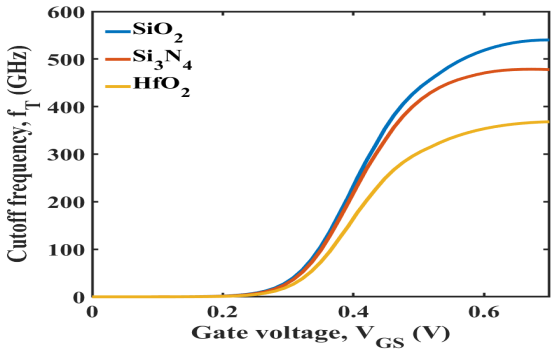


Fig. 7: Cutoff frequency of the GAA NSFET with different spacer materials.

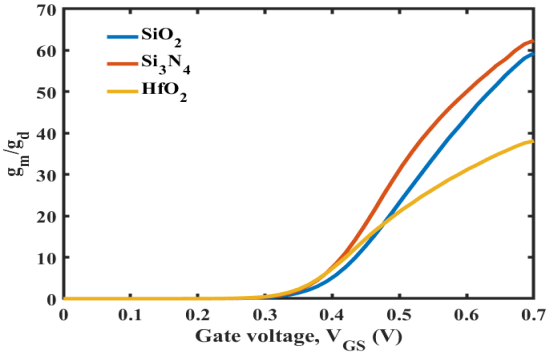


Fig. 8: Intrinsic voltage gain of the GAA NSFET with different spacer materials.

and better electrostatic control, primarily owing to increased fringing capacitances associated with their high dielectric permittivity.

The g_m/g_d of the GAA NSFET shows a strong dependence on spacer dielectric behaviour, reflecting the trade-off between minimizing g_d and maximizing g_m. The device with Si_3N_4 spacer attains the highest g_m/g_d (exceeding 62.40 at $V_{GS} = 0.7$ V) by maintaining high g_m while effectively reducing g_d. As illustrated in Fig. 8, the device with SiO_2 spacer also illustrate favourable g_m/g_d characteristics, though slightly lower than that of Si_3N_4. In contrast, the GAA NSFET employing HfO_2 spacer shows the lowest intrinsic gain, primarily owing to increased parasitic capacitances that limit voltage amplification and elevate g_d. These results show that low to moderate-k dielectrics are better appropriate for analog/RF applications demanding high intrinsic gain. While high-k materials enhance drive current, they tend to degrade g_m/g_d due to increased parasitic effects. Consequently, spacer configurations that maintain high g_m while suppressing g_d are most effective for achieving superior voltage amplification.

The TGF of GAA NSFET shows strong sensitivity to spacer dielectric behaviour, with a sharp peak near $V_{GS} = 0.2$ V, reaching values of nearly 34.5 V^{-1}. The device

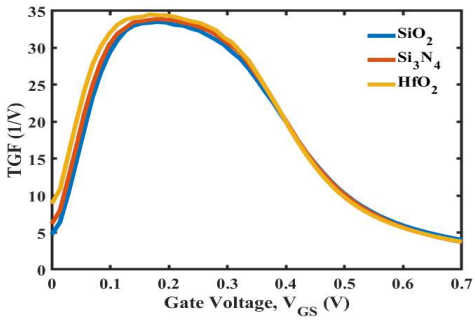


Fig. 9: TGF of the GAA NSFET with different spacer materials at $V_{\mathrm{GS}} = 0.7$ V.

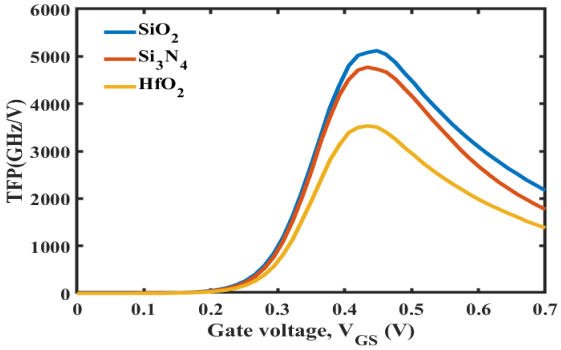


Fig. 10: TFP of the GAA NSFET with different spacer materials.

incorporating Si_3N_4, SiO_2, and HfO_2 spacers maintain relatively high TGF over a extensive range of gate biases, representing their ability to sustain substantial g_m even at decreased I_D. As demonstrated in Fig. 9, these results exhibit that moderate to high permittivity spacers offer an effective balance between current efficiency and electrostatic control, making them well appropriate for low power analog/RF applications.

The TFP of GAA NSFET exhibits an inverse dependence on the spacer dielectric constant, highlighting the importance of dielectric selection for high-frequency performance. As shown in Fig. 10, the GAA NSFET employing low-k spacers such as SiO_2 achieve the highest TFP values, exceeding approximately 5120 GHz/V. In contrast, device with HfO_2 spacer results in reduced TFP due to increased parasitic capacitance.

The combined effects of g_m/g_d and operational speed show a strong dependence on spacer dielectric properties, as illustrated in Fig. 11. The results reveal an inverse relationship between GFP and dielectric constant: device with SiO_2 spacer achieves the highest GFP, while those employing high-k (HfO_2) spacer exhibits the lowest performance. These findings confirm that low-k spacers are more suitable for applications

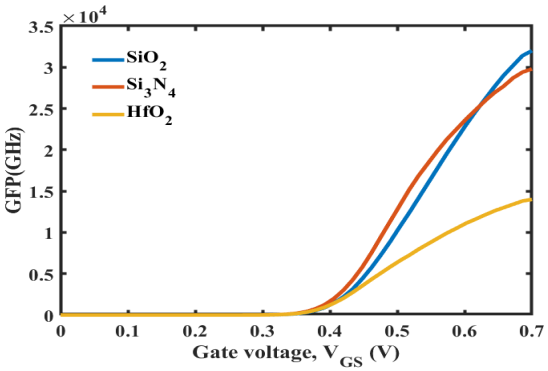


Fig. 11: GFP of the GAA NSFET with different spacer materials.

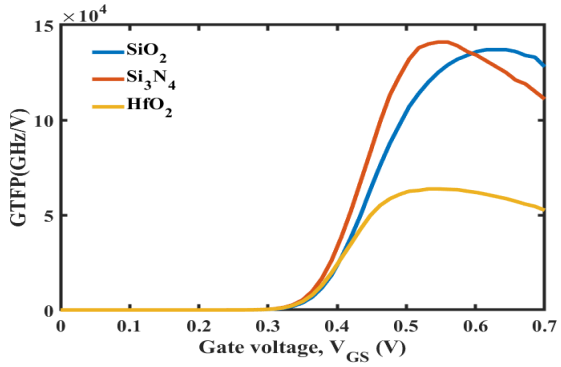


Fig. 12: GTFP of the GAA NSFET with different spacer materials.

requiring a balance between moderate gain and high-speed operation in the GAA NSFET.

Fig. 12 presents GTFP of the GAA NSFET with different spacer materials. The results show a the device with Si_3N_4 achieving the highest peak GTFP, outperforming SiO_2, and HfO_2 spacers. These findings indicate that intermediate-k spacer materials provide the best balance among composite performance metrics such as GTFP, making them well suited for high-performance, linear RF applications.

The voltage gain (A_V) and current gain (A_I) of the GAA NSFET with different single-layer spacer materials, shown in Fig. 13. Both A_V and A_I decrease with increasing frequency due to the growing influence of parasitic capacitances. The device with Si_3N_4 and SiO_2 spacers provide superior voltage gain in the mid-frequency range (10^9-10^{10} Hz), offering a favourable balance between electrostatic control and parasitic effects. Although device with SiO_2 spacer minimizes parasitic capacitance, they exhibit slightly lower mid-band voltage gain due to weaker fringe-field coupling, while maintaining higher A_I at elevated frequencies. Overall, these results indicate that

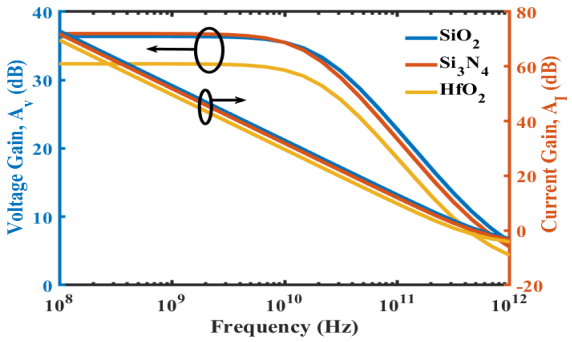


Fig. 13: The A_V and A_I of the GAA NSFET with different spacer materials.

device with Si_3N_4 spacer deliver the best RF gain performance, whereas high-k spacer degrades high-frequency operation due to increased gate capacitance.

3.2 Performance analysis of the GAA NSFET with dual layer spacer

Fig. 14 and 15 present the transfer and drain characteristics of the GAA NSFET with different dual-layer spacer configurations, evaluated at V_{DS} = 0.7 V and V_{GS} = 0.7 V, respectively. Among the structures, configurations such as the device with Si_3N_4+HfO_2 and SiO_2+HfO_2 achieve a favourable trade-off between I_D, g_m, and electrostatic integrity. This improved performance arises from the strategic placement of low-k materials near the source/drain regions, which suppress parasitic capacitances, while high-k dielectrics positioned adjacent to the gate, enhance field penetration and strengthen channel modulation. In contrast, configurations such as the device with HfO_2+SiO_2 and Si_3N_4+SiO_2 exhibit reduced g_m and g_d due to weaker gate to channel coupling and limited carrier confinement. These results highlight the important role of spacer material ordering in balancing parasitic effects and electrostatic control for optimized NSFET behaviour.

The dependence of total gate capacitance on V_{GS} of the GAA NSFET, shown in Fig. 16, characterizes the capacitive behaviour of dual-layer spacer structures at 10^8 Hz. The inner spacer dielectric plays a dominant role in determining C_{GG}: device configurations with a high-k material such as HfO_2 in the inner layer exhibit the highest capacitance, whereas those with low-k materials such as SiO_2 show the lowest values, primarily due to differences in fringing capacitance.

As shown in Fig. 17, the f_T characteristics of the GAA NSFET with dual-layer spacers highlight the critical role of spacer material placement near the source/drain regions. Among the configurations studied, the device with SiO_2+Si_3N_4 structure achieves the highest peak f_T of 580.96 GHz, significantly outperforming other combinations. In contrast, the device employing an HfO_2 outer layer exhibit degraded RF performance due to increased parasitic capacitances. This comparison indicates that a low-k outer spacer, such as SiO_2, effectively reduces fringing capacitance,

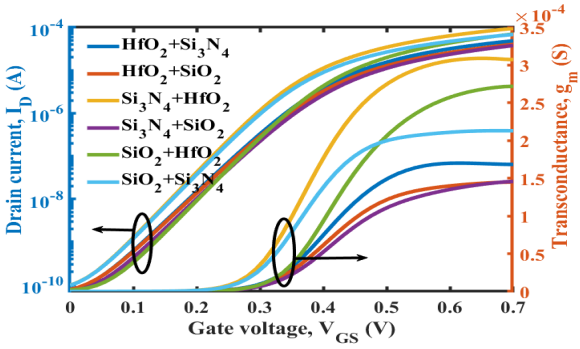


Fig. 14: Transfer characteristics and transconductance of the GAA NSFET with dual-layer spacer materials at $V_{\mathrm{DS}} = 0.7$ V.

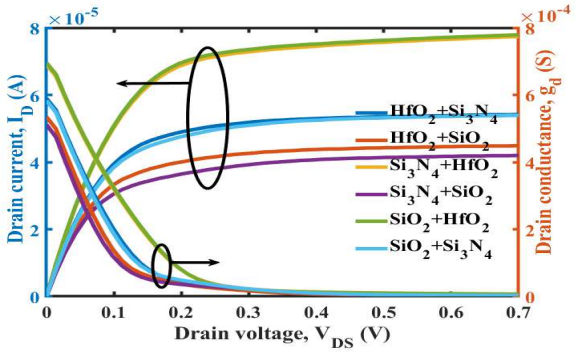


Fig. 15: Drain characteristics and output conductance of the GAA NSFET with dual-layer spacer materials at $V_{\mathrm{GS}} = 0.7$ V.

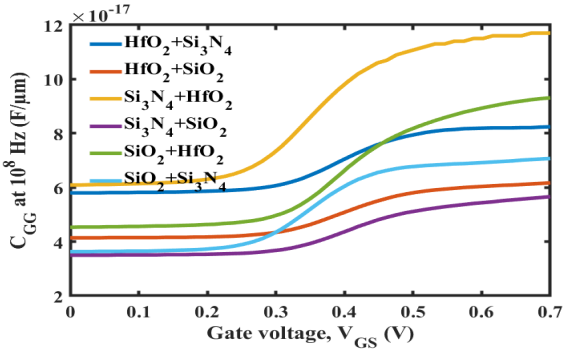


Fig. 16: Gate capacitance at 10^8 Hz of the GAA NSFET with dual-layer spacer materials at $V_{\mathrm{DS}} = 0.7$ V.

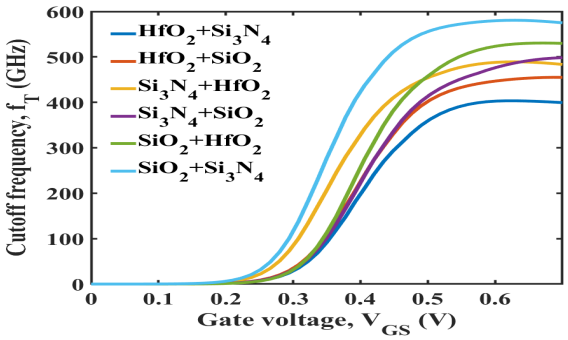


Fig. 17: Cutoff frequency of the GAA NSFET with dual-layer spacer materials.

which is a primary limitation for high-speed operation. These results establish a clear design guideline, to maximize f_T in the GAA NSFET, the spacer material near the drain/source extensions should have a low dielectric constant.

The g_m/g_d of the GAA NSFET with dual layer spacer structures demonstrates a strong dependence on both spacer positioning and dielectric constant, reflecting the combined effects of g_d suppression and g_m enhancement, as demonstrated in Fig. 18. the NSFET with a moderate-k inner spacer, specifically those including Si_3N_4, show superior g_m/g_d owing to effective mitigation of channel length modulation and improved electrostatic control. Among all configurations, the device with SiO_2+Si_3N_4 structure achieves the highest intrinsic gain, benefiting from strong channel modulation provided by the moderate-k inner layer. In contrast, configurations such as the device with Si_3N_4+HfO_2 and SiO_2+HfO_2 exhibit lower g_m/g_d, primarily due to increased parasitic coupling associated with the high-k HfO_2 layer. These results indicate that dual-layer spacer architectures combining a low-k outer layer with a moderate-k inner layer are most effective for maximizing intrinsic gain in the GAA NSFET.

Fig. 19 presents the TGF of the GAA NSFET for various dual-layer spacer configurations, highlighting their suitability for low-power analog applications. The results show that the NSFET with Si_3N_4+HfO_2 configuration achieves the highest peak TGF of approximately 36.7 V^{-1}, indicating superior current efficiency. This enhancement arises from the complementary roles of the two layers, the inner high-k HfO_2 improves gate electrostatic control, increasing the g_m/I_D ratio in moderate and weak inversion, while the outer low-k SiO_2 decreases parasitic coupling and preserves stability. Overall, the low-k/high-k hetero-structure offers an effective pathway for enhancing power efficiency in ultra-low power analog/RF applications.

Fig. 20 demonstrates the TFP of the GAA NSFET employing dual layer spacers, providing important perceptions into RF behaviour. Among all structures, the GAA NSFET with SiO_2+Si_3N_4 attains the highest peak TFP of approximately 6720 GHz/V, obviously outperforming the others. This improvement is mainly driven by

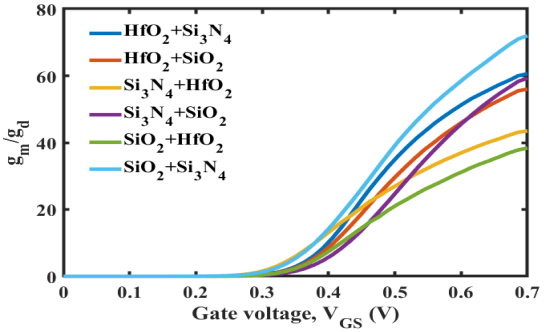


Fig. 18: Intrinsic gain of the GAA NSFET with dual-layer spacer materials.

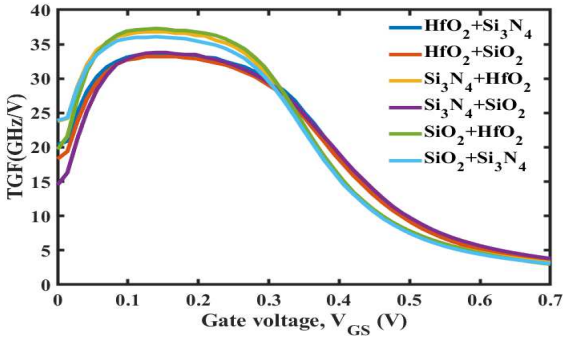


Fig. 19: TGF of the GAA NSFET with dual-layer spacer materials at $V_{\mathrm{DS}} = 0.7$ V.

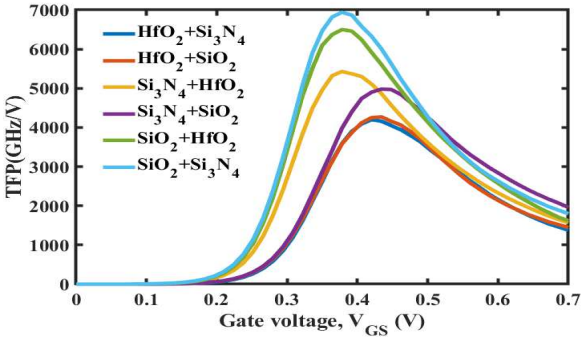


Fig. 20: TFP of the GAA NSFET with dual-layer spacer materials.

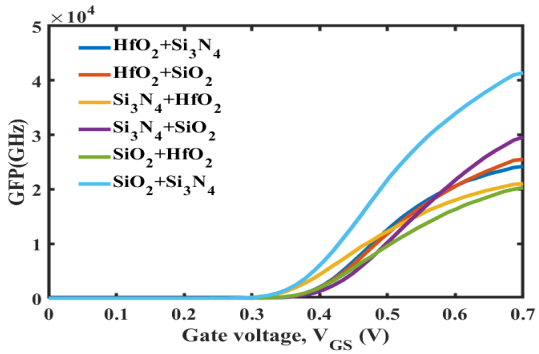


Fig. 21: GFP of the GAA NSFET with dual-layer spacer materials.

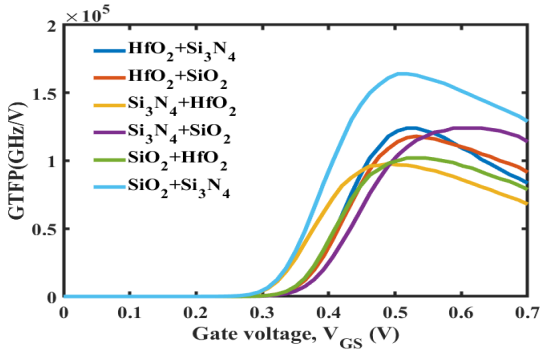


Fig. 22: GTFP of the GAA NSFET with dual-layer spacer materials.

the enhancement in f_T, which plays a leading role in determining TFP. The outer low-k SiO_2 spacer effectively decreases parasitic capacitances, thereby increasing f_T and, consequently, the overall TFP.

Fig. 21 shows the variation of GFP of the GAA NSFET with dual layer spacer structures. The GAA NSFET with SiO_2+Si_3N_4 attains the highest peak GFP, approaching 4.14×10^4 GHz, meaningfully outperforming other combinations. This superior behaviour results from the concurrent optimization of its key parameters, the outer low-k SiO_2 layer improves f_T by decreasing parasitic capacitances, while the inner intermediate-k Si_3N_4 layer enhances electrostatic control, leading to higher g_m/g_d.

GTFP of the GAA NSFET, as illustrated in Fig. 22. The GAA NSFET with SiO_2+Si_3N_4 shows the highest performance, attaining a peak GTFP beyond 1.64×10^5 GHz/V, significantly outperforming all other structures. These findings confirm that combining a low-k outer spacer for speed with an intermediate-k inner spacer for gain offers an effective strategy for attaining superior analog/RF performance in the GAA NSFET.

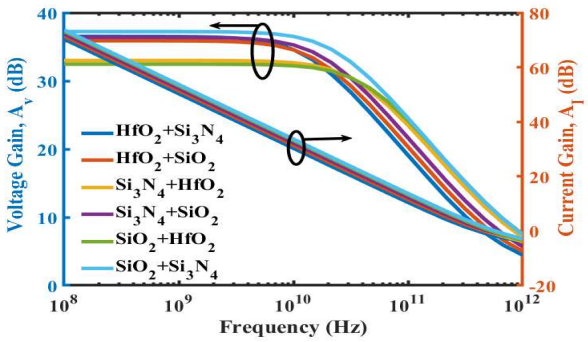


Fig. 23: Voltage gain and current gain of the GAA NSFET with dual-layer spacer materials.

Table 2: Comparison of RF performance metrics for various spacer configurations

Spacer Material	C_{GG}(F)	f_t (GHz)	Intrinsic Gain	TGF (GHz/V)	TFP (GHz/V)	GFP (GHz)	GTFP (GHz/V)	A_V	A_I
SiO_2	5.34×10^{-17}	540.19	59.30	33.50	5.12×10^3	3.20×10^4	1.37×10^5	36.40	72.96
Si_3N_4	7.20×10^{-17}	478.60	62.40	33.90	4.77×10^3	2.98×10^4	1.41×10^5	36.79	71.88
HfO_2	1.36×10^{-16}	368.13	38.0	34.50	3.53×10^3	1.40×10^4	6.37×10^4	32.38	69.71
HfO_2+Si_3N_4	8.24×10^{-17}	403.40	60.6	33.20	4.06×10^3	2.42×10^4	1.24×10^5	36.52	69.64
HfO_2+SiO_2	6.17×10^{-17}	455.05	56.00	32.80	4.50×10^3	2.55×10^4	1.18×10^5	35.88	71.41
Si_3N_4+HfO_2	1.17×10^{-16}	489.19	43.50	36.70	5.21×10^3	2.10×10^4	9.78×10^4	32.00	72.53
Si_3N_4+SiO_2	5.66×10^{-17}	498.34	59.30	33.20	4.74×10^3	2.96×10^4	1.24×10^5	36.40	72.22
SiO_2+HfO_2	9.31×10^{-17}	530.54	38.40	35.80	5.86×10^3	2.03×10^4	1.02×10^5	34.49	73.21
SiO_2+Si_3N_4	7.07×10^{-17}	580.96	72.00	35.90	6.72×10^3	4.14×10^4	1.64×10^5	37.24	73.67

Fig. 23 shows the A_V and A_I of the GAA NSFET with spacer material. the device with SiO_2+Si_3N_4, maintain higher voltage gain in the mid frequency range (10^9-10^{10} Hz) owing to enhanced electrostatic control and partial degradation of parasitic effects. In contrast, combinations dominated by HfO_2 show faster gain roll-off, as the high-k layer increases overlap and fringe capacitances, reducing both A_I and A_V. Table 2 shows a comparative assessment of the analog/RF behaviour of the GAA NSFET with different spacer structures.

4 Conclusion

This work investigates the analog and RF performance of the the GAA NSFET with various single- and dual-layer spacer configurations. Among the single-layer spacers, SiO_2 provides the most balanced performance, achieving a cutoff frequency (f_T) of 540.19 GHz, a TFP of 5120 GHz/V, and g_m/g_d of 59.30. However, the proposed GAA NSFET employing the SiO_2 + Si_3N_4 dual-layer spacer exhibits the best overall analog/RF performance. Compared with the single-layer SiO_2 spacer, the GFP increases by **29.38%** to 4.14×10^4 GHz, while the intrinsic gain improves by **21.42%** to 72.00. Similarly, the GTFP increases by **19.71%** to 1.64×10^5 GHz/V, and the TFP improves by **31.25%** to 6720 GHz/V. Furthermore, the cutoff frequency (f_T) increases by **7.55%** to 580.96 GHz, and the TGF improves by **7.16%** to 35.90 V^{-1}. In addition, the voltage gain (A_V) and current gain (A_I) exhibit modest improvements of **2.31%** and **0.97%**, respectively.

5 Author Contributions

L.C: Conceptualization, methodology, Simulation-Result analysis, Investigation, Validation, Writing-original draft preparation, S.R.S: Conceptualization, methodology, Investigation, Validation, Writing-review and editing, All authors have read and approved the final version of the manuscript.

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7 Declarations Competing Interests

The authors declare no competing interests.

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