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A Reconfigurable Ferroelectric Acoustic Computational Primitive for Analog In-Memory Computing

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Abstract

The growing computational demands of artificial intelligence (AI) have renewed interest in emerging nonvolatile memory (eNVM) crossbar array technologies for in-memory computing to reduce the energy cost of moving data between processors and memory. Here we report a computational primitive that merges ferroelectric memory and acoustic resonators in a single platform: Ferroelectric memory Embedded in Nanoscale Acoustic resonators (FENA). We experimentally demonstrate over 100 nonvolatile analog admittance states arising from partial ferroelectric polarization switching in lithium niobate resonators. The devices exhibit highly symmetric potentiation and depression characteristics, which directly impact computation accuracy, favorable dynamic range and linearity, and low projected read and write energies after scaling. We further propose a radio frequency (RF) peripheral readout architecture that extracts frequency- and phase-sensitive effective conductance states to offer an expanded state space and hardware-level reconfigurability. System-level evaluation using the NeuroSim multi-layer perceptron (MLP) simulator demonstrates the suitability of FENA for both online and offline neural-network training, with scaled devices achieving competitive 84% and 92% classification accuracies, respectively.

1 Introduction

The increasing computational demands of artificial intelligence (AI) are driving growing interest in compute-in-memory (CIM) architectures that perform computation directly within memory arrays [1, 2]. By eliminating the repeated movement of data between processors and memory, CIM ar-

chitectures can significantly improve the energy efficiency of vector-matrix multiplication (VMM) operations that dominate modern neural-network workloads [3, 4]. Emerging non-volatile memory (eNVM) technologies [5], including resistive random-access memory (ReRAM) [6], phase-change memory (PCM) [7], ferroelectric field-effect transistors (FeFETs) [8], ferroelectric tunnel junctions (FTJs) [8, 9], and magnetic memories [10], have therefore attracted substantial attention as programmable analog synaptic devices for neural-network accelerators [11–13].

Despite significant progress, achieving the combination of device characteristics required for efficient online learning remains challenging for existing eNVMs. High training accuracy requires a large number of programmable analog states, low write energy, and, critically, highly symmetric potentiation and depression characteristics [13, 14]. However, most resistance-based memories, such as resistive random access memory (ReRAM) [6] and phase change memory (PCM) [7], exhibit asymmetric weight updates resulting from fundamentally different physical mechanisms governing the increase and decrease of conductance. Such asymmetry introduces systematic weight-update errors that accumulate during training and degrade neural-network accuracy [13, 14]. Although various programming schemes can partially compensate for these effects, they typically require complex peripheral circuitry and carefully optimized pulse sequences that reduce system efficiency and are often impractical for on-chip implementations [14]. At the same time, most eNVM technologies rely on purely conductance-based readout mechanisms. Information is encoded and retrieved through entirely dissipative electrical currents, resulting in unavoidable Joule heating during operation. While ferroelectric capacitors offer an attractive alternative due to their highly symmetric polarization switching behavior [15] and mostly reactive power consumption, their relatively limited dynamic range limits the maximum achievable neural network training accuracy [15, 16]. Beyond these conventional memory characteristics, mapping stored states to different computational representations without reprogramming could provide hardware-level reconfigurability. Consequently, there remains a need for memory devices combining favorable analog programming characteristics, energy-efficient readout, and computational flexibility.

Here we introduce Ferroelectric memory Embedded in Nanoscale Acoustic resonators (FENA), a new class of analog computation primitive that combines non-volatile memory based on ferroelectrically tunable lithium niobate with acoustic resonators (Fig. 1). Building upon our preliminary demonstration of nonvolatile admittance tuning in ferroelectric lithium niobate acoustic resonators

[17], this work establishes their suitability for analog in-memory computing through analysis of the underlying equivalent circuit parameter variations, proposal of a radio frequency (RF) readout architecture, switching energy evaluation, and system-level neural network crossbar array validation using NeuroSim. Rather than storing information in purely resistive states, FENA stores information in multiple programmable RF admittance states generated through partial ferroelectric polarization switching. The interaction between ferroelectric domains and piezoelectric transduction enables multiple nonvolatile admittance states (100+ states) that can be programmed using low-voltage pulses ($\sim$ 2 V) while maintaining highly symmetric bidirectional weight updates. Unlike conventional memories, the stored state is represented by both the magnitude and phase of the device admittance, enabling operation at highly reactive current-voltage phase angles and reducing the real power dissipated during readout.

Using 17 GHz lithium niobate bulk acoustic wave (BAW) resonators [18], we experimentally demonstrate multiple nonvolatile analog admittance states arising from partial ferroelectric switching for both potentiation and depression. The devices exhibit large tunability of admittance amplitude and magnitude while preserving strong resonance characteristics in the fully polarized state. Device scaling projections indicate sub-picojoule programming energies, while RF phase-sensitive readout enables the extraction of frequency-dependent effective conductance states suitable for crossbar-array computation. Moreover, the same physical admittance state can be mapped into different effective conductance representations through the selection of operating frequency and sampling phase, providing a unique form of hardware-level reconfigurability unavailable in conventional memory technologies.

To evaluate the system-level implications of this approach on a compute-in-memory-based neural network accelerator, we integrate experimentally extracted device characteristics into the NeuroSim framework [19]. Simulations demonstrate that the combination of multilevel analog states and highly symmetric weight updates with sufficient dynamic range enables classification accuracies of up to 92% in multi-layer perceptron (MLP) neural networks. These results establish ferroelectrically tunable lithium niobate acoustic resonators as a promising platform for energy-efficient, reconfigurable in-memory computing.

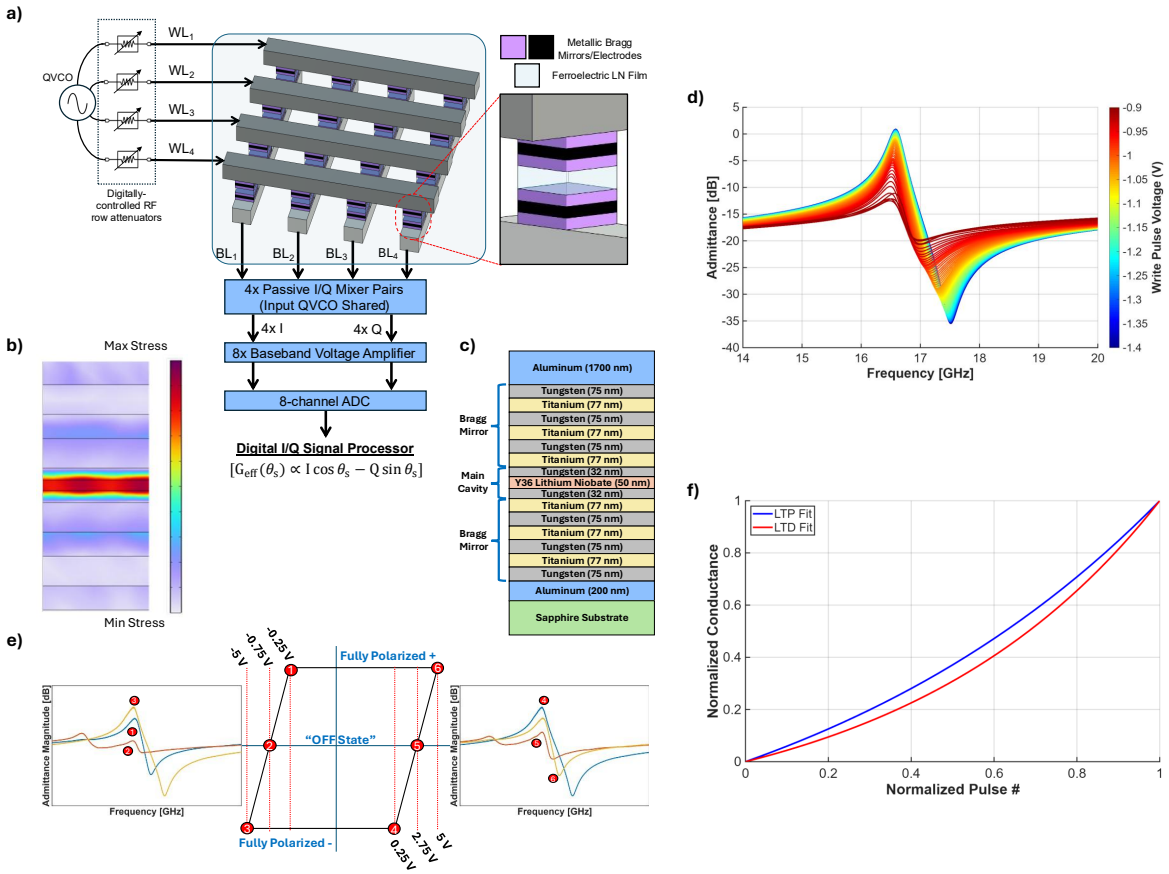


Figure 1: Overview of the FENA platform — **a**, 3D rendering of the FENA crossbar array and frequency/phase-sensitive in-phase/quadrature (I/Q) column current component readout circuitry. The signal path begins at the frequency-tuned quadrature voltage-controlled oscillator (QVCO) and the input vector is fed through voltage-variable attenuators on each row. The resulting column currents through each admittance element are summed, passively downconverted to baseband and transformed to voltage by current-driven I/Q mixer pairs, amplified/filtered, and sampled by analog-to-digital converters (ADCs) on each column, followed by digital processing of I/Q signals to extract an effective conductance. Note that low-pass filtering (LPF) of the $2f_0$ mixing product is performed by the baseband amplifier and ADC input sampling capacitor (explicit LPF not included). **b**, Diagram showing device z-axis stress mode shape from COMSOL piezoelectric simulation which proves successful longitudinal acoustic wave energy confinement using tungsten/titanium Bragg mirrors. **c**, Diagram showing theoretical designed stack with piezoelectric LN layer within the main cavity and chosen Bragg mirror layer thicknesses. **d**, Plot of fitted resonator admittance curves for various polarization voltages. After full positive polarization, admittance states are attained by applying pulse voltages from -0.9 V to -1.4 V, which significantly suppresses the resonance. **e**, Plot showing the link between RF admittance response and partial ferroelectric polarization switching. Switching from the fully polarized state in one direction (maximum resonance) to the OFF state (resonance suppressed) requires applying ~ 2.75 V opposite polarity coercive field voltage. Applying an increasing opposite polarity voltage again restores the strong resonance state. **f**, Plot of effective conductance vs. voltage used in NeuroSim online training simulations showing highly symmetric long-term potentiation (LTP) and long-term depression (LTD) exponential curve fittings.

2 Ferroelectric Control of Multi-Level RF Admittance Memory States

The defining requirement of analog nonvolatile memory devices is the ability to program and retain multiple analog states without an external bias voltage. As shown in Fig. 2c-f, FENA satisfies this requirement by exhibiting approximately 100 experimentally measured nonvolatile RF admittance states generated through partial ferroelectric polarization switching. Beginning from a fully polarized maximum-resonance ON state, increasing opposite-polarity voltage pulses progressively suppress the resonance (OFF state), while subsequent increasing-voltage pulses of the original polarity restore the original resonant response. Unlike conventional purely resistive or capacitive memory elements, FENA devices have a complex state space since both the magnitude and phase of the admittance vary significantly around resonance. Critically, all RF admittance measurements (read operations) were performed using low read voltages (0.1 V) without a large DC programming voltage applied, confirming that the programmed states are retained without an applied external bias. The ability to repeatedly program and recover many intermediate admittance states establishes FENA as a multi-level analog memory suitable for compute-in-memory architectures.

The experimentally measured memory states were realized using a 17 GHz ferroelectrically tunable lithium niobate solidly mounted bulk acoustic wave resonator shown in Fig. 2a,b. Lithium niobate (LN) is well suited for electrically reconfigurable bulk acoustic wave (BAW) resonators as it combines strong piezoelectric coupling with ferroelectric polarization switching. Thin-film BAW resonators are the backbone of the RF filtering industry with billions of components sold every year for frequencies ranging from 1 GHz to >8 GHz [20]. The fabricated device consists of a main cavity of 43 nm Y36 lithium niobate film sandwiched between tungsten electrodes to enable piezoelectric transduction. Alternating tungsten/titanium acoustic Bragg mirrors provide strong longitudinal acoustic energy confinement to maximize electromechanical coupling with all layer thicknesses chosen to achieve a series resonance near 17 GHz in the fully polarized state. This tunable resonator design translates partial ferroelectric polarization switching into programmable complex admittance states.

Previous studies of lithium niobate metal-ferroelectric-metal capacitors [21–23] have shown that partial polarization reversal proceeds through electric-field-driven domain wall motion and/or opposite domain nucleation and growth [24], producing stable intermediate polarization states following

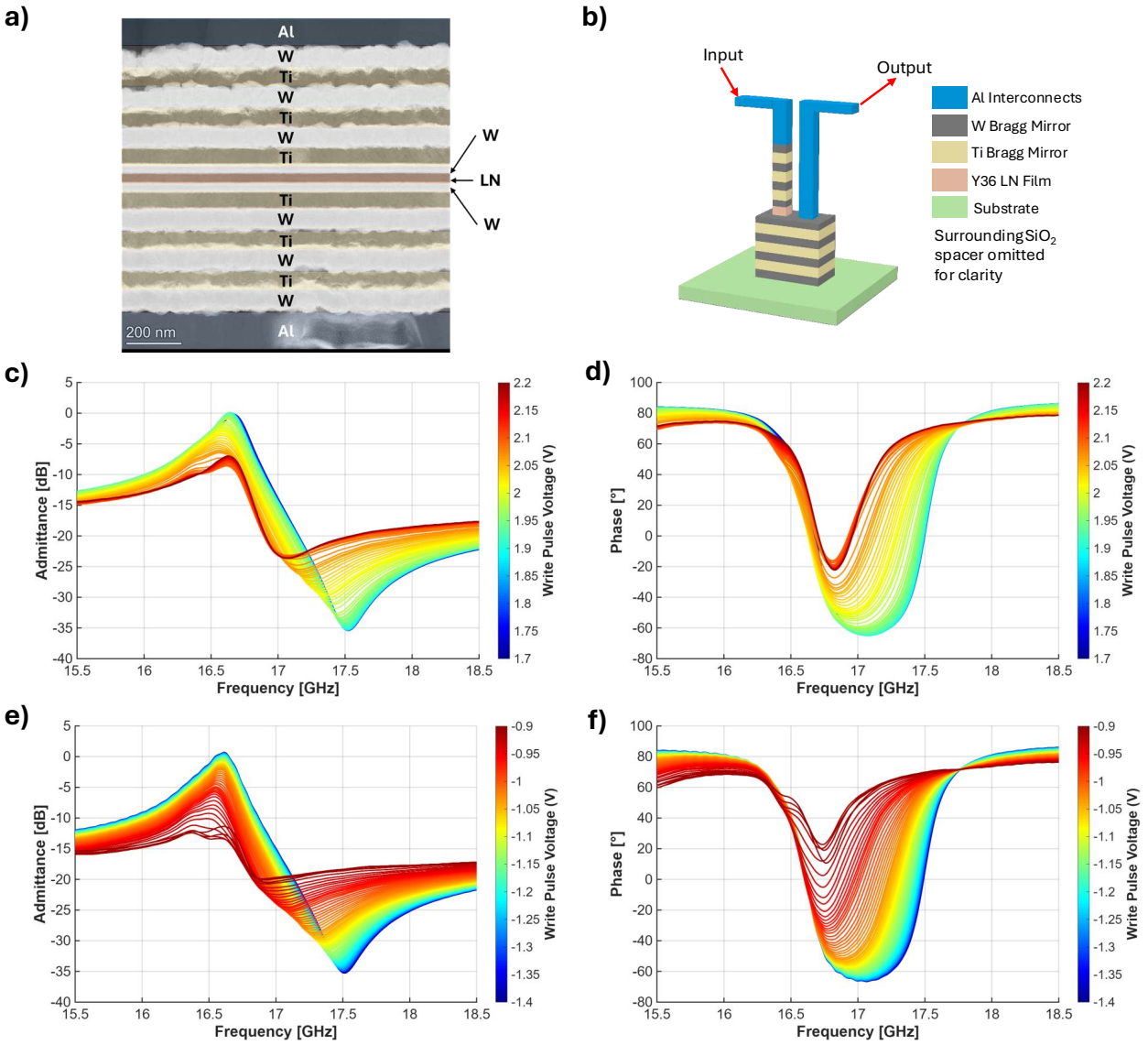


Figure 2: Ferroelectrically-Tunable Acoustic Resonators — **a**, Fabricated device TEM image. **b**, 3D model of device for context. **c**, Measured admittance magnitude plot for positive write voltage pulses after de-embedding and Savitzky-Golay smoothing showing multiple nonvolatile memory states. **d**, Measured admittance phase plot for positive write voltage pulses after de-embedding and Savitzky-Golay smoothing showing multiple nonvolatile memory states. **e**, Measured admittance magnitude plot for negative write voltage pulses after de-embedding and Savitzky-Golay smoothing showing multiple nonvolatile memory states. **f**, Measured admittance phase plot for negative write voltage pulses after de-embedding and Savitzky-Golay smoothing showing multiple nonvolatile memory states.

removal of an applied electric field. We hypothesize that these intermediate domain configurations directly modify the effective piezoelectric properties of the lithium niobate film, thereby altering the resonator admittance frequency response as shown in Fig. 1e. After fully polarizing the de-

vice, opposite-polarity voltage pulses progressively increase the fraction of reversed domains until a highly depolarized and lossy state is reached near the coercive field voltage, resulting in competing ferroelectric domain orientations that significantly reduce the effective piezoelectric response and increase acoustic losses. Applying even larger pulses of the same polarity would eventually restore the mechanical resonance, although in practice the original state is typically recovered using smaller increasing-voltage pulses of the opposite polarity. Because both potentiation and depression arise from the same underlying ferroelectric switching mechanism involving partial polarization reversal, FENA naturally exhibits highly symmetric bidirectional programming characteristics even with identical write voltage pulses unlike resistance-based analog memories.

Additionally, unlike conventional analog memories that encode state information in conductance alone, FENA stores information in the complex RF admittance of the resonator. Consequently, both admittance magnitude and phase evolve during programming as functions of write voltage and frequency, substantially expanding the accessible analog state space from a single device. As shown in Fig. 2d and Fig. 2f, between the series and parallel resonance frequencies, most states have a large admittance (current/voltage) phase angle, which is maximized at $\sim 60^\circ$ as the maximum resonance ON state is approached. In this state, only about half ($\cos(60^\circ)$) of the supplied read power is dissipated as heat while the remaining power is exchanged reactively within the resonator, improving device power efficiency.

To identify the dominant physical origin of the experimentally observed memory behavior in fabricated acoustic resonators, the measured admittance responses were fitted using a version of the modified Butterworth-Van-Dyke (mBVD) model [25] with tunable components as shown in Fig. 3a. Using combinations of mBVD model parameters and the appropriate Methods section equations, the equivalent resonator/capacitor performance characteristics were derived as shown in Fig. 3b-f. As shown in Fig. 3f, the change in clamped capacitance (and hence relative permittivity) of the LN dielectric is fairly small, resulting in a relatively small capacitive ON/OFF ratio if only permittivity was modulated for fixed LN thickness and area. The series resonance frequency change in Fig. 3e is also small ($<1\%$), suggesting minimal change in overall effective acoustic velocity. However, the changes in the electromechanical coupling coefficient (k_t^2) and quality factors (Q_s/Q_p) are much more pronounced. Both parameters (and hence the resonator figure of merit, $k_t^2 Q$) drop with increasing positive pulses but are recovered to nearly the same original level after applying increasing magnitude

negative voltage pulses. Together, these observations suggest that the dominant tuning mechanism is modification of the electromechanical transduction and loss rather than a simple change in the dielectric permittivity. This behavior is consistent with ferroelectric domain reorientation reversibly degrading the piezoelectric response (Fig. 1e). The repeatability of this tuning mechanism is further supported by the endurance characterization presented in Supplementary Note 1 and Supplementary Fig. 5. The stored states originate from remanent ferroelectric polarization configurations rather than charge storage and are therefore intrinsically nonvolatile. Short-term retention of analog states over 100 seconds has already been demonstrated in the same lithium niobate films [26]. In addition, RF measurements of a fully polarized resonator state after 24 hours showed only a 1.3 mS change in admittance magnitude and a negligible 0.07° phase change at the 16.9 GHz operating point used for online training (Section 4). This variation remains below the minimum 1.6 mS separation between distinguishable memory states, supporting stable retention. The acoustic readout mechanism itself is also based on the mature BAW resonator platform, which has demonstrated excellent long-term operational stability in commercial RF systems [27].

Preserving strong resonator performance in the programmed ON state is essential for RF admittance-based memory operation. Large electromechanical coupling increases the separation between the series and parallel resonances, expanding the range of frequency operating points exhibiting high inductive reactance available for readout, while high quality factors maximize the achievable phase angle in that range and hence minimize device-level read power dissipation for a given read voltage. Despite the introduction of ferroelectric programmability, the fabricated devices maintain electromechanical coupling coefficients around 12% and quality factors of approximately 70–80 in the maximum-resonance state (Fig. 3b-d). Collectively, these experimental data demonstrate that two-terminal FENA devices combine three key characteristics desirable for analog compute-in-memory hardware: a large multilevel nonvolatile memory space, intrinsically symmetric bidirectional programming, and reduced device-level read power dissipation. The following section demonstrates how these experimentally measured RF admittance states are transformed into effective conductance values using frequency- and phase-sensitive RF readout circuitry suitable for crossbar-array computation to fully leverage the unique complex admittance state space and hardware-level reconfigurability offered by tunable acoustic resonators.

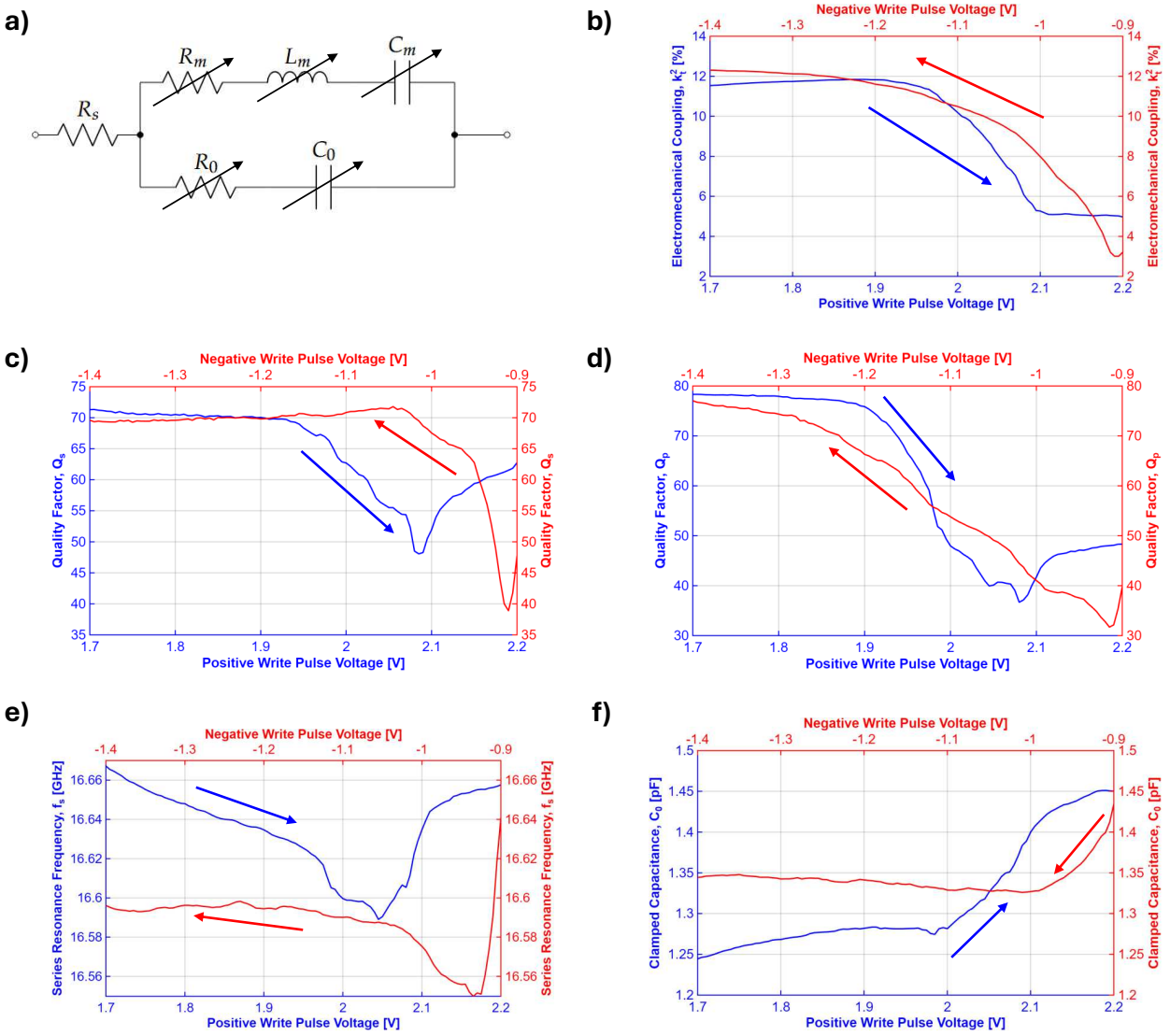


Figure 3: Resonator mBVD Model Parameter Extraction — **a**, mBVD model with variable components used to model tunable resonators. **b**, mBVD-extracted electromechanical coupling plots over positive and negative write voltages. **c**, mBVD-extracted series resonance quality factor plots over positive and negative write voltages. **d**, mBVD-extracted parallel resonance quality factor plots over positive and negative write voltages. **e**, mBVD-extracted series resonance frequency plots over positive and negative write voltages. **f**, mBVD-extracted clamped capacitance plots over positive and negative write voltages.

3 RF Readout Architecture and Energy Scaling

Having demonstrated that FENA devices store analog nonvolatile information in complex RF admittance states, we next show how these states are transformed into quantities suitable for compute-in-memory crossbar arrays. Conventional resistive crossbars perform vector-matrix multiplication

by applying input voltages along rows and summing the resulting conductance-weighted currents along columns. The proposed FENA RF crossbar architecture in Fig. 1a uses the same current-summation readout principle, but each cell stores a frequency-dependent complex admittance rather than purely real conductance. Using a quadrature voltage-controlled oscillator (QVCO) tuned near the ∼17 GHz resonance frequency, the input voltage vector is encoded through voltage-variable (digital step) attenuators. The resulting admittance-weighted column currents are then summed and read out using a passive direct-conversion RF receiver chain consisting of current-driven passive in-phase/quadrature (I/Q) mixer pairs, baseband amplifiers, and analog-to-digital converters (ADCs) [28, 29]. The same quadrature VCO drives all row inputs (I signals) and the per-column I/Q mixer pairs with I and Q signals respectively. Write operations are performed similarly to conventional ReRAM and PCM arrays with a standard 1-transistor/1-resistor (1T1R) configuration to isolate selected cells (two-terminal devices) and also to suppress sneak-path currents during read and write operations [30].

The I/Q readout converts the complex admittance state into a programmable effective conductance suitable for conventional crossbar computation. For a device admittance with magnitude $|Y|$ and phase ϕ, the downconverted I and Q components are proportional to $|Y|\cos\phi$ and $|Y|\sin\phi$, respectively. After digital projection of these components onto a chosen sampling phase, θ_s, the following effective conductance is obtained for a given QVCO operating frequency and write voltage-based device state:

$$G_{\text{eff}}(\theta_s) = |Y|\cos(\phi + \theta_s). \tag{1}$$

This proposed readout approach is consistent with the vector network analyzer (VNA) measurement technique used to obtain Fig. 2c-f data (albeit at a single frequency) and post-processing with Eq. (1) to extract effective conductance as discussed in Methods. It is a standard direct-conversion RF receiver design, which can attain extremely low power consumption [28, 29]. This readout also provides a unique form of hardware-level reconfigurability unavailable in conventional broadband conductance memories. Since both $|Y|$ and ϕ depend on frequency, the same write voltage-determined physical admittance state can be mapped into different effective conductance values by changing only the QVCO frequency and digital sampling phase (θ_s). This enables the same

programmed FENA array to access different effective weight representations simply by varying the RF operating point. Unlike conventional conductance memories, where each programmed physical state corresponds to a single conductance value, FENA enables the same programmed admittance state to be mapped into different effective weights through changes in the RF operating point. The system level impact of this feature will be presented in the next section.

The write energy scaling of FENA is governed by ferroelectric switching in the lithium niobate layer. For complete polarization reversal, the switched charge is proportional to the ferroelectric device area,

$$Q_{sw} = 2P_r A, \tag{2}$$

where P_r is the remnant polarization and A is the switched device area. The corresponding switching energy scales approximately as

$$E_{\text{write}} \gtrsim Q_{sw} V_{\text{write}} \approx 2P_r A E_c d, \tag{3}$$

where E_c is the coercive field and d is the ferroelectric film thickness. The area dependence is confirmed experimentally by lithium niobate capacitor and resonator measurements (Fig. 4) using the Positive-Up Negative-Down (PUND) technique discussed in Methods. The resonator switching energies follow the same area scaling trend as the capacitor measurements, suggesting that the designed resonators remain compatible with area-scaled ferroelectric programming. The difference in calculated positive and negative voltage switching energies for both capacitors and resonators reflects the asymmetric coercive voltages of the ferroelectric device, consistent with a built-in electric field (imprint) reported in thin-film ferroelectrics [31]. Extrapolation to a 300 nm $\times$ 300 nm FENA cell gives projected complete-switching energies of approximately 266 fJ and 184 fJ for positive and negative write pulses, respectively. Analog memory updates correspond to only partial polarization switching and therefore require proportionally smaller switching energies. Further reductions in write energy are also expected through scaling of the lithium niobate thickness, since the required switching voltage scales with ferroelectric thickness for a fixed coercive electric field strength, although practical film thickness scaling remains constrained by fabrication capabilities.

Read operation energy comprises both device-level dissipation and peripheral circuit energy,

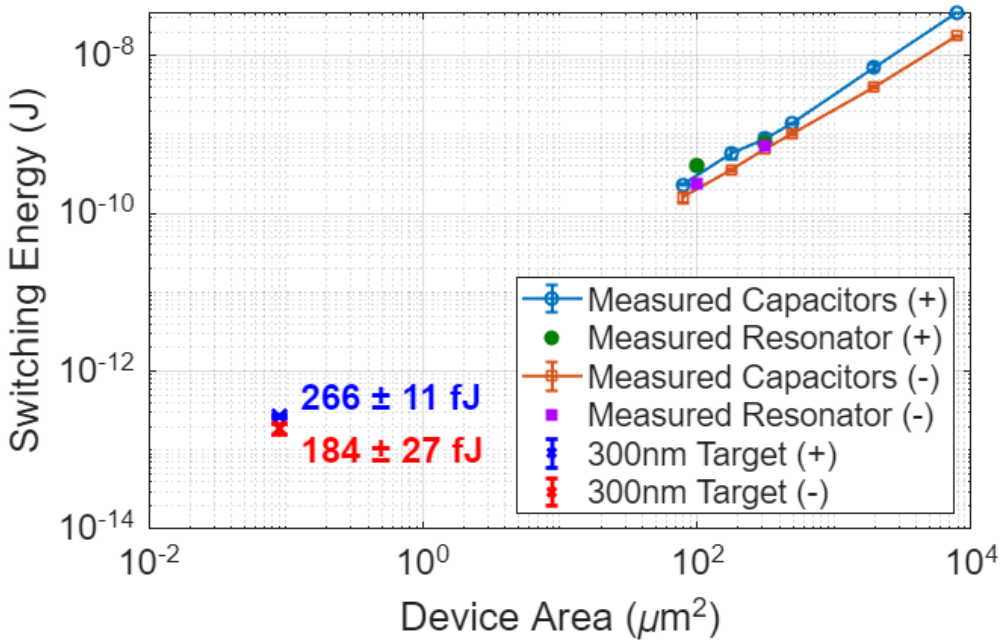


Figure 4: Write energy scaling — Switching energy change over area including LN-film resonators and capacitors with device scaling to 300 nm × 300 nm area. These results were estimated from Positive-Up Negative-Down (PUND) measurements for positive and negative pulse voltages as detailed in the Methods section.

with the latter typically dominating in large analog compute-in-memory arrays. As discussed in the previous section, the high phase angle (inductive reactance) of programmed admittance states can significantly reduce real device-level power dissipation in most memory states. At the circuit level, the proposed RF readout architecture avoids a dedicated active transimpedance amplifier (TIA) or low noise amplifier (LNA) on each column by using current-driven passive mixers for current-to-voltage transformation and quadrature downconversion, followed by low-frequency/low-power baseband voltage amplifiers. This relaxes the dependence of peripheral power on cell impedance and enables operation at lower read voltages for a given signal-to-noise ratio (SNR). Although RF operation introduces additional frequency-generation circuitry, the quadrature VCO is shared across all rows and operates with reduced output-swing requirements, thereby amortizing its energy overhead across the array. Consequently, the proposed architecture is expected to achieve overall read energy comparable to existing analog compute-in-memory architectures while providing the additional benefit of reduced device-level dissipation through reactive admittance-based RF computation.

The use of a 17 GHz acoustic resonator addresses a key latency concern associated with high-Q

resonators. The resonator settling time constant [32] is given by

$$\tau = \frac{Q}{\pi f_0}. \tag{4}$$

Using the highest mBVD extracted quality factor of 78 from Fig. 3d and the corresponding 17.5 GHz resonance frequency, the 3τ settling time is approximately 4.3 ns, which corresponds to a 234 MHz bandwidth and Nyquist-limited ADC sampling rate requirement of 468 MSa/s. Other low-Q device states will settle faster, but ADC energy consumption is generally far greater and scales proportionally to sampling rate, so an energy-efficient FENA array would ideally have ADC-limited read latency (∼450 MSa/s based on the currently fabricated devices). Higher resonance frequencies, achieved by resonator thickness scaling, would further reduce the settling time, enabling support for higher-speed ADCs at the expense of increased peripheral energy.

Together, the proposed frequency- and phase-sensitive readout architecture links the experimentally demonstrated RF admittance memory states to conventional conductance-based compute-in-memory operation while providing favorable read/write energy scaling, hardware-level reconfigurability, and practical readout latency. The following section evaluates and benchmarks the resulting neural-network performance using experimentally extracted device characteristics within the NeuroSim framework.

4 Machine Learning Performance Evaluation

To evaluate the system-level implications of the proposed FENA-based compute-in-memory architecture, the experimentally extracted effective conductance states were incorporated into NeuroSim — a device-to-architecture simulation framework for analog neural-network eNVM hardware [19]. These states were used to simulate online and offline training of a multi-layer perceptron (MLP) using the MNIST handwritten-digit dataset [33] and to evaluate classification accuracy under both training scenarios. The effective conductance extraction, normalization, nonlinearity fitting, and NeuroSim MLP implementation procedures are described in Methods.

Fig. 5 summarizes the experimentally-extracted effective conductance states from the same Fig. 2c-f device data used in NeuroSim online and offline training simulations. The extracted effective conductance curves show highly symmetric long-term potentiation (LTP) and long-term

depression (LTD) behavior, which is essential for online learning accuracy. For online training, an operating point of 16.9 GHz and 330° sampling phase was selected because it provides a large number of programmable effective conductance states while maintaining a sufficiently high effective conductance ON/OFF ratio of 19.5. The corresponding LTP and LTD characteristics are shown in Fig. 5a, while the normalized conductance trajectories used to extract NeuroSim NL parameters are shown in Fig. 5b. Although over 100 device admittance states were measured in each direction, only a subset of them are valid as online (and offline) training weights since the LTP and LTD effective conductance ranges must overlap and adhere to the NeuroSim exponential weight update model. The chosen operating point balances requirements for online training, including large state count (bit precision), update symmetry, and sufficient dynamic range (ON/OFF ratio), as detailed in Methods.

A second operating point of 17.575 GHz and 227° sampling phase was chosen for offline training, where the larger effective conductance ON/OFF ratio of 36.2 provides a wider memory window for mapped weights and the higher R_{ON} value is also consistent with the offline training requirements after device scaling as detailed in Methods. The corresponding effective conductance and normalized fitting curves are shown in Fig. 5c,d. These distinct frequency and sampling phase operating points from a single device demonstrate how the proposed RF readout architecture can optimize the same physical memory crossbar array for different training scenarios or machine learning (ML) tasks. Traditional eNVMs typically do not have memory states that satisfy online and offline training requirements simultaneously in the same device and do not have reconfigurable operating points.

Using the experimentally extracted effective conductance characteristics after applying 300 nm × 300 nm scaling assumptions as discussed in Methods, the simulated FENA crossbar array achieved classification accuracies of 84% and 92% for online and offline training, respectively. The lower online training accuracy primarily results from the finite state count and residual weight-update nonlinearity of the experimentally measured device, although the high LTP/LTD weight update symmetry partially mitigates the effect of nonlinearity. Additional NeuroSim simulations suggest that improving the programming resolution can further enhance online training performance. For example, reducing the write voltage step size from 5 mV to 2.5 mV doubles the state count from 31/42 to 62/84 for LTP/LTD and increases simulated online training accuracy to 92%. These results suggest that greater bit precision, through optimized programming schemes or reduced measurement

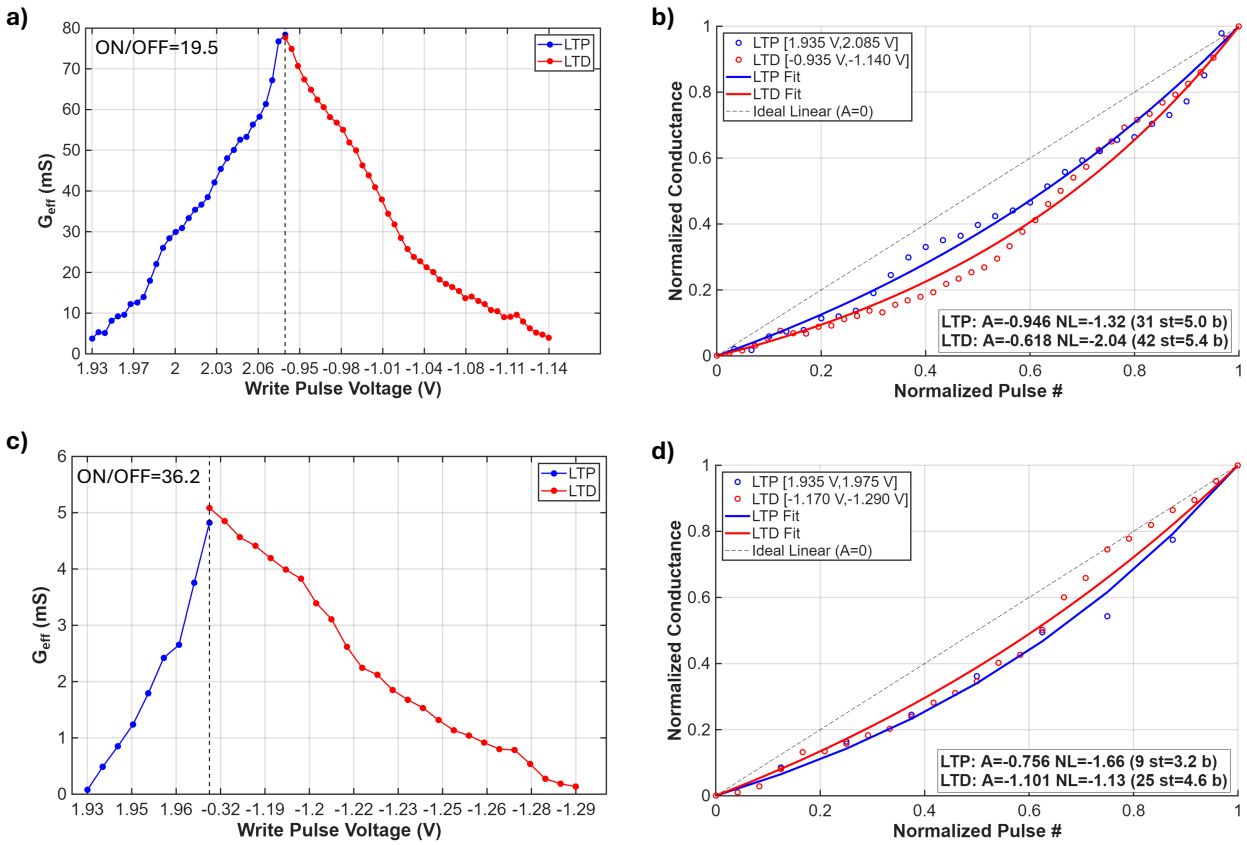


Figure 5: Effective Conductance at Selected Operating Points for NeuroSim Online Training and Offline Training — **a**, Effective conductance plot showing LTP and LTD curves for online training simulations. **b**, Normalized conductance plot of LTP and LTD used for NeuroSim exponential curve fitting to extract non-linearity for the online training operating point: 16.9 GHz frequency and 330° sampling phase. The LTP curve fits 31 states (st), equivalent to 5.0 bits (b), while the LTD curve fits 42 states (st), equivalent to 5.4 bits (b). **c**, Effective conductance plot showing LTP and LTD curves for offline training operating point: 17.575 GHz frequency and 227° sampling phase. **d**, Normalized conductance plot of LTP and LTD used for NeuroSim exponential curve fitting to extract non-linearity for offline training simulations. The LTP curve fits 9 states (st), equivalent to 3.2 bits (b), while the LTD curve fits 25 states (st), equivalent to 4.6 bits (b).

noise, could further improve online training accuracy. In addition, improved dynamic range through higher resonator quality factors could help close the remaining gap to ideal analog memory behavior.

Table 1 compares the proposed FENA architecture with representative existing analog eNVM technologies evaluated using the same MLP+NeuroSim V3.0 framework, MNIST dataset, stochastic gradient descent algorithm, learning rates, and other system-level parameters [19]. Although the measured FENA weight update curves are not perfectly linear, they are substantially more symmetric (similar NL magnitude and same sign) than many representative memristive devices, which

Table 1: Comparison of MLP+Neurosim V3.0 Online and Offline Training Accuracy — Literature-reported analog eNVM devices and targets [19, 34] vs. FENA device at 16.9 GHz/330° online and 17.575 GHz/227° offline training operating points.

Device / Scenario	NL (LTP/LTD)	States	R_{ON}	Ratio	Acc. (Online)	Acc. (Offline)*
Literature-Reported Analog eNVMs [19]						
Ag:a-Si	2.4 / -4.88	102	26 MΩ	12.5	∼72%	13%
TaO_x/HfO_2	0.04 / -0.63	128	100 kΩ	10	∼80%	6%
PCMO	3.68 / -6.76	50	23 MΩ	6.84	∼33%	10%
AlO_x/HfO_2	1.94 / -0.61	40	16.9 kΩ	4.43	∼20%	10%
GST PCM	0.105 / 2.4	100-120	4.71 kΩ	19.8	89%	23%
EpiRAM (Ag:SiGe)	0.5 / -0.5	64	81 kΩ	50.2	92%	94%
HZO FeFET	1.75 / 1.46	32	559.28 kΩ	45	88%	94%
Tunable Ferroelectric Resonator (This Work)						
Nominal Scaled Device	-1.32 / -2.04	31 / 42	57.2 kΩ	19.5	84%	-
Effect of Bit Precision						
2× States	-1.32 / -2.04	62 / 84	57.2 kΩ	19.5	92%	-
Nominal Scaled Device	-1.66 / -1.13	9 / 25	922 kΩ	36.2	-	92%
NeuroSim Targets [34]						
Targeted eNVM	1.0 / -1.0	64	200 kΩ	50	90%	94.5%
Ideal eNVM	0 / 0	64	200 kΩ	50	94.8%	94.5%

*Offline training accuracy results for benchmark devices were simulated in this work using the same literature-reported NeuroSim cell parameters as for online training [19].

is highly beneficial for online training since it reduces systematic weight update error. Weight-update asymmetry has been shown to degrade learning accuracy because history-dependent weight updates accumulate systematic errors during training [14]. Additional NeuroSim sweeps (Supplementary Fig. 7a) indicate that, to a significant extent, high LTP/LTD symmetry can compensate for reduced weight update linearity (high NL magnitude). Some resistance-based memristors, such as TaO_x/TiO_2, may achieve better symmetry and linearity through non-identical pulse durations, but this requires nontrivial peripheral circuit design and makes such pulsing schemes impractical for on-chip implementations [14]. In contrast, the symmetric bidirectional updates observed in FENA arise naturally from partial ferroelectric polarization switching using identical duration programming pulses.

The results in Table 1 also highlight the role of hardware-level reconfigurability. The same measured FENA admittance states can be mapped onto different effective conductance values by changing only the RF operating point, allowing online training evaluations to prioritize state count and

weight update symmetry while offline training evaluations prioritize high R_{ON} and dynamic range. This capability is fundamentally unavailable in conventional conductance-based analog memories, where a programmed physical state corresponds to a single conductance value. Together, the experimentally demonstrated multilevel nonvolatile memory states, symmetric bidirectional updates, frequency- and phase-reconfigurable readout, and NeuroSim-validated classification performance establish FENA as a promising new platform for reconfigurable RF compute-in-memory hardware.

5 Conclusion

Ferroelectrically tunable lithium niobate resonators offer a promising approach to energy-efficient in-memory computing, particularly for highly parallel multiply-accumulate operations in large-scale VMM. By exploiting partial ferroelectric polarization switching, the demonstrated devices achieve multiple stable analog impedance states, retained without bias power, and programmed using low-voltage pulses. Unlike most existing eNVM technologies that rely on purely conductance-based readout mechanisms, FENA devices utilize reactive admittance-based operation. Furthermore, area scaling can make write energies in the femtojoule regime feasible.

The field-driven coupling between ferroelectric domain wall motion and piezoelectric properties of lithium niobate ensures highly symmetric bidirectional weight update curves without requiring complex non-identical write voltage pulse durations. In addition, the frequency- and phase-sensitive effective conductance readout peripheral circuitry significantly expands the available state space of a single device, provides hardware-level reconfigurability of the set of memory states used for computation, and supports lower read voltages for reduced system-level read power after device scaling. Device-to-architecture simulations in the NeuroSim neural network training simulator validated these advantages (especially symmetric weight updates and reconfigurability), achieving classification accuracies of 84% and 92% for online and offline training, respectively, with the same device. Future work will focus on further device scaling, experimental implementation of crossbar arrays with RF peripheral readout circuitry, and optimization of tunable acoustic resonator performance.

6 Methods

6.1 Device Fabrication

The fabrication process for the acoustic lithium niobate (LN) resonators shown in Supplementary Fig. 1 begins with a silicon substrate carrying a nominally 50 nm-thick, 36° rotated Y-cut lithium niobate film supplied by NGK Insulators.

First, as shown in Supplementary Fig. 1(1), the lower metal stack is deposited onto the Y-36 LN thin film using plasma sputtering. This stack consists of tungsten (W) (32 nm), titanium (Ti) (77 nm), W (75 nm), Ti (77 nm), W (75 nm), Ti (77 nm), W (75 nm), and aluminum (Al) (200 nm). Following this deposition, 1.6 µm of silicon dioxide (SiO_2) is sputtered to stiffen the film in preparation for bonding and Si removal (Supplementary Fig. 1(1)). The sample is then flipped and bonded to a sapphire substrate coated with cured benzocyclobutene (BCB), as depicted in Supplementary Fig. 1(2). Subsequently, the top Si layer is removed through a sulfur hexafluoride (SF_6) reactive ion etch (RIE) followed by a dry etch using xenon difluoride (XeF_2), leaving the Y-36 LN film as the topmost layer (Supplementary Fig. 1(3)). Deposition of the upper metal stack follows (Supplementary Fig. 1(4)), comprising the same alternating W and Ti films described previously and a final layer of 1700 nm thick Al. A physical etch is then performed to remove a portion of the upper metal stack, stopping at the LN layer (Supplementary Fig. 1(5)). This is followed by another physical etch to isolate the LN resonator by removing a portion of the lower metal stack, stopping at the SiO_2 layer (Supplementary Fig. 1(6)). The LN resonator is then encapsulated by sputtered SiO_2 (Supplementary Fig. 1(7)). Next, a reactive ion etch (RIE) of the encapsulating SiO_2 layer is processed to open the vias for the interconnects (Supplementary Fig. 1(8)). Finally, sputter deposition and RIE are used to form the Al interconnects and complete the LN resonator fabrication (Supplementary Fig. 1(9)). All four lithographic patterning steps were performed using a 375 nm direct-write laser system.

The geometries fabricated included both circular and square electrodes. The circles were 20 µm in diameter and the squares included both 20 µm width and length as well as 10 µm width and length. Most of the results discussed in this article are for 20 µm-diameter circular electrodes, with the exception of the Fig. 4 switching energy characterization, which uses electrodes of both sizes for area scaling comparisons. The supplementary endurance characterization in Supplementary Fig. 5

also used 10 µm square electrode devices.

6.2 RF Admittance Measurement Experimental Setup

To characterize the tunability of the admittance states (magnitude and phase), the LN resonator was subjected to a sequence of DC voltage pulses (square waves) of varying magnitude and polarity using the experimental setup shown in Supplementary Fig. 2. All pulse durations were fixed with 1 μs rise/fall times and a 10 ms flat time. After each DC voltage pulse had ended (0 V), the RF 1-port S-parameters were measured with a vector network analyzer (VNA) frequency sweep of -10 dBm sinusoidal signals from 14 GHz to 20 GHz. The equipment and components used for the experimental set-up, along with their purpose and technical descriptions, are provided below:

- Keysight PNA-X N5247A: A high frequency (10 MHz to 67 GHz) vector network analyzer (VNA) to extract the S_{11} parameters from a 1-port measurement.
- Zurich Instruments (ZI) Ultra High Frequency Lock-in Amplifier (UHFLI): A lock-in amplifier, used for its arbitrary waveform generator (AWG) module (14 MSa/s aux outputs), which generates identical-width DC voltage pulses of varying amplitudes and polarities (square waves).
- ZBT-K283+ Bias Tee: Bias Tee with an RF bandwidth of 1.5 GHz to 28 GHz. Allows DC pulses generated by the AWG to be applied to the device without leaking into the VNA. It also allows the high frequency VNA signals to pass into the device without leaking into the Zurich Instruments amplifier.
- ZHSS-8G-S+ High Pass Filter: A 8 GHz to 24 GHz high pass filter that blocks high-power DC signals from the AWG, which could damage the VNA RF ports.
- 40A-SG-250-P RF Probes: Picoprobe Model 40A Signal/Ground (SG) RF/microwave probes (DC to 40 GHz rating) used to measure device frequency response through electrode contact.

Before performing any 1-port RF device measurements, the VNA is calibrated by the short-open-load (SOL) technique on a set of known standards (calibration substrate) to correct systematic measurement errors associated with the VNA and cables in the experimental setup. After verifying the accuracy of the calibration, a de-embedding short structure is measured to later correct for

the effects of interconnect parasitics (inductance and capacitance) not associated with the devices themselves. Finally, the device to be measured is first pulsed multiple times with a large fixed DC voltage (5 V) of a single polarity to 'wake up' the device and ensure it is in a known initial state before starting with low DC voltage pulses of the opposite polarity in the reported device measurements.

Through the use of the application programming interface (API), provided by the manufacturers of the ZI instrument and PNA-X, a computer communicates the order of the experimental procedure. First, the UHFLI AWG module sends a DC voltage pulse from its auxiliary output port to the bias tee shown in Supplementary Fig. 2a (with RF stimulus disabled). The bias tee then allows the DC signal to travel to the signal-ground (SG) probe, blocking it from leaking into the PNA-X. The device then sees the DC voltage pulse at its interconnects from the SG probe landed as shown in Supplementary Fig. 2c. Once the DC voltage pulse has been applied and DC feedline returns to 0 V, the computer triggers the PNA-X S-parameter frequency sweep from 14 GHz to 20 GHz using a -10 dBm-power sinusoidal signal. The bias tee blocks the RF signal from traveling back into the AWG output (shown in the Supplementary Fig. 2b circuit diagram), ensuring the device sees the full extent of the VNA-applied RF signal. This procedure of DC write followed by RF readout repeats until memory states corresponding to the entire DC write voltage pulse range are read out. When post-processing raw data, the 1-port S-parameter (S_{11}) magnitude and phase of the measured device and the measured de-embedding short are first converted into their Z-parameter (Z_{11}) equivalents (impedance) with the following relation:

$$Z_{11} = Z_0 \left(\frac{1 + S_{11}}{1 - S_{11}} \right), \tag{5}$$

where the reference impedance, Z_0, is 50 Ω. De-embedded is then performed by subtracting the measured short impedance from the measured device impedance to eliminate interconnect parasitics and to establish the measurement reference plane at the device input. The resulting de-embedded complex impedance is converted to complex admittance ($Y_{11} = 1/Z_{11}$). Finally, after applying third-order Savitzky-Golay smoothing over frequency (window length of 555) to correct for calibration drift, the admittance magnitude and phase data are plotted for both write voltage sweep polarities (positive then negative) to obtain the results shown in Fig. 2c-f. Note that all admittance

magnitudes (dB) are normalized with respect to a 1 S characteristic admittance.

6.3 Resonator mBVD Model Analysis

The FENA memory element is fundamentally a tunable acoustic resonator with an equivalent motional RLC branch and electrical RC branch associated with its clamped capacitance as well as series interconnect resistance. Therefore, an adapted electrically-equivalent tunable modified Butterworth-Van Dyke (mBVD) circuit model [25] was implemented in the scattering parameter (S-parameter)-based Keysight Advanced Design System (ADS) circuit simulator to analyze which specific physical mechanisms are primarily responsible for the observed admittance frequency response changes. The analysis was performed by curve-fitting to raw measured data (after de-embedding parasitics) using the ADS model and gradient-based optimizer shown in Supplementary Fig. 3. An example of the curve fit quality over the 15.5 GHz to 18.5 GHz frequency range of interest for both admittance magnitude and phase demonstrating excellent fitting accuracy is shown in Supplementary Fig. 4.

The implemented mBVD model works by keeping a fixed series interconnect electrical resistance (R_s) and allows all other parameters to be optimized over multiple iterations until the simulated and measured admittance curves converge. This fitting procedure was repeated for the measured frequency response associated with each LTP (+) and LTD (-) memory state (write pulse voltage). Electrical series resistance was kept constant (0.3 Ω) to avoid an underconstrained model that does not converge consistently. This is also physically realistic as R_s represents only the electrical metal contact resistance which should be constant to first order across the ferroelectric tuning voltage range, regardless of its absolute value. The parameters allowed to vary and extracted after accurate convergence for each memory state are: motional resistance (R_m), motional inductance (L_m), motional capacitance (C_m), clamped electrical capacitance (C_0), and dielectric loss-associated resistance (R_0).

For a more physically insightful trend-based analysis of the changes in acoustic resonator properties, the extracted parameters for each memory state were converted into their equivalent physical parameters using the following equations adapted from the original IEEE Ultrasonics symposium paper that introduces the mBVD model [25]:

$$f_s = \frac{1}{2\pi\sqrt{L_m C_m}}, \tag{6}$$

$$f_p = f_s\sqrt{1+\frac{C_m}{C_0}}, \tag{7}$$

$$k_t^2 = \frac{\pi^2}{8}\frac{C_m}{C_0}\left(1-\frac{C_m}{C_0}\right), \tag{8}$$

$$Q_s = \frac{1}{2\pi f_s R_m C_m\left(1+\frac{R_s}{R_m}\right)}, \tag{9}$$

$$Q_p = \frac{1}{2\pi f_p R_m C_m\left(1+\frac{R_0}{R_m}\right)}, \tag{10}$$

where f_s is the series resonance frequency, f_p is the parallel resonance frequency, k_t^2 is the effective electromechanical coupling coefficient, Q_s is the quality factor at the series resonance frequency, and Q_p is the quality factor at the parallel resonance frequency. All circuit model parameters are also consistent with measurement-based extraction using f_s, f_p, and their corresponding 3-dB bandwidths to determine k_t^2 and Q, thus validating the curve-fitting procedure and equations used. These data (together with the trend in C_0) were used to generate Fig. 3b-f, which informed the primary analysis.

6.4 Ferroelectric Switching Energy Characterization

The ferroelectric switching energy results shown in Fig. 4 were obtained from Positive Up and Negative Down (PUND) measurements [35] for both MFM (Al/LN/Al) capacitors and resonators. These measurements were performed using a very similar setup to the tunable resonator measurements. The current resulting from the application of voltage pulses (2 DC probes) was read out using the UHFLI scope after passing through the Zurich Instruments HF2TA transimpedance amplifier (TIA). The pulsing procedure involved applying a reset negative pulse, followed by 2 positive then 2 negative pulses of equal magnitude and duration. These pulses each had a 5 V amplitude trapezoidal waveform with 5 μs rise/fall durations, 1 μs flat time, and 1 μs delays. This PUND measurement procedure was discussed further in a prior publication [26], where the measurements were used to extract remnant polarization and coercive field voltages of a 43 nm lithium niobate thin film between Al/Cr electrodes (though not switching energy specifically). The switching energy is

determined by first plotting absolute power (absolute value of the product of write pulse voltage and TIA output current) over time. We then integrate the absolute power over time, subtracting the energy associated with the second PUND pulse from the first, effectively subtracting out capacitive and leakage current-associated energy to isolate the device switching energy. The same extraction procedure is performed for negative polarity switching energy using the third and fourth PUND pulses instead, and then repeated for different capacitor/resonator areas to generate Fig. 4, which is analyzed in the section on write energy scaling.

6.5 Effective Conductance Extraction and NeuroSim Implementation

The fundamental architecture of the NeuroSim simulation framework is designed for resistive memories (e.g., RRAM, PCM) where the device state is defined by a scalar DC conductance (G), resulting in a current product $I = V \cdot G$. In contrast, the ferroelectric resonators proposed here operate in the radio frequency (RF) domain, where the electrical behavior is governed by a complex admittance, $Y(\omega) = G(\omega) + jB(\omega) = |Y|e^{j\phi}$. This results in a current vector possessing both magnitude and phase shift relative to the input voltage. To benchmark these resonator devices within the NeuroSim framework, which requires scalar conductance states, a metric termed "effective conductance" (G_{eff}) was derived. This metric represents the projection of the complex RF current onto a real scalar value, chosen after reading out both in-phase (I) and quadrature (Q) data streams using the peripheral readout circuit in Fig. 1a. Because the addition of complex currents in a hypothetical crossbar array would involve only simple addition of their real and imaginary parts, we can use the real and imaginary currents read from a single device (and known fixed real read voltage of 0.1 V) to determine the real conductance (G) and the imaginary susceptance (B) of the memory state associated with a single device. Further, it can be shown that sampling phase projections performed using Eq. 1 before and after the column currents sum naturally are mathematically equivalent and that $|Y|\cos(\phi+\theta_s) \equiv G\cos(\theta_s) - B\sin(\theta_s)$. The proposed architecture would perform the sampling phase projection for I and Q data from each column after digitization using a digital signal processor (DSP) in a similar manner to demodulation in commercial RF receivers [28] or VNA operation.

Both frequency (ω) and sampling phase (θ_s) may be chosen dynamically to optimize neural network training. After extracting the effective conductance curves at a particular frequency and sampling phase operating point (Fig. 5a,c), the LTP and LTD curves were normalized along the

y axes such that 0 and 1 represented the minimum and maximum effective conductances (for each curve) respectively. Along the x axis both data had pulse counts normalized and the LTD data was mirrored along the x-axis to form a potentiation and depression loop (Fig. 5b,d) consistent with Supplementary Fig. 6. An exponential fit in MATLAB ($R^2 \approx 99\%$ goodness of fit) using the LTP and LTD equations from Supplementary Fig. 6 then determined the exponential rate constant, A, which is directly mapped to the NeuroSim nonlinearity parameter (NL) for each curve based on a lookup table from the NeuroSim manual. As shown in Supplementary Fig. 6, larger NL magnitude corresponds to less linear curves, where positive NL polarity represents a concave-up shape and negative NL represents a concave-down shape relative to the ideal NL=0 linear case. Identical polarity NL would represent more symmetric potentiation and depression behavior due to matching concavities.

To determine the ideal operating point, an optimization script was run based on the measured frequency responses (Fig. 2) with iteration through various frequency and sampling phase parameters. Multiple targets needed to be optimized for including dynamic range (ON/OFF ratio), linearity, and ON-state resistance. The relative priorities of each optimization target depended on whether online or offline training classification accuracy was being evaluated. Initial NeuroSim simulations were performed by using a dummy ideal device and then introducing various non-idealities (one at a time) to determine their associated classification accuracy degradation. These results are shown in Supplementary Fig. 7 and are consistent with those reported in the NeuroSim reference paper [34]. They showed that symmetry matters to a much greater extent than non-linearity magnitude and that having similar LTP and LTD magnitudes and signs can mitigate the accuracy degradation even with relatively large NL magnitude (up to NL ≈ 5), so the optimization goal for online training was to minimize the absolute value difference in NL. The secondary objective was to maximize the number of states (bit precision) to further improve accuracy. Lastly, operating points resulting in states having ON/OFF ratio below 10 were discarded for online training. After examining all online training operating points in the 15.5 GHz to 18.5 GHz frequency range with a sampling phase resolution of 1°, several optimal operating points were found and ranked with the best one being at a frequency of 16.9 GHz and sampling phase of 330°. A similar procedure was used for offline training, but this time ensuring that R_{ON} and ON/OFF ratio were prioritized instead of linearity or bit precision. The best operating point found in this case was 17.575 GHz frequency

with 227° sampling phase. For both operating points, the write voltage range used needed to be clipped to ensure that only overlapping LTP and LTD effective conductance ranges were evaluated. In a crossbar array implementation, this operating point selection could be done as part of a startup calibration routine where the QVCO frequency is tuned and per-column sampling phase selected to find the ideal operating point that meets the aforementioned ML task-dependent requirements.

At the software level, a 400(input layer)-100(hidden layer)-10(output layer) MLP was simulated using the modified national institute of standards and technology (MNIST) handwritten digit dataset [33] over 125 training epochs and a stochastic gradient descent (SGD) algorithm. For consistency with the benchmarked devices reported in [19] and Table 1, all peripheral and algorithm parameters (such as the 32 nm process node, learning rates, and differential-pair mapped signed weight representation) were left unchanged from their default settings that were used to originally simulate the representative ReRAM devices. In accordance with the NeuroSim MLP v3 manual, offline training involves identical Param.cpp hardware settings, but with the use of hardware in training feed forward and in weight update disabled (hardware only used in feed forward testing/inference). Only the extracted global maximum effective conductance ($G_{\max}$), global minimum effective conductance ($G_{\min}$), number of LTP/LTD states, NL for LTP/LTD, and LTP/LTD write-pulse voltage ranges were used as device-level NeuroSim inputs (Cell.cpp) for a "RealDevice" model. Note that the ON/OFF ratio is internally calculated as $G_{\max}/G_{\min}$. Because the measured 20 μm diameter devices were larger than the target 300 nm scaled memory cell diameter, $G_{\max}$ and $G_{\min}$ were scaled linearly with device area for online and offline training simulations, consistent with the first-order linear area scaling of static capacitance and hence admittance over frequency for fixed stack thickness and mode shape. After running the NeuroSim simulations for online and offline training operating points over 125 epochs, the resulting classification accuracies were reported in Table 1 and evaluated alongside literature-reported devices.

7 Data Availability

The authors declare that the data supporting the findings of this study are available within the paper, its supplementary information files, and the Figshare repository at https://doi.org/10.6084/m9.figshare.33325053.

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References

[1] Sebastian, A., Le Gallo, M., Khaddam-Aljameh, R. & Eleftheriou, E. Memory devices and applications for in-memory computing. *Nature Nanotechnology* **15**, 529–544 (2020). URL https://doi.org/10.1038/s41565-020-0655-z.

[2] Ielmini, D. & Wong, H.-S. P. In-memory computing with resistive switching devices. *Nature Electronics* **1**, 333–343 (2018). URL https://doi.org/10.1038/s41928-018-0092-2.

[3] Talati, N. *et al.* mmpu—a real processing-in-memory architecture to combat the von neumann bottleneck. In Suri, M. (ed.) *Applications of Emerging Memory Technology: Beyond Storage*, 191–213 (Springer Singapore, Singapore, 2020). URL https://doi.org/10.1007/978-981-13-8379-3_8.

[4] Gholami, A. *et al.* Ai and memory wall. *IEEE Micro* **44**, 33–39 (2024).

[5] Sun, Z. *et al.* A full spectrum of computing-in-memory technologies. *Nature Electronics* **6**, 823–835 (2023). URL https://doi.org/10.1038/s41928-023-01053-4.

[6] Duan, Y., Gao, H. & Yang, Y. Analyzing switching variability of sinx-based rram in terms of joule heating dissipation. *Applied Physics Letters* **125**, 173501 (2024). URL https://doi.org/10.1063/5.0228252. https://pubs.aip.org/aip/apl/article-pdf/doi/10.1063/5.0228252/20216812/173501_1_5.0228252.pdf.

[7] Bhatnagar, V. & Kumar, A. The profound influence of temperature on phase change memory: Challenges and research breakthroughs. *Next Energy* **12**, 100614 (2026). URL https://www.sciencedirect.com/science/article/pii/S2949821X26001043.

[8] Covi, E., Mulaosmanovic, H., Max, B., Slesazeck, S. & Mikolajick, T. Ferroelectric-based synapses and neurons for neuromorphic computing. *Neuromorphic Computing and Engineering* **2**, 012002 (2022). URL https://doi.org/10.1088/2634-4386/ac4918.

[9] Berdan, R. *et al.* Low-power linear computation using nonlinear ferroelectric tunnel junction memristors. *Nature Electronics* **3**, 259–266 (2020). URL https://doi.org/10.1038/s41928-020-0405-0.

[10] Rzeszut, P. *et al.* Multi-state mram cells for hardware neuromorphic computing. *Scientific Reports* **12**, 7178 (2022). URL https://doi.org/10.1038/s41598-022-11199-4.

[11] Wan, W. *et al.* A compute-in-memory chip based on resistive random-access memory. *Nature* **608**, 504–512 (2022). URL https://doi.org/10.1038/s41586-022-04992-8.

[12] Yao, P. *et al.* Fully hardware-implemented memristor convolutional neural network. *Nature* **577**, 641–646 (2020). URL https://doi.org/10.1038/s41586-020-1942-4.

[13] Ambrogio, S. *et al.* Equivalent-accuracy accelerated neural-network training using analogue memory. *Nature* **558**, 60–67 (2018). URL https://doi.org/10.1038/s41586-018-0180-5.

[14] Yu, S. Neuro-inspired computing with emerging nonvolatile memorys. *Proceedings of the IEEE* **106**, 260–285 (2018).

[15] Wu, S. *et al.* Multi-state nonvolatile capacitances in hfo2-based ferroelectric capacitor for neuromorphic computing. *Applied Physics Letters* **124**, 102902 (2024). URL https://doi.org/10.1063/5.0180088. https://pubs.aip.org/aip/apl/article-pdf/doi/10.1063/5.0180088/19712019/102902_1_5.0180088.pdf.

[16] Zhang, X. *et al.* Single-crystalline batio3-based ferroelectric capacitive memory via membrane transfer. *Science Advances* **11**, eadz2553 (2025). URL https://www.science.org/doi/abs/10.1126/sciadv.adz2553. https://www.science.org/doi/pdf/10.1126/sciadv.adz2553.

[17] Baek, J., Hurtado, L. D., Noronha, D. J. & Piazza, G. Tunable multi-state impedance in ferroelectric based 17 ghz bulk acoustic wave resonators. In *2026 IEEE 39th International Conference on Micro Electro Mechanical Systems (MEMS)*, 1446–1448 (2026).

[18] Kaitila, J. Baw device basics. In ya Hashimoto, K. (ed.) *RF Bulk Acoustic Wave Filters for Communications*, chap. 3, 51–90 (Artech House, Norwood, MA, 2009).

[19] Luo, Y., Peng, X. & Yu, S. Mlp+neurosimv3.0: Improving on-chip learning performance with device to algorithm optimizations. In *Proceedings of the International Conference on Neuromorphic Systems*, ICONS '19 (Association for Computing Machinery, New York, NY, USA, 2019). URL https://doi.org/10.1145/3354265.3354266.

[20] Hagelauer, A. *et al.* From microwave acoustic filters to millimeter-wave operation and new applications. *IEEE Journal of Microwaves* **3**, 484–508 (2023).

[21] Kim, S., Gopalan, V. & Gruverman, A. Coercive fields in ferroelectrics: A case study in lithium niobate and lithium tantalate. *Applied Physics Letters* **80**, 2740–2742 (2002). URL https://doi.org/10.1063/1.1470247. https://pubs.aip.org/aip/apl/article-pdf/80/15/2740/18565804/2740_1_online.pdf.

[22] Grilli, S. *et al.* Investigation on reversed domain structures in lithium niobate crystals patterned by interference lithography. *Opt. Express* **11**, 392–405 (2003). URL https://opg.optica.org/oe/abstract.cfm?URI=oe-11-4-392.

[23] Hurtado, L. D. & Piazza, G. 43nm ferroelectric y-36 linbo3 multi-state conductance with low coercive field for in-memory computing. In *2025 IEEE International Symposium on Applications of Ferroelectrics (ISAF)*, 1–4 (2025).

[24] Chen, Z., Zhang, Y., Li, S., Lu, X.-M. & Cao, W. Frequency dependence of the coercive field of 0.71pb(mg1/3nb2/3)o3-0.29pbtio3 single crystal from 0.01 hz to 5 mhz. *Applied Physics Letters* **110**, 202904 (2017). URL https://doi.org/10.1063/1.4983712. https://pubs.aip.org/aip/apl/article-pdf/doi/10.1063/1.4983712/14497413/202904_1_online.pdf.

[25] Larson, J., Bradley, P., Wartenberg, S. & Ruby, R. Modified butterworth-van dyke circuit for fbar resonators and automated measurement system. In *2000 IEEE Ultrasonics Symposium. Proceedings. An International Symposium (Cat. No.00CH37121)*, vol. 1, 863–868 vol.1 (2000).

[26] Hurtado, L. & Piazza, G. Characterization of ferroelectric switching in 43 nm y-36 lithium niobate films. *Applied Physics Letters* **127**, 082904 (2025). URL https://doi.org/10.1063/5.0285779. https://pubs.aip.org/aip/apl/article-pdf/doi/10.1063/5.0285779/20667390/082904_1_5.0285779.pdf.

[27] Gilbert, S. R. *et al.* Manufacturing and reliability of chip-scale packaged fbar oscillators. In *2014 IEEE International Ultrasonics Symposium*, 89–92 (2014).

[28] Razavi, B. *RF Microelectronics* (Prentice Hall, 2011), 2 edn.

[29] Razavi, B. Design considerations for direct-conversion receivers. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* **44**, 428–435 (1997).

[30] Li, H. *et al.* Memristive crossbar arrays for storage and computing applications. *Advanced Intelligent Systems* **3**, 2100017 (2021). URL https://advanced.onlinelibrary.wiley.com/doi/abs/10.1002/aisy.202100017. https://advanced.onlinelibrary.wiley.com/doi/pdf/10.1002/aisy.202100017.

[31] Liu, F., Fina, I., Bertacco, R. & Fontcuberta, J. Unravelling and controlling hidden imprint fields in ferroelectric capacitors. *Scientific Reports* **6**, 25028 (2016). URL https://doi.org/10.1038/srep25028.

[32] Zhang, M. & Llaser, N. Review of resonator's q-factor measurement with focus on design of analog and mixed circuits for in-situ measurement. *IEEE Open Journal of Circuits and Systems* **2**, 577–586 (2021).

[33] LeCun, Y., Cortes, C. & Burges, C. Mnist handwritten digit database. *ATT Labs [Online]* **2** (2010).

[34] Chen, P.-Y., Peng, X. & Yu, S. Neurosim+: An integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures. In *2017 IEEE International Electron Devices Meeting (IEDM)*, 6.1.1–6.1.4 (2017).

[35] Rabe, K. M., Dawber, M., Lichtensteiger, C., Ahn, C. H. & Triscone, J.-M. *Modern Physics of Ferroelectrics:Essential Background*, 1–30 (Springer Berlin Heidelberg, Berlin, Heidelberg, 2007). URL https://doi.org/10.1007/978-3-540-34591-6_1.

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