Supporting Information for

Monolithic in-plane integration of gate-modulated switchable supercapacitors (*ip*G-Cap)

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Methods

Calculation and normalization of capacitances

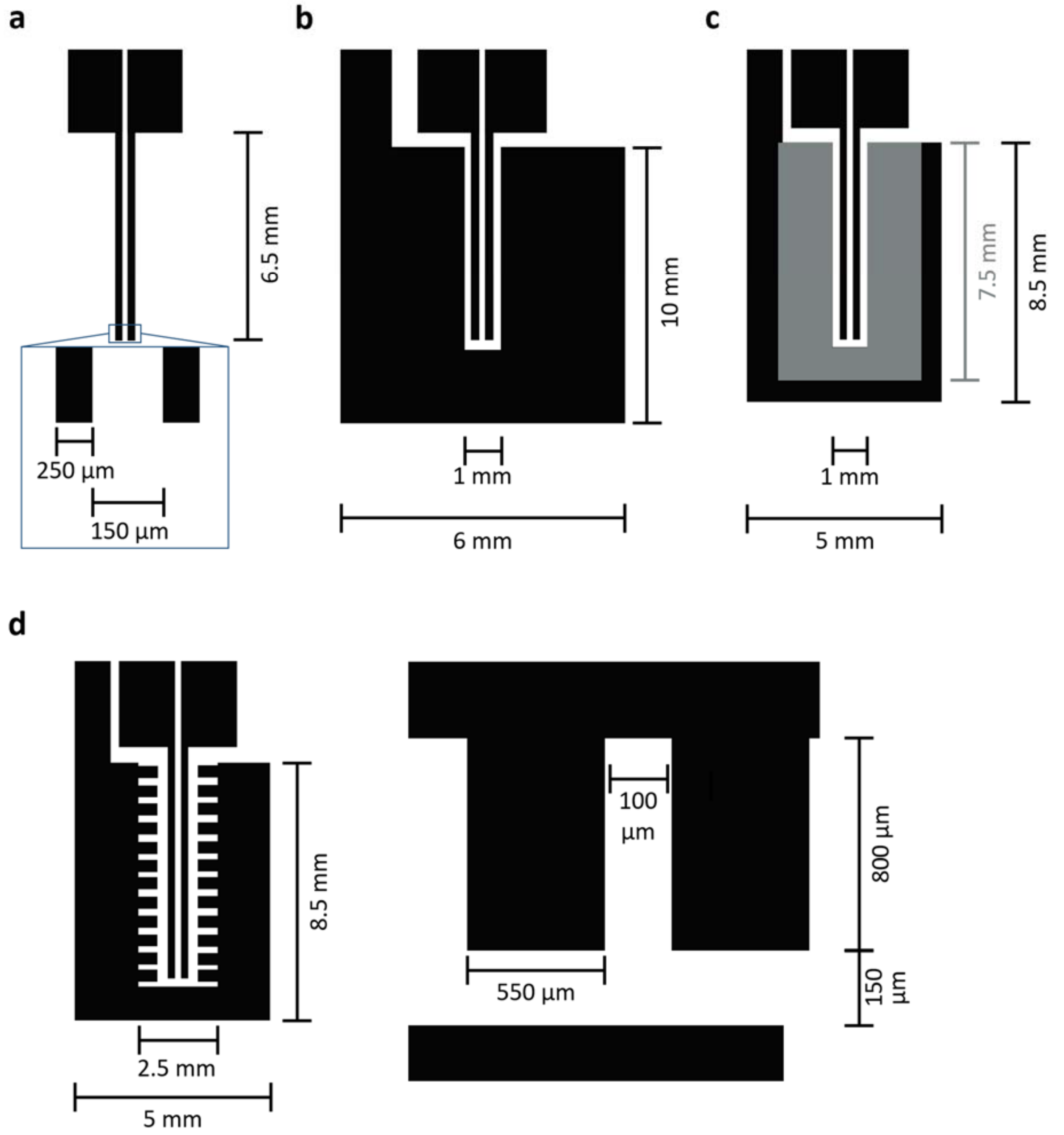
The capacitance of interdigital SCs was determined by cyclic voltammetry. The integrated area A_{CV} is divided by the potential range ΔU and the scan rate ν (1). The following equation for capacitance calculation is used:

$$C = \frac{\int_0^1 I\,dU}{\Delta U\,\nu} \tag{1}$$

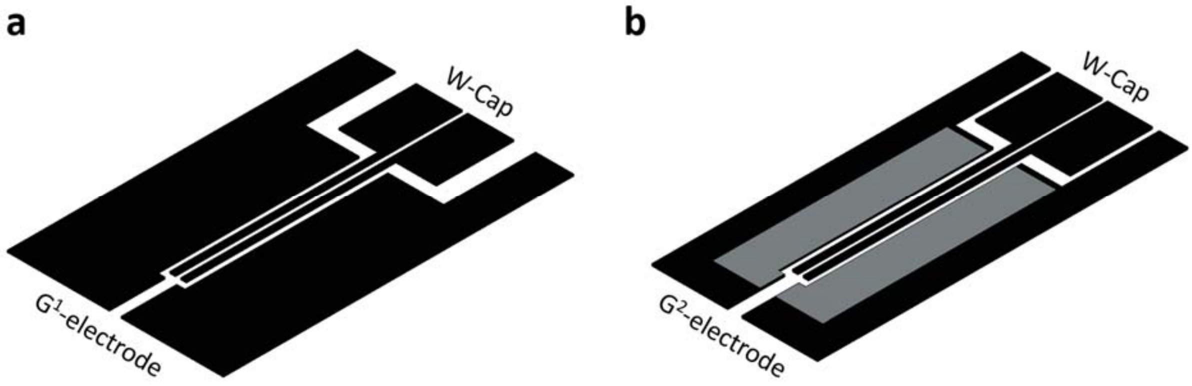
For comparison to other energy storage systems, the capacitances were normalized to the device area A_D including the total electrode and electrolyte area in the following equation (2):

$$C_{Device} = \frac{C}{A_D} \tag{2}$$

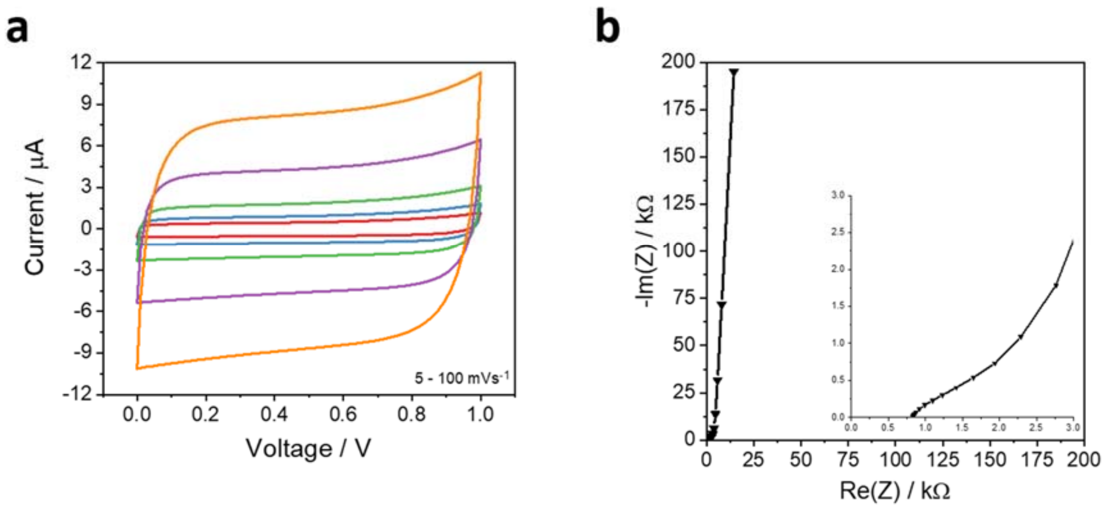
Supplementary figures



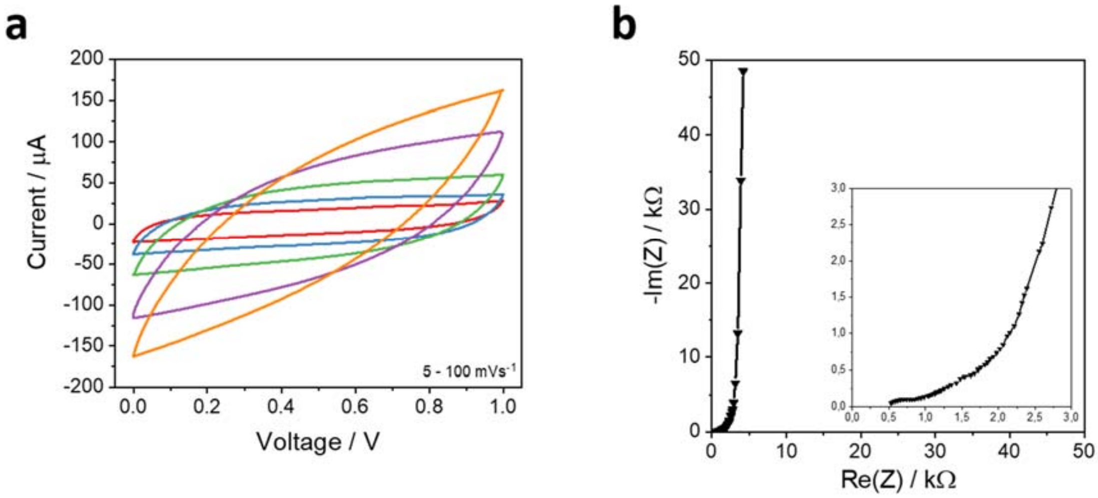
Supplementary Figure 1. Dimensions of the simplified interdigitated W-Cap (**a**) and of G-electrode architectures for in-plane G-Cap devices in 1st generation (**b**), 2nd generation (**c**), 3rd generation (**d**).



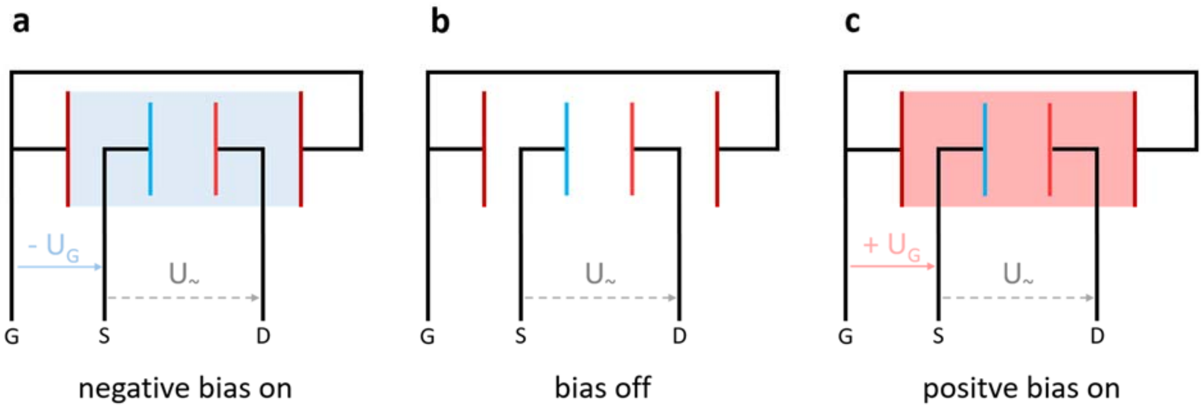
Supplementary Figure 2. Schematic illustration of devices with divided gate electrodes. 1st generation (**a**), 2nd generation (**b**).



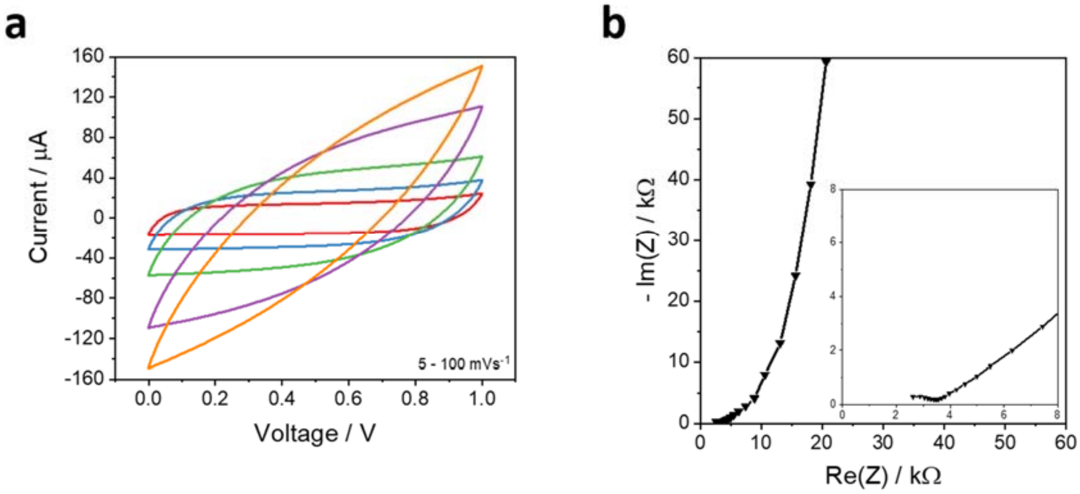
Supplementary Figure 3. Cyclic voltammograms of the simplified interdigitated W-Cap at varying scan rates (**a**) and the Nyquist plot (**b**).



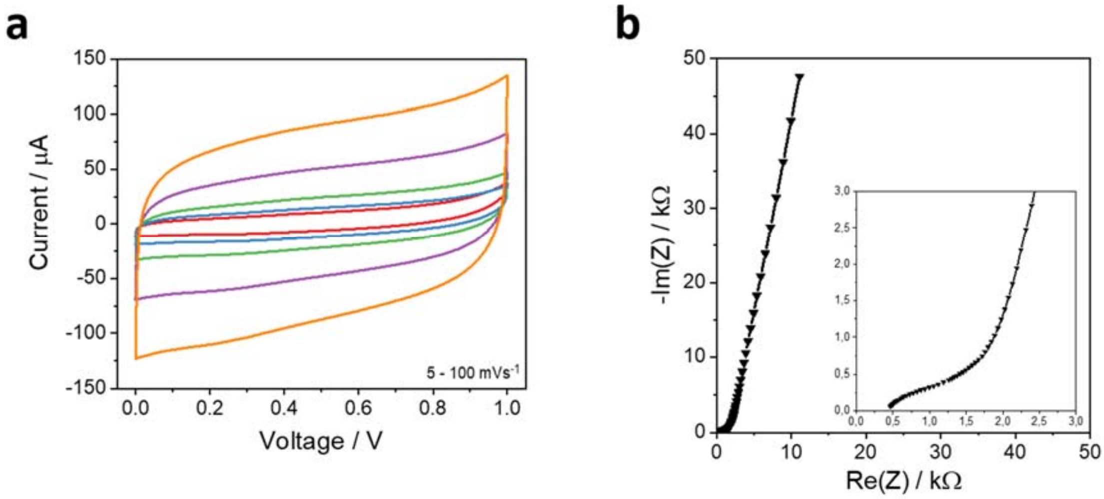
Supplementary Figure 4. Cyclic voltammograms of sucrose-derived carbon G-electrode (*ip*-G[1]) at varying scan rates (**a**) and the Nyquist plot (**b**).



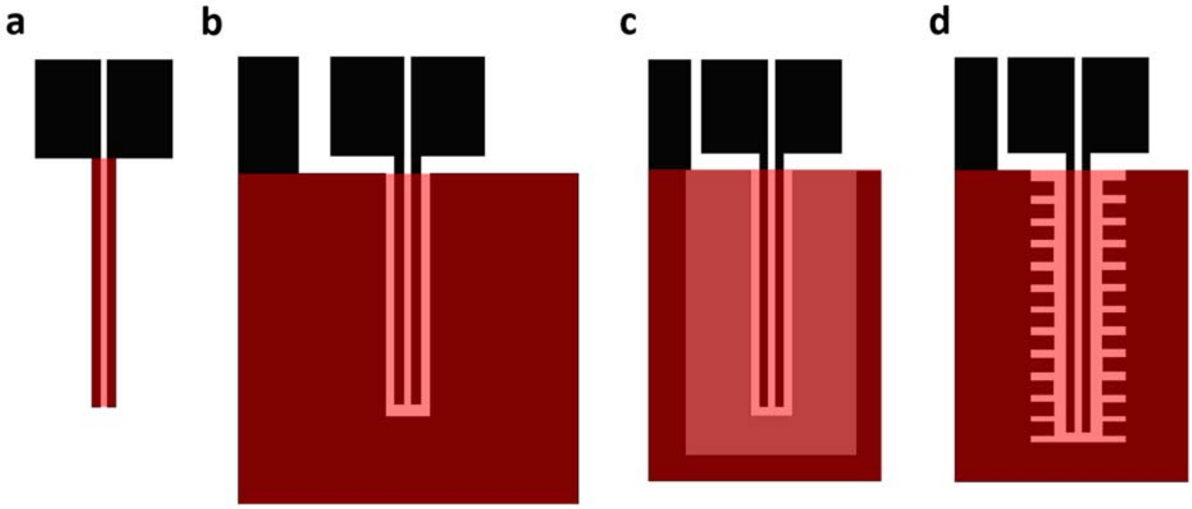
Supplementary Figure 5. Electric circuit diagrams for different sections of the measurement: blue negative bias on ($-U_G = -1.0$ V) for W-Cap switching "off" (**a**), bias off (**b**) and red positive bias ($U_G = +1.0$ V) for switching W-Cap back to "on" (**c**).



Supplementary Figure 6. Cyclic voltammograms of sucrose-derived carbon G-electrode (*ip*-G^2) at varying scan rates (**a**) and the Nyquist plot (**b**).



Supplementary Figure 7. Cyclic voltammograms of sucrose-derived carbon G-electrode (*ip*-G^3) at varying scan rates (**a**) and the Nyquist plot (**b**).



Supplementary Figure 8. Structures of the simplified interdigitated W-Cap (**a**) and of G-electrode architectures for in-plane G-Cap devices in 1st generation (**b**), 2nd generation (**c**), 3rd generation (**d**) with the red marked device area (A_D).

Supplementary Tables

Supplementary Table 1. Rate-dependent capacitances of the W-Cap and the *ip*G1-electrode based EDLC (*ip*G1-Cap).

Scan rates [mV s^{-1}]	W-Cap		Gate electrode	
	Capacitance [mF]	Device capacitance [mF cm^{-2}]	Capacitance [mF]	Device capacitance [mF cm^{-2}]
5	0.21	1.6	5.3	8.8
10	0.20	1.5	4.9	8.2
20	0.19	1.5	3.4	5.7
50	0.18	1.3	2.6	4.3
100	0.16	1.2	1.6	2.7

Supplementary Table 2. Rate-dependent capacitances of *ip*G^2-electrode based EDLC (*ip*G^2-Cap).

Scan rates [mV s^{-1}]	G^2-electrode	
	Capacitance [mF]	Device capacitance [mF cm^{-2}]
5	5.2	12.2
10	4.6	10.9
20	3.4	8.1
50	2.2	5.2
100	1.2	2.8

Supplementary Table 3. Rate-dependent capacitances of *ip*G^3-electrode based EDLC (*ip*G^3-Cap).

Scan rates [mV s^{-1}]	G^3-electrode	
	Capacitance [mF]	Device capacitance [mF cm^{-2}]
5	3.0	7.1
10	2.4	5.7
20	2.2	5.0
50	1.9	4.5
100	1.7	3.9