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Quantum Capacitance and High- κ Dielectric Engineering in Black Phosphorus MOSFETs: A Unified Analytical Framework for Electrostatic Scaling

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Abstract

Black phosphorus (BP) has emerged as a promising two-dimensional semiconductor for next-generation nanoelectronic devices, owing to its finite bandgap and high carrier mobility. This work presents an analytical model for the electrostatic and transport characteristics of BP MOSFETs with SiO₂, HfO₂, and ZrO₂ gate dielectrics. Unlike conventional analytical treatments, the proposed framework integrates quantum capacitance with high- κ dielectric engineering within a single electrostatic model, capturing oxide capacitance, quantum capacitance, electrostatic scaling, threshold voltage, drain-induced barrier lowering (DIBL), subthreshold swing (SS), and current transport across the three dielectric configurations. The model is implemented in Python and qualitatively validated with the reported literature. Results show that increasing the dielectric constant strengthens the effective gate capacitance, improving electrostatic control and suppressing short-channel effects. Among the dielectrics studied, ZrO₂ delivers the smallest scaling length (2.00 nm), lowest DIBL (3.28 mV/V), minimum SS (61.73 mV/dec), highest ON-state current (16.99 mA), and largest ON/OFF current ratio (1.05×10^{16}). Hence, outperforming both HfO₂ and SiO₂. The framework offers a computationally efficient tool for analyzing BP MOSFETs and provides design guidance for future low-power nanoelectronic devices.

Keywords: Black phosphorus; MOSFET; High- κ dielectric; Quantum capacitance; Electrostatic scaling; Drain-induced barrier lowering (DIBL); Subthreshold swing (SS)

1 Introduction

Continued scaling of complementary metal–oxide–semiconductor (CMOS) technology has driven decades of progress in integrated circuits, but as channel dimensions of silicon MOSFETs shrink into the nanometer regime, maintaining electrostatic control over the channel becomes increasingly difficult. Aggressive miniaturization brings pronounced short-channel effects (SCEs) like threshold voltage roll-off, drain-induced barrier lowering (DIBL), degraded subthreshold swing (SS), and rising leakage current that compromise reliability, switching performance, and power efficiency. Gate-stack engineering and architectural innovations have only partially addressed these limits, motivating a search for alternative channel materials capable of sustaining high performance at deeply scaled dimensions [7], [8], [12], [13].

Two-dimensional (2D) layered semiconductors have emerged as strong candidates for this role, owing to their atomically thin body, superior electrostatic gate control, and inherently suppressed short-channel effects. Graphene was an early focus for its exceptionally high carrier mobility, but its zero bandgap limits digital-logic applications due to poor switching and low ON/OFF ratio. Transition metal dichalcogenides (TMDs) such as MoS₂ offer a finite bandgap and better switching behavior, but their lower mobility restricts high-speed performance hence motivating the search for a 2D material combining high mobility, a suitable bandgap, and strong electrostatic characteristics [1], [2], [11], [18], [19].

Black phosphorus (BP) meets this need through a unique combination of a direct, thickness-tunable bandgap, high intrinsic mobility, and anisotropic transport. Its bandgap ranges from ~ 0.3 eV in bulk to nearly 2.0 eV at the monolayer limit, enabling both strong switching performance and low standby power, while its anisotropic crystal structure adds a further degree of freedom for optimizing device behavior. Experimental BP FETs have already demonstrated high ON-state current, enhanced mobility, and strong current modulation, establishing BP as a promising channel material for aggressively scaled MOSFETs where electrostatic control is critical [1], [2], [4], [9], [15], [26], [27].

Even so, BP MOSFET electrostatics depend heavily on the gate dielectric. Conventional SiO₂ suffers rising gate leakage and falling capacitance as oxide thickness scales down, degrading performance. High- κ dielectrics such as HfO₂ and ZrO₂ address this by allowing a physically thicker layer while preserving high equivalent oxide capacitance, improving gate control, suppressing leakage, and strengthening threshold voltage stability, DIBL, SS, and ON-current, which makes dielectric choice a key optimization axis for BP MOSFETs [3], [7], [8], [14]. At atomic-scale channel thickness, the finite density of states in BP introduces a quantum capacitance (C_Q), making gate capacitance no longer be treated as purely oxide-limited. The effective gate capacitance is then set by the series combination of oxide and quantum capacitance, directly shaping charge accumulation, threshold voltage, transconductance, and subthreshold behavior; making (C_Q) essential to include in any analytical model aiming to accurately capture BP MOSFET performance with high- κ dielectrics [5], [6], [10], [13], [17], [18].

Prior work including spanning experiment, numerical simulation, and compact analytical modeling, has advanced understanding of BP transistors considerably. Hence, establishing the roles of channel thickness, anisotropic transport, quantum capacitance, and dielectric engineering in device behavior. However, most studies address these factors individually rather than combining electrostatic scaling with multiple performance metrics under a unified framework across different high- κ dielectric configurations [17] – [22], [28], [29]. This work addresses that gap by developing an analytical model for BP MOSFETs that incorporates quantum capacitance together with oxide capacitance to obtain the effective gate capacitance, and use it to systematically evaluate scaling length, threshold voltage, DIBL, SS, transfer and output characteristics, ON/OFF current, and ON/OFF ratio across SiO₂, HfO₂, and ZrO₂ dielectrics under identical operating conditions. The resulting framework offers a computationally efficient tool for understanding electrostatic scaling in BP MOSFETs and the role of high- κ engineering in optimizing next-generation low-power BP-based nanoelectronics.

2 Device Configuration

The BP MOSFET considered in this study consists of a BP channel controlled by a top gate through a dielectric layer. SiO₂ ($\kappa = 3.9$), HfO₂ ($\kappa = 20$), and ZrO₂ ($\kappa = 25$) are the three gate oxides of increasing permittivity, compared to study the effect of dielectric engineering on electrostatic performance under identical device conditions. Gate oxide thickness is fixed at 2 nm and BP channel thickness at 5 nm throughout, while channel length is swept from 5 to 20 nm to capture electrostatic scaling and short-channel behavior. Unless stated otherwise, all results correspond to room temperature (300 K) and a drain voltage of 1 V.

Because BP is atomically thin, the gate field couples strongly to the channel and modulates carrier concentration directly, so device behavior depends sensitively on both the oxide dielectric constant and the semiconductor's quantum capacitance. The analytical framework developed below combines electrostatic scaling, quantum capacitance, and high- κ dielectric effects to evaluate threshold voltage, DIBL, SS, transfer and output characteristics, and current transport in the BP MOSFET.

2.1 Analytical Model

2.1.1 Capacitance Framework

Gate electrostatic coupling to the BP channel is governed by two capacitance components in series: the oxide capacitance and the quantum capacitance arising from BP's finite density of states.

For an oxide of thickness t_{ox} and permittivity κ , the oxide capacitance per unit area is [7,8]:

$$C_{ox} = \frac{\kappa \epsilon_0}{t_{ox}} \quad (1)$$

where ϵ_0 is the permittivity of free space; a larger κ directly improves gate control by raising C_{ox} .

The channel's density of states, which determines carrier availability, follows the standard 2D form [10,13]:

$$D(E) = \frac{g_s g_v m^*}{2\pi \hbar^2} \Theta(E - E_c) \quad (2)$$

with spin/valley degeneracies g_s , g_v , effective mass m^* , and Heaviside step function Θ . The effective mass is obtained from BP's anisotropic band structure as $m^* = \sqrt{m_x m_y}$ (3), where m_x and m_y are the armchair- and zigzag-direction effective masses [4]. The theoretical value of $m^* = \sqrt{m_x m_y} \approx 0.35 m_e$, derived from the armchair and zigzag effective masses reported by Qiao et al. [4], is used as the DOS effective mass throughout this work. This is in reasonable agreement with the cyclotron mass of $0.27 m_e$ measured via quantum oscillations in few-layer BP [5], with the ~23% deviation likely attributable to differences between the idealized parabolic-band approximation and the true anisotropic band structure near the Fermi level.

Combining this DOS with Fermi–Dirac statistics gives the carrier concentration [10,13]:

$$n(E_F) = D_0 k_B T \ln \left[1 + e^{\frac{E_F - E_c}{k_B T}} \right] \quad (4)$$

and the corresponding quantum capacitance [10,13,17]:

$$C_Q = \frac{q^2 D_0}{1 + \exp[-(E_F - E_c)/k_B T]} \quad (5)$$

The two capacitances combine in series to give the effective gate capacitance that governs charge modulation throughout the device [10,13,17]:

$$C_{Total} = \frac{C_{ox} C_Q}{C_{ox} + C_Q} \quad (6)$$

2.1.2 Short-Channel Electrostatics

Gate control over the channel potential is characterized by the electrostatic scaling length, following the analytical framework of [24,25]:

$$\lambda = \sqrt{\frac{\epsilon_{BP} t_{BP} t_{ox}}{\kappa}} \quad (7)$$

where ε_{BP} and t_{BP} are the BP permittivity and channel thickness; a smaller λ reflects stronger gate control and weaker short-channel effects. This scaling length sets both the threshold-voltage roll-off and DIBL. Threshold voltage follows [24,25]:

$$V_{th} = V_{th0} - V_{bi} e^{-\frac{L}{2\lambda}} \quad (8)$$

approaching the long-channel value V_{th0} as L increases, while DIBL — the threshold reduction caused by the drain field — is given by [24,25]:

$$DIBL = \frac{V_{bi}}{L} e^{-L/2\lambda} \quad (9)$$

Subthreshold swing, incorporating the quantum capacitance from Eq. (5), is [7,8,17]:

$$SS = 60 \left(1 + \frac{C_{dep}}{C_{ox} + C_Q} \right) \quad (10)$$

Lower DIBL and SS both indicate improved electrostatic integrity and faster switching.

2.1.3 Current Transport

Drain current is modeled separately in the subthreshold and strong-inversion regimes. Below threshold [7,8,17]:

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \quad (11)$$

with prefactor current I_0 , ideality factor n , and thermal voltage V_T . Above threshold ($V_{GS} > V_{th}$), the gradual-channel approximation gives [7,8]:

$$I_D = \frac{1}{2} \mu C_{Total} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (12)$$

where using C_{Total} rather than C_{ox} alone captures the influence of quantum capacitance on carrier transport. The ON-state current follows directly at $V_{GS} = V_{DD}$ [7,8]:

$$I_{ON} = \frac{1}{2} \mu C_{Total} \frac{W}{L} (V_{DD} - V_{th})^2 \quad (13)$$

while the OFF-state current comes from subthreshold conduction at $V_{GS} = 0$ [7,8,17]:

$$I_{OFF} = I_0 \exp\left(\frac{-V_{th}}{nV_T}\right) \quad (14)$$

Their ratio, I_{ON}/I_{OFF} (15), serves as the overall figure of merit for switching performance and static power dissipation.

3 Simulation Parameters

The analytical model is evaluated under identical operating conditions to isolate the effect of gate dielectric choice on the electrostatic and electrical performance of the BP MOSFET. The material parameters are adopted from previously reported BP studies, whereas the geometrical, biasing, and compact-model parameters are selected for the present analytical investigation. Table 1 summarizes the complete parameter set and corresponding sources.

Table 1. Simulation parameters used in the analytical model.

Parameter	Symbol	Value
Temperature	T	300 K
Channel length	L	5, 10, 15, 20 nm
Aspect ratio	W/L	10
BP thickness	t_{BP}	5 nm, [3]
Oxide thickness	t_{ox}	2 nm
Drain voltage	V_{DS}	1 V
Gate-voltage range	V_{GS}	0 – 2 V
Long-channel threshold voltage	V_{th0}	0.55 V
Built-in potential	V_{bi}	0.40 V
Carrier mobility	μ	205 cm ² /V·s, [3]
Ideality factor	n	1.5
Current prefactor	I_0	1×10 ⁻¹² A
Depletion capacitance	C_{dep}	0.01 F m ⁻²
Effective mass (armchair)	m_x	0.14 m_e , [4]
Effective mass (zigzag)	m_y	0.89 m_e , [4]
DOS/cyclotron mass (theoretical)	$m^* = \sqrt{m_x m_y}$	0.35 m_e , [4]
Cyclotron mass (measured)	m_{meas}^*	0.27 m_e , [5]
Spin degeneracy	g_s	2
Valley degeneracy	g_v	1, [3- 4]

The model was implemented in Python, and electrostatic and transport characteristics were compared across the three gate dielectrics to evaluate the influence of dielectric permittivity on scaling length, threshold voltage, DIBL, subthreshold swing, transfer and output characteristics, and ON/OFF current ratio.

4 Results and Discussion

4.1 Oxide and Quantum Capacitance

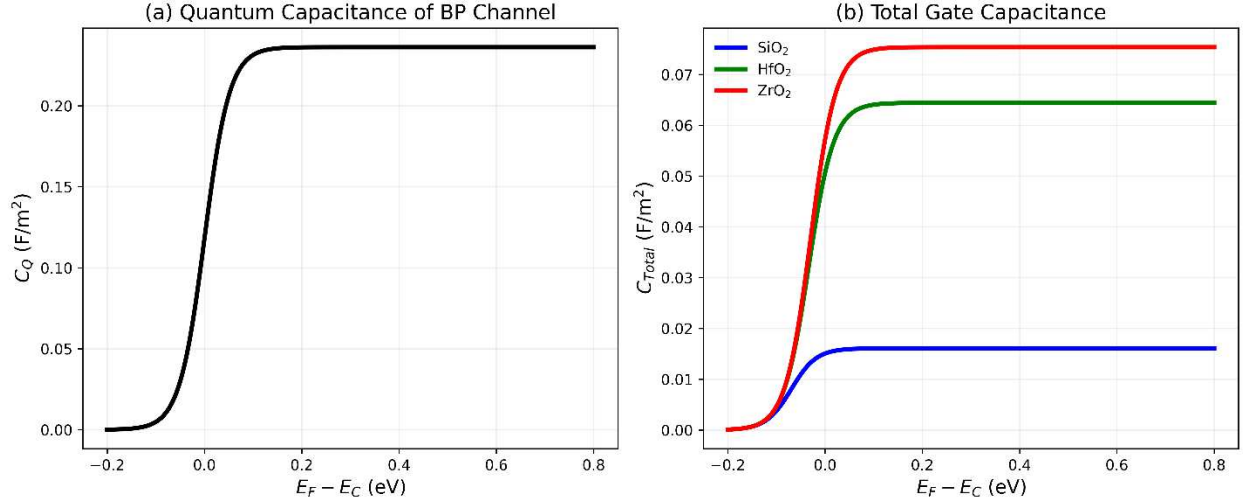


Figure 1: (a) Quantum capacitance of the BP channel and (b) Total gate capacitance for SiO₂, HfO₂, and ZrO₂ gate dielectrics.

The oxide capacitance increases with dielectric constant, consistent with the linear dependence in Eq. (1), the calculated values are 0.0173, 0.0885, and 0.1107 F/m² for SiO₂, HfO₂, and ZrO₂, respectively. Strongly confirming coupling with the higher- κ dielectrics.

Figure 1(a) shows quantum capacitance of BP channel increases as $E_F - E_C$ increases and saturating at higher carrier occupation with a peak value of 0.2363 F/m². This confirms that BP's finite density of states contributes meaningfully to the overall gate capacitance rather than being negligible, as is often assumed for bulk semiconductors. Figure 1(b) shows the resulting effective gate capacitance from the series combination in Eq. (6). The maximum C_{Total} values are 0.01609, 0.0644, and 0.07537 F/m² for SiO₂, HfO₂, and ZrO₂. Quantum capacitance caps how much the total can rise even as oxide capacitance increases, but the high- κ dielectrics still deliver a substantial net gain. Hence ZrO₂ gives the highest value among the investigated dielectrics.

Table 2. Extracted electrostatic parameters for different gate dielectrics.

Gate dielectric	C_{ox} (F/m ²)	C_Q^{max} (F/m ²)	C_{Total}^{max} (F/m ²)
SiO ₂	0.01727	0.23625	0.01609
HfO ₂	0.08854	0.23625	0.06440
ZrO ₂	0.11068	0.23625	0.07537

4.2 Electrostatic Scaling Performance

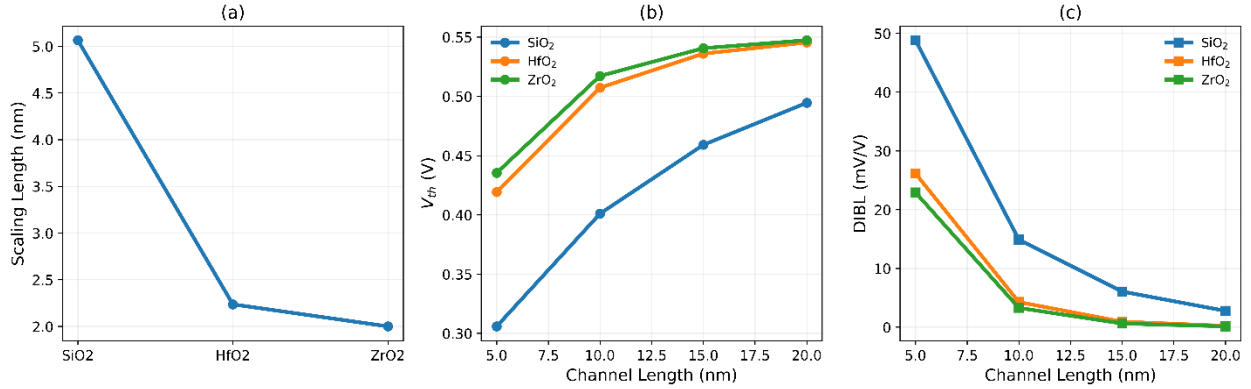


Figure 2(a) – (c): Scaling length, threshold voltage, and DIBL vs. channel length

Figure 2 shows scaling length, threshold voltage, and DIBL for the three dielectrics, a direct measure of electrostatic integrity against short-channel effects.

Scaling length falls sharply with dielectric constant (Fig. 2a) from 5.06 nm for SiO₂ to 2.24 nm for HfO₂ and 2.00 nm for ZrO₂, tightening gate control over the channel potential. Threshold voltage (Fig. 2b) increases with channel length toward its long-channel value for all three dielectrics; at $L = 10$ nm it rises from 0.401 V (SiO₂) to 0.507 V and 0.517 V (HfO₂, ZrO₂), reflecting reduced roll-off under stronger electrostatic confinement. DIBL (Fig. 2c) falls correspondingly with channel length, from 14.90 mV/V (SiO₂) to 4.28 and 3.28 mV/V (HfO₂, ZrO₂) at $L = 10$ nm. Hence, a clear suppression of drain-induced barrier lowering (DIBL) with the higher- κ dielectrics. he extracted SS values are **62.37, 61.85, and 61.73 mV/dec** for SiO₂, HfO₂, and ZrO₂, respectively.

ZrO₂ therefore delivers the smallest scaling length, and lowest DIBL, together with highest threshold voltage among the three, consistent with the stronger gate capacitance established in Section 4.1.

Table 3. Extracted Electrostatic scaling parameters.

Dielectric	Scaling length (nm)	V_{th} @10 nm (V)	DIBL@10nm(mV/V)	SS (mV/dec)
SiO ₂	5.06	0.401	14.90	62.37
HfO ₂	2.24	0.507	4.28	61.85
ZrO ₂	2.00	0.517	3.28	61.73

4.3 Transfer Characteristics

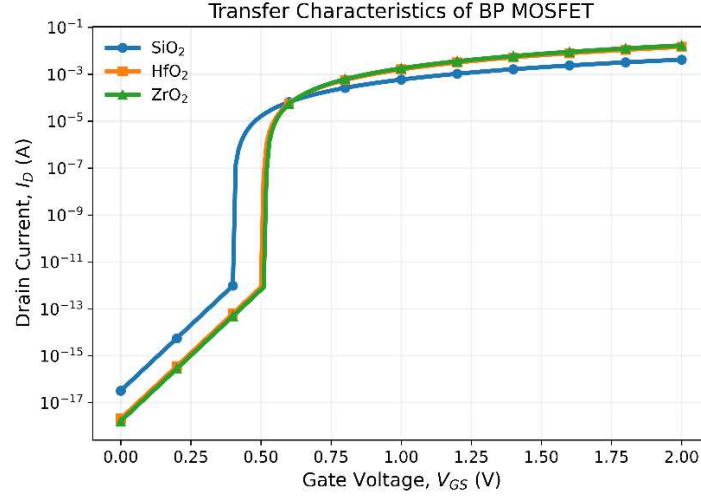


Figure 3: Transfer characteristics (I_D – V_{GS}) of BP MOSFET

Figure 3 shows the I_D – V_{GS} transfer characteristics of BP MOSFET at $V_{DS}=1$ V and a channel length of 10 nm for SiO_2 , HfO_2 , and ZrO_2 gate dielectrics. The drain current rises with gate voltage for all three dielectrics, tracing the subthreshold-to-strong-inversion transition, and the stronger gate capacitance of HfO_2 and ZrO_2 translates directly into higher carrier accumulation and drain current. At $V_{GS} = 2.0$ V, predicted ON-state currents are 4.22 mA (SiO_2), 14.71 mA (HfO_2), and 16.99 mA (ZrO_2). Hence, confirming the improved electrostatic control obtained with the high-dielectrics, with ZrO_2 giving the best transfer performance.

4.4 Output Characteristics

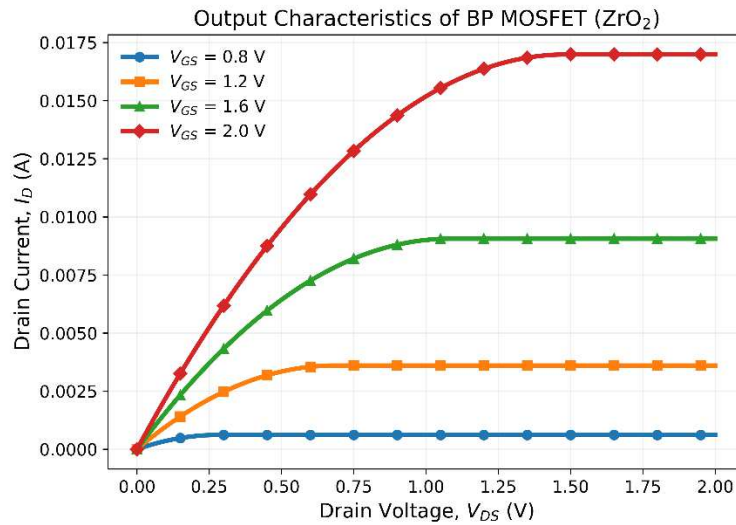


Figure 4: Output characteristics (I_D – V_{DS}) of BP MOSFET

Figure 4 shows the I_D-V_{DS} output characteristics of BP MOSFET employing ZrO_2 as the gate dielectric for different gate voltages ($V_{GS} = 0.8, 1.2, 1.6,$ and 2.0 V). Here, drain current rises linearly at low V_{DS} and saturates at higher bias, as expected for standard MOSFET operation. ZrO_2 gives the highest saturation current at $V_{GS} = 2.0$ V, reaching approx. **16.99 mA**, consistent with the extracted for the ZrO_2 device.

4.5 Performance Comparison

Table 4 consolidates I_{ON} , I_{OFF} , ON/OFF ratio, V_{th} , DIBL, and SS across all three dielectrics. I_{ON} rises from 4.22 mA (SiO_2) to 14.71 mA and 16.99 mA (HfO_2 , ZrO_2), while I_{OFF} falls from 3.23×10^{-17} A to 1.61×10^{-18} A — together lifting the ON/OFF ratio from 1.31×10^{14} to 1.05×10^{16} . ZrO_2 also gives the highest V_{th} (0.517 V), lowest DIBL (3.28 mV/V), and minimum SS (61.73 mV/dec), making it the strongest performer overall, followed by HfO_2 and SiO_2 .

Table 4. Device performance comparison.

Dielectric	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	V_{th} (V)	DIBL (mV/V)	SS (mV/dec)
SiO_2	0.004217	3.23×10^{-17}	1.31×10^{14}	0.401	14.90	62.37
HfO_2	0.014710	2.08×10^{-18}	7.06×10^{15}	0.507	4.28	61.85
ZrO_2	0.016986	1.61×10^{-18}	1.05×10^{16}	0.517	3.28	61.73

* I_{ON} is extracted at $V_{GS} = 2.0$ V and $V_{DS} = 1.0$ V for $L = 10$ nm.

5 Validation

To ensure the reliability of the proposed analytical model, the predicted electrostatic and transport characteristics were compared with previously reported theoretical and experimental studies on BP MOSFETs. Existing Literature shows that high- κ gate dielectrics improve electrostatic control by increasing effective gate capacitance, which suppresses short-channel effects and improves current transport [3,17,28,29]. The proposed model aligns with the trend: as the dielectric constant increases from SiO_2 to HfO_2 and ZrO_2 , the scaling length and DIBL decreases, while the threshold voltage and ON-state current increases, consistent with previously reported behavior of BP transistors [7,8,17,28].

For a more direct, quantitative evaluation, the predicted subthreshold swing was compared against experimental results reported for HfO_2 -gated BP transistors. Liu et al. [30] demonstrated BP FETs incorporating HfO_2 achieving a near-ideal SS of approx. **69 mV/dec**, even though operating in a long-channel regime where short-channel effects are negligible. This model predicts **SS = 61.85 mV/dec** for HfO_2 at nanoscale channel lengths. A comparable, modestly lower value consistent with the idealized (trap-free) nature of the analytical framework, which does not explicitly account

for interface trap density or defect-mediated scattering. Although direct nanoscale benchmarking data is limited in the literature, this comparison supports that the model's SS predictions fall within a physically reasonable range relative to experimentally observed behavior of BP/high- κ interfaces. It is noted that the ON/OFF ratio and threshold voltage of the referenced device are not directly comparable to the present nanoscale predictions, owing to differences in channel length, carrier type, and contact resistance effects.

Overall, the combination of qualitative trend agreement across scaling, DIBL, and current metrics, together with this quantitative SS benchmark, indicates that the proposed model captures the principle electrostatic behavior expected for nanoscale BP MOSFETs. The incorporation of quantum capacitance with high- κ dielectric engineering provides a computationally efficient approach to assessing device performance and guiding the design of future BP-based nanoelectronic devices.

6 Conclusion

This work introduces a physics-based analytical model for BP MOSFETs using SiO₂, HfO₂, and ZrO₂ as gate dielectrics, combining oxide capacitance, quantum capacitance, electrostatic scaling, and current transport into a unified framework. Increasing the dielectric constant strengthens the effective gate capacitance and, leading to improvements in all evaluated electrostatic and transport characteristics. ZrO₂ provides the smallest scaling length (**2.00 nm**), lowest DIBL (**3.28 mV/V**), minimum subthreshold swing (**61.73 mV/dec**), highest ON-state current (**16.99 mA**), and largest ON/OFF ratio (**1.05×10^{16}**) among the three dielectrics. Hence, indicating the best switching performance and strongest immunity to short-channel effects. The model offers a computationally efficient method for analyzing nanoscale BP MOSFETs, with results consistent with reported device trends, and can be extended to other 2D semiconductor channels and gate dielectric materials for future low-power nanoelectronics.

Data Availability: This study did not generate any new datasets. All input parameters and reference values employed in the simulations are obtained from published literature cited in the manuscript.

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References

- [1] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, and Y. Zhang, "Black phosphorus field-effect transistors," *Nature Nanotechnology*, vol. 9, no. 5, pp. 372–377, 2014. doi: 10.1038/nnano.2014.35.
- [2] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, and P. D. Ye, "Phosphorene: An unexplored 2D semiconductor with a high hole mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, 2014. doi: 10.1021/nn501226z.

- [3] F. Xia, H. Wang, and Y. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics," *Nature Communications*, vol. 5, Art. no. 4458, 2014. doi: 10.1038/ncomms5458.
- [4] J. Qiao, X. Kong, Z.-X. Hu, F. Yang, and W. Ji, "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus," *Nature Communications*, vol. 5, Art. no. 4475, 2014. doi: 10.1038/ncomms5475.
- [5] X. Chen et al., "High-quality sandwiched black phosphorus heterostructure and its quantum oscillations," *Nature Communications*, vol. 6, Art. no. 7315, 2015. doi: 10.1038/ncomms8315.
- [6] J. D. Wood et al., "Effective passivation of exfoliated black phosphorus transistors against ambient degradation," *Nano Letters*, vol. 14, no. 12, pp. 6964–6970, 2014. doi: 10.1021/nl5032293.
- [7] J. Robertson, "High dielectric constant oxides," *Reports on Progress in Physics*, vol. 69, no. 2, pp. 327–396, 2006. doi: 10.1088/0034-4885/69/2/R02.
- [8] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High- κ /metal-gate stack and its MOSFET characteristics," *IEEE Electron Device Letters*, vol. 25, no. 6, pp. 408–410, 2004. doi: 10.1109/LED.2004.827742.
- [9] A. Konar, T. Fang, and D. Jena, "Effect of high- κ gate dielectrics on charge transport in graphene-based field-effect transistors," *Physical Review B*, vol. 82, Art. no. 115452, 2010. doi: 10.1103/PhysRevB.82.115452.
- [10] S. Luryi, "Quantum capacitance devices," *Applied Physics Letters*, vol. 52, no. 6, pp. 501–503, 1988. doi: 10.1063/1.99649.
- [11] J. Xia, F. Chen, J. Li, and N. Tao, "Measurement of the quantum capacitance of graphene," *Nature Nanotechnology*, vol. 4, no. 8, pp. 505–509, 2009. doi: 10.1038/nnano.2009.177.
- [12] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Applied Physics Letters*, vol. 91, Art. no. 092109, 2007. doi: 10.1063/1.2776887.
- [13] P. Sengupta and S. Rakheja, "Anisotropy-driven quantum capacitance in multi-layered black phosphorus," *Journal of Applied Physics*, vol. 123, Art. no. 184301, 2018. doi: 10.1063/1.5020047.
- [14] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007.
- [15] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge, U.K.: Cambridge University Press, 2009.
- [16] S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge, U.K.: Cambridge University Press, 2005.

- [17] M. Lundstrom and J. Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation*. New York, NY, USA: Springer, 2006.
- [18] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1585–1602, 2013. doi: 10.1109/JPROC.2013.2252313.
- [19] A. Allain, J. Kang, K. Banerjee, and A. Kis, "Electrical contacts to two-dimensional semiconductors," *Nature Materials*, vol. 14, no. 12, pp. 1195–1205, 2015. doi: 10.1038/nmat4452.
- [20] E. Yarmoghaddam, N. Haratipour, S. J. Koester, and S. Rakheja, "An analytic virtual-source-based current-voltage model for ultra-thin black phosphorus field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3894–3901, 2019. doi: 10.1109/TED.2019.2922634.
- [21] S. V. Suryavanshi and E. Pop, "S2DS: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities," *Journal of Applied Physics*, vol. 120, Art. no. 224503, 2016. doi: 10.1063/1.4971365.
- [22] A. Nandi, N. Pandey, and S. Dasgupta, "Analytical modeling of gate-stack DG-MOSFET in subthreshold regime by Green's function approach," *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 4900–4907, 2018. doi: 10.1109/TED.2018.2862872.
- [23] J. R. Brews, "A charge-sheet model of the MOSFET," *Solid-State Electronics*, vol. 21, no. 2, pp. 345–355, 1978.
- [24] R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to thin-film devices," *IEEE Transactions on Electron Devices*, vol. 39, no. 7, pp. 1704–1710, 1992.
- [25] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 40, no. 12, pp. 2326–2329, 1993.
- [26] T. Low et al., "Tunable optical properties of multilayer black phosphorus thin films," *Physical Review B*, vol. 90, Art. no. 075434, 2014. doi: 10.1103/PhysRevB.90.075434.
- [27] R. Fei and L. Yang, "Strain-engineering the anisotropic electrical conductance of few-layer black phosphorus," *Nano Letters*, vol. 14, no. 5, pp. 2884–2889, 2014. doi: 10.1021/nl500935z.
- [28] M. Poljak and M. Matić, "Bandstructure and size-scaling effects in the performance of monolayer black phosphorus nanodevices," *Materials*, vol. 15, no. 1, Art. no. 243, 2022. doi: 10.3390/ma15010243.
- [29] L. Feng, K. Liu, and M. Wang, "Exact relationship between black phosphorus thickness and behaviors of field-effect transistors," *Applied Sciences*, vol. 13, no. 3, Art. no. 1736, 2023. doi: 10.3390/app13031736.

[30] Liu X, Ang K-W, Yu W, et al. Black phosphorus-based field effect transistors with simultaneously achieved near ideal subthreshold swing and high hole mobility at room temperature. *Scientific Reports*. 2016; 6:24920. <https://doi.org/10.1038/srep24920>