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A Passive Voltage Spike Suppression Strategy for High-Frequency Link Inverters Based on Primary-Side Resonance

Bowen Zheng¹ · Zhijian Feng¹ · Xinyuan Zhang¹ · Yingnan Guo¹ · Tao Zhao¹

Abstract

To mitigate the voltage spikes triggered by the resonance between transformer leakage inductance and parasitic capacitance of switching devices in high-frequency link (HFL) inverters, this paper proposes a primary-side resonance suppression passive voltage spike suppression strategy for high-frequency link inverters. This scheme suppresses the resonant spike amplitude by reshaping the excitation waveform on the primary side of the transformer, without adding extra active devices and complex control logic, and completes the compensation for duty cycle loss at the same time. A 1kW experimental prototype has been developed for verification tests. The proposed scheme reduces the voltage spike from 800V to 530V with a self-loss of only 1W, which is lower than that of the traditional RC snubber. The hybrid scheme integrated with the feedback transformer passive snubber circuit can further suppress the voltage spike to 460V. The results show that the proposed scheme achieves excellent voltage-spike suppression performance with low power losses. Moreover, it requires neither complex auxiliary control algorithms nor additional drive circuits, thereby offering high engineering feasibility and cost effectiveness for medium- and low-power photovoltaic high-frequency-link inverter applications.

Keywords High-frequency link inverter · resonance · snubbers · voltage overshoot.

1. Introduction

In the context of the global transition toward clean and distributed energy, the large-scale application of renewable energy sources, such as photovoltaics, has become pivotal to achieving "carbon peak and carbon neutrality" goals. As the core component for power conversion, the performance of the inverter directly dictates the efficiency of energy utilization [1]–[3]. Traditional line-frequency inverters rely on bulky line-frequency transformers, which suffer from inherent drawbacks such as large volume, high magnetic loss, and low efficiency, making them difficult to adapt to miniaturized and high-efficiency application scenarios. To address these issues, high-frequency link (HFL) inverters, which replace line-frequency transformers with high-frequency counterparts, have successfully overcome the bottlenecks of traditional topologies and emerged as a research hotspot in the field of power electronics [4]–[6]. The topology of the HFL inverter is illustrated in Fig. 1. By leveraging high-frequency power transmission, the HFL inverter significantly reduces the volume of magnetic components. With appropriate modulation schemes, soft-switching can be achieved to mitigate switching losses and enhance overall efficiency. Furthermore, its inherent high-frequency galvanic isolation ensures electrical safety, making it suitable for various scenarios with stringent electromagnetic compatibility (EMC) requirements. Depending on the number of power conversion stages, HFL inverters can be categorized into single-stage and multi-stage configurations. Among them, the single-stage topology eliminates the need for an intermediate DC/DC conversion stage, performing power conversion and isolation within a single stage. Due to its compact structure and low power loss, the single-stage HFL inverter has become a vital topology and a primary research focus in small-to-medium power applications[7].

However, several inherent issues persist in HFL inverters. Due to the presence of transformer leakage inductance and

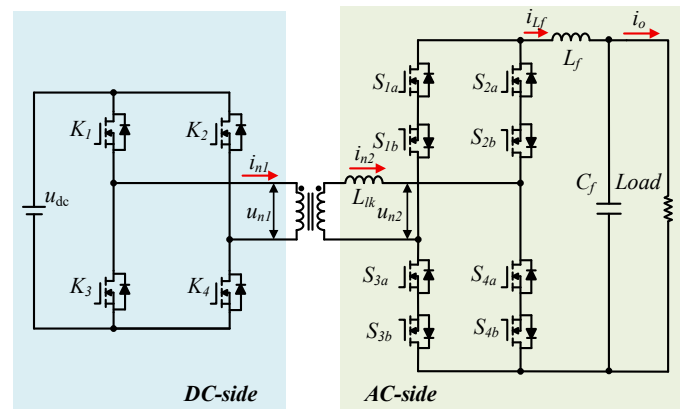


Fig. 1. Single-stage HFL inverter topology.

output filter inductance, abrupt changes in inductor current may induce severe voltage spikes, which can be mitigated by implementing appropriate modulation strategies [8]–[11]. In addition, the leakage inductance resonates with the parasitic capacitances of the semiconductor devices during switching transitions and polarity changes, leading to high-frequency voltage oscillations and overshoots [12]–[15]. These voltage spikes not only threaten the reliable operation of the switches but also necessitate the use of devices with higher voltage ratings, thereby increasing the overall cost. More importantly, unlike the former issue, these resonance-induced voltage spikes cannot be eliminated solely by optimizing the modulation strategy of the inverter itself.

To address these challenges, researchers have proposed various suppression schemes. The most straightforward approach is to connect RC snubber circuits in parallel across the switching devices [16]. Although this scheme is characterized by its simplicity and ease of implementation, it suppresses voltage spikes through a dissipative mechanism. Consequently, it introduces significant auxiliary power losses, which inevitably compromise the overall conversion efficiency of the

inverter. In [17], a passive suppression circuit comprising an auxiliary transformer and a rectifier bridge was proposed. This scheme mitigates voltage spikes by regenerating the overshoot energy back to the input DC source via the transformer, without necessitating additional active devices or increasing modulation complexity. However, the suppression performance remains suboptimal due to the inevitable presence of the auxiliary transformer's own leakage inductance. Active clamp schemes are characterized as energy-recovery solutions with significantly lower losses[18]–[21]. In these topologies, the energy stored in the leakage inductance during the resonance process is absorbed into a clamping capacitor, and subsequently fed back to the main circuit for recycling and utilization. In [22], a symmetrical bidirectional clamping structure consisting of positive and negative clamping units was employed. These two units independently process positive and negative voltage spikes, respectively, thereby accommodating non-unity power factor loads. To simplify the control, an active clamp circuit compatible with dual-phase-shift modulation was proposed in [23], where the auxiliary switches are driven with a fixed duty cycle to reduce modulation complexity. Furthermore, the work in [24] attempted to minimize the component count by multiplexing the switches of the cycloconverter. Despite these advancements, active clamp schemes generally necessitate additional active semiconductor devices and auxiliary control circuitry. This leads to increased structural complexity, as well as higher hardware costs and overall design challenges compared to passive alternatives. Alternatively, some researchers have explored structural modifications to the main circuit by incorporating an additional switching leg on the primary side. Together with two high-frequency transformers, this configuration generates a two-step stair-case voltage, which is precisely applied in sequence to suppress the resonance-induced voltage spikes [25]. However, the implementation of this scheme is highly challenging, owing to the increased control complexity and stringent timing requirements for precise voltage application. Reference [26] proposes a voltage-spike suppression method based on secondary-side modulation, which reduces the reverse-recovery current of the body diode by optimizing the MOSFET turn-off instant, thereby suppressing voltage spikes. This method does not require additional hardware snubber circuits; however, its suppression performance is relatively sensitive to the accuracy of the turn-off timing, device characteristics, and

leakage inductance, and its improvement is limited when devices with low reverse-recovery charge (Q_{rr}) are employed.

To address the inherent voltage spike issues in HFL inverters, this article proposes a novel passive suppression scheme. By incorporating passive components on the primary side of the inverter, the proposed scheme modifies the transformer's transmission voltage waveforms to effectively suppress the magnitude of voltage spikes. This approach eliminates the need for additional active semiconductor devices and avoids increasing the complexity of the control logic, resulting in a more streamlined circuit structure. Meanwhile, compared with traditional passive suppression schemes, the proposed method fundamentally alters the resonance conditions by reshaping the primary-side excitation waveform, rather than directly dissipating or recovering energy on the secondary side. The proposed scheme not only achieves superior performance in voltage spike mitigation but also exhibits lower power losses within the suppression circuitry.

The remainder of this article is organized as follows. Section II elucidates the generation mechanism of the voltage spikes, the operating principles of the proposed passive suppression scheme, and the derivation of relevant analytical formulas. In Section III, the voltage spike suppression performance of the proposed scheme is verified through experimental results. By comparing the proposed scheme with other existing suppression methods, the advantages of the proposed solution in terms of voltage spike mitigation and loss reduction are clearly demonstrated.

2. Analysis of Voltage Spike Generation and Mitigation Strategy

2.1 Mechanism of Voltage Spike Generation

The voltage spikes in HFL inverters primarily originate from two sources. First, the abrupt changes in the current flowing through the transformer leakage inductance or the output filter inductor can induce significant voltage transients. This phenomenon can generally be mitigated by implementing appropriate modulation strategies.

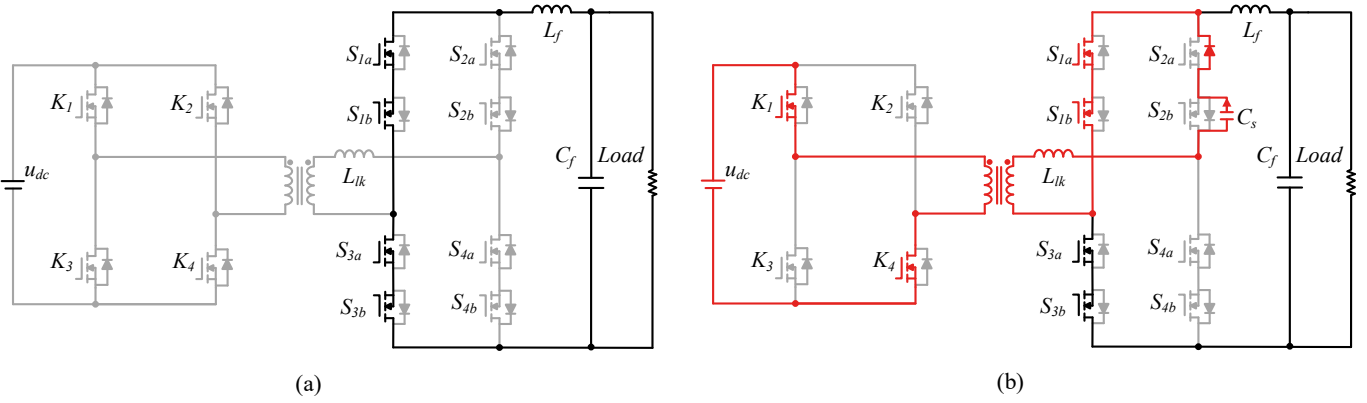


Fig. 2. Operational modes of the inverter before and after resonance (a) freewheeling stage.(b) voltage spike resonant stage.

Second, the resonance between the transformer leakage inductance and the parasitic capacitances of the secondary-side switches leads to persistent voltage oscillations. Unlike the former, this resonance-induced spike is inherently unavoidable during the turn-on and turn-off transitions of the semiconductor devices. The operating modes before and after the occurrence of this resonance are illustrated in Fig. 2.

As depicted in Fig. 2(a), the secondary side of the HFL inverter operates in the freewheeling state. During this interval, the primary-side switches are turned off, and the primary voltage is not coupled to the secondary side. Consequently, the output filter and the load current circulate through the cycloconverter via a freewheeling path. As shown in Fig. 2(b), once the primary-side switches K2 and K3 are turned on, the transformer begins to transfer power, imposing a corresponding voltage stress across the second bridge of the secondary-side cycloconverter. The parasitic capacitance C_s of switch S2b within the second bridge, which initially has zero voltage, begins to be charged through the transformer leakage inductance. Consequently, a resonant tank is formed between the leakage inductance L_{lk} and the parasitic capacitance C_s . The simplified equivalent circuit for this resonance transition is depicted in Fig. 3.

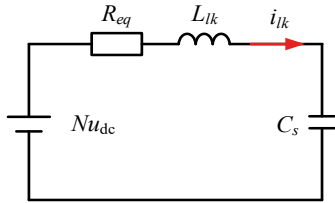


Fig. 3. Equivalent resonant circuit model.

Based on the analysis of the aforementioned equivalent circuit, the differential equations governing the high-frequency resonance can be derived as follows:

$$\begin{cases} Nu_{dc} = R_{eq} i_{lk} + L_{lk} \frac{di_{lk}}{dt} + u_{Cs} \\ i_{lk} = C_s \frac{du_{Cs}}{dt} \end{cases} \quad (1)$$

Where i_{lk} is the leakage inductance current, C_s is the parasitic capacitance of the switch, R_{eq} is the equivalent series resistance u_{Cs} and i_{Cs} represent the voltage and current associated with the parasitic capacitance, respectively. By simplifying the aforementioned differential equations, the time-domain expressions can be derived as:

$$Nu_{dc} = L_{lk} C_s \frac{d^2 u_{Cs}}{dt^2} + R_{eq} C_s \frac{du_{Cs}}{dt} + u_{Cs} \quad (2)$$

By substituting the initial conditions $i_{lk}=0$ and $u_{Cs}=0$ into the aforementioned differential equations, the analytical solutions for the resonance process can be obtained as follows:

$$u_{Cs}(t) = Nu_{dc} [1 - e^{-\alpha t} (\cos \omega_d t + \frac{\alpha}{\omega_d}) \sin \omega_d t] \quad (3)$$

Where:

$$\alpha = R_{eq} / 2L_{lk}, \omega_d = \sqrt{\omega_0^2 - \alpha^2}, \omega_0 = 1 / \sqrt{L_{lk} C_s}.$$

The maximum value of the peak voltage $u_{Cs,max}$ can be derived as:

$$u_{Cs,max} = Nu_{dc} (1 + e^{-\alpha \pi / \omega_d}) \quad (4)$$

It can be inferred that the peak value of the resonant voltage reaches $2Nu_{dc}$. This indicates that the voltage spike induced by the resonance between the transformer leakage inductance and the switch parasitic capacitance can theoretically be as high as twice the nominal operating voltage. The corresponding resonant voltage waveforms and the primary-side excitation of the transformer during this process are illustrated in Fig. 4.

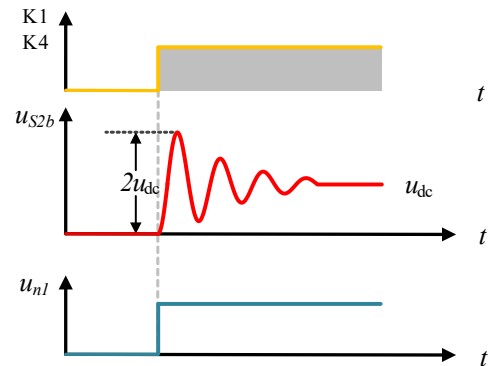


Fig. 4. Voltages of switch S2b and transformer primary during the resonance.

2.2 Proposed Passive Suppression Scheme

To address the aforementioned voltage spike issues, the proposed strategy in this article focuses on suppressing the spikes by modifying the waveform of the resonant excitation voltage. By series-connecting an inductor L_r on the primary side, the resonance on the secondary side will also occur on the primary side simultaneously. Consequently, the rising edge of the transformer primary-side voltage is no longer a step waveform. Instead, it exhibits a sinusoidal transition that rises gradually from zero due to the resonant effect. This transition effectively modifies the excitation conditions under which the resonance between the transformer leakage inductance and the switch parasitic capacitance occurs. Aiming to achieve a more gradual du/dt , a parallel capacitor C_r is introduced. This addition modifies the resonant frequency of the primary-side tank, effectively prolonging the transition interval and reshaping the excitation into a more favorable profile for spike suppression. Nevertheless, the added series inductor can still resonate with the parasitic capacitances of the secondary-side switches, leading to significant residual voltage spikes. To address this, two clamping diodes are incorporated behind the series inductor, with the specific connection configuration illustrated in Fig. 5.

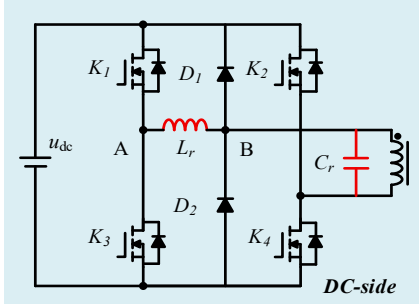


Fig. 5. Structure of the proposed suppression circuit.

When the voltage at node B is lower than u_{dc} , the clamping diodes are reverse-biased and remain non-conductive. Conversely, when the voltage at node B exceeds u_{dc} , the clamping diodes become forward-biased and start to conduct, effectively clamping the voltage at node B to u_{dc} . This clamping action efficiently suppresses the voltage spikes induced by the resonance involving the series inductor. Fig. 6 presents the rising edge waveforms of u_{n1} under different conditions.

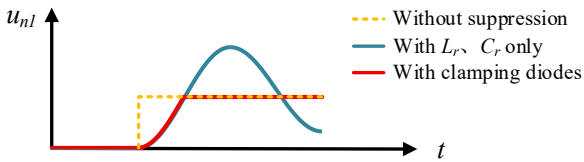


Fig. 6. Transformer primary voltages under different operating conditions.

With the integration of the clamping diodes, the resonant process can be divided into two distinct stages. The first stage

corresponds to the interval where $u_{Cr} < u_{dc}$. During this interval, the clamping diodes are in the cut-off state, and the resonance is primarily determined by L_r and C_r . The corresponding equivalent circuit for this stage is illustrated in Fig. 7. The second stage begins when $u_{Cr} = u_{dc}$. At this instant, the clamping diodes start to conduct, clamping u_{Cr} to u_{dc} and forcing u_{Lr} to zero. Consequently, L_r and C_r no longer participate in the resonance during this stage.

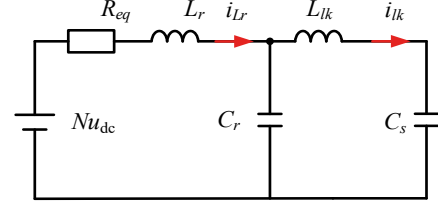


Fig. 7. Equivalent circuit during resonance with the proposed suppression strategy.

By analyzing the equivalent circuit in Fig. 7, the differential equations for the first stage can be formulated as:

$$\begin{cases} Nu_{dc} = R_{eq} i_{lk} + L_r \frac{di_{Lr}}{dt} + u_{Cr} \\ u_{Cr} = L_{lk} \frac{di_{lk}}{dt} + u_{Cs} \\ i_{Lr} = i_{lk} + C_r \frac{du_{Cr}}{dt} \\ i_{lk} = C_s \frac{du_{Cs}}{dt} \end{cases} \quad (5)$$

Assuming the initial states of the circuit are zero and neglecting the equivalent series resistance R_{eq} , the voltage across C_s during this stage can be derived. By setting the design parameters as $L_r = 2.5 L_{lk}$ and $C_r = 5C_s$, the analytical expression for $u_{Cs}(t)$ is obtained as:

$$u_{Cs}(t) = Nu_{dc} \left[1 - 1.0574 \cos(0.2567t / \sqrt{L_{lk} C_s}) + 0.0574 \cos(1.1019t / \sqrt{L_{lk} C_s}) \right] \quad (6)$$

At the instant when clamping occurs, the voltage across C_s and the current through L_{lk} can be calculated as follows:

$$\begin{cases} u_{Cs}(t_0) = 1.062 Nu_{dc} \\ i_{lk}(t_0) = 0.302 Nu_{dc} \sqrt{C_s / L_{lk}} \end{cases} \quad (7)$$

At the commencement of the second stage, L_r and C_r cease to participate in the resonance. The equivalent circuit for this stage becomes identical to the one shown in Fig. 4, with the exception that the initial states are updated to the values captured at the instant of clamping. By substituting the current and voltage values of L_r and C_r at this instant into the previously established differential equations (1), the peak resonant voltage is calculated as $u_{Cs,max} \approx 1.31 Nu_{dc}$. This result represents a significant reduction compared to the original peak voltage of $2Nu_{dc}$ observed without the suppression circuit.

The resonant voltage waveforms and the transformer primary-side excitation under the proposed suppression scheme are illustrated in Fig. 8.

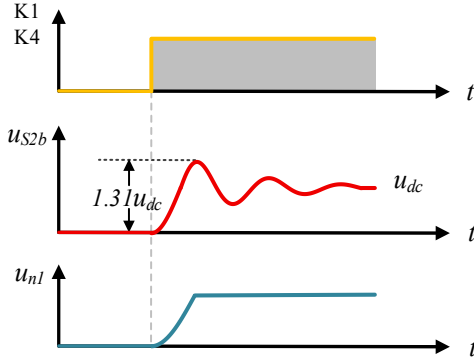


Fig. 8. Voltages of switch S2b and transformer primary after adding the suppression circuit.

Ideally, the peak resonant voltage decreases as L_r and C_r increase. However, a larger L_r leads to a significant duty cycle loss, which reduces the output voltage magnitude.

Furthermore, a minor resonance between L_r and C_r occurs prior to the main resonance between L_{lk} and C_s , which potentially compromises the spike suppression effectiveness. Additionally, the practical inverter system involves other parasitic elements, such as the transformer winding capacitance and line capacitances. Therefore, a comprehensive consideration is required when determining the optimal values for L_r and C_r . The relationship between the value of C_r and the peak resonant voltage is illustrated in Fig. 9:

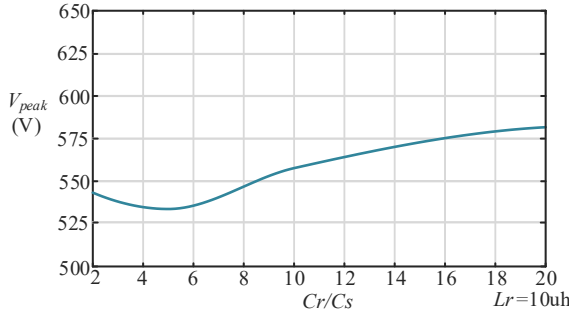


Fig. 9. Relationship between C_r values and resonant peak voltages.

To further suppress the voltage spikes, an additional passive snubber circuit, as proposed in [13], can be integrated into the existing scheme, with its specific structure illustrated in Fig. 10. This snubber consists of a feedback transformer and a rectifier. The turns ratio of the feedback transformer is designed to be slightly higher than that of the main transformer. The rectifier bridge is connected to the DC source, while the secondary side of the feedback transformer is connected in parallel with the secondary side of the main transformer. When resonance occurs on the secondary side of the main transformer and the voltage exceeds the nominal operating level, this passive snubber circuit redirects the excess energy back to the DC source. This mechanism effectively clamps the voltage within the normal range and suppresses the peak voltage spikes. By combining these two schemes, the voltage spikes can be suppressed more effectively.

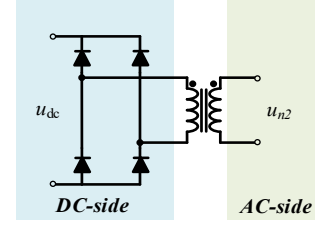


Fig. 10. Passive snubber circuit using transformer feedback.

2.3 Duty Cycle Loss Analysis and Compensation

In HFL inverters, the transformer leakage inductance prevents instantaneous changes in the inductor current. Consequently, during the switching commutation period, a finite time interval is required for the primary-side current to ramp up to the desired magnitude. During this interval, the primary-side current is insufficient to meet the combined demands of the transformer's excitation current and the load's output current. As a result, the secondary-side freewheeling paths remain conductive, effectively short-circuiting and clamping the secondary windings to zero voltage. Consequently, the output voltage of the transformer drops to zero during this commutation period. During this period, although the driving signals and voltage have been applied to the primary side, no effective voltage is delivered to the secondary side. This interval, characterized by the presence of gate pulses but the absence of active power transfer, is known as the duty cycle loss phenomenon. Notably, this effect becomes more significant when the series inductor L_r is integrated into the primary side. The duty cycle loss directly diminishes the output voltage magnitude of the inverter. To eliminate these adverse effects, the duty cycle loss can be analytically calculated and then compensated for by adjusting the switching timings during the modulation process.

To accurately calculate the duty cycle loss and achieve effective compensation, the analytical formula is derived based on the circuit parameters. The ideal duty cycle (neglecting the duty cycle loss) and the volt-second product of the cyclo-converter's output square wave are defined as follows:

$$D(\alpha) = m \cdot \sin(\alpha), \quad \alpha \in (0, \pi) \quad (8)$$

$$S = U_{n2} \cdot D(\alpha) = U_{n2} \cdot m \cdot \sin(\alpha) \quad (9)$$

The duty cycle loss caused by the transformer leakage inductance is given by:

$$D_{\text{loss}}(\alpha) = \frac{t_{\text{loss}}}{T} = \frac{2I_m \cdot \sin(\alpha) \cdot L_{lk}}{U_{dc} \cdot T} \quad (10)$$

Where I_m denotes the peak amplitude of the output current, and t_{loss} represents the duration of the duty cycle loss. After integrating the series inductor L_r , the total commutation interval is expressed as:

$$D_{\text{loss}}'(\alpha) = \frac{t_{\text{loss}}'}{T} = \frac{2I_m \cdot \sin(\alpha) \cdot (L_r + L_{lk})}{U_{dc} \cdot T} \quad (11)$$

As evidenced by the equation, the duty cycle loss is determined by the magnitudes of both the series inductance L_r and the transformer leakage inductance L_{lk} . A higher value of L_r results in a more pronounced duty cycle loss. Under these conditions, the actual volt-second product of the cyclo-converter's output square wave is expressed as:

$$S' = U_{n2} \cdot (D_\alpha - D_{\text{loss}}) \\ = U_{n2} \left[m \sin(\alpha) - \frac{2I_m \cdot \sin(\alpha) \cdot (L_r + L_{lk})}{U_{dc} \cdot T} \right] \quad (12)$$

Equation (12) can be simplified to:

$$S' = U_{n2} \cdot \sin(\alpha) \left(m - \frac{2I_m \cdot L_{\text{loss}}}{U_{in} \cdot T} \right) \quad (13)$$

As can be inferred, the proposed method requires no complex modifications to the existing modulation framework. By simply introducing a calculated offset to the modulation index, the volt-second product attenuation caused by duty cycle loss can be effectively counteracted. This allows the volt-second product of the output square wave to be restored to its nominal level, thereby eliminating the adverse impact of duty cycle loss on the output AC voltage magnitude.

3. EXPERIMENTAL VERIFICATION

To verify the voltage overshoot suppression capability and energy-saving characteristics of the proposed hybrid snubber, an experimental HFL inverter, as shown in Fig. 11, is employed as a unified testing platform. Comparative tests are conducted among the proposed LC resonant suppression scheme, the conventional RC snubber, and the feedback transformer-based scheme. The evaluation focuses on the performance discrepancies in both voltage overshoot mitigation and power loss, providing experimental evidence for the optimal selection of snubber configurations.

TABLE I

SPECIFICATIONS OF THE INVERTER PROTOTYPE

Parameter	Symbol	Value
DC-side voltage	V_{DC}	400V
AC-side voltage	V_{AC}	220Vrms
Switching frequency	f_{sw}	20kHz
Main transformer turns ratio	n_{MT}	1:1
Snubber transformer turns ratio	n_{ST}	1:1.05
Rated power	P	1kW
MOSFET	-	C3M0021120K
Diode	-	CH10S65C3
Series inductor	L_r	10uH
Parallel capacitor	C_r	1nF

The detailed parameters and component specifications of the HFL inverter used in the experiments are summarized in Table 1. Throughout the testing process, the converter operates in DC-AC mode under an open-loop control strategy. A purely resistive load is employed to ensure consistent experimental conditions and to guarantee the reliability of the comparative results. During the testing process, the performance of each

scheme is evaluated sequentially. First, the conventional RC snubber is tested to record its peak resonant voltage and power consumption. Subsequently, the scheme utilizing a feedback transformer is implemented to assess its voltage overshoot suppression capability and the corresponding power loss under identical operating conditions. Following this, the proposed LC resonant suppression scheme is integrated into the system to observe its operational state and performance metrics. Finally, the hybrid suppression scheme, which combines both the feedback transformer and the LC resonant circuit, is evaluated. To ensure a comprehensive comparison, the efficiency variations across different schemes are recorded at both the rated power and various partial load conditions.

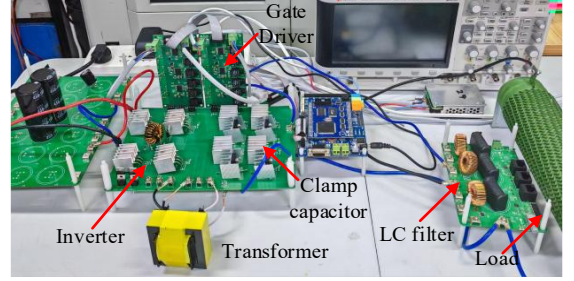


Fig. 11. Prototype of the inverter

Fig. 12 presents a performance comparison of the secondary-side voltage and current waveforms under various suppression strategies.

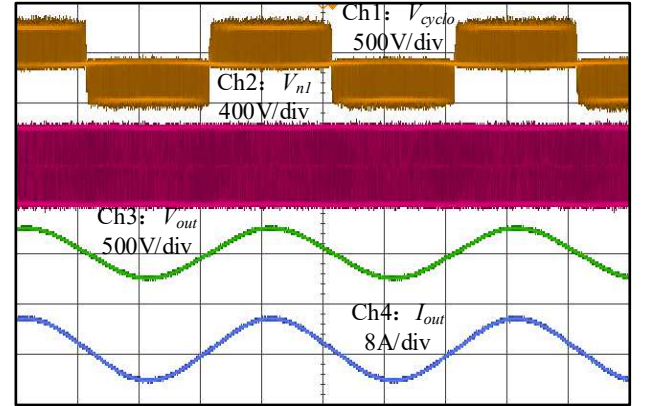


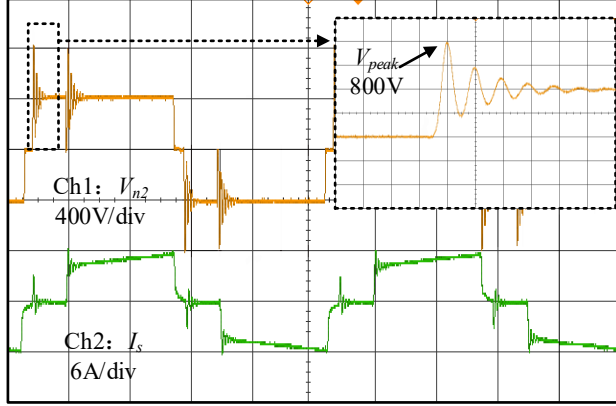
Fig. 12. Output waveforms of the inverter with the proposed scheme.

As shown in Fig. 13(a), the voltage spike across the AC-side switches without any suppression is severe, with the initial overshoot reaching 800 V. By integrating an RC snubber, the spike is reduced to 600 V in Fig. 13(b), though it incurs a high power loss of approximately 10 W, limiting its practicality. The feedback transformer scheme, shown in Fig. 13(c), exhibits a slightly better suppression capability by lowering the peak to 560 V with a reduced loss of 4 W. The suppression performance of the proposed snubber is shown in Fig. 12(c), where the peak voltage overshoot is reduced to 530 V while introducing only a small amount of additional power loss. The additional losses introduced by the proposed scheme are mainly associated with the added inductor, capacitor, and clamping

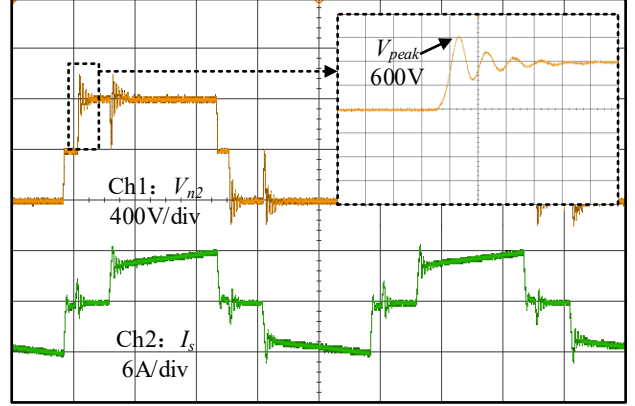
diode, with the majority of the losses occurring in the clamping diode. When the primary-side voltage reaches u_{dc} , the clamping diode feeds the excess voltage back to the DC source. During this process, current flows through the clamping diode, resulting in conduction losses. However, since the clamping current is relatively small, the resulting power loss is also very

low. In the experiment, the power loss was determined by measuring the voltage and current of the additional circuit. The measured power loss was approximately 1 W.

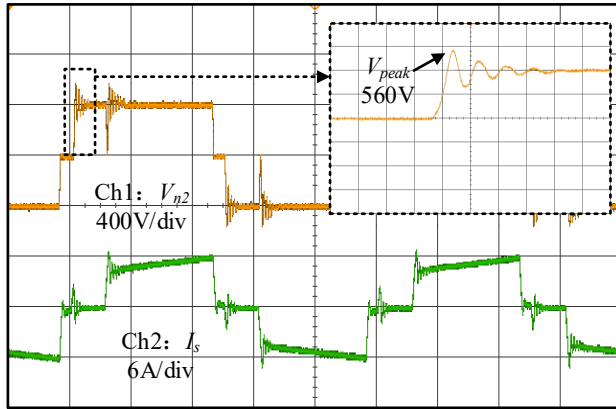
Finally, Fig. 13(e) demonstrates the best performance achieved by the hybrid scheme, which combines the proposed strategy with the feedback transformer.



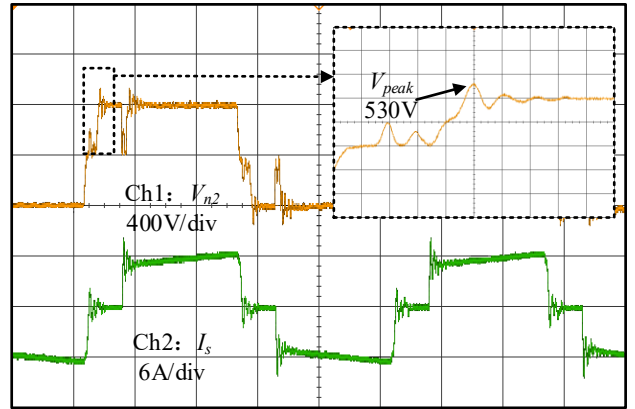
(a)



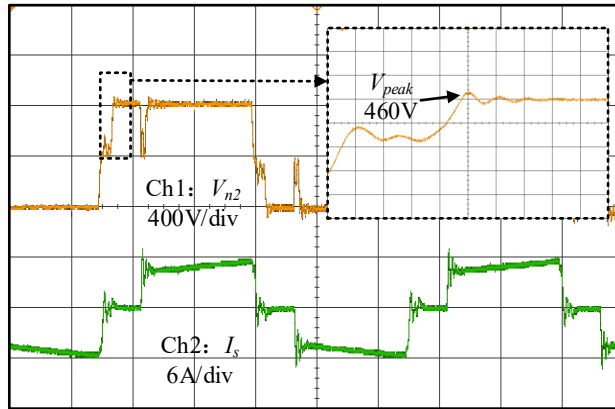
(b)



(c)



(d)



(e)

Fig. 13. Secondary-side voltage and current waveforms under different suppression schemes (a) without suppression. (b) with the parallel RC snubber. (c) with the feedback transformer scheme. (d) with the proposed suppression scheme. (e) with the hybrid scheme.

This hybrid approach suppresses the voltage spike to 460 V while maintaining a total loss of approximately 4 W.

Experimental results demonstrate distinct differences in the voltage overshoot suppression performance among the three snubber configurations. Both the proposed LC suppression circuit and the hybrid snubber exhibit superior effectiveness, significantly damping the oscillations on the AC side of the converter. These solutions effectively constrain the peak voltage overshoot to a relatively low level while maintaining minimal power loss, thereby exerting a negligible impact on the overall inverter efficiency.

4. Conclusion

To address the transformer leakage inductance resonant voltage spikes in HFL inverters for small-and-medium power photovoltaic applications, this paper proposes a primary-side resonance-based passive suppression strategy. By reshaping the primary-side voltage waveforms, the proposed scheme effectively mitigates resonant peaks without the need for additional active devices or complex control logic. Furthermore, duty cycle loss compensation is simultaneously integrated. The proposed topology is characterized by its simple structure and low implementation difficulty.

Validation results from a 1kW experimental prototype demonstrate that the proposed scheme reduces the inverter voltage spikes from 800 V to 530 V, with an auxiliary power loss of only 1 W. This is significantly lower than that of the conventional RC snubber (approximately 10 W), leading to a marked improvement in overall converter efficiency. A comprehensive comparison among various snubber configurations confirms that the proposed solution offers distinct advantages in terms of peak suppression effectiveness, power loss, and circuit simplicity.

In summary, the strategy proposed in this paper features superior voltage spike suppression, structural simplicity, low power dissipation, and controllable cost. By effectively addressing the inherent technical bottlenecks of HFL inverters, this approach is well-suited for engineering applications in small-and-medium power photovoltaic power conversion systems.

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