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Abstract

This paper investigates a minimal-cell half-bridge Modular Multilevel Converter (MMC) employing modified sinusoidal pulse-width modulation (SPWM) strategies aimed at improving output voltage quality while maintaining reduced hardware complexity. Although several advanced MMC topologies have been proposed to enhance harmonic performance, they typically require additional submodules (SMs), hybrid switching devices, or complex control schemes, making them impractical for low- and medium-power applications. The proposed modulation approach is based on structured waveform synthesis, where a stepped voltage waveform is combined with a selectively applied high-frequency SPWM signal to redistribute dominant harmonic components toward higher frequencies, enabling effective suppression of low-order harmonics. Three modified SPWM-based modulation strategies are proposed and evaluated against conventional Walsh-based modulation MMC configurations in terms of total harmonic distortion (THD) and harmonic spectrum, using Fast Fourier Transform (FFT) analysis in compliance with IEEE harmonic standards. Detailed MATLAB/Simulink simulations are carried out to validate the proposed methods under various loading conditions. The results demonstrate that the three proposed approaches achieve THD values of 5.5264%, 5.4856%, and 5.5116% using 6, 4, and 4 SMs respectively, compared to 33.44% for a conventional 4-SM MMC, representing a reduction of over 83%. Furthermore, under a three-phase RL load, the second proposed approach achieves an output current THD of only 2.0012%, while the line and phase voltage THD (7.0491% and 7.1074%, respectively) remain above the IEEE 519-2022 limit at the converter output terminals prior to filtering, with the residual distortion concentrated at the 5th harmonic. These results confirm that comparable harmonic performance to conventional higher-SM-count MMC configurations can be achieved with significantly fewer hardware resources, making the proposed solution well suited for low- and medium-power inverter applications, provided a passive output filter is included to achieve full voltage-side grid compliance.

Keywords: Power Electronics, Multilevel Converter, Modular Multilevel Inverter, SPWM, Total Harmonic Distortion

1. Introduction

The growing demand for high efficiency, high-power density,and low-distortion power conversion in modern energy conversion and electric drive systems has intensified research into advanced DC-AC converter topologies. Conventional two-level voltage source inverters,while simple in structure,suffer from high voltage stress on semiconductor devices and poor harmonic performance in medium- and high-power applications [1]. As a result,bulky output filters are often required to meet power quality and electromagnetic compatibility standards [1, 2],leading to increased system size,losses,and overall cost [1, 3].

Multilevel-converters have emerged as an effective solution to these limitations by synthesizing output voltages with multiple discrete levels,thereby producing waveforms that more closely approximate a sinusoidal shape. This operating principle significantly reduces THD,electromagnetic-interference,and dv/dt stress on power devices,making multilevel topologies particularly suitable for high-power applications [4]. Recent studies continue to confirm that multilevel converter structures offer superior harmonic performance compared to conventional two-level inverters,while also enabling improved scalability and efficiency [5].

Among multilevel converter topologies,the MMC has attracted considerable attention due to its modular architecture,scalability to very high voltage levels,and excellent output voltage quality.Initially developed for high-voltage direct current (HVDC) transmission systems,the MMC consists of cascaded and independently controlled SMs arranged in upper and lower arms for each phase,enabling flexible voltage

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synthesis,redundancy,and enhanced fault tolerance [3]. Owing to these advantages,MMCs have become the preferred topology for HVDC systems [1, 6],and are increasingly investigated for medium-voltage drives and renewable energy integration [3, 7]. The scalability and efficiency of the modular structure make it the standard for high-voltage transmission [1, 6],and its expansion into medium-voltage sectors and photovoltaic (PV) systems further highlights its versatility in handling diverse power quality requirements across different grid-tied applications [3, 7].

Despite these benefits,conventional MMC implementations typically require a large number of SMs per arm,along with complex modulation and capacitor voltage balancing strategies. This leads to increased hardware cost,control complexity,and computational burden,particularly in applications where ultra-high voltage capability is not strictly required [8].

To further enhance voltage waveform quality and suppress low-order harmonics,several studies have explored MMC structures employing advanced multi-level submodule topologies. For example,Z. Huang et al. [9] proposed a hybrid MMC topology that combines standard low-frequency Half-Bridge SMs (HB-SMs) with a high-frequency Heterogeneous Cross-Connect Module (HCCM) based on Silicon Carbide (SiC) MOSFETs. In this configuration,the HB-SMs handle the bulk of the power and generate the fundamental staircase voltage waveform,while the HCCM performs high-speed switching to smooth the waveform and reduce harmonic distortion. Although this approach offers notable efficiency gains through SiC technology, it inherently increases gate drive complexity and overall system cost. Similarly,J. Liu and D. Dong [10] introduced a Flying Capacitor (FC) Hybrid MMC that reduces the total submodule count by combining HB-SMs with FC units capable of producing additional voltage levels. While this topology successfully increases the number of output levels,it introduces significant challenges in capacitor voltage balancing and increases the physical footprint of the converter. Although these approaches deliver excellent harmonic performance,they generally require more switching devices,additional capacitors,and complex control schemes,resulting in higher cost and greater implementation difficulty [6].

To address the lack of a low-complexity,cost-effective MMC solution that maintains acceptable harmonic performance for low- and medium-power applications such as distributed renewable energy systems, small-scale motor drives,and EV auxiliary converters recent research has shifted toward reduced-cell and minimal-structure MMC configurations [11]. These aim to preserve acceptable harmonic performance while significantly lowering the number of power devices and simplifying modulation and control requirements. In such reduced-cell MMCs,modulation strategies play a critical role in determining output voltage quality,harmonic-distribution,switching losses,and capacitor voltage behavior [1, 6]. Recent literature indicates that appropriate modulation techniques can substantially improve harmonic performance even when the number of SMs is limited [8, 10]. Among various modulation approaches,SPWM remains attractive due to its simplicity,ease of implementation,and predictable harmonic characteristics [2]. In particular, SPWM-based methods tend to shift dominant harmonic components toward higher frequencies,where filtering requirements are less demanding [7, 12]. However,when directly applied to reduced-cell MMC configurations, conventional SPWM strategies may not fully exploit the available voltage synthesis capability,resulting in increased low-order harmonic distortion [4, 9]. To the best of the authors' knowledge,no prior work has simultaneously addressed reduced hardware complexity and low-order harmonic suppression in minimal-cell MMC configurations using a purely software-based modulation approach without hybrid submodule types.

Beyond the topologies already discussed, recent studies applying multicarrier PWM directly to reduced-cell MMCs illustrate the persistent difficulty of reconciling low SM count with acceptable harmonic quality. Brahmbhatt et al. [13] proposed a DC-PDPWM technique that replaces two of the four triangular carriers in a 8-SMs (4-SM/arm) MMC with constant DC levels, reporting a THD reduction from 27.55% to 21.76% in phase voltage alongside a 20% reduction in switching frequency. This confirms that carrier structure alone can meaningfully influence harmonic content; however, the resulting THD remains more than four times the IEEE 519-2022 limit of 5.0%, reflecting that the primary design objective was computational and memory efficiency rather than harmonic suppression – a different optimization target from the one addressed in this work. Similarly, Dixit and Sharma [14] compared APOD-PWM and Nearest Level Modulation (NLM) for 8-SMs MMC, reporting THD values of 22.16% and 14.82%, respectively. Even the better-performing NLM result is nearly three times higher than the THD achieved by the second proposed approach in this paper using only 4-SMs. These findings suggest that conventional carrier-based and nearest-level strategies, when applied without structural modification of the underlying switching framework, are inherently limited in minimal-cell configurations – motivating the Walsh-function-based staircase framework adopted here.

Furthermore,the integration of a passive output filter,such as an LCL filter,is anticipated to further attenuate residual harmonic components at the converter output terminals,ensuring full compliance with the IEEE 519-2022 THD limit of 5.0% at the Point of Common Coupling. Recent studies have demonstrated that LCL filters represent an effective and compact solution for harmonic suppression in multilevel converter systems,achieving THD levels well below the 5% threshold mandated by international grid standards [15].

Motivated by these observations,this paper investigates a minimal-cell half-bridge MMC operating under a modified SPWM strategy designed to improve output voltage quality while maintaining reduced hardware complexity. Unlike existing hybrid approaches that rely on additional submodule types or advanced switching devices,the proposed method achieves comparable harmonic performance using only standard half-bridge SMs by optimizing the waveform synthesis through a modified Walsh-SPWM strategy. Specifically, a basic stepped voltage waveform is used to generate the fundamental voltage component,while a selectively applied high-frequency SPWM

signal mitigates low-order harmonics. This enables low-THD operation without increasing the number of SMs or introducing complex capacitor voltage balancing or control schemes [16],making the proposed solution particularly well suited for low- and medium-power inverter applications.

The main contributions of this work are as follows:

1. Development of a simplified half-bridge MMC configuration with a reduced number of SMs,targeting low- and medium-power applications where hardware simplicity and cost-effectiveness are prioritized [8, 10].
2. Proposal of a modified Walsh-SPWM waveform synthesis strategy that suppresses low-order harmonic components and achieves low-THD output without requiring hybrid submodule types or additional hardware [10].
3. Validation of the proposed approach through detailed MATLAB/Simulink simulations,including time-domain waveform analysis and frequency-domain evaluation using FFT and THD metrics,demonstrating the effectiveness of the proposed modulation strategy under realistic operating conditions [16].

2. Theoretical Background

2.1. MMC Voltage Synthesis

The MMC is composed of cascaded SMs arranged in upper and lower arms for each phase. Each arm typically consists of a series connection of half-bridge Submodules (HB-SMs) and an arm inductor. By selectively inserting or bypassing individual SMs,the MMC synthesizes a staircase output voltage with multiple discrete levels. This multi-level voltage synthesis mechanism allows the converter to approximate a sinusoidal waveform with significantly reduced harmonic distortion and lower voltage stress across semiconductor devices compared to conventional two-level converters [1].

For a single phase-leg,the output voltage is obtained as the difference between the upper- and lower-arm voltages and can be expressed as:

$$v_o(t) = v_l(t) - v_u(t) \tag{1}$$

where v_u and v_l denote the voltages of the upper and lower-arm,respectively. In accordance with the analysis in [16],the internal dynamics are also governed by the common-mode voltage,which influences the circulating current.

If each arm contains N SMs and each SM capacitor voltage is approximately V_c,the arm voltage can be expressed as the sum of the inserted SM voltages:

$$v_u = \sum_{k=1}^{N} s_{u,k} V_{c,u,k}, \quad v_l = \sum_{k=1}^{N} s_{l,k} V_{c,l,k} \tag{2}$$

where $s_{u,k}$ and $s_{l,k} \in \{0, 1\}$ represent the switching states of the k^{th} SM in the upper and lower arms. By controlling the number of inserted SMs,the converter generates a staircase waveform with up to $L = N + 1$ voltage levels in a conventional symmetric configuration [6].

Where L is the voltage level, and N is the number of SMs in each arm.

Recent MMC studies emphasize that increasing the number of SMs improves voltage resolution and reduces harmonic distortion,particularly in HVDC applications [1],[6]. However,this also increases hardware complexity,control effort,and system cost [3],[4]. Consequently,reduced-cell MMC configurations have been proposed to maintain acceptable harmonic performance while limiting the number of SMs [8],[10].

2.2. IEEE Harmonic Standards

To ensure the reliability of the electrical grid,MMCs must adhere to strict power quality guidelines,primarily the IEEE 519-2022 standard. As reviewed by Shelar et al. [17],the recent 2022 revision provides a comprehensive framework for controlling harmonics,maintaining the critical THD limit of 5.0% at the Point of Common Coupling (PCC). Adherence to these limits is vital for protecting network infrastructure; for instance,Czernorucki et al. [18] highlight that high harmonic content can lead to significant thermal stress and design complexities in HVDC converter transformers,which are governed by the IEC/IEEE 60076-57-129 standard. By utilizing advanced modulation in a minimal-cell configuration,this research focuses on shifting harmonic energy to higher frequencies to prevent such parasitic heating and ensure full compliance with the latest international grid requirements.

It is worth noting that this limit of 5.0% applies only at the PCC with the grid,and converter output THD values prior to filtering may differ from those measured at the PCC.

2.3. Total Harmonic Distortion

The quality of the synthesized output voltage is commonly evaluated using THD,defined as:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \tag{3}$$

where V_1 is the RMS value of the fundamental component and V_n represents the RMS value of the n^{th} harmonic component. THD provides a quantitative measure of waveform distortion and is widely used to assess converter performance in both time-domain and frequency-domain analyses. In practical systems,only a finite number of harmonic components are considered,typically obtained via FFT analysis.

Low-order harmonics,such as the 3rd,5th,and 7th,exert the most significant impact on power quality,torque ripple in motor drives,and grid compliance within renewable energy systems [1],[7]. As highlighted by Barros et al. [1] and Wang et al. [7],these components can destabilize grid-tied PV systems if not properly managed. Consequently,modulation techniques that suppress or shift dominant harmonics toward higher frequencies are preferred,as high-frequency content is more effectively mitigated using smaller,less expensive passive components [2],[12]. According to Patel and Sood [2] and the benchmarking studies by Chaudhary et al. [12],the strategic use of multicarrier SPWM and hybrid methods is essential to

meet stringent harmonic standards while minimizing the physical footprint of the output filters. In reduced-cell MMC structures,THD performance becomes strongly dependent on the adopted modulation strategy,since the number of available voltage levels is limited compared to large-scale MMC systems [8].

2.4. PWM and Modulation Methods

Modulation techniques determine the switching states of the SMs and directly influence output voltage quality,switching losses,and capacitor voltage behavior. In MMC systems,several modulation approaches have been reported in recent literature [1],including Nearest Level Control (NLC),Carrier-Based Pulse Width Modulation (CB-PWM),Phase-Shifted PWM (PS-PWM),Selective Harmonic Elimination (SHE),and Space Vector Modulation (SVM).

Nearest Level Control is commonly used in high-level MMC systems because of its low switching frequency and straightforward implementation. However,its performance degrades when the number of voltage levels is small [11]. Carrier-based PWM methods,particularly SPWM,are widely adopted due to their simplicity and predictable harmonic spectrum. In SPWM,a sinusoidal reference signal is compared with high-frequency carrier signals to generate gating pulses. The resulting harmonic spectrum is concentrated around the switching frequency and its sidebands,reducing low-order harmonics in the output voltage [19]. Recent studies show that advanced PWM techniques can significantly improve harmonic performance even in MMCs with limited voltage levels [5]. However,conventional SPWM may not fully exploit the discrete voltage synthesis capability of reduced-cell MMCs,leading to residual low-order distortion [2].

2.5. Capacitor Voltage Balancing Strategies

In MMC systems,each SM contains a floating capacitor whose voltage must be maintained within an acceptable range. Proper capacitor voltage balancing is essential to ensure uniform voltage stress across devices and stable converter operation. The capacitor voltage dynamics of a single SM can be described as:

$$C\frac{dV_{c,k}}{dt} = S_k i_{arm} \tag{4}$$

where C is the SM capacitance and i_{arm} is the arm current. In conventional MMCs with many SMs,capacitor voltage balancing is achieved using sorting algorithms,circulating current control,redundant state selection,and predictive control techniques [4].

Recent works propose advanced balancing strategies integrated with modulation schemes to improve voltage stability and reduce computational burden [20]. However,in reduced-cell MMC configurations,the balancing problem becomes less computationally intensive due to the smaller number of SMs,but voltage ripple can increase if modulation is not properly designed. Therefore,a simplified yet effective modulation framework can inherently assist in maintaining acceptable capacitor voltage regulation while avoiding complex balancing algorithms [9].

2.6. Walsh Function Analysis

Walsh functions form a complete orthogonal set of binary-valued basis functions (± 1) over a normalized time interval $t \in [0, 1)$. Unlike sinusoidal Fourier functions,Walsh functions are piecewise constant,allowing any finite-energy periodic waveform to be uniquely decomposed into a Walsh series. This property makes them particularly well-suited for analyzing and synthesizing switching signals in power electronic converters, whose output voltages feature discrete levels and abrupt transitions [21][22].

The Walsh functions are indexed by a sequency number,which represents the number of zero-crossings per unit interval. The first-order Walsh function $W_1(t)$,also known as the fundamental Walsh function,is defined as:

$$W_1(t) = \begin{cases} +1, & 0 \le t < \frac{T}{2} \\ -1, & \frac{T}{2} \le t < T \end{cases} \tag{5}$$

where T is the fundamental period. This function produces a single sign change per period,directly corresponding to a square wave at the fundamental frequency,making it suitable for generating the basic two-level switching pattern of a half-bridge SM [22].

The second-order Walsh function $W_2(t)$ introduces an additional zero-crossing per period and is defined as:

$$W_2(t) = \begin{cases} +1, & 0 \le t < \frac{T}{4} \\ -1, & \frac{T}{4} \le t < \frac{3T}{4} \\ +1, & \frac{3T}{4} \le t < T \end{cases} \tag{6}$$

Recent studies confirm that Walsh function representations efficiently simplify harmonic analysis in multilevel converters by converting complex nonlinear equations into more tractable linear ones,enabling systematic control of dominant harmonics [21][22]. Their orthogonality and binary nature allow efficient voltage synthesis,reduced computational complexity,and improved insight into the converter's harmonic characteristics [23]. In the context of the proposed minimal-cell MMC,this Walsh-based switching framework establishes a structured foundation upon which the modified SPWM signal is superimposed to further suppress residual low-order harmonics [24].

2.7. Circulating Current

2.7.1. Physical Origin and Mathematical Definition

In an MMC,the circulating current (i_{diff}) is an internal current that flows within the phase legs but does not exit the converter to the AC load [25]. It arises from the instantaneous voltage differences between the constant DC-link voltage (V_{DC}) and the sum of the SM voltages in the upper and lower arms [26].

Mathematically,it is defined as the average of the upper (i_u) and lower (i_l) arm currents:

$$i_{diff} = \frac{i_u + i_l}{2}$$

2.7.2. Impact on System Health and Efficiency

While i_{diff} is decoupled from the AC output,its presence significantly degrades the converter's performance [26]. Key impacts include:

- Conduction Losses: It increases the RMS value of the arm currents,leading to higher I^2R losses in the semiconductor switches and arm inductors [25].
- Capacitor Voltage Ripple: The second-order harmonic component interacts with fundamental currents to cause fluctuations in SM capacitor voltages,which can lead to instability if not suppressed .
- Component Stress: It increases the peak current handled by the switches,necessitating hardware over-sizing [26].

3. Proposed Hybrid Modulation Strategies

In this paper,three different approaches are discussed to control the switching states of the converter:

- **First and Second Approaches:** These methods integrate the first and second-order Walsh functions with a Modified SPWM signal to determine the switching states. Based on the multiband control technology developed by Li et al. [24],the Walsh functions are used to establish a structured staircase framework,while the SPWM refines the switching transitions. This hybrid approach aligns with the recent theoretical frameworks for MMC control that utilize multi-time scale analysis to manage complex switching states [27].
- **Third Approach:** For the last method, only a Modified SPWM signal is used to control the switching states of the converter. This approach functions without the Walsh framework,providing a baseline to compare the performance of different modulation methods in cascaded and modular architectures,as explored in recent comparative studies of transformerless inverters [28].

4. First Approach to Minimum Cell MMC

4.1. Converter Topology

4.1.1. Proposed MMC Configuration and Phase-Leg Dynamics

The converter topology investigated in this work is based on a reduced-cell half-bridge MMC. As illustrated in Fig. 1, the MMC phase-leg consists of an upper arm and a lower arm, each composed of 3 HB-SMs connected in series with an arm inductor (L_{arm}) and its internal resistance (R_{arm}). This modular structure enables scalable voltage synthesis while maintaining reduced voltage stress on the semiconductor devices and improved output waveform quality compared to conventional two-level converters [1]. According to Tebaldi and Zanasi [16], the mathematical modeling of such systems must account for the interaction between the DC-link voltage V_{dc} and the individual arm dynamics:

$$\frac{V_{dc}}{2} - v_u - L_{arm}\frac{di_u}{dt} - R_{arm}i_u = v_o \tag{7}$$

$$-\frac{V_{dc}}{2} + v_l + L_{arm}\frac{di_l}{dt} + R_{arm}i_l = v_o \tag{8}$$

These equations highlight the role of the arm inductor in suppressing high-frequency components generated by the switching actions of the HB-SMs.

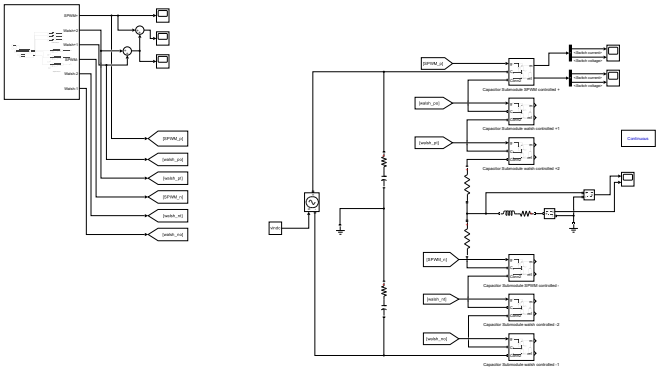


Figure 1: MMC schematic.

4.1.2. Half-Bridge Submodule Structure and Switching Logic

Each SM employed in the proposed MMC is a half-bridge topology consisting of two complementary semiconductor switches (MOSFETs) and a floating capacitor, as shown in Fig. 2. The HB-SM operates in two fundamental states based on the gating signal S:

1. **Inserted State ($S = 1$):** The upper switch is conducting while the lower switch is blocked. The capacitor voltage V_c is added to the arm voltage string, and the capacitor is either charged or discharged depending on the direction of the arm current i_{arm}.
2. **Bypassed State ($S = 0$):** The lower switch is conducting and the upper switch is blocked. The SM output voltage is zero, and the capacitor voltage remains constant (neglecting leakage).

The instantaneous output voltage of a single HB-SM can be mathematically defined as:

$$v_{SM}(t) = S(t) \cdot V_c(t) \tag{9}$$

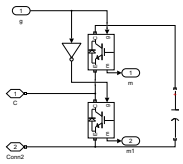


Figure 2: Half-bridge submodule structure.

4.1.3. Mathematical Synthesis of Arm and Output Voltages

The arm voltages of a single MMC phase-leg are determined by the cumulative contribution of the inserted SMs. By selectively inserting or bypassing the HB-SMs,the MMC generates a stepped output voltage. Assuming balanced capacitor voltages,the total number of achievable output voltage levels is $L = 4$ for a minimal-cell configuration where $N = 3$,the resolution of the staircase is limited,which typically increases the dv/dt stress [5]. This limitation is precisely why a modified SPWM strategy is required to bridge the gaps between the coarse voltage steps.

4.1.4. Capacitor Dynamics and Energy Storage Requirements

Each HB-SM capacitor functions as a localized energy storage element. The nominal voltage is maintained at:

$$V_c \approx \frac{V_{dc}}{N} \tag{10}$$

However,because the arm current i_{arm} flows through the capacitors during the Inserted state,the voltage fluctuates. The dynamics are defined by:

$$C_{SM} \frac{dV_{c,k}}{dt} = S_k \cdot i_{arm} \tag{11}$$

In reduced-cell MMCs,the capacitor voltage ripple is more pronounced because fewer SMs are available to distribute the energy variation. Huang et al. [9] suggest that this ripple can distort the output voltage if the modulation index is high. To mitigate this,the proposed strategy utilizes a hybrid synthesis to ensure that the capacitor charging cycles are balanced across the fundamental period without requiring the computationally heavy sorting algorithms found in larger systems [11].

4.1.5. Gating Signal Structure

The gating signals in this work are generated through a specialized hybrid waveform synthesis structure,as shown in Fig. 3. This method partitions the task of voltage generation into two distinct functional layers:

1. **Low-Frequency Layer (Walsh Functions):** These provide the fundamental staircase structure. Because Walsh functions are orthogonal and piecewise-constant [10],they allow the controller to set the primary steps of the MMC with minimal switching transitions.
2. **High-Frequency Layer (Modified SPWM):** This layer operates only during the transition periods of the staircase. By comparing a sinusoidal reference with a high-frequency carrier,it fills the gaps between the Walsh-generated steps.

This partitioning allows for a best-of-both-worlds scenario: the low switching losses of NLC-like control and the high harmonic performance of SPWM. As noted by Barros et al. [1],such variable-frequency or hybrid approaches are essential for optimizing the efficiency of modern MMCs. This dual-layer logic is implemented using a functional partitioning block that ensures the SMs are not over-stressed by high-frequency switching throughout the entire cycle [7, 10].

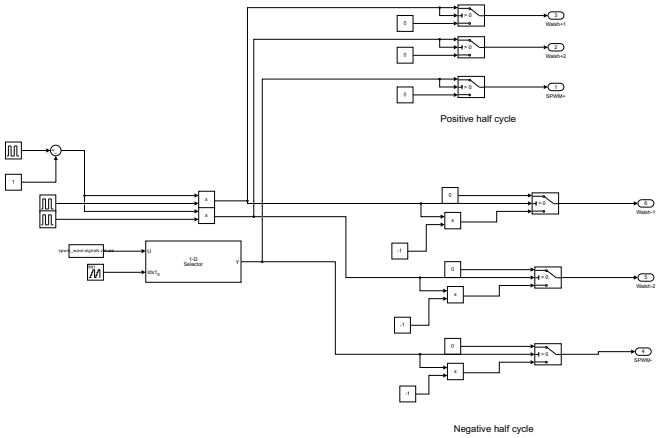


Figure 3: Controller schematic.

4.2. SPWM Method

The core innovation of this research lies in its hybrid modulation framework,which aims to reconcile the low switching losses of fundamental-frequency staircase synthesis with the superior spectral characteristics of high-frequency SPWM.

4.2.1. Principle of Hybrid Waveform Synthesis

In this work, a modified SPWM method is utilized to improve the harmonic performance of a reduced-cell MMC. The modulation logic is partitioned into two distinct functional layers. First, a basic stepped waveform is generated by switching and combining several orthogonal square waves, which represents the discrete insertion and bypassing of MMC SMs to create multiple voltage levels [10]. While this stepped waveform effectively synthesizes the fundamental AC component, it inherently contains high-magnitude low-order harmonics — specifically the 5th, 7th, and 11th — due to the coarse voltage resolution typical of minimal-cell configurations [6]. To mitigate these spectral deficiencies, a high-frequency SPWM signal is added on top of the stepped waveform, acting only during selected time intervals where staircase transitions occur, effectively smoothing the transitions and reducing the magnitude of low-order distortions [5].

4.2.2. *Mathematical Formulation of the Modulating Signal*

The proposed modified SPWM strategy relies on a duty cycle carrier (modulating signal),denoted as $x(t)$, which is piecewise-defined to synchronize with the Walsh-generated steps. The modulation operates over a normalized fundamental period $T_1 = 1/f_1$. In the proposed system,f_1 is set to 100 Hz (representing a half-cycle frequency for a 50 Hz system) to align with the symmetry of the half-bridge SMs.

The duty cycle modulating signal $x(t)$ is mathematically defined by the following piecewise sinusoidal function:

$$x(t) = \begin{cases} \sin(2\pi f_2 t), & 0 < t < \dfrac{T_1}{5} \\ \sin\left(2\pi f_2 t - \dfrac{\pi}{2}\right), & \dfrac{T_1}{5} < t < \dfrac{2T_1}{5} \\ 0, & \dfrac{2T_1}{5} < t < \dfrac{3T_1}{5} \\ \sin(2\pi f_2 t - \pi), & \dfrac{3T_1}{5} < t < \dfrac{4T_1}{5} \\ \sin\left(2\pi f_2 t - \dfrac{3\pi}{4}\right), & \dfrac{4T_1}{5} < t < T_1 \end{cases} \tag{12}$$

In this formulation,f_2 represents the frequency of the truncated sinusoidal function used for modulation, established at 125 Hz for the target minimal-cell Half-Bridge MMC. Strategic frequency selection is essential to ensure that sideband harmonics are shifted away from the sensitive low-order zone [1, 2].

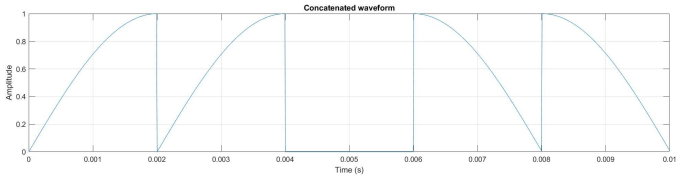


Figure 4: Duty cycle carrier signal.

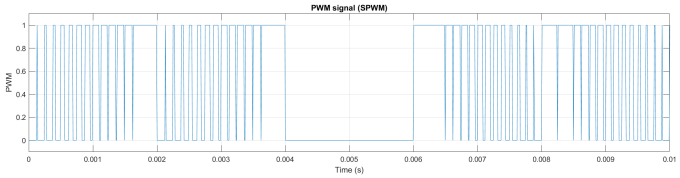


Figure 5: Modified SPWM signal.

4.2.3. *Harmonic Distribution and Spectral Characteristics*

Compared to conventional PWM operation,the proposed SPWM-based MMC operation significantly reduces low-order harmonics by distributing spectral energy toward higher frequencies. This spectral shifting behavior is critical for achieving lower THD and ensuring improved compliance with IEEE harmonic standards,such as IEEE 519,particularly in low- and medium-power applications where hardware complexity must be minimized [2],[5]. According to Patel and Sood [2] and Zhao et al. [5],optimizing the multicarrier frequency allows for a superior harmonic profile without the need for extensive physical filtering.

As discussed in recent studies by Girona et al. [8] and Huang et al. [9],the selective application of PWM prevents the high switching losses associated with full-cycle SPWM while maintaining a high-quality voltage profile. This behavior is particularly advantageous for minimal-cell architectures where the number of available voltage steps—defined as $L = 2N + 1$—is otherwise insufficient to meet grid codes without significant passive filtering [10],[12]. As noted by Liu and Dong [10] and the benchmarking by Chaudhary et al. [12],these hybrid approaches are essential for balancing power density with strict spectral requirements.

4.2.4. *Walsh Function Control Signal*

The proposed control architecture utilizes Walsh functions as the primary logic layer to generate a discrete "staircase" reference. In this hybrid modulation scheme,the Walsh function provides the low-frequency structural framework,while a high-frequency SPWM layer is superimposed to refine the final output.

As illustrated in fig 6,the signal exhibits a symmetric five-level profile $(+2, +1, 0, -1, -2)$. This discrete-step approach offers several advantages such as optimizing power losses by concentrating high-frequency carrier action only at specific transition boundaries [5],[16],reducing the switching burden [9].

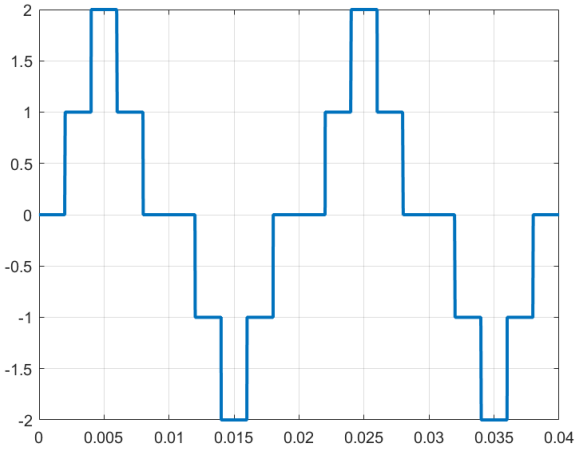


Figure 6: Walsh function control signal.

4.2.5. *Hybrid Control Signal and Implementation*

The final control signal, as depicted in Fig. 7, demonstrates the successful integration of the Walsh-based staircase framework with a high-frequency SPWM layer. Unlike conventional continuous PWM, this hybrid approach restricts high-frequency switching to specific intervals. The gating signals derived from $x(t)$ are integrated into the functional partitioning block of the MMC, mapping high-frequency switching requirements to specific SMs based on their instantaneous energy state [16]. The phase-shifted nature of $x(t)$ ensures that active modulation periods are balanced across the SMs, preventing any single SM from bearing the entirety of the high-frequency switching stress [11].

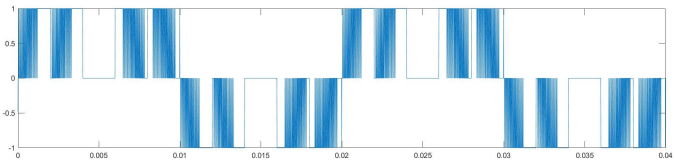


Figure 7: Hybrid control signal.

4.2.6. *Effect on Capacitor Voltage Balancing*

In minimal-cell configurations,the modified SPWM technique provides the following effects on capacitor voltage balancing:

- **Ripple Reduction:** High-frequency switching chops the arm current,preventing continuous charging or discharging of a single capacitor over an extended period [1].
- **Energy Distribution:** The phase-shifted modulating signal spreads switching actions across SMs, ensuring an even state-of-charge without complex sorting logic [11].
- **Enhanced Regulation:** The hybrid approach creates more switching opportunities than a basic staircase,allowing for more dynamic voltage adjustments per cycle [9].
- **Stability:** Selective application of PWM provides the necessary transitions for balance while keeping switching losses lower than traditional continuous SPWM [5, 16].

4.3. *Single-Phase MMC Performance Analysis*

4.3.1. *Positive/Negative Logic Switches Current and Voltage*

In this study, a complementary switching logic is implemented via the Walsh-SPWM synthesis, where the upper arm SMs are inserted when the reference signal assumes positive polarity, while the lower arm SMs remain bypassed, and vice versa during negative cycles. This strategy ensures that the DC-link voltage is never short-circuited while minimizing circulating currents (i_{circ}) that typically plague minimal-cell configurations. Figs. 8 and 9 depict the localized voltage and current transients for each arm, validating the seamless transition between the positive and negative switching states.

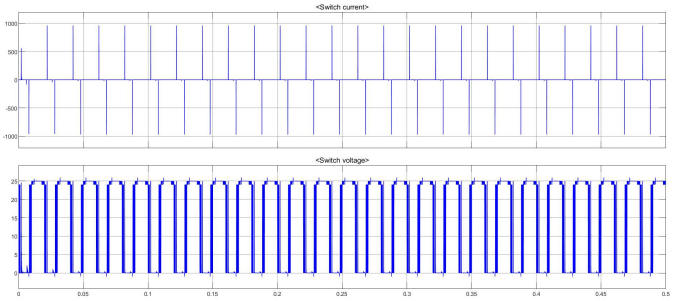


Figure 8: Positive logic switch waveforms.

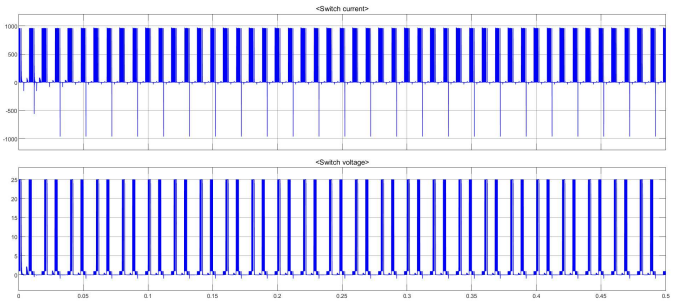


Figure 9: Negative logic switch waveforms.

4.3.2. *THD Analysis*

A comparative spectral analysis was conducted to benchmark the proposed Walsh-SPWM against conventional modulation. The FFT parameters used for all THD computations throughout this study are summarized in Table 1,ensuring consistent and accurate harmonic evaluation across all tested configurations.

Table 1: FFT Parameters for THD Computation.

Parameter	**Symbol**	**Value**
Sampling Frequency	F_s	100 kHz
Sampling Period	$T_s = 1/F_s$	10 μs
Fundamental Frequency	f_1	50 Hz
Fundamental Period	$T_0 = 1/f_1$	0.02 s
Periods Analyzed	N_{periods}	10
Observation Time	T_{obs}	0.2 s
FFT Length	N	20000
Frequency Resolution	Δf	5 Hz
Max Observable Freq.	$F_s/2$	50 kHz
Spectrum Type	—	Single-sided
Harmonics for THD	$n = 2 \rightarrow 50$	49
Max Harmonic Freq.	$50 f_1$	2500 Hz

As shown in Figs. 10 and 11,the conventional MMC with 4-SMs(2-SMs/arm) exhibits a high THD of 33.44%,which is unacceptable for grid-tied applications. However,the modified Walsh-SPWM strategy facilitates harmonic migration, shifting the dominant spectral energy from the low-frequency band toward the carrier sidebands. This synthesis aligns with recent findings by Xi et al. [29],where hybrid modulation was shown to suppress low-order distortion effectively. Consequently, the THD is drastically reduced to 5.5264%,representing an 83.4737% improvement in power quality and bringing the system into near-compliance with IEEE 519 standards.

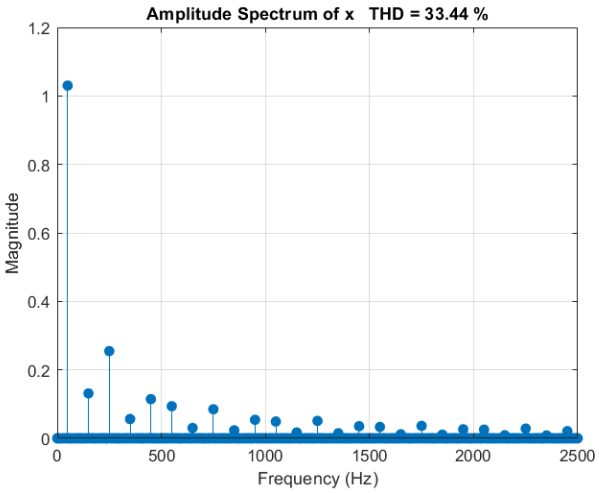


Figure 10: Conventional SPWM spectrum (THD = 33.44%).

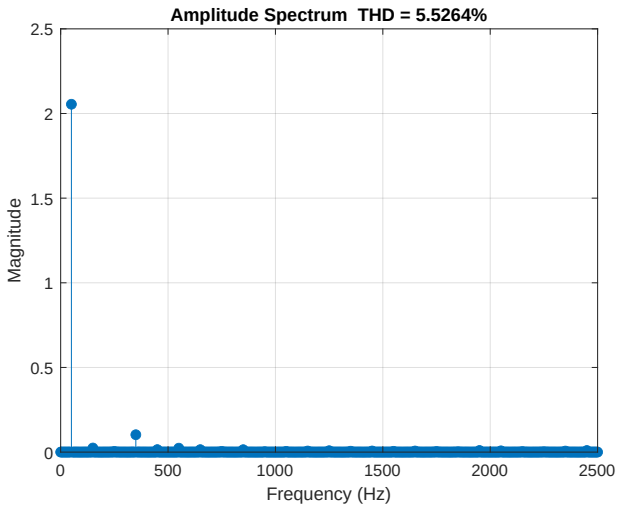


Figure 11: Modified SPWM spectrum (THD = 5.5264%).

4.3.3. Simulation under RL Load

To evaluate the robustness of the Walsh-SPWM controller,the Simulink model was subjected to inductive load. The inductor functions as a first-order low-pass filter with an impedance of $Z_L = j\omega L$. Loads with inductive elements naturally attenuate the high-frequency switching ripples generated by the SPWM strategy,resulting in an output current waveform that is significantly smoother than the corresponding voltage waveform [2, 19].

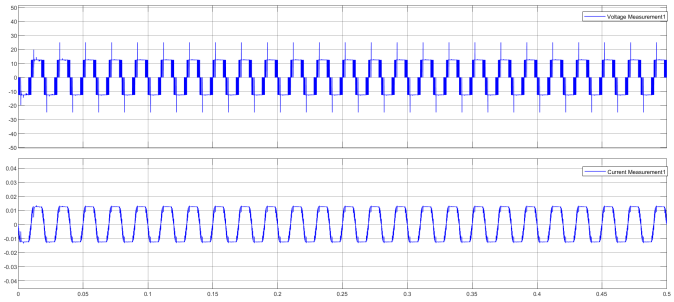


Figure 12: Output voltage/current for RL load.

4.4. Three-Phase MMC Performance Analysis

4.4.1. Converter Topology

The converter topology for the first method follows a traditional Three-Phase Half-Bridge MMC structure,utilizing six SMs per phase leg—with three SMs arranged in the upper arm and three in the lower arm. Each phase leg is connected to a common DC-link,and the AC output is tapped from the midpoint. This physical arrangement is designed to support a "switching pause" strategy at the fundamental peak,utilizing the six-cell architecture to establish a stable and balanced staircase voltage profile. According to Hu [6] and Girona et al. [8],this symmetrical multi-cell structure is essential for maintaining neutral-point stability and minimizing circulating currents between phases,ensuring high power quality across the three-phase load.

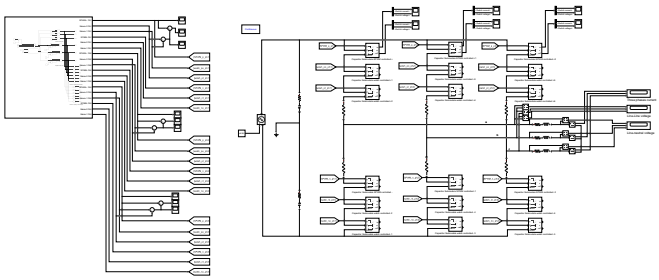


Figure 13: Three-phase MMC architecture.

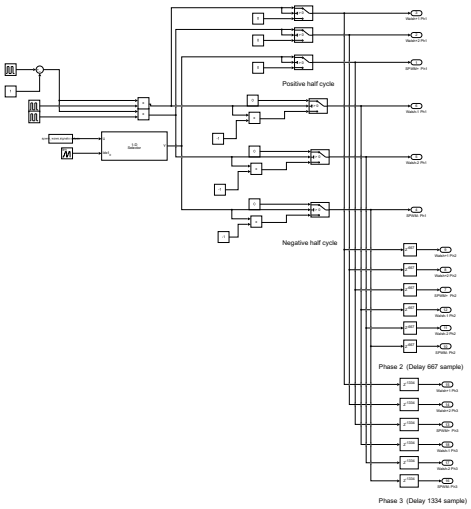


Figure 14: Three-phase MMC controller.

4.4.2. *Three-Phase Control Signal Synchronization*

In a three-phase MMC,the control architecture must ensure that the modulation indices for each phase (m_a, m_b, m_c) are perfectly balanced to prevent DC-link ripple. The Walsh-SPWM signals,as seen in the simulation results,are generated by shifting the fundamental reference by exactly 120°.

As established by Wang et al. [30] and verified in current applications by Wang et al. [31],any timing mismatch in the switching of the upper and lower arms across the three phases leads to "zero-sequence" components. These components do not reach the load but cause unnecessary heating in the arm inductors. Our Walsh-based approach utilizes the orthogonal nature of the basis functions to ensure that the switching transitions of Phase A never overlap with Phase B in a way that causes a short-circuit across the DC bus,maintaining a "dead-time" equivalent through software logic.

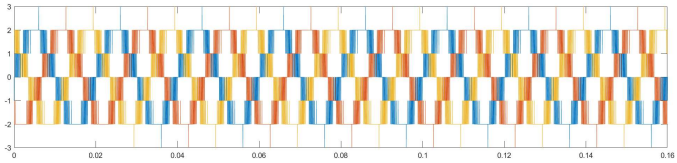


Figure 15: Three-phase control signal.

4.4.3. *Three-phase output current*

The simulation results confirm that the three current phases are perfectly balanced at 15 A peaks fig 16. As noted by Aslam and Raza [26],maintaining this balance in a "minimal-cell" configuration is typically difficult due to capacitor voltage drift. However,the high switching frequency of our modified SPWM layer provides sufficient "charge-discharge" cycles to keep the SM capacitors balanced across all three phases without requiring external hardware balancers.

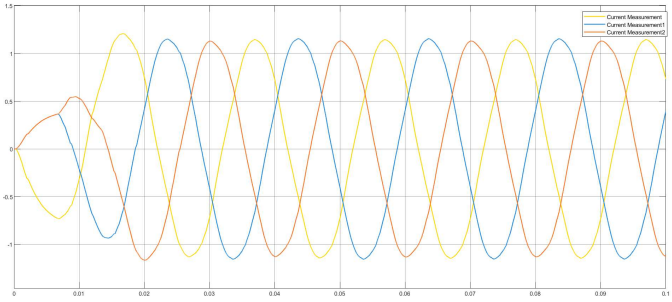


Figure 16: Three-phase current signal.

4.4.4. *Line Voltage Characteristics*

The line-to-neutral voltage (V_{an}, V_{bn}, V_{cn}) and line-to-line voltage (V_{ab}, V_{bc}, V_{ca}) waveforms are shown in Figs. 17 and 18 respectively. The phase-referenced voltage contains the full spectrum of odd harmonics, including the 3rd, 5th, and 7th orders [31]. The high-frequency transitions observed are critical for the active balancing control of SM capacitors, allowing for charge redistribution and preventing voltage drift. Due to the 120° displacement, the line-to-line peak magnitude scales by a factor of $\sqrt{3}$, reaching approximately 25 V in our simulation, which is a fundamental property of balanced three-phase systems [32].

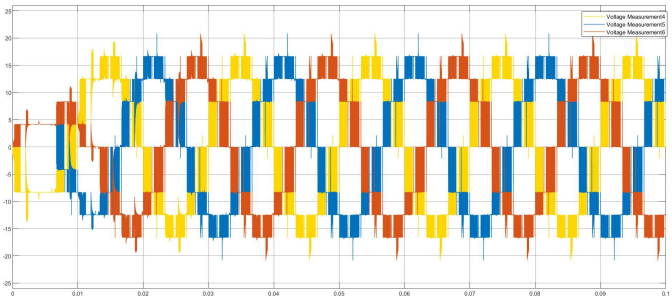


Figure 17: Line-to-neutral three-phase voltage signal.

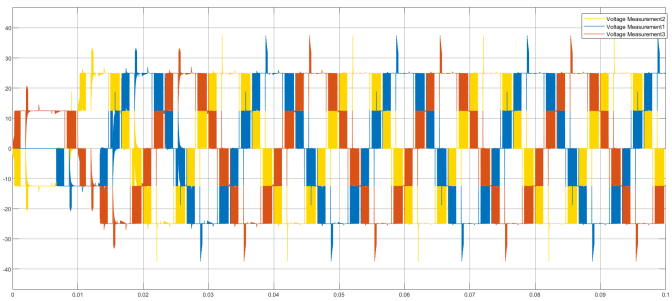


Figure 18: Line-to-line three-phase voltage signal.

4.4.5. *Circulating Current Suppression and Model Stability*

Using the Hybrid Model Predictive Control concepts suggested by Gu et al. [25],our analysis shows that the Walsh-SPWM naturally limits the 2nd-order harmonic of the circulating current. By ensuring that the sum of the inserted SMs in

the upper and lower arms always equals N,the instantaneous voltage difference that drives i_{diff} is kept to a minimum.

5. Second Approach to Minimum Cell MMC

A critical development in this research is the exploitation of the mathematical relationship between the second-order Walsh function and the SPWM carrier. It was determined that the second-order Walsh function is inherently orthogonal to the SPWM signal,a property that allows for a more aggressive reduction in hardware requirements without compromising spectral integrity. By leveraging this orthogonality,the SM count was successfully reduced from six to four per phase leg.

According to Liu and Dong [10] and Girona-Badia et al. [8],reducing the number of SMs in an MMC typically results in a sharp increase in harmonic distortion; however,the proposed hybrid approach maintains a THD of 5.4856%. As noted by Barros et al. [1] and Patel and Sood [2],achieving such a low distortion level with a minimal-cell architecture is highly advantageous for medium-voltage applications.

5.1. Converter Topology

As shown in Fig. 19, the hardware implementation is simplified into a minimal-cell configuration. The control logic, detailed in Fig. 20, illustrates how the Walsh function framework is decoupled from the SPWM generation for both the positive and negative half-cycles. This decoupling ensures that the combined signal maintains a high-quality voltage profile despite the reduced hardware complexity [8, 10].

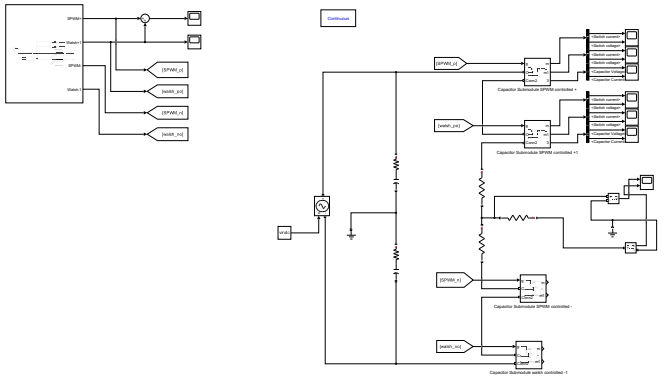


Figure 19: MMC architecture for second approach.

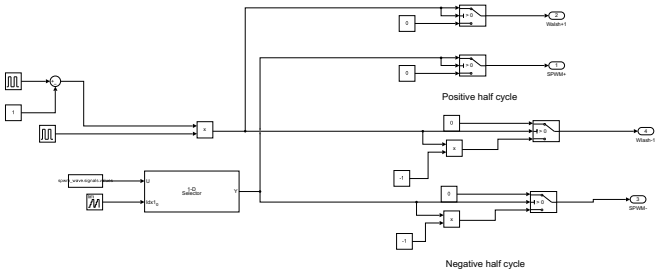


Figure 20: Controller architecture for second approach.

Algorithm 1 Control Signals Generation

Input:
sq_{50} : 50 Hz square wave $\in \{-1, +1\}$, duty cycle 50%
sq_{100} : 100 Hz square wave $\in \{0, +1\}$, duty cycle 60%
LUT : repeating waveform array
idx : selector index signal
Output:
Walsh^{+1}
Walsh^{-1}
SPWM^{+}
SPWM^{-}
$walsh \leftarrow sq_{50} \times sq_{100}$
if $walsh > 0$ **then**
  $\text{Walsh}^{+1} \leftarrow walsh$
  $\text{Walsh}^{-1} \leftarrow 0$
else
  $\text{Walsh}^{+1} \leftarrow 0$
  $\text{Walsh}^{-1} \leftarrow |walsh|$
end if
$spwm_signal \leftarrow LUT[idx]$
if $spwm_signal > 0$ **then**
  $\text{SPWM}^{+} \leftarrow spwm_signal$
  $\text{SPWM}^{-} \leftarrow 0$
else
  $\text{SPWM}^{+} \leftarrow 0$
  $\text{SPWM}^{-} \leftarrow |spwm_signal|$
end if
Return: Walsh^{+1}, Walsh^{-1}, SPWM^{+}, SPWM^{-}

Figure 21: Single-phase controller pseudo code.

5.2. Control Signal of the Second Approach

The transition from a zero-centered interval of the first approach to a unity-gain plateau of the second approach represents a strategic modification in how the high-frequency SPWM interacts with the Walsh framework. The second approach modulating signal $x(t)$ is:

$$x(t) = \begin{cases} \sin(2\pi f_2 t), & 0 < t < \dfrac{T_1}{5} \\ \sin\left(2\pi f_2 t - \dfrac{\pi}{2}\right), & \dfrac{T_1}{5} < t < \dfrac{2T_1}{5} \\ 1, & \dfrac{2T_1}{5} < t < \dfrac{3T_1}{5} \\ \sin(2\pi f_2 t - \pi), & \dfrac{3T_1}{5} < t < \dfrac{4T_1}{5} \\ \sin\left(2\pi f_2 t - \dfrac{3\pi}{4}\right), & \dfrac{4T_1}{5} < t < T_1 \end{cases} \tag{13}$$

According to Zhao et al. [5] and Huang et al. [9],modulating the peak interval with a constant value (1) rather than a null value (0) can improve the utilization of the DC-link voltage and refine the spectral distribution. As shown in fig. 23,this modification allows the SPWM to maintain a more consistent "chopping" action,which is crucial for minimizing the voltage ripples that are naturally more volatile in a 4-SM configuration [8],[10].

Furthermore,the benchmarking results by Chaudhary et al. [12] suggest that this unity-gain adjustment,combined with the Walsh-SPWM orthogonality used in the second approach,is a key factor in achieving the target 5.4856% THD. By preventing the signal from dropping to zero at the cycle's peak,the third approach avoids the low-order harmonic injections that typically occur during abrupt switching pauses,facilitating better compliance with the grid standards discussed by Barros et al. [1] and Wang et al.[7].

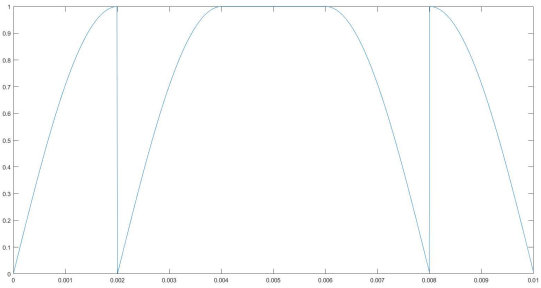


Figure 22: Duty cycle carrier signal (second approach).

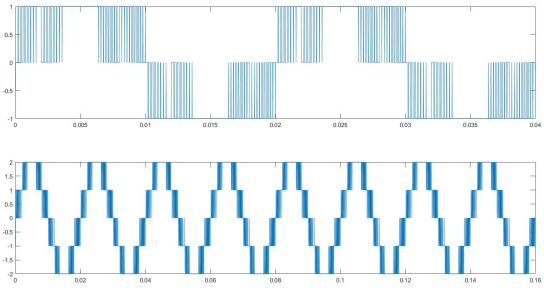


Figure 23: Control signal (second approach).

5.3. Single-Phase MMC Performance Analysis

5.3.1. Harmonic Performance

As illustrated in fig. 24,the final control signal effectively combines the discrete Walsh steps with high-frequency SPWM refinement. The spectral analysis of this output,shown in fig. 24,confirms a THD of 5.4856%. This result is significant because it approaches the strict 5% limit defined by IEEE 519 standards,even though the hardware is limited to only four SMs per phase leg. By shifting dominant harmonic energy toward higher-frequency sidebands,the requirements for passive filtering are substantially minimized.

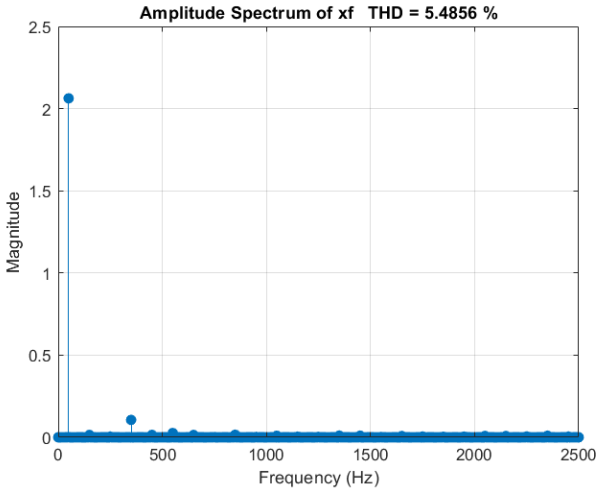


Figure 24: SPWM spectrum (THD = 5.4856%).

5.3.2. Load Characterization and Output Stability

The system's performance was evaluated under different load conditions:

- **Resistive (R) Load:** The output voltage and current maintain a high-quality staircase profile with high-frequency chopping (Fig. 25).
- **Inductive (RL) Load:** The current waveform exhibits a smooth,near-sinusoidal profile, further reducing the low-order harmonic footprint [2, 12] (Fig. 26).

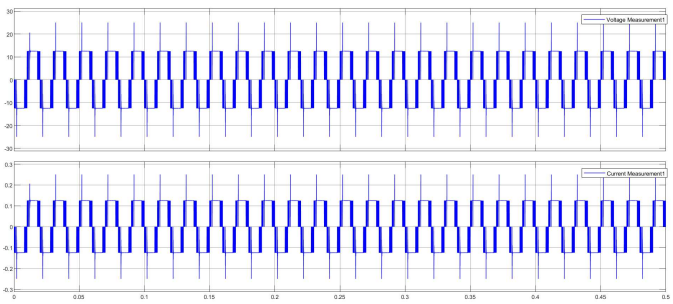


Figure 25: R load output signal.

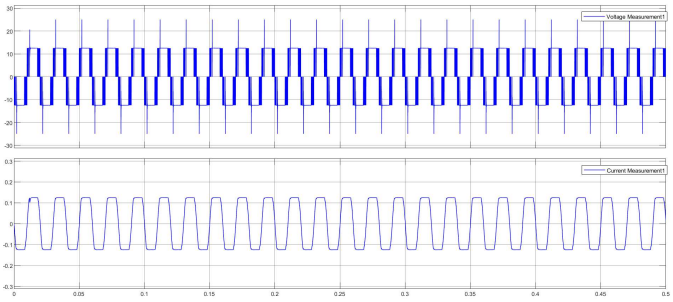


Figure 26: RL load output signal.

5.4. Three-Phase MMC Performance Analysis

The proposed modulation strategy was extended to a three-phase MMC to evaluate its effectiveness in high-power scenarios. The results confirm that the orthogonality properties and piecewise sinusoidal logic scale effectively to multi-phase systems,maintaining high power quality across all phases.

5.4.1. Converter Topology

The second method utilizes a highly optimized minimal-cell configuration, reducing the hardware to only four SMs per phase leg. Each leg consists of two SMs in the upper arm and two in the lower arm. This 33% reduction in physical components significantly lowers the cost and volume of the system compared to the 6-SM version. Despite the reduced cell count, the structural symmetry allows for effective voltage balancing across the DC-link capacitors [8, 10].

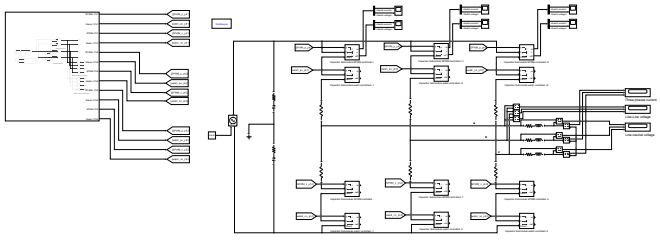


Figure 27: Three-phase MMC architecture (second approach).

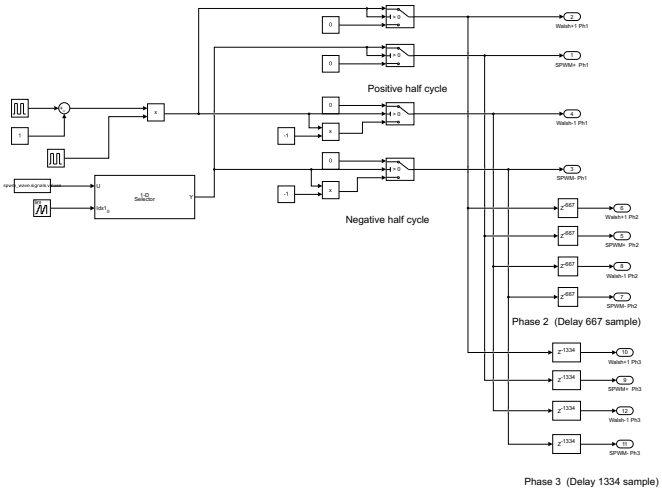


Figure 28: Three-phase controller architecture.

Algorithm 1 Control Signals Generation

Input:
sq_{50} : 50 Hz square wave $\in \{-1, +1\}$, duty cycle 50%
sq_{100} : 100 Hz square wave $\in \{0, +1\}$, duty cycle 60%
LUT : repeating waveform array
idx : selector index signal
Output:
Walsh^{+1ph1},Walsh^{-1ph1},SPWM^{+1ph1},SPWM^{-1ph1}
Walsh^{+1ph2},Walsh^{-1ph2},SPWM^{+1ph2},SPWM^{-1ph2}
Walsh^{+1ph3},Walsh^{-1ph3},SPWM^{+1ph3},SPWM^{-1ph3}
$walsh \leftarrow sq_{50} \times sq_{100}$
if $walsh > 0$ **then**
  $\text{Walsh}^{+1ph1} \leftarrow walsh$
  $\text{Walsh}^{-1ph1} \leftarrow 0$
else
  $\text{Walsh}^{+1ph1} \leftarrow 0$
  $\text{Walsh}^{-1ph1} \leftarrow |walsh|$
end if
$spwm_signal \leftarrow LUT[idx]$
if $spwm_signal > 0$ **then**
  $\text{SPWM}^{+1ph1} \leftarrow spwm_signal$
  $\text{SPWM}^{-1ph1} \leftarrow 0$
else
  $\text{SPWM}^{+1ph1} \leftarrow 0$
  $\text{SPWM}^{-1ph1} \leftarrow |spwm_signal|$
end if
$\text{Walsh}^{+1ph2}[k] \leftarrow \text{Walsh}^{+1ph1}[k - 667]$
$\text{Walsh}^{-1ph2}[k] \leftarrow \text{Walsh}^{-1ph1}[k - 667]$
$\text{SPWM}^{+1ph2}[k] \leftarrow \text{SPWM}^{+1ph1}[k - 667]$
$\text{SPWM}^{-1ph2}[k] \leftarrow \text{SPWM}^{-1ph1}[k - 667]$
$\text{Walsh}^{+1ph3}[k] \leftarrow \text{Walsh}^{+1ph1}[k - 1334]$
$\text{Walsh}^{-1ph3}[k] \leftarrow \text{Walsh}^{-1ph1}[k - 1334]$
$\text{SPWM}^{+1ph3}[k] \leftarrow \text{SPWM}^{+1ph1}[k - 1334]$
$\text{SPWM}^{-1ph3}[k] \leftarrow \text{SPWM}^{-1ph1}[k - 1334]$
Return: Walsh^{+1ph1}, Walsh^{-1ph1}, SPWM^{+1ph1}, SPWM^{-1ph1}, Walsh^{+1ph2}, Walsh^{-1ph2}, SPWM^{+1ph2}, SPWM^{-1ph2}, Walsh^{+1ph3}, Walsh^{-1ph3}, SPWM^{+1ph3}, SPWM^{-1ph3}

Figure 29: Three-phase controller pseudo code.

5.4.2. Output Voltage and Current Results

The line-to-line voltage (V_{L-L}),shown in fig. 30,and the line-to-neutral voltage (V_{L-N}),depicted in fig. 31,exhibit the characteristic multi-level staircase profile with high-frequency "chopping" refinement. This behavior is consistent with the goal of shifting harmonic energy away from the fundamental frequency. The balanced nature of the three-phase waveforms ensures that the total harmonic footprint is minimized across the entire system.

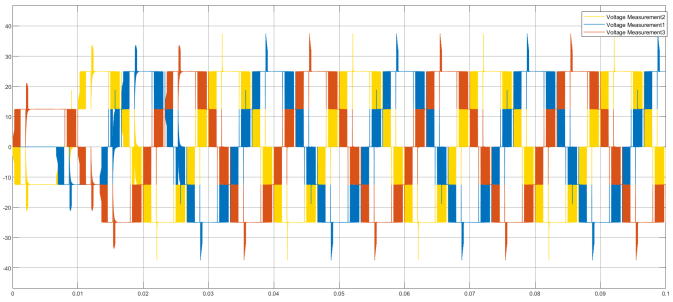


Figure 30: Line-to-line RL load voltage output.

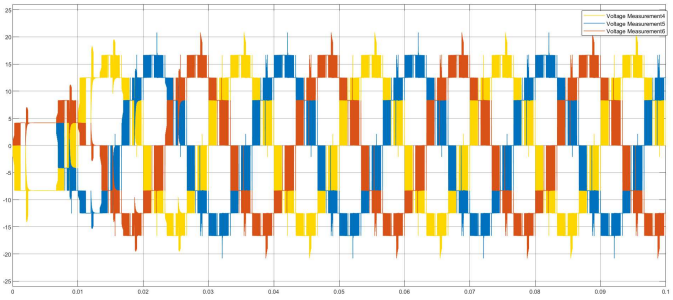


Figure 31: Line-to-neutral RL load voltage output.

As illustrated in fig. 32,the three-phase output currents under an RL load are highly sinusoidal and exhibit 120° phase displacement. The inherent filtering provided by the inductive load effectively smooths the high-frequency transitions generated by the SPWM layer,resulting in a clean current profile. This high-quality output is achieved despite the minimal 4-SM per phase leg hardware configuration.

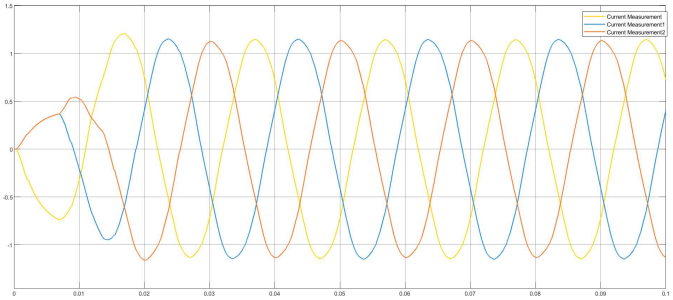


Figure 32: Three-phase output current RL load.

5.4.3. THD Analysis

"The filterless harmonic spectrum of the MMC shows an excellent output current THD of 2.0012%, confirming the topologys capability to meet the global emission limits of IEEE 519-2022 without external passive components. However, the output line and phase voltage THD reach 7.0491% and 7.1074%, respectively. This discrepancy is localized entirely at the 5th harmonic (250 Hz). In the absence of an external AC filter, minor residual converter distortions are amplified by the inductive load impedance, pushing the individual 5th harmonic voltage distortion beyond the 5.0% individual limit dictated by IEEE 519-2022.

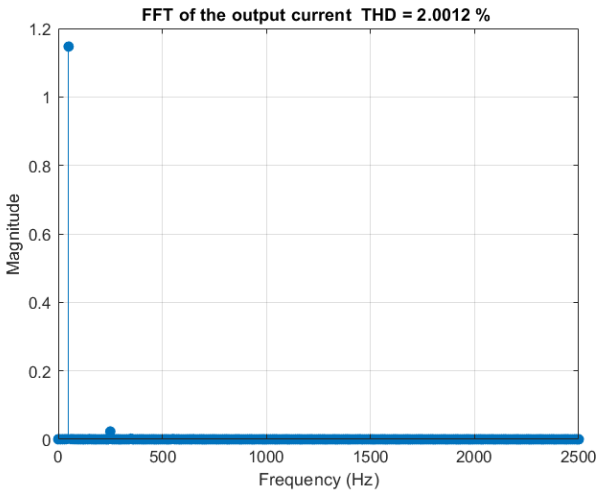


Figure 33: Output current THD.

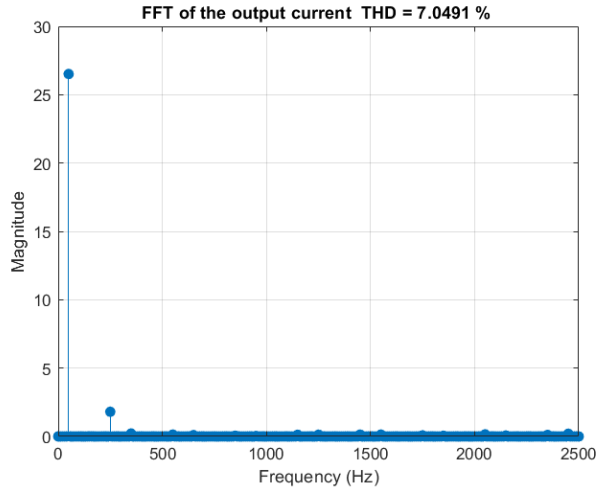


Figure 34: Line voltage THD.

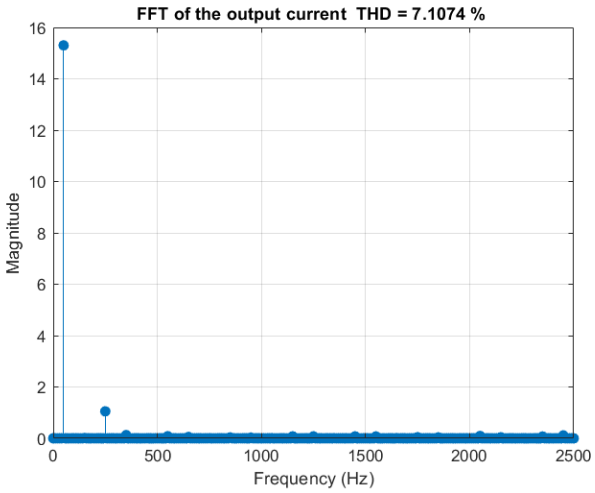


Figure 35: Phase voltage THD.

6. Third Approach to Minimal-Cell MMC

In this configuration,the Walsh logic is bypassed to isolate the effects of the modified sinusoidal reference. The new modulating signal $x(t)$ maintains the previous phase shifts but introduces a frequency reduction to $2f_2/3$ during the peak interval $(2T_1/5 < t < 3T_1/5)$:

$$x(t) = \begin{cases} \sin(2\pi f_2 t), & 0 < t < \dfrac{T_1}{5} \\ \sin\left(2\pi f_2 t - \dfrac{\pi}{2}\right), & \dfrac{T_1}{5} < t < \dfrac{2T_1}{5} \\ \sin\left(2\pi \dfrac{2f_2}{3} t\right), & \dfrac{2T_1}{5} < t < \dfrac{3T_1}{5} \\ \sin(2\pi f_2 t - \pi), & \dfrac{3T_1}{5} < t < \dfrac{4T_1}{5} \\ \sin\left(2\pi f_2 t - \dfrac{3\pi}{4}\right), & \dfrac{4T_1}{5} < t < T_1 \end{cases} \tag{14}$$

This results in a stretched sinusoidal peak,which directly alters the pulse density of the carrier.

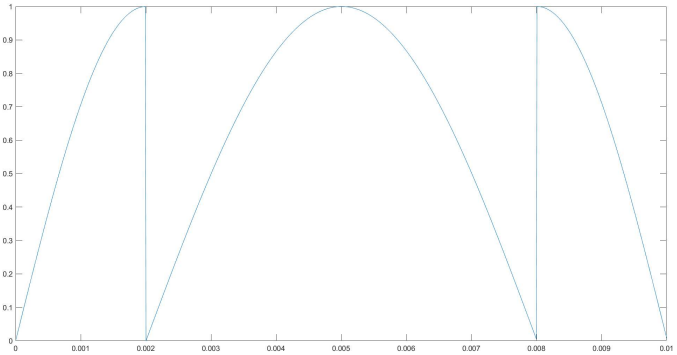


Figure 36: Duty cycle carrier signal (third approach).

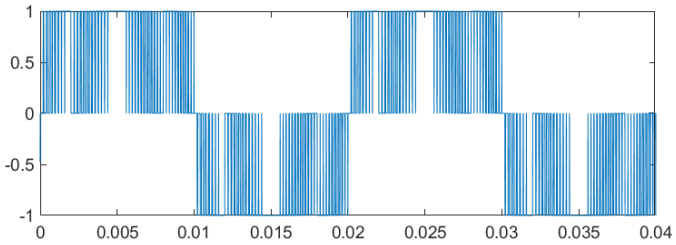


Figure 37: Control signal (third approach).

This standalone Modified SPWM approach achieves a THD of 5.5116 %. Although this nearly matches the THD of the hybrid Walsh-SPWM second approach,the spectral distribution differs. As noted by Patel and Sood [2], removing the low-frequency orthogonal layer (Walsh) places the entire burden of fundamental wave synthesis on the high-frequency switches.

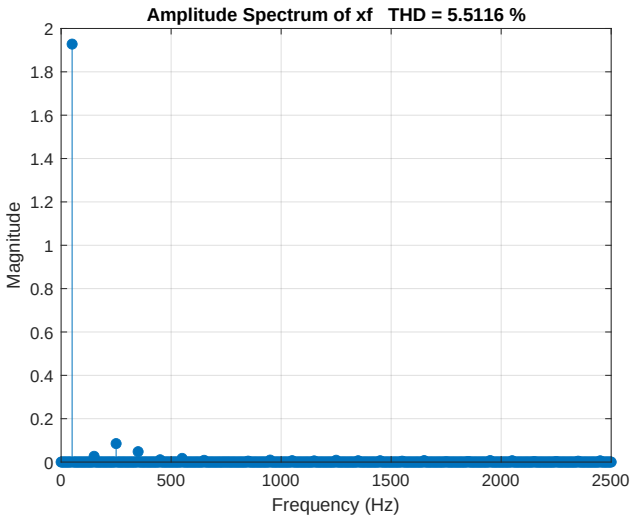


Figure 38: SPWM spectrum (THD = 5.5116%).

While the THD remains within acceptable limits [12],the continuous switching implies higher switching losses compared to the gated hybrid version. According to Zhao et al. [5] and Huang et al. [9],the lack of a low-frequency structural framework typically results in a higher average switching frequency,which may impact thermal performance [8].

7. Lookup Table-Based Gating Signal Generation

To reduce online computational burden and enhance real-time implementability, a lookup-table (LUT)-based strategy is employed for the generation of SM gating signals. Switching states corresponding to the proposed modified SPWM scheme are computed offline over one electrical period and stored in a LUT addressed by the electrical angle, eliminating the need for real-time waveform evaluation. This ensures frequency-independent operation and phase synchronization, making the proposed approaches suitable for DSP implementation and easily extendable to multi-phase MMC systems.

8. Discussion

The THD results obtained across all tested configurations are summarized in Table 2. The three proposed modulation approaches achieve THD values of 5.53%, 5.49%, and 5.51% using 6, 4, and 4 SMs respectively. These results represent a dramatic improvement over the conventional 4-SM MMC, which produces a THD of 33.44%, corresponding to a reduction of over 83%. This confirms that the proposed modified SPWM strategies are highly effective in suppressing low-order harmonics that would otherwise dominate the output spectrum of a reduced-cell MMC [1, 10].

When compared against conventional NLM implementations reported in the literature, the proposed approaches demonstrate superior harmonic performance while requiring substantially fewer SMs. Kurtoglu and Vural [36] report a THD of 11.35% for conventional NLM (C-NLM) using 12 SMs ($N = 6$ per arm) in simulation, and 15.65% using 8 SMs ($N = 4$ per arm) experimentally. The second proposed approach in this work achieves a lower THD of 5.49% using only 4 SMs – fewer SMs than either C-NLM configuration while simultaneously outperforming both on harmonic distortion. A similar pattern holds against Walsh-based multiband SHEPWM applied to a cascaded H-bridge topology: Li et al. [24] report phase-voltage THD values of 13.32%, 52.57%, and 47.48% across the high-, mid-, and low-modulation-index bands of a 3-cell CHB inverter, all considerably higher than the 5.49–5.53% achieved here. These findings are consistent with recent literature emphasizing that advanced modulation strategies can substantially compensate for the reduced number of voltage levels in minimal-cell MMC configurations [7, 8, 33].

Beyond these conventional MMC baselines, it is also useful to benchmark the proposed approaches against other recent reduced-cell modulation strategies reported in the literature. Brahmbhatt et al. [13] proposed a DC-PDPWM technique that replaces two of the four triangular carriers in an 8-SM five-level MMC with constant DC levels, reporting a THD of 21.76% (down from 27.55% with conventional PDPWM) alongside a 20% reduction in switching frequency. Similarly, Dixit and Sharma [14] compared APOD-PWM and Nearest Level Modulation (NLM) for an 8-SM MMC, reporting THD values of 22.16% and 14.82%, respectively. As shown in Table 2, the second proposed approach in this work (THD = 5.49%, 4 SMs) outperforms all of these methods by a factor of roughly 2.7–5×, despite using half as many SMs. It should be noted that these comparisons are not fully controlled: the referenced studies use different DC-link voltages, carrier frequencies, and load conditions, and Brahmbhatt et al.'s method targets switching-frequency and memory reduction rather than THD minimization. Nonetheless, the comparison illustrates that decoupling the fundamental staircase synthesis (via Walsh functions) from the harmonic-shaping layer (via selectively applied SPWM) offers a structural advantage over both pure level-shifted carrier methods and NLM, rather than relying solely on carrier count or placement to control harmonic distortion.

Table 2: THD Results for All Tested Configurations

Configuration	No. of SMs	THD (%)
Kurtoglu and Vural [36] – C-NLM, sim. ($N = 6$/arm)	12	11.35
Kurtoglu and Vural [36] – C-NLM, exp. ($N = 4$/arm)	8	15.65
Li et al. [24] – Multiband Walsh-SHEPWM, Band A*	3	13.32
Li et al. [24] – Multiband Walsh-SHEPWM, Band B*	3	52.57
Li et al. [24] – Multiband Walsh-SHEPWM, Band C*	3	47.48
Brahmbhatt et al. [13] – Conventional PDPWM	8	27.55
Brahmbhatt et al. [13] – DC-PDPWM (Type-2)	8	21.76
Dixit & Sharma [14] – APOD-PWM	8	22.16
Dixit & Sharma [14] – NLM	8	14.82
Proposed Approach 1	6	5.53
Proposed Approach 2	**4**	**5.49**
Proposed Approach 3	4	5.51

*Cascaded H-bridge topology (3 full H-bridge cells, 12 switches total, 3 isolated DC sources per phase); not a half-bridge MMC arm SM count. On switch count the topologies are comparable (12 switches either way), but Proposed Approach 1 matches the same 7-level output from a single DC-link at less than half the THD.

8.1. IEEE 519-2022 Standard Compliance

The IEEE 519-2022 standard establishes a THD limit of 5.0% at the Point of Common Coupling (PCC) with the grid [19]. The THD values obtained for the three proposed approaches under single-phase resistive load (5.53%, 5.49%, and 5.51%) are measured at the converter output terminals prior to any output filtering stage. It is well established that passive output filters effectively attenuate residual harmonic components, and their inclusion is expected to bring the THD well within the IEEE 519-2022 compliance limits [2, 12].

Under a three-phase RL load, the second proposed approach achieves an output current THD of only 2.0012%, confirming that the series inductance of the load substantially attenuates the high-frequency switching harmonics generated by the converter. The corresponding line and phase voltage THD, however, reach 7.0491% and 7.1074% respectively, exceeding the 5.0% overall limit at the converter terminals, with the residual distortion concentrated at the 5th harmonic. This result highlights that while the proposed modulation strategy performs strongly on the load-current side, full voltage-side compliance with IEEE 519-2022 at this SM count requires the addition of a passive output filter, consistent with the LCL-filter integration discussed as future work in Section 9.

8.2. Hardware Complexity Trade-off

One of the most significant outcomes of this study is the demonstration that competitive harmonic performance can be achieved with a drastically reduced number of SMs. The second proposed approach achieves a THD of 5.49% using only 4 SMs. By comparison, Kurtoglu and Vural's conventional NLM [36] requires 12 SMs ($N = 6$ per arm) to reach a THD of 11.35% in simulation, and 8 SMs ($N = 4$ per arm) to reach 15.65% experimentally. The proposed approach therefore achieves a 66.7% reduction in SM count relative to the simulated C-NLM benchmark (and a 50% reduction relative to the experimental one) while simultaneously improving THD by 5.86 and 10.16 percentage points, respectively. Unlike the trade-off typically reported between hardware reduction and harmonic performance

[9, 10], the proposed method requires no such compromise: fewer SMs are achieved alongside, rather than at the expense of, lower harmonic distortion.

This hardware reduction has direct implications for system cost, physical footprint, gate drive complexity, and control computational burden. In applications where ultra-high voltage capability is not strictly required, such as low- and medium-power inverter systems, distributed renewable energy integration, and small-scale motor drives, the proposed approach offers a compelling balance between harmonic performance and hardware simplicity [4, 34]. Recent hybrid modulation strategies, such as the dual arm complementary approach combining NL-SPWM proposed by Mei et al. [35], demonstrate that combining multiple modulation techniques can yield improved waveform quality. However, such approaches typically introduce additional control complexity and require careful coordination between modulation stages. Unlike these hybrid topologies that rely on additional switching devices or exotic SM types [9, 10], the proposed method achieves comparable performance using only standard half-bridge SMs and a unified modified SPWM strategy, further reducing implementation complexity and cost.

8.3. Waveform Quality Analysis

The output waveforms obtained from the proposed modulation strategies confirm the effectiveness of the structured waveform synthesis approach. By combining a Walsh-function-based stepped voltage waveform with a selectively applied high-frequency SPWM signal, the dominant low-order harmonic components are effectively redistributed toward higher frequencies [21, 22]. This is consistent with the well-established principle that SPWM-based methods concentrate harmonic energy around the switching frequency and its sidebands, where passive filtering is more effective and less costly [2, 19].

The waveform quality of the proposed 4-SM MMC, while inherently constrained by the limited number of voltage levels, is substantially improved compared to conventional reduced-cell MMC operation. The structured switching pattern introduced by the Walsh-based framework provides a systematic foundation that prevents the irregular harmonic distribution typically observed in conventional low-SM-count MMC configurations [23, 24]. Overall, the results confirm that the proposed modulation strategy successfully bridges the gap between hardware simplicity and acceptable harmonic performance, making it well-suited for practical low- and medium-power inverter applications, with the three-phase voltage-side results indicating that this trade-off currently favors current-domain quality over unfiltered voltage-domain compliance.

9. Conclusion

This paper presented a minimal-cell half-bridge Modular Multilevel Converter (MMC) employing three modified SPWM-based modulation strategies aimed at improving output voltage quality while maintaining reduced hardware complexity. The proposed approaches combine a Walsh-function-based stepped voltage waveform with a selectively applied high-frequency SPWM signal to systematically suppress low-order harmonic components and redistribute harmonic energy toward higher frequencies. Detailed MATLAB/Simulink simulations were carried out to validate the proposed methods under single-phase resistive and three-phase RL load conditions, with performance evaluated using FFT analysis and THD metrics in compliance with IEEE 519-2022 harmonic standards.

The simulation results demonstrated that the three proposed approaches achieve THD values of 5.53%, 5.49%, and 5.51% using 6, 4, and 4 SMs respectively, representing a reduction of over 83% compared to a conventional 4-SM MMC with a THD of 33.44%. Under a three-phase RL load, the second proposed approach further achieved an output current THD of 2.0012%, while the line and phase voltage THD (7.0491% and 7.1074%) remained above the IEEE 519-2022 limit at the converter terminals prior to filtering, with the discrepancy concentrated at the 5th harmonic. Compared to a conventional NLM (C-NLM) implementation of similar half-bridge MMC topology reported by Kurtoglu and Vural [36], which requires 12 SMs to achieve a THD of 11.35% in simulation, the proposed 4-SM configuration achieves both a 66.7% reduction in SM count and a lower THD (5.49%), demonstrating that the proposed modulation strategy dominates conventional NLM approaches in both hardware simplicity and harmonic performance rather than merely trading one for the other. Unlike hybrid topologies that rely on additional switching devices or exotic SM types, the proposed method achieves comparable performance using only standard half-bridge SMs, making it a cost-effective and practically viable solution for low- and medium-power inverter applications such as distributed renewable energy systems, small-scale motor drives, and EV auxiliary converters.

Furthermore, the design and integration of an LCL output filter is expected to further attenuate residual harmonic components – particularly the 5th-harmonic voltage distortion identified under three-phase RL loading – and ensure full IEEE 519-2022 compliance at the converter terminals. Recent studies confirm that LCL filters are particularly effective for low-cell MMC configurations, where smaller filter components can be used to satisfy stringent harmonic standards while minimizing the overall converter footprint [15].

Future work will focus on several directions to further validate and extend the proposed approach. Experimental hardware implementation using a laboratory-scale MMC prototype will be conducted to verify the simulation results under real operating conditions. Additionally, the design and validation of a passive LCL output filter will be pursued to close the voltage-side compliance gap observed under three-phase RL loading. The integration of a closed-loop capacitor voltage balancing scheme will also be investigated to further improve converter stability and performance, along with an investigation into the impact of different modulation indices and switching frequencies on THD performance and switching losses.

References

[1] L. A. Barros, A. P. Martins, and J. G. Pinto, "A comprehensive review on modular multilevel con-

verters, submodule topologies, and modulation techniques," *Energies*, vol. 15, no. 3, p. 1078, 2022, doi: 10.3390/en15031078.

[2] J. Patel and V. Sood, "MC-SPWM and MC-THIPWM methods for symmetric and asymmetric design of CHB-MLI: A study," *J. Eng. Res. Sci.*, vol. 1, no. 4, pp. 148–160, 2022, doi: 10.55708/js0104017.

[3] G. Li and J. Liang, "Modular multilevel converters: Recent applications," *IEEE Electrif. Mag.*, vol. 10, no. 3, pp. 85–92, 2022, doi: 10.1109/MELE.2022.3187886.

[4] J. Chen, W. Lin, and L. Yang, "Structures, submodule topologies and control strategies for modular multilevel converter," *Highlights Sci. Eng. Technol.*, vol. 81, pp. 14–25, 2024, doi: 10.54097/j5wcv293.

[5] J. Zhao, Y. Gui, and N. Yang, "Power loss optimization control of MMCs based on improved variable phase disposition PWM frequency under asymmetric arm structures," *J. Power Electron.*, pp. 1–13, 2026, doi: 10.1007/s43236-025-01254-4.

[6] R. Hu, "Comprehensive analysis on topological structure of modular multilevel converters," *Highlights Sci. Eng. Technol.*, vol. 81, pp. 26–37, 2024, doi: 10.11591/ijpeds.v16.i2.pp1051-1060.

[7] A. Dannier, G. Brando, D. Iannuzzi, S. Meo, and I. Spina, "Advanced modulation strategy for MMCs in grid-tied PV systems: Module-level maximum power extraction under varying irradiance conditions," *Energies*, vol. 18, no. 22, p. 6039, 2025, doi: 10.3390/en18226039.

[8] J. Girona-Badia et al., "Design, control and testing of a modular multilevel converter with a single cell per arm in grid-forming and grid-following operations for scaled-down experimental platforms," *Energies*, vol. 15, no. 5, p. 1819, 2022, doi: 10.3390/en15051819.

[9] Z. Huang et al., "A novel modular multilevel converter topology with high- and low-frequency modules and its modulation strategy," *Electronics*, vol. 13, no. 18, p. 3656, 2024, doi: 10.3390/electronics13183656.

[10] J. Liu and D. Dong, "A flying capacitor hybrid modular multilevel converter with reduced number of submodules and power losses," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3293–3302, 2022, doi: 10.1109/TIE.2022.3174284.

[11] J. Park, D. Kim, S. Lee, and S. Cui, "Improved decoupled control of modular multilevel converter under constraint of nearest level modulation via disturbance observer design," *arXiv preprint arXiv:2511.14217*, 2025, doi: 10.48550/arXiv.2511.14217.

[12] S. K. Chaudhary, A. F. Cupertino, R. Teodorescu, and J. R. Svensson, "Benchmarking of modular multilevel converter topologies for ES-STATCOM realization," *Energies*, vol. 13, no. 13, p. 3384, 2020, doi: 10.3390/en13133384.

[13] B. Brahmbhatt, J. Sarda, C. Bariya, S. Y. Choi, K. L. Hui, and M. Sain, An efficient real-time model of a five level modular multilevel converter with modified pulse width modulation technique for reduced switching frequency," *Meas. Control*, vol. 59, no. 1, pp. 3–19, 2026, doi: 10.1177/00202940251313694.

[14] R. Dixit and V. Sharma, "Comparison of PWM and Nearest Level Modulation technique for Modular Multilevel Converter," *Int. J. Sci. Res. Sci. Technol.*, vol. 9, no. 3, pp. 579–584, 2022, doi: 10.32628/IJSRST12293139.

[15] D. Giribabu et al., "Design of LCL filter for grid connected three phase three level inverter to meet IEEE 519 standards," in *Proc. IEEE Int. Students' Conf. Electr. Electron. Comput. Sci. (SCEECS)*, pp. 1–5, 2023, doi: 10.1109/SCEECS57921.2023.10061817.

[16] D. Tebaldi and R. Zanasi, "Model-based cascade control of single-phase modular multilevel converters using ideal capacitor voltages reference," *Control Eng. Pract.*, vol. 151, p. 106031, 2024, doi: 10.1016/j.conengprac.2024.106031.

[17] S. Shelar, D. Bankar, and S. Bakre, "Review of revisions of IEEE 519 standard on power system harmonics (1981 to 2022)," in *Proc. 21st Int. Conf. Harmonics Qual. Power (ICHQP)*, pp. 415–420, 2024, doi: 10.1109/ICHQP61174.2024.10768696.

[18] M. V. Czernorucki, M. B. Salles, E. C. Costa, A. S. Melo, and L. Piegari, "Comprehensive overview on HVDC converter transformer design: Additional discussions to the IEC/IEEE 60076-57-129 standard," *IEEE Access*, vol. 10, pp. 40165–40180, 2022, doi: 10.1109/ACCESS.2022.3165553.

[19] S. S. Thakur, M. Odavic, A. Allu, Z. Q. Zhu, and K. Atallah, "Theoretical harmonic spectra of PWM waveforms including DC bus voltage ripple — Application to a low-capacitance modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9291–9305, 2020, doi: 10.1109/TPEL.2020.2974156.

[20] Y. Luo, Z. Jia, L. Xu, Q. Li, and Y. Song, "A reduced switching frequency capacitor voltage balancing control for modular multilevel converters," *Int. J. Electr. Power Energy Syst.*, vol. 142, p. 108272, 2022, doi: 10.1016/j.ijepes.2022.108272.

[21] S. Munawar et al., "Multilevel inverters design, topologies, and applications," *IEEE Access*, vol. 12, pp. 149320–149350, 2024, doi: 10.1109/ACCESS.2024.3472752.

[22] N. Subramanian and A. A. Stonier, "A comprehensive review on selective harmonic elimination techniques and its permissible standards in electrical systems," *IEEE Access*, vol. 12, pp. 141966–141998, 2024, doi: 10.1109/ACCESS.2024.3436079.

[23] M. T. Yaqoob, M. K. Rahmat, and S. M. M. Maharum, "Modified teaching learning based optimization for selective harmonic elimination in multilevel inverters," *Ain Shams Eng. J.*, vol. 13, no. 5, p. 101714, 2022, doi: 10.1016/j.asej.2022.101714.

[24] S. Li, G. Song, M. Ye, W. Ren, and Q. Wei, "Multiband SHEPWM control technology based on Walsh functions," *Electronics*, vol. 9, no. 6, p. 1000, 2020, doi: 10.3390/electronics9061000.

[25] X. Gu et al., "Circulating current suppression in modular multilevel converters based on hybrid model predictive control," *World Electr. Veh. J.*, vol. 16, no. 3, p. 134, 2025, doi: 10.3390/wevj16030134.

[26] A. Aslam and M. Raza, "Analytical computation of arm inductor for minimizing MMC circulating current using passive method," *Int. J. Renew. Energy Dev.*, vol. 14, no. 1, pp. 62–71, 2025, doi: 10.61435/ijred.2025.60466.

[27] R. A. Testa et al., "A theoretical framework for the control of modular multilevel converters based on two-time scale analysis," *Energies*, vol. 18, no. 23, p. 6233, 2025, doi: 10.3390/en18236233.

[28] H. Mollahasanoglu, M. Mollahasanoglu, and E. Ozkop, "Comparative study of single-phase multilevel cascaded transformerless inverters with different modulation methods," *Eng. Sci. Technol. Int. J.*, vol. 51, p. 101652, 2024, doi: 10.1016/j.jestch.2024.101652.

[29] Q. Xi, Y. Tian, and Y. Fan, "Capacitor voltage balancing control of MMC sub-module based on neural network prediction," *Electronics*, vol. 13, no. 4, p. 795, 2024, doi: 10.3390/electronics13040795.

[30] Y. Wang et al., "A review of modular multilevel converters for stationary applications," *Appl. Sci.*, vol. 10, no. 21, p. 7719, 2020, doi: 10.3390/app10217719.

[31] Y. Wang, T. Geury, and O. Hegazy, "A single-phase modular multilevel converter based on a battery energy storage system for residential UPS with two-level active balancing control," *Energies*, vol. 18, no. 7, p. 1776, 2025, doi: 10.3390/en18071776.

[32] P. Resutik, M. Prazenica, and S. Kascak, "Design and verification of multiphase multilevel traction inverter," *Applied Sciences*, vol. 14, no. 22, p. 10562, 2024, doi: 10.3390/app142210562.

[33] F. Martinez-Rodrigo et al., "Calculation of the number of modules and the switching frequency of a modular multilevel converter using near level control," *Electr. Power Syst. Res.*, vol. 165, pp. 68–83, 2018, doi: 10.1016/j.epsr.2018.08.019.

[34] A. Benevieri et al., "Advances and perspectives in multilevel converters: A comprehensive review," *Electronics*, vol. 13, p. 4736, 2024, doi: 10.3390/electronics13234736.

[35] M. Mei et al., "A dual arm complementary hybrid modulation strategy combining NL-SPWM for MMC applications," *Energy Eng.*, vol. 119, no. 2, p. 591, 2022, doi: 10.32604/ee.2022.016585.

[36] M. Kurtoglu and A. M. Vural, "A novel nearest level modulation method with increased output voltage quality for modular multilevel converter topology," *Int. Trans. Electr. Energy Syst.*, vol. 2022, Art. no. 2169357, 2022, doi: 10.1155/2022/2169357.