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2-Terminal refresh-free memory for high-density and low power consumption during data retention

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Abstract

We propose a new 2-terminal refresh-free memory suitable for 1T-DRAM applications. This memory cell is composed of a multilayer nanowire including silicon (Si), silicon-germanium (SiGe) storage regions and a silicon buffer layer and the nanowire is surrounded by a polysilicon layer. A 2-terminal structure with a $4F^2$ footprint enables high-density implementation. The valence-band offset at the Si/SiGe heterojunction suppresses hole diffusion in the SiGe storage region, thereby improving hole retention. The polysilicon layer reduces electron inflow, thereby inducing holes to accumulate locally in the SiGe storage region rather than the Si storage region, which reduces impact ionization and retains the state "1". The polysilicon layer enables to form a holding region that can retain data at low power consumption even when using only two electrodes, providing a low standby current of 4.5 pA when retaining state “1” and a wide holding margin with a gradual current slope of 220 mV/dec. This device achieves a memory operation speed within 10 ns. In particular, the buffer layer suppresses excessive hole generation, thereby improving the speed of write "0" operation.

Introduction

Dynamic random-access memory (DRAM) has been widely used as the main memory in computing systems because of its high-speed operation and high-density. As the demand for higher memory capacity continues to rise, DRAM cells have been aggressively scaled down[1–2]. However, as the cell area decreases, it is becoming increasingly difficult to secure sufficient storage capacitance to reliably distinguish each memory state. To address this problem, various technological approaches have been attempted, such as the introduction of high-k dielectric materials and high-aspect-ratio capacitor structures[3–5]. However, these approaches inevitably increase process complexity and manufacturing cost. To overcome these limitations, extensive research on 1T-DRAMs is being conducted.

Generally, 1T-DRAMs distinguish memory states by storing charge in the floating body[6–13]. However, the stored charge in the floating body is gradually depleted by recombination and leakage currents, which degrades the retention characteristics[14]. Therefore, 1T-DRAMs require shorter refresh intervals than conventional DRAMs, leading to significant data access latency[15–19]. To solve these problems, a voltage-assisted holding operation has been proposed. In this operation, a holding voltage continuously supplies excess charges to the floating body to suppress charge depletion and retaining the stored state without periodic refresh[20–22]. This can be realized in 1T-DRAMs exhibiting hysteric I-V characteristics because the current level corresponding to each memory state can be maintained by applying the holding voltage. Based on this principle, bistable resistor (biristor) and thyristor random-access memory (TRAM) have been widely studied as representative hysteresis-based 1T-DRAMs.

The biristor has attracted attention due to its simple two-terminal structure for high-density[20–22]. However, it shows a latch-down phenomenon at a relatively high current level because the charge generation rapidly decreases as the electric field decreases in a positive feedback system based on

impact ionization. This results in a high standby current during the holding operation, leading to substantial power consumption[20–22]. On the other hand, TRAM can maintain a low current level before latch-down due to its positive feedback system based on charge transport. Thanks to these characteristics, the holding operation with low standby current is possible near the latch-down voltage[23,24]. However, the steep current slope near the holding voltage region amplifies standby current fluctuations caused by process variations and line-resistance-induced voltage drops in cross-point array operation. There is a possibility that standby power consumption during array operation may increase as the allowable holding voltage range for maintaining low power consumption becomes narrow[23,24]. In our previous study, a low standby current and a wide holding margin were achieved through the application of band offset engineering[25]. However, this mechanism is possible in a 3-terminal structure where the potential of the base region is controlled by the gate electrode.

In this study, we propose a new 1T-DRAM with a simple two-terminal structure capable of refresh-free operation at low power consumption. Low power consumption during data retention is achieved without an additional gate contact through a polysilicon layer that extends the potential across the entire base regions.This 2-terminal structure reduces the number of metal interconnects, providing advantages in terms of integration density and fabrication cost[26]. The cell structure and its memory operation are designed by technology computer-aided design (TCAD) simulation[27]. During the holding operation, the retention mechanism is analyzed based on an energy band diagram and the time-dependent variation in hole density stored in a storage layer designed with a heterojunction structure. The feasibility of stable write “0” operation is demonstrated by investigating the relative dominance of impact ionization and recombination depending on the presence and absence of a buffer layer that alleviates electric field concentration.

Methods

Device structure and simulation. Figure 1a shows a schematic diagram of the proposed cell composed of a cross-sectional view of a unit cell. This device consists of a silicon (Si) nanowire structure with sequential N_1-P_1-P_2-P_3-N_2 regions, where the P_2 region is silicon-germanium (SiGe) material. The channel area is set to 20 × 20 nm^2 to achieve high-density. The N_1 region is heavily doped with a doping concentration of 10^{20} cm^{-3}. The N_2 region is doped with a doping concentration of 10^{18} cm^{-3}, which reduces the electric field at a junction. The P_1 and P_2 regions are designed with a doping concentration of 1.1 × 10^{18} cm^{-3} and a length of 50 nm to ensure a sufficiently low standby current. The germanium content of the P_2 region (x in $Si_{1-x}Ge_x$) is set to 0.3, enabling deposition without defects caused by lattice mismatch over a given length[28–30]. The P_3 region is designed with a doping concentration of 10^{17} cm^{-3} and a length of 50 nm. This region acts as a buffer layer by reducing the peak electric field at the junction. To implement the 2-terminal structure capable of refresh-free operation at low power consumption, the polysilicon layer is formed with a doping concentration of 10^{18} cm^{-3} to extend the potential of the N_2 region. Figure 1b shows a schematic diagram of a vertical cross-point array that can

be constructed using the unit cell. This array structure enables access to each cell and high-density integration of a $4F^2$ footprint.

The proposed cell is simulated using TCAD. Figure 1c shows a calibration result for hysteresis characteristics with the fabricated biristor. Since both the biristor and our device operate based on the generation of charges through impact ionization and the floating body effect, the calibration is performed using the experimental data from the biristor for reliable simulation[31]. The Fermi-Dirac statistics and drift-diffusion model are used as the basic physical models. The OldSlotboom model is applied to explain bandgap narrowing under heavily doped conditions. A high-field saturation model is applied to consider carrier velocity saturation caused by scattering under high electric fields. In addition, the Philips unified mobility model is used to explain mobility degradation caused by impurity scattering due to doping and carrier-carrier scattering. The Auger and SRH recombination models are also applied. To reflect the retention characteristics of the actual device, the surface recombination model at the Si/SiO_2 and $SiGe/SiO_2$ interfaces is included. The Avalanche model is used to consider the generation of excess holes by impact ionization in the space charge region.

Device Characteristics. Figure 2a shows the quasi-static I_A-V_{AC} hysteresis characteristics of the proposed cell. When the V_{AC} reaches the latch-up voltage (V_{LU} = 1.53 V), the device rapidly transitions from the high-resistance state (HRS) to the low-resistance state (LRS). During the reverse sweep after latch-up, the high I_A is observed in the voltage region for section (1) ($V_{AC} \geq$ 1.42 V) corresponding to the LRS. As the V_{AC} decreases below the first latch-down voltage ($V_{LD,1}$ = 1.42 V), the voltage region for section (2) (0.76 V ≤ V_{AC} < 1.42 V) appears. When the second latch-down voltage ($V_{LD,2}$ = 0.76 V) is reached, the device returns to the HRS. This double latch-down characteristic forms a holding region for data retention between the two latch-down voltages, and this region is characterized by a lower current level than that in section (1) with a standby current of 4.5 pA and a gradual current slope of 220 mV/dec.

Figure 2b shows the energy band diagram at V_{AC} = 1.0 V in the HRS. Some of the electrons in the N_2 region overcome the energy barrier and reach the N_1-P_1 junction. The injected electrons induce impact ionization under the high electric field, generating electron-hole pairs (EHPs). As a result, the excess holes are accumulated in the P_1 and P_2 storage regions, thereby increasing the potential and partially reducing the energy barrier. This lowered energy barrier facilitates additional electron transport, which can further enhance impact ionization. However, the electric field at V_{AC} = 1.0V is insufficient to generate enough excess holes, so the positive feedback cannot occur. When the V_{AC} increases to 1.53 V, the excess holes are regenerated by the positive feedback as shown in Fig. 2c. This can be explained as the amplification of I_A through M and β, as shown in Eq. (1)[32–33]:

$$I_A = \frac{M \cdot \beta}{1 - (M - 1) \cdot \beta} I_B$$

1

M is related to how well excess holes are supplied to the base, and β is related to how well excess holes are retained in the base. I_B is the effective base current due to the generated holes. When sufficient excess holes are generated by impact ionization to satisfy (M-1)•β = 1, the positive feedback is occurs, resulting in the latch-up phenomenon where the current increases rapidly. Consequently, a low energy barrier height is maintained by sufficient hole accumulation after latch-up, which is shown in the energy band at V_{AC} = 1.54 V.

Figure 2d shows the energy band under the steady-state condition at V_{AC} = 0.8 V after the latch-up, which corresponds to section (2). The lower current level of section (2) than that in section (1) is maintained down to a low voltage region through reduced impact ionization resulting from the combined effect of the bandgap engineering based on heterojunction and the polysilicon layer. A valence band offset is induced by a silicon(Si)/silicon-germanium(SiGe) heterojunction, dividing the storage region into P_1 and P_2 regions. The P_3 region does not function as a storage region because of its low doping concentration of 10^{17} cm^{-3}. The diffusion of stored holes in the P_2 region is effectively suppressed by the valence band offset, resulting in better retention characteristics in the P_2 region than in the P_1 region. The polysilicon layer extends the potential of the N_2 region toward the entire P regions. This potential extension effect reduces the energy band bending and the total electron influx into N_1-P_1 junction during the reverse sweep. In section (2), by the above effect, the holes generated are not evenly distributed in the P_1 and P_2 storage regions but are locally accumulated in the P_2 region, while the lowered potential of the P_1 region forms a hump that inhibits electron injection. As a result, the impact ionization is adjusted to remain reduced, and the current level is lower compared to section (1). At the same time, a deep potential well of the P_2 region formed by the valence band offset maintains the positive feedback with low M and β without rapid decrease in the holding region, leading to a gradual current slope of 220 mV/dec. By setting the V_{hold} to V_{AC} = 0.8 V to continuously compensate for losses without refresh operation to maintain stored holes, the standby current can be minimized to 4.5 pA. Bandgap engineering based on a heterojunction differentiates the retention characteristics of the P_1 and P_2 regions. This leads to distinct roles of the P_1(Hump) and P_2(Storage) regions, while the valence-band offset of the P_2 region suppresses the rapid decrease in current in section (2). The polysilicon layer reduces the total electron influx and induces a local hole accumulation between the P_1 and P_2 regions, enabling the double latch-down characteristic for section (2) to be formed using only two electrodes.

To preserve data with low power consumption, both a low standby current and a gradual current slope are inevitably required. In particular, the gradual current slope provides sufficient holding margin to maintain low power consumption, which reduces standby current fluctuations due to process variations and voltage drops by line resistance during memory array operation. Although strict comparisons are limited due to differences in device size, previously reported biristors have high standby currents exceeding 0.1 μA, resulting in significant standby power consumption[20–22,31]. TRAMs have been reported to achieve a low standby current of approximately 1 pA but show a steep current slope of 65 mV/dec[23–24]. This steep slope narrows the holding margin during memory array operation, increasing

standby power consumption. The proposed device demonstrates the possibility of retaining data with low power consumption by achieving a relatively low standby current of 4.5 pA and a gradual current slope of 220 mV/dec in section (2).

Memory operations. Table 1 summarizes the operating conditions and corresponding speeds. Sub-10 ns operation is achieved in memory operation. Figure 3a shows the energy band diagram during the write “1” operation. If V_{AC} is set to 5.7 V with a pulse width of 2 ns, the device stably switches to the LRS and forms a state "1". Figure 3b compares the energy band diagrams for state “0” and the steady-state condition after the write “1” operation at V_{hold} = 0.8 V. In state “1”, sufficient holes are locally stored in the P_2 region due to the application of V_{hold}. This results in lower energy band height than that in state "0". Figure 3c shows the stored hole density in P_2 region of state “0” and state “1” as a function of standby time, depending on whether V_{hold} is applied. If V_{hold} is not applied, the stored holes in state “1” gradually recombine and become completely depleted after 10 ms. On the other hand, when V_{hold} is applied, the stored hole density initially decreases but converges to 6.3×10^{17} cm^{-3} after 10 μs, so that state "1" can be sufficiently distinguished from state "0" without the refresh operation. This is because sufficient holes with excellent retention characteristics of the P_2 region allow sufficient holes to remain accumulated even at a low V_{AC} of 0.8 V, maintaining a positive feedback.

A stable write “0” operation is enabled by a buffer layer (P_3) to ensure that recombination occurs predominantly over impact ionization. Figure 4a shows the energy band diagram for the write “0” operation. This operation is performed by applying a V_{AC} of -0.5 V to efficiently remove stored holes in the P_1 and P_2 storage regions. Electrons from the N_2 region are injected into the entire storage regions, causing the stored holes to recombine with the electrons. As a result, the stored holes in the P_1 and P_2 storage regions are depleted. However, impact ionization occurring near the N_2 region junction generates excess holes and degrades write “0” operation, so this phenomenon must be taken into account. The buffer layer (P_3) is introduced to effectively disperse the electric field and suppress the generation of excess holes caused by impact ionization. Figure 4b compares the energy band diagrams (dotted line) and the impact ionization rate (solid line) with and without the buffer layer (P_3) at the V_{AC} = -0.5 V. In the absence of the buffer layer, the abrupt energy band bending occurs at the P_2-N_2 junction. Therefore, the peak electric field increases and a high impact ionization rate of up to 1.1×10^{28} $cm^{-3} \bullet s^{-1}$ occurs. In contrast,in our device, the gradual energy band bending is formed between the P_2 region and the N_2 region due to low doping concentration ofthe P_3 region. So, the peak electric field decreases and thus a relativelylow impact ionization rate of up to 1.1×10^{26} $cm^{-3} \bullet s^{-1}$ occurs at the P_2-P_3 junction. Figure 4c shows the stored hole densities in the P_2 region for cases with and without the buffer layer during write “0” operation. In our device, the hole density decreases rapidly to 3.0×10^{17} cm^{-3}, whereas in a device without a buffer layer, the hole density remains almost constant at 7.1×10^{17} cm^{-3} due to excess hole accumulation. Figure 4d shows the energy band diagram and hole density at the V_{hold} for state “1” and state “0”. The stored holes are successfully depleted and the potential of the P_1 and P_2 regions is

lowered, resulting in forming a high energy barrier. Therefore, the write “0” operation is reliably completed with a speed of 6 ns.

Figure 5a shows the write “1” and the subsequent read “1” operations. During the 10 s holding period, the standby current converges from an approximately 1μA to 4.5 pA, while state “1” is maintained during this process. Afterwards, when a read pulse of 2.7 V for 10 ns is applied to detect the state “1”, the read “1” current level increases to 1.5 μA. This is because the positive feedback occurs due to low energy barrier height caused by stored holes and increased V_{AC}. Figure 5b shows the read “0” operation after write “0” operation. Since there are not enough excess holes in the P_1 and P_2 storage regions, the energy barrier height is maintained high and a low "0" reading current level of 1 pA is observed. The proposed cell can retain state “1” with a low holding current of 4.5 pA and has a state current ratio of 1.5×10^6, which is sufficient to distinguish between state “1” and state “0”.

Conclusions

We firstly propose a new 2-terminal 1T DRAM capable of refresh-free operation with low power consumption. The proposed device can achieve high-density through a 2-terminal configuration and vertical cross-point array architecture. A holding region for data retention with a low standby current of 4.5 pA and a gradual current slope of 220 mV/dec is achieved using only two electrodes. The gradual current slope of 220 mV/dec provides a sufficient holding margin for data retention in memory array operation. These characteristics enable low power consumption during data retention. In addition, it demonstrates stable memory operation characteristics with an operation speed of less than 10 ns and a read current ratio of 10^6 for data sensing between state “1” and state “0”. Consequently, these results demonstrate the potential of the new memory device for high-density memory applications.

Declarations

Competing interests

The authors declare no competing interests.

Author Contribution

H.S. and Y.K. conceptualized the project and developed the methodology. H.S. led the simulation design, execution, data analysis, and manuscript writing. J.P. and K.K supported simulation and characterization of the devices. K.O. and J.-H.P. provided advice on the simulation work and contributed to manuscript preparation. C.-K.B. provided guidance and supervision throughout the research. All authors actively participated in result discussions and contributed to manuscript editing.

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Data Availability

The data generated and/or analyzed during the current study are not publicly available for legal/ethical reasons but are available from the corresponding author on reasonable request.

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Table 1

Table 1 is available in the Supplementary Files section.

Figures

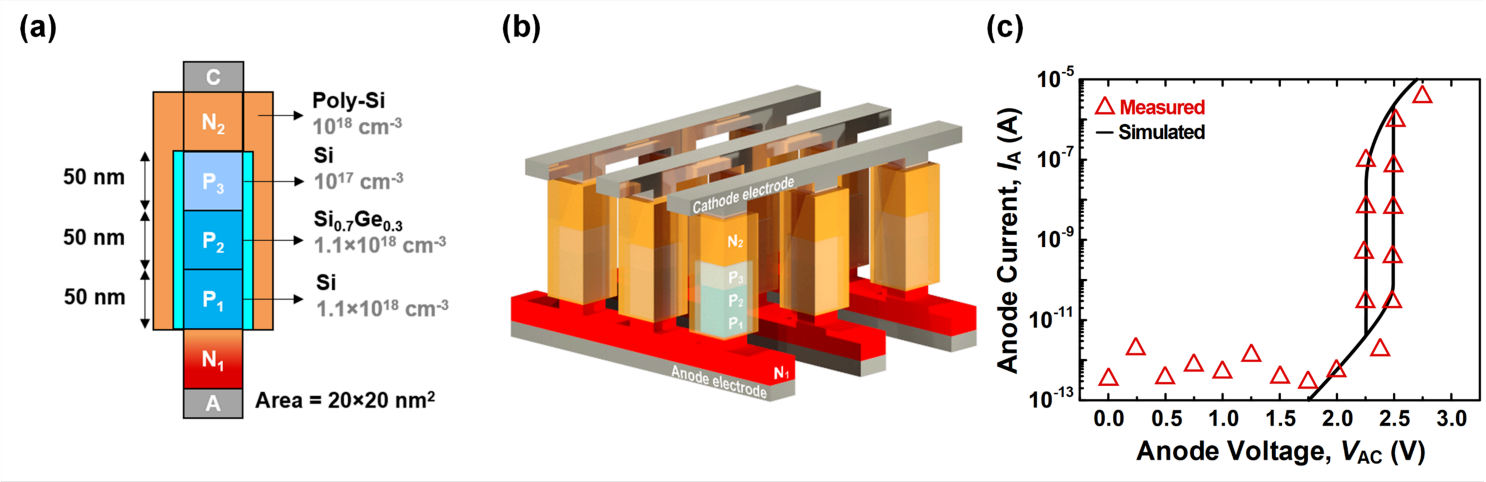


Figure 1

Schematic diagram of a proposed cell as (a) cross-sectional view of a unit cell and (b) vertical cross-point array. (c) A calibration result for hysteresis characteristics using experimental data obtained from the fabricated biristor.

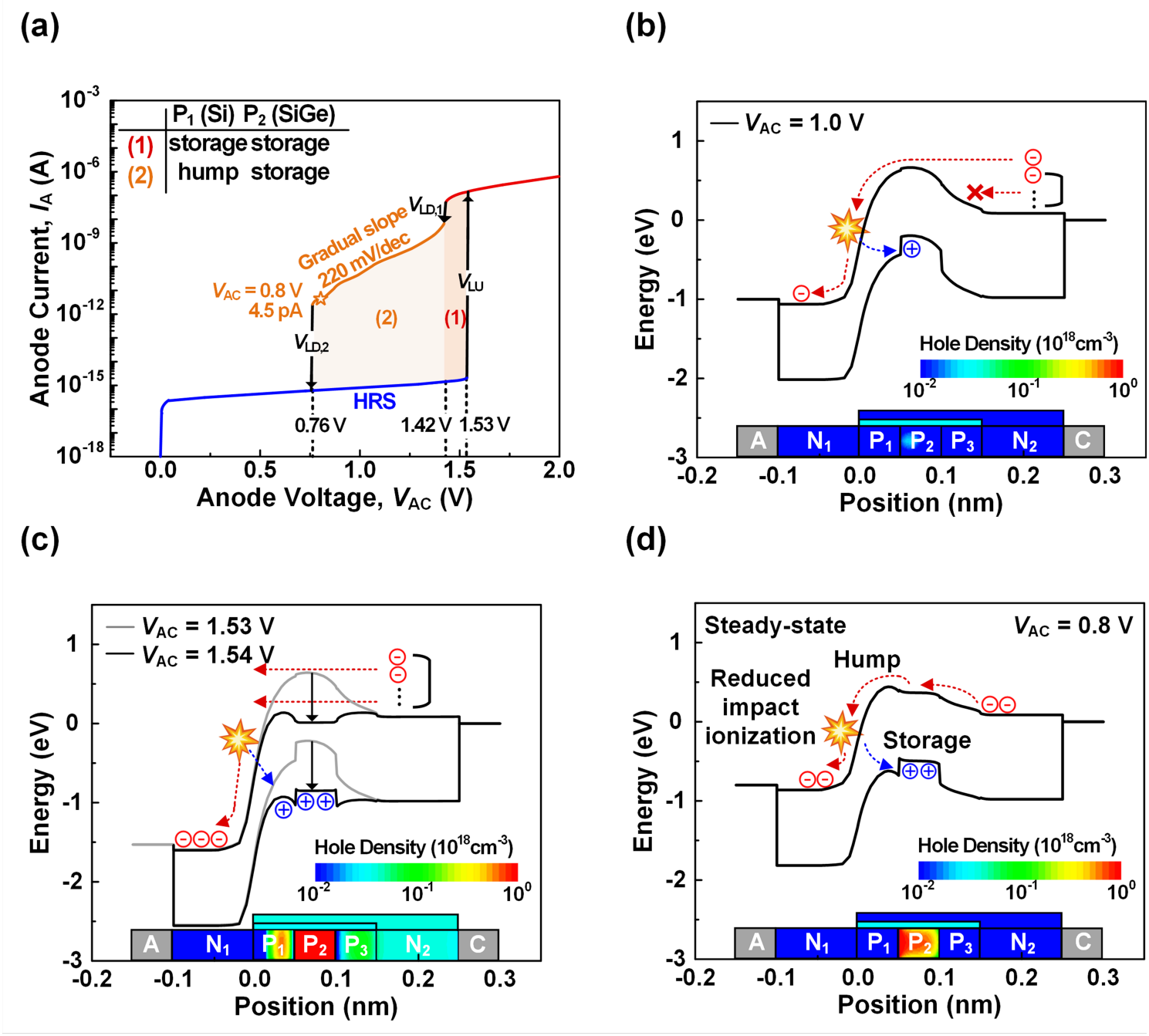


Figure 2

(a) I_A-V_{AC} hysteresis. (b) Energy band diagram at V_{AC} = 1.0 V in the HRS (c) Energy band diagram at V_{AC} = 1.53 V and 1.54 V, when the latch up phenomenon begins and completes. (d) Energy band diagram in the steady- state condition after latch-up at V_{AC} = 0.8 V.

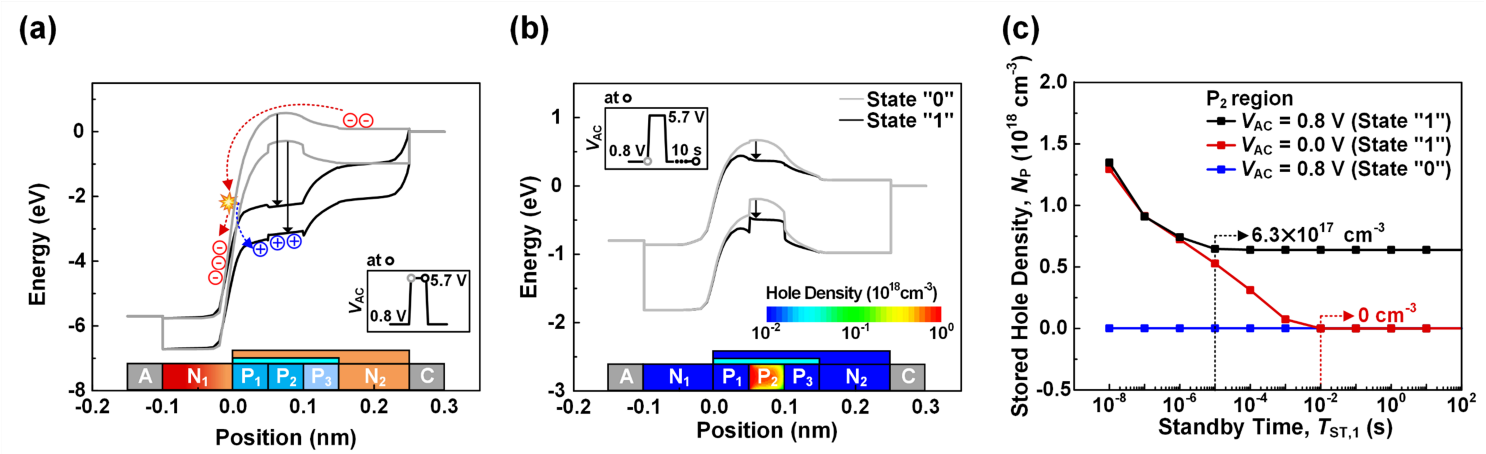


Figure 3

Write “1” operation (a) Energy band diagrams during the write “1” operation. (b) Energy band diagram at the V_{hold} (V_{AC} = 0.8 V) for state “0” and the steady-state condition after the write “1” operation. (c) Stored hole densities in the P_2 region for state “0” and state “1” with and without the V_{hold} as a function of standby time.

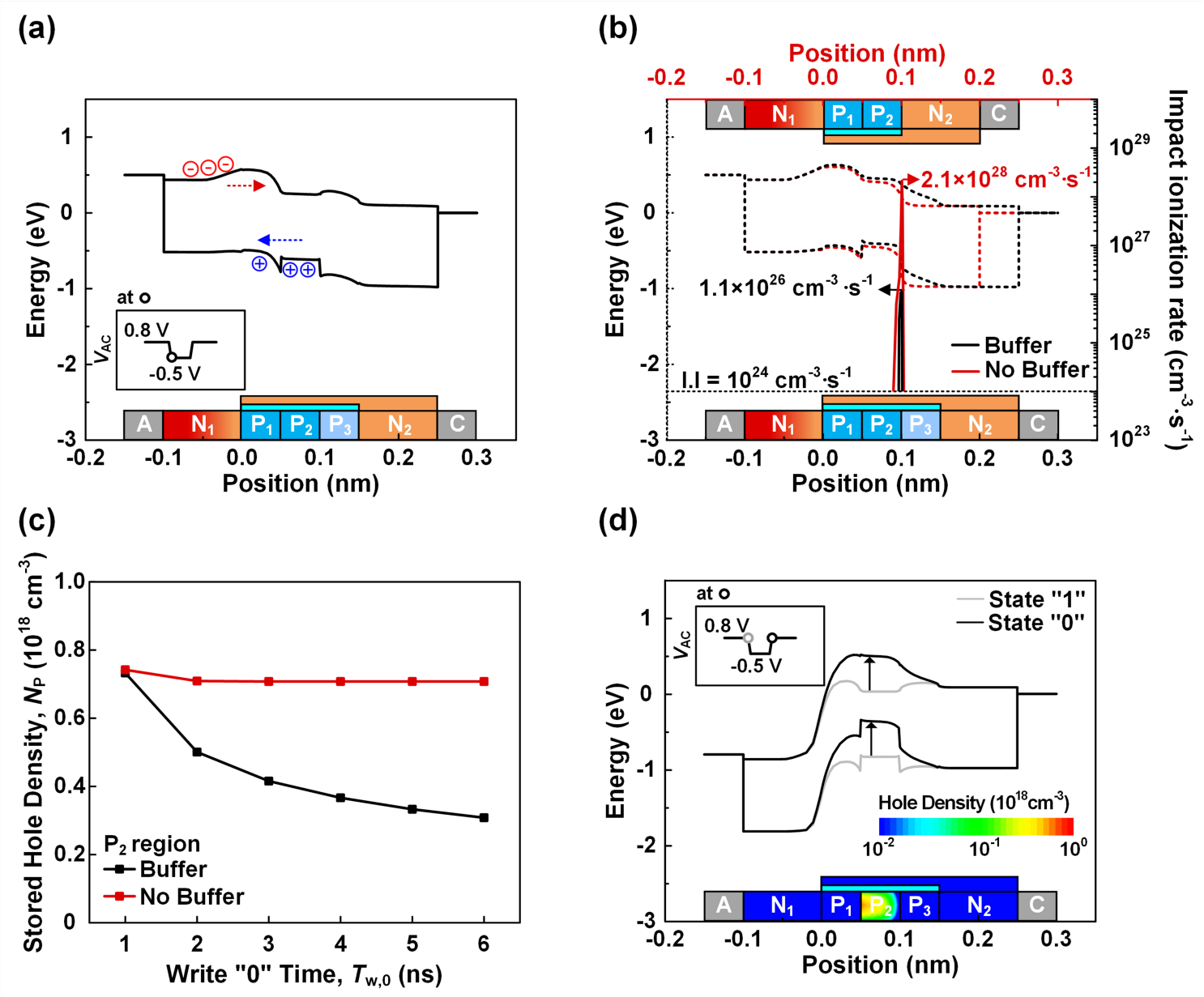


Figure 4

Write “0” operation (a) Energy band diagram at V_{AC} = -0.5 V when the write “0” pulse is applied for state “1”. (b) Comparison of the impact ionization rate and energy band diagrams during the write “0” operation with and without the buffer layer. (c) Stored hole densities in the P_2 region as a function of write “0” time for cases with and without the buffer layer. (d) Energy band diagram at the V_{hold} (V_{AC} = 0.8 V) for state “1” and state “0”.

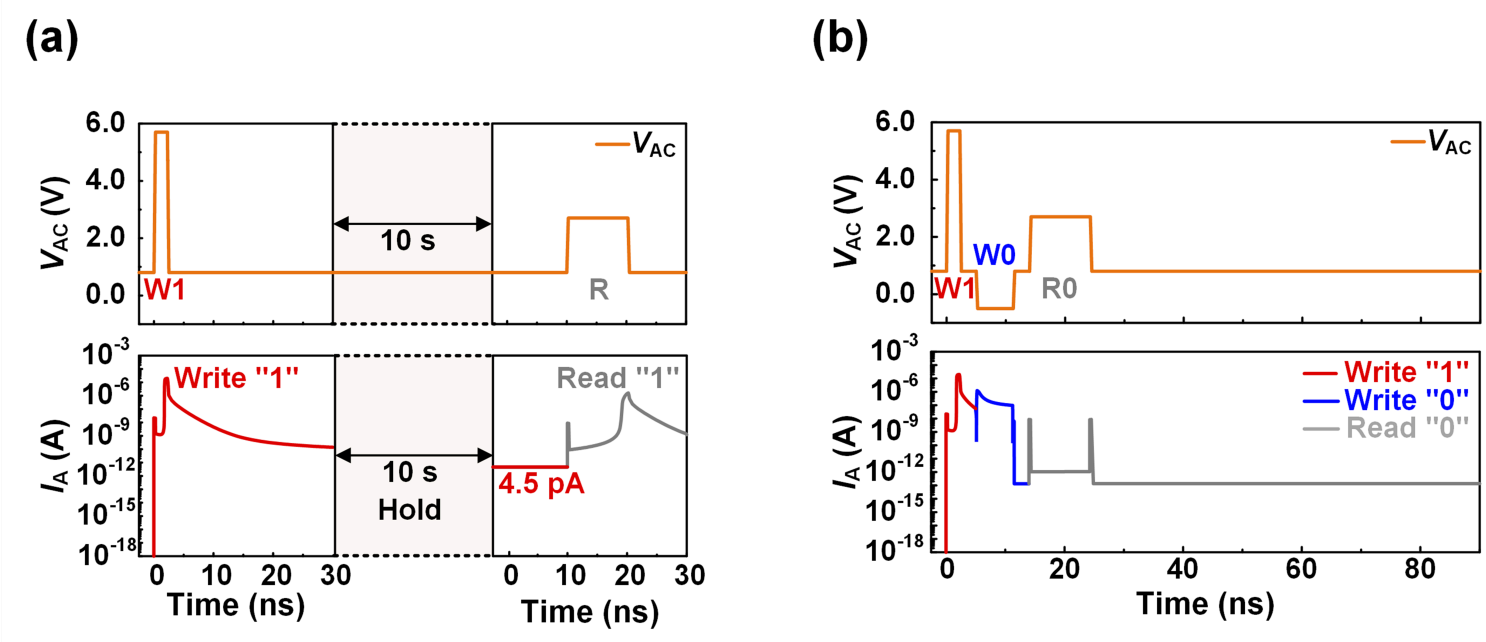


Figure 5

Read operation (a) The read “1” operation after retention of state “1” with a low standby current of 4.5 pA. (b) The read “0” operation after the write “0” operation.

Supplementary Files

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- Table1.tif