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A High-Gain Dual-Switch Non-Isolated Boost Converter: Analysis, Control, and Experimental Validation

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Abstract- This paper presents a dual-switch non-isolated boost converter (DSNIBC) for high gain DC-DC conversion in low-power applications. The proposed converter combines a switched-inductor topology with an additional switch-diode pair to attain a high voltage gain with moderate duty ratios. Two active switches, S_1 and S_2 , operate with interdependent duty cycles (d_1, d_2), yielding three CCM operating modes ($d_2 > d_1, d_1 > d_2, d_2 = d_1$). Steady-state analysis of all operating modes yields generalized expressions for voltage and current gain. Design guidelines for the inductors and capacitors are given to confirm continuous conduction and low current ripple. Comparative analysis confirms that DSNIBC obtain a favourable trade-off of voltage gain versus component count and stress. Small-signal state-space modeling is carried out for controller design. A sensitivity analysis is performed to identify the most suitable operating region for achieving a high voltage gain. A dominant duty-cycle control with PI controller is implemented to improve flexibility and transient response by seamlessly distributing control actions between the switches. The proposed DSNIBC is evaluated with a conventional INC MPPT algorithm, indicating stable photovoltaic power extraction under irradiance variation. The experimental results validate the proposed DSNIBC remains stable under load and source variation. The converter offers improved performance over conventional boost.

Index Terms- Two-switch high-gain DC-DC converter, switched-inductor, dominant duty-cycle control, MPPT, small-signal modeling.

I. INTRODUCTION

The growing demand for integration of low-voltage energy sources with higher-voltage DC distribution systems has driven the need for high gain DC-DC converters, especially for 12 V to 48 V conversions in applications like photovoltaic microinverters, electric vehicle auxiliary systems, telecom power supplies, point of load converters (POLC) and battery-based microgrids [1], [2], [3], and in multiport energy management systems integrating PV, battery, and DC loads [4]. Although conventional boost converters feature a simple design, achieving a voltage gain of four-times (4x) the source voltage requires operating it at a high duty ratio (around 0.75), which causes significant conduction and switching losses, high voltage and current stress on semiconductor devices, increased diode reverse-recovery losses, and greater sensitivity to parasitic elements, all of which degrade efficiency and

reliability [5], [6]. Cascading of converter is one option to mitigate these problems but it suffers from higher number of components, low power density, low efficiency due to cumulative losses through several conversion stages, and mainly sub-system interactions [7], [8]. In order to solve such problems, different high-gain converters have been developed which uses boosting cells formed by reconfiguring the interconnection of inductors, capacitors, diodes, and switches, such as switched-inductor, coupled-inductor, switched-capacitor, voltage multiplier cell, Z-source and quasi-Z-source etc. for exhibiting high voltage gain [9], [10]. Nevertheless, they can also pose certain challenges such as larger number of components, complicated control algorithms, and higher expenses [11]. Another approach to attain high voltage gain at lesser duty ratio was reported in [12], [13], [14] in which a switched-inductor topology is combined with two switches. Switched-inductor topology increases voltage level through the modification of the inductor connection from the parallel connection during charging to series connection during discharging, while two-switch enables more than one energy transfer path in each switching cycle. This technique allows voltage gains from 12 V to 48 V while operating at moderate duty cycles ($d \approx 0.5$) thereby providing flexibility for dynamic regulation and sufficient control margin. This minimizes voltage stresses on the switching devices leading to enhanced efficiency. Evaluation of high-gain converters includes parameters such as voltage gain, efficiency, duty cycle, stress on power switches, output ripple, transient responses, and EMI etc.

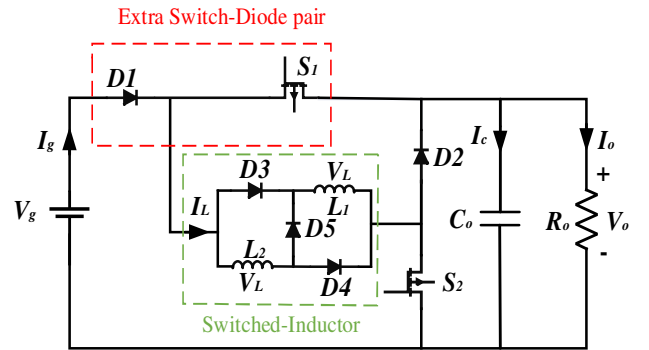


Fig. 1. Circuit diagram of proposed DSNIBC

TABLE I OPERATING MODES

Mode	S_1	S_2	$D1$	$D2$	$D3$	$D4$	$D5$	$d_2 > d_1$	$d_1 > d_2$	$d_2 = d_1$
1	ON	ON	OFF	OFF	ON	ON	OFF	✓	✓	✓
2	OFF	ON	ON	OFF	ON	ON	OFF	✓	✗	✗
3	ON	OFF	OFF	ON	ON	ON	ON	✗	✓	✗
4	OFF	OFF	ON	ON	OFF	OFF	ON	✓	✓	✓

Based on above discussion, this paper proposes and analyses a high voltage gain DC-DC boost converter which incorporates switched inductor together with switch-diode pair in a structure to ensure high voltage gain, efficient energy transfer, and minimize current ripple while keeping the circuit simple and able to operate under varying load conditions. In this converter extra switch is added, which provide partial energy transfer during one of the switching modes, where the inductor is charged by the output capacitor energy, along with the input source. As a result, the energy stored in the inductive element gets increased, enhancing the converter's voltage gain [15].

The topology, operational modes, and steady-state analysis of the proposed DSNIBC is presented in Section II. Section III presents the component design. In Section IV, the proposed topology is compared with other high-gain converters. Section V describes sensitivity analysis. Section VI presents dynamics analysis of the proposed DSNIBC. In Section VII, the theoretical developments are experimentally verified on laboratory-scale prototype of the converter. The last Section VIII, includes the conclusion.

II. PROPOSED CONVERTER, OPERATIONAL MODES AND STEADY-STATE ANALYSIS

This second-order boost derived converter is formulated using two inductors of equal value ($L=L_1=L_2$), two switches (S_1 and S_2), five diodes ($D1$ to $D5$), and one capacitor (C_o). Diodes $D1$, and $D2$ are forward-biased whenever switches S_1 and S_2 are turned OFF. Fig. 1. shows a proposed DSNIBC circuit with output voltage V_o , input voltage V_g , and load R_o .

A. Converter operational modes

Assuming that S_1 and S_2 have the duty ratios d_1 and d_2 , respectively, the DSNIBC has three distinct operational modes ($d_2 > d_1$, $d_1 > d_2$, and $d_2 = d_1$). The Continuous-Conduction

Mode (CCM) operation of the proposed DSNIBC is illustrated in Table I. The inductor current and output voltage waveforms for the various operating modes are shown in Fig. 2. Fig. 3 shows the circuit representation of the DSNIBC for all switching modes 1, 2, 3, and 4. The operation of the DSNIBC under different scenarios is described here.

a. Operating Mode when $d_2 > d_1$

For this operating mode, the suggested converter operates in three distinct switching modes (Mode 1, 2, and 4).

Mode 1- This stage includes the time interval t_{11} , where S_1 , S_2 , $D3$, and $D4$ are ON whereas $D1$, $D2$, and $D5$ are OFF as shown in Fig. 4 (a). The inductors L_1 and L_2 discharge their energy into the capacitor C_o . The equations corresponding to this stage are (1), and (2) as follows:

$$V_L = V_o \quad (1) \quad I_c = -I_L - I_o \quad (2)$$

Mode 2- For the time instant t_{12} , S_1 is reverse biased and S_2 is conducting. $D2$ and $D5$ are reverse biased and therefore are OFF whereas $D1$, $D3$, and $D4$ are forward biased as illustrated in Fig. 4 (b). For this case, C_o , the output capacitor, is the only available energy storage device to power the load while the inductors L_1 , and L_2 store energy from the input voltage V_g . The results in (3), and (4) can be obtained for this situation.

$$V_L = V_g \quad (3) \quad I_c = -I_o \quad (4)$$

Mode 4- S_1 , and S_2 are OFF during the time interval t_{13} , they are not conducting at this point as shown in Fig. 4 (d). The energy accumulated in the magnetic energy-storage elements L_1 , and L_2 is shifted to the load R_o . Accordingly, diodes $D3$, and $D4$ remain reversed-biased whereas $D1$, $D2$, and $D5$ provide the current conduction path. The inductor voltage and the capacitor current are determined using the circuit analysis in (5), and (6).

$$V_L = \frac{V_g - V_o}{2} \quad (5) \quad I_c = I_L - I_o \quad (6)$$

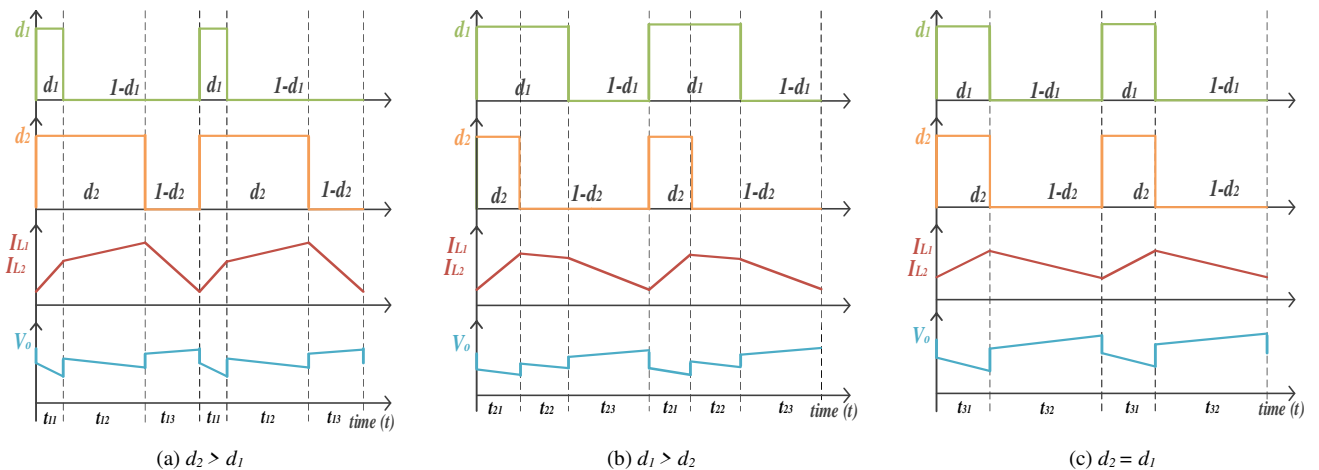


Fig. 2. Switching waveforms for different operation

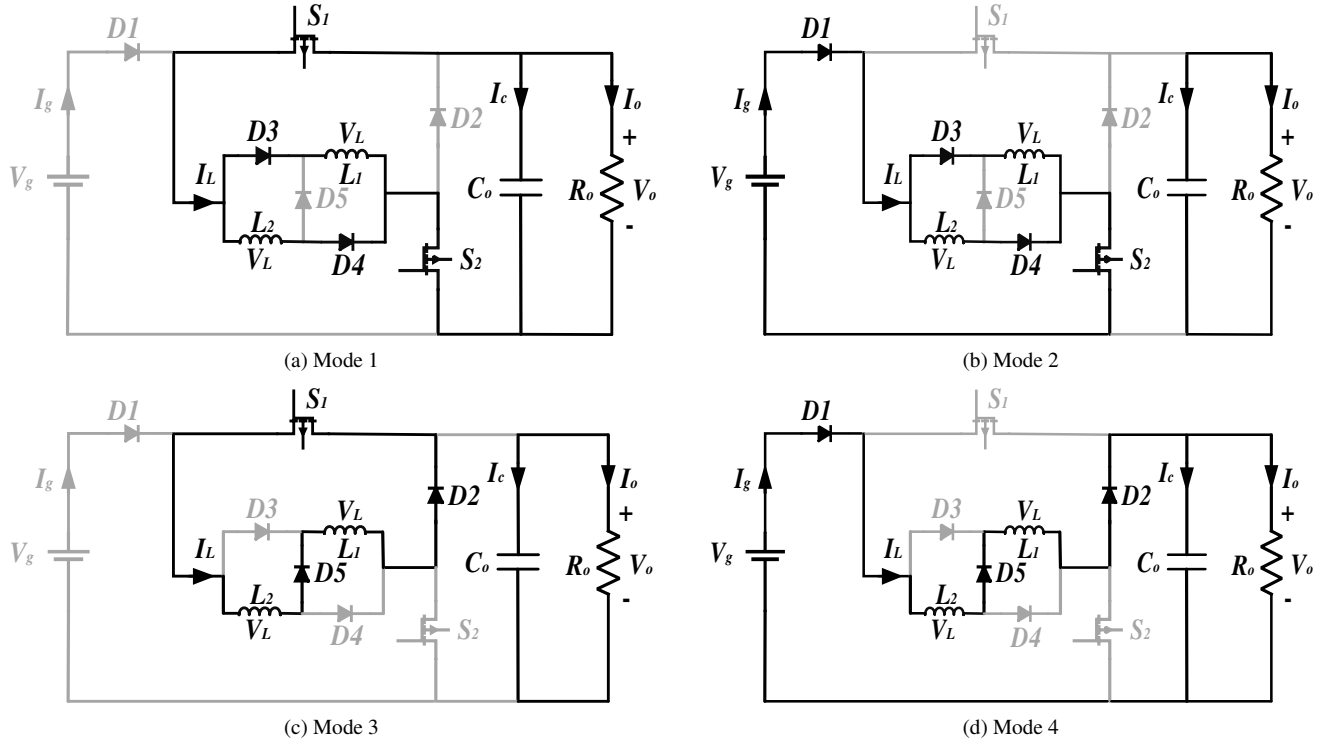


Fig. 3. Switching mode of proposed DSNIBC

b. Operating Mode when $d_1 > d_2$

In this mode of operation, the converter also shows three switching modes (Mode 1, 3, and 4). Mode 1, and Mode 4 are the same in operation as described in subsection a. The operation of Mode 3 is described as follows.

Mode 3- During the switching interval t_{22} , switch S_1 is turned ON and switch S_2 is turned OFF. D_2 , and D_5 are conducting whereas D_1 , D_3 , and D_4 are reversed-biased, as shown in Fig. 4 (c). By applying KVL and KCL, (7) and (8) are obtained.

$$V_L = 0 \quad (7) \quad I_c = -I_o \quad (8)$$

c. Operating Mode when $d_2 = d_1$

When the converter works in this operational mode, it only demonstrates two switching modes (Mode 1, and Mode 4). The activities in Mode 1 and Mode 4 are the same as mentioned in subsection a.

B. Steady-State Analysis

During CCM operation, the proposed DSNIBC is governed by the d_1 , and d_2 of the two switches S_1 , and S_2 , respectively, resulting in three switching sequences as discussed in the previous section. The derivation assumes ideal and lossless passive components, such that the net energy variation over a complete switching period T is zero. The steady-state governing equations are derived by applying the energy balance condition, resulting in the expressions listed in (1)-(8) of Table II.

The generalized formula for all operating mode of voltage gain and current gain as indicated in (9) and (10), respectively.

$$\frac{V_o}{V_g} = \frac{1 - d_1 + d_2 - d_m}{1 - d_1 - d_2 - d_m}; d_m = \min(d_1, d_2) \quad (9)$$

$$\frac{I_L}{I_o} = \frac{1}{1 - d_1 - d_2} \quad (10)$$

TABLE II VOLTAGE AND CURRENT GAIN FORMULA

Operational Mode	Voltage Gain (V_o/V_g)	Current Gain (I_L/I_o)
$d_2 > d_1$	$\frac{1 - 2d_1 + d_2}{1 - 2d_1 - d_2}$	$\frac{1}{1 - d_1 - d_2}$
$d_1 > d_2$	$\frac{1 - d_1}{1 - d_1 - 2d_2}$	
$d_2 = d_1$	$\frac{1 - d_2}{1 - 3d_2}$	$\frac{1}{1 - 2d_2}$

III. DESIGN CONSIDERATIONS

The passive components of proposed DSNIBC are governed by the requirements for CCM operation while meeting the specified current and voltage ripple constraints. The inductance values are obtained, so that the inductor current ripple is maintained within 10% to 30% of the average inductor current, thereby reducing peak current stress on inductors and semiconductor devices while reducing conduction loss. Accordingly, the inductance is chosen to be greater than the critical inductance determined from (11). Similarly, the output capacitor is selected according to the allowable output-voltage ripple and is chosen to be greater than the minimum capacitance specified by (12). Consequently, the selected passive-component values satisfy the CCM operating conditions and ensure stable converter operation under the rated operating conditions. The detailed derivation of the inductor and capacitor design procedure is provided in [15].

$$L_{crit.} = \frac{R_o d_2 (1 - d_1 - d_2)(1 - d_1 - d_2 + d_m)}{2p f_s (1 - d_1 - d_2 - d_m)} \quad (11)$$

$$C_o = \frac{(d_1 + d_2)(1 - d_1 - d_2 + d_m)}{R_o q f_s (1 - d_1 - d_2)} \quad (12)$$

TABLE III VOLTAGE AND CURRENT STRESSES ACROSS THE SWITCHES AND DIODES

Switching Component	Voltage Stress	Current Stress
S_1	$V_o - V_g$	$\frac{I_o}{1 - d_1 - d_2}$
S_2	V_o	
$D1$	$V_g - V_o$	
$D2$	$-V_o$	
$D3, D4$	$\frac{V_g - V_o}{2}$	$\frac{I_o}{2(1 - d_1 - d_2)}$
$D5$	$-\frac{V_o d_1 + V_g(d_2 - d_1)}{d_2}$	$\frac{I_o}{1 - d_1 - d_2}$

The selection of switching devices is governed according to maximum voltage and current stress requirements. The voltage

stress of power switches (S_1, S_2) and diodes ($D1-D5$) is evaluated during blocking state whereas the corresponding current stress is determined during conduction state. The analytical expression for voltage and current stresses is summarized in Table III.

IV. COMPARATIVE STUDY WITH OTHER TOPOLOGIES

A detailed comparison of the proposed DSNIBC with other reported high-gain dc-dc converters is carried out to evaluate its performance and merits over other converters. The specifications of the DSNIBC and other relevant converters, encompassing parameters such as voltage gain, voltage stress on power switches and diodes, total device count (TDC), and power density are listed in Table IV.

From Fig. 4, the proposed DSNIBC topology demonstrates a when compared with converters [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. In Fig. 4 (a) (voltage gain vs d_2), DSNIBC exhibits a steadily increasing and well-regulated gain profile, outperforming converters [16], [17], [18] and [23] across the entire duty cycle range, while remaining reasonably close to high-gain topologies such as [20], [21], [22], [24] and [25]. Although these converters achieve higher absolute gain,

TABLE IV COMPARISON BETWEEN THE DSNIBC AND EXISTING TOPOLOGIES

Ref.	Voltage Gain	Maximum Voltage stress across Switches w.r.t source voltage	Maximum Voltage stress across Diodes w.r.t source voltage	No. of		TDC	Power Density
				S	L		
				C	D		
[16]	$\frac{2}{1 - d_1 - d_2}$	$\frac{1}{1 - d_1 - d_2}$	$\frac{2}{1 - d_1 - d_2}$	3	2	12	Low
[17]	$\frac{2 - d_2}{1 - d_1 - d_2}$	$\frac{2 - d_2}{2(1 - d_1 - d_2)}$	$\frac{2 - d_2}{1 - d_1 - d_2}$	3	2	9	Medium
[18]	$\frac{3 - d_1 - 2d_2}{1 - d_1 - d_2}$	$\frac{2 - d_2}{2(1 - d_1 - d_2)}$	$\frac{2 - d_2}{1 - d_1 - d_2}$	3	2	12	Low
[19]	$\frac{3 + d_1 - d_2}{1 - d_1 - d_2}$	$\frac{2 - d_2}{2(1 - d_1 - d_2)}$	$\frac{2 - d_2}{1 - d_1 - d_2}$	3	2	12	Low
[20]	$\frac{3 + d_1 - d_2}{1 - d_1 - d_2}$	$\frac{2 - d_2}{2(1 - d_1 - d_2)}$	$\frac{2 - d_2}{1 - d_1 - d_2}$	3	2	14	Low
[21]	$\frac{5 - d_1 - 2d_2}{1 - d_1 - d_2}$	$\frac{6 - 2d_1 - 3d_2}{1 - d_1 - d_2}$	$\frac{3 + d_1}{1 - d_1 - d_2}$	3	4	20	Low
[22]	$\frac{5 + d_1 - 2d_2}{1 - d_1 - d_2}$	$\frac{2 - d_2}{2(1 - d_1 - d_2)}$	$\frac{2 - d_2}{1 - d_1 - d_2}$	3	2	16	Low
[23]	$\frac{1 + d_1}{1 - d_1 - d_2}$	$\frac{2 - d_2}{1 - d_1 - d_2}$	$\frac{1 + d_1}{1 - d_1 - d_2}$	3	2	8	High
[24]	$\frac{1 + 3d_1 + d_2}{1 - d_1 - d_2}$	$\frac{1 + 3d_1 + d_2}{1 - d_1 - d_2}$	$\frac{2(1 + d_1)}{1 - d_1 - d_2}$	3	4	16	Low
[25]	$\frac{3 + d_1 + d_2}{1 - d_1 - d_2}$	$\frac{3 + d_1 + d_2}{2(1 - d_1 - d_2)}$	$\frac{3 + d_1 + d_2}{1 - d_1 - d_2}$	3	4	20	Low
DSNIBC	$\frac{1 - 2d_1 + d_2}{1 - 2d_1 - d_2}$	$\frac{1 - 2d_1 + d_2}{1 - 2d_1 - d_2}$	$\frac{1 - 2d_1 + d_2}{1 - 2d_1 - d_2}$	2	2	10	Medium
				1	5		

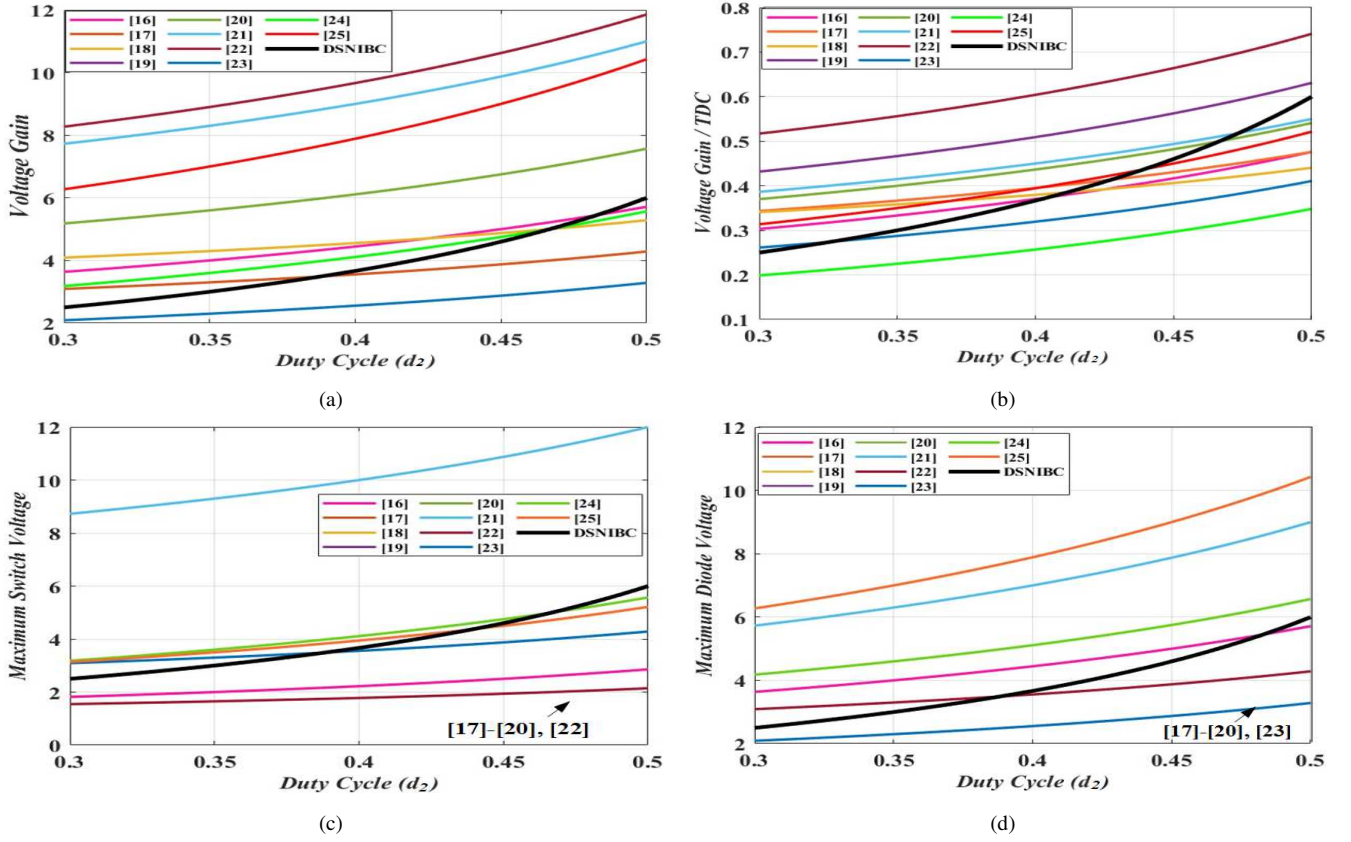


Fig. 4. Comparison results ($d_1 = 0.15$). (a) Voltage gain. (b) Ratio of voltage gain to TDC. (c) Maximum switch voltage. (d) Maximum diode voltage.

they rely on more complex structures and high duty cycle, whereas DSNIBC achieves a practical level of high gain without operating near extreme duty cycle. Fig. 4 (b) compares voltage gain-to-total device component (TDC) ratio as a function of d_2 . The proposed DSNIBC exhibits superior voltage gain per TDC over wide duty-cycle operating region. Although proposed converter operates at relatively lower duty cycle value, thereby surpassing the converters reported in [16], [17], [18], [23], [24], [25], while conversing toward the performance level of [20], [21], [22] at higher d_2 . These results confirm that proposed converter provides higher voltage conversion capability per device component. Fig. 4 (c) presents maximum switch voltage stress as a function of d_2 . The proposed DSNIBC maintain switch voltage stress throughout the operating range with gradual increase as the duty cycle increases, thereby avoiding the high switch stress as observed in [21] and [22]. Although converter reported in [16] and [17] exhibit lower stress; however, this advantage is achieved at an expense of reduced voltage gain, reflecting trade-off between voltage conversion capability and switch stress. In contrast, the proposed converter achieves an improved design balance between voltage conversion capability and switch stress. A similar trend is detected in Fig. 4 (d), where the maximum diode voltage stress as a function of d_2 . The proposed DSNIBC exhibits a gradual increase in diode voltage stress over the operating range with increasing duty cycle while maintaining significantly lower stress than the converter reported in [21] and [22]. The converter presented in [23] maintains, lower diode voltage stress; however, its voltage conversion capability

significantly lower voltage gain. This further reinforces the advantage of DSNIBC in achieving a balanced performance.

Overall, DSNIBC successfully addresses the fundamental design trade-offs in high gain DC-DC converters by simultaneously achieving competitive voltage gain, improved voltage gain-to-TDC ratio, and moderate semiconductor stress. Unlike converters [20], [21], [22], [23], [24], [25], which rely on increased complexity to achieve high gain, and converter [16], [17], [18], [19], which sacrifice gain for simplicity, the proposed DSNIBC provides a well-balanced and practically viable solution. Therefore, as clearly illustrated in Fig. 4, DSNIBC represents an efficient and optimized topology that effectively bridges the gap between high performance and implementation simplicity.

V. SENSITIVITY ANALYSIS

The proposed converter employs two switches whose duty cycles have unequal impact on the output voltage. Therefore, a sensitivity analysis is required to be performed to examine the influence of each duty cycle on the voltage gain. To identify the most effective control input for output-voltage regulation, the sensitivity of the voltage gain with respect to the duty cycles is evaluated. The sensitivity of the voltage gains with respect to a parameter d_1 and d_2 are defined in (13) and (14) respectively.

$$S_{M,d_1} = \frac{\partial M}{\partial d_1} \quad (13) \quad S_{M,d_2} = \frac{\partial M}{\partial d_2} \quad (14)$$

where M denotes the voltage gain. A larger magnitude of the sensitivity indicates that the voltage gain is more responsive to variations in the respective duty cycle.

Case I: $d_2 > d_1$

For this operating region, voltage gain is presented in (15).

$$M = \frac{1 - 2d_1 + d_2}{1 - 2d_1 - d_2} \quad (15)$$

The sensitivities with respect to d_1 and d_2 are obtained and presented in (16) and (17) respectively.

$$S_{M,d_1} = \frac{4d_2}{(1 - 2d_1 - d_2)^2} \quad (16)$$

$$S_{M,d_2} = \frac{2(1 - 2d_1)}{(1 - 2d_1 - d_2)^2} \quad (17)$$

The variation of the sensitivity coefficients over the operating region is illustrated in Fig. 5 (a). It is observed that the magnitude of S_{M,d_1} is higher than that of S_{M,d_2} , indicating that the output voltage is more sensitive to variations in duty cycle d_1 .

Case II: $d_1 > d_2$

For this operating region, voltage gain is presented in (18).

$$M = \frac{1 - d_1}{1 - d_1 - 2d_2} \quad (18)$$

The corresponding sensitivities are presented in (19) and (20) respectively.

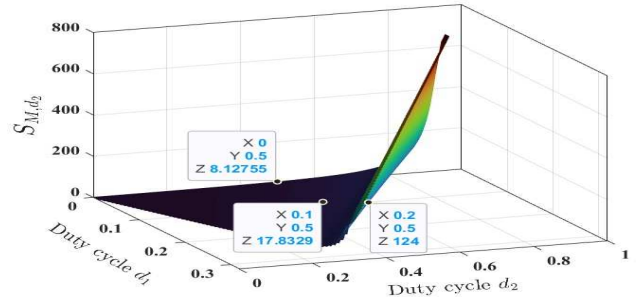
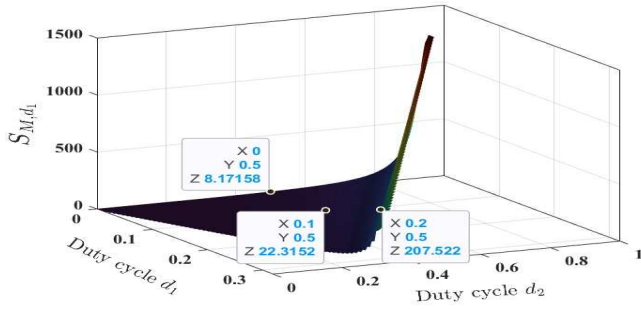
$$S_{M,d_1} = \frac{2d_2}{(1 - d_1 - 2d_2)^2} \quad (19)$$

$$S_{M,d_2} = \frac{2(1 - d_1)}{(1 - d_1 - 2d_2)^2} \quad (20)$$

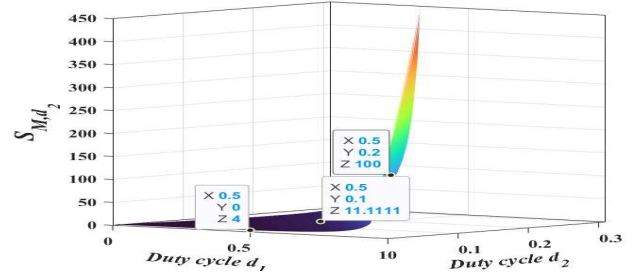
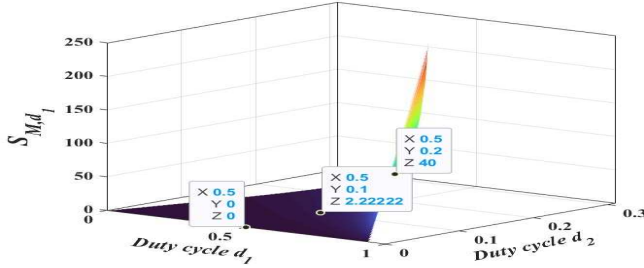
The sensitivity characteristics for this operating region are shown in Fig. 5 (b). The obtained results indicate that the voltage gain exhibits greater sensitivity to duty cycle d_2 .

The sensitivity analysis exposes that the impact of the duty cycles variation on the voltage gain depends on the operating mode. Specifically, the voltage gain is more sensitive to variations in d_1 for Case I, whereas it is more sensitive to variations in d_2 for Case II.

Therefore, it is necessary to identify the most suitable operating case for achieving a high voltage gain. To facilitate this comparison, 3D diagram of voltage-gain for case I and case II are presented in Fig 6 (a) and Fig 6 (b) respectively. Fig. 6 indicate that Case I provides a higher voltage gain over the feasible operating region than Case II. Consequently, Case I is identified as the preferred operating mode for achieving high-voltage-gain operation.

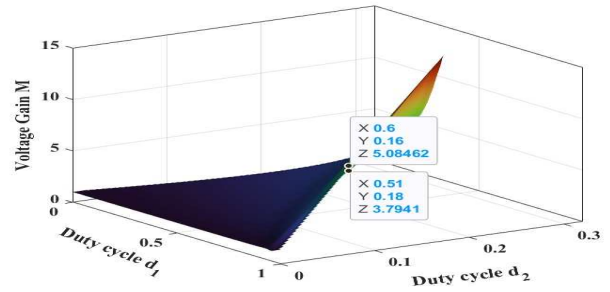
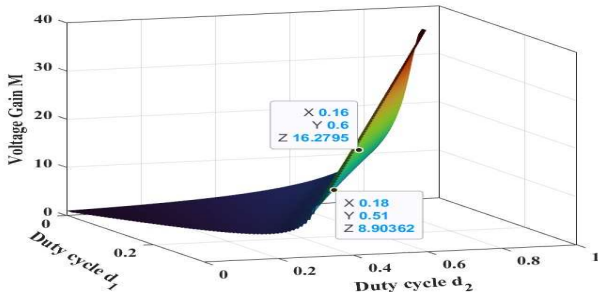


(a) Case I: $d_2 > d_1$



(b) Case II: $d_1 > d_2$

Fig. 5. 3D diagram of sensitivity



(a)

(b)

Fig. 6. 3D diagram of voltage-gain (a) $d_2 > d_1$, (b) $d_1 > d_2$

VI. DYNAMIC ANALYSIS

A. Small Signal Modeling

In this segment, a small-signal analysis is carried out, using state-space averaging for the various operational modes, to obtain the system dynamics and behavior to configure an appropriate controller for the proposed DSNIBC. The voltage loop equations for the converter are solved for the various operational modes in order to construct the state-space matrices. The average equations for large-signal state-space models for the various modes are obtained for the average equations over one switching period (T), shown in (21). For small-signal analysis, the perturbation variable is added to the DC steady-state of the system to obtain the variable, defined in (22). This method allows for the analysis of the small variations in the system inputs, states and the overall dynamics of the converter. (V_g, X, V_o, D) are the large-signal (DC) values and ($\hat{v}_g(t), \hat{x}(t), \hat{v}_o(t), \hat{d}(t)$) are the small-signal perturbations. Neglecting the second order perturbations (e.g. $\hat{x}(t) \cdot \hat{x}(t), \hat{x}(t) \cdot \hat{d}(t)$) is the simplifications of the model and separating the perturbation from steady-state terms. The small-signal model of the proposed DSNIBC is obtained in (23) to (25).

B. Dominant Duty-Cycle control

A single PI controller is designed based on small-single control-to-output transfer function with respect to dominant duty cycle d_2 . The auxiliary duty cycle d_1 is derived from the operating mode and duty constraints. Consequently, this approach ensures coordinated operation of the two active switches while maintaining accurate output-voltage regulation. The controller generates a duty command d_c , which is then allocated to the switches according to predefined weighting factors. For a two-switch converter, the duty ratios of switches S_1 , and S_2 , denoted by d_1 , and d_2 , are expressed in (26) and (27), respectively, where α_1 , and α_2 represent the duty's weighting factors. These factors limit the contribution of each switch in regulating the output voltage and are selected such that the generalized duty allocation constraint given in (28), is satisfied to prevent duty-cycle saturation and preserve operational margin.

Converters characterized by a state-space operation subject to an extra duty constraint are presented in (29). Substituting (26) and (27) into (29) yields the controller output constraint presented in (30), which defines the controller output range required for stable operation. This concept can be applied to converters that have multiple switches. The duty-cycle functions for each switch are expressed in (31), while generalized duty's weighting factors constraint governing flexible operating region in (32). This generalized duty-cycle formulation enables coordinated duty-cycle allocation between multiple switches through a single voltage loop control over the feasible operating region. As a result, the presented control strategy reduces controller implementation complexity while maintaining stable and coordinated operation throughout the feasible operating region.

$$d_1 = \alpha_1 d_c \quad (26)$$

$$d_2 = \alpha_2 d_c \quad (27)$$

$$\alpha_1 + \alpha_2 \leq 1 \quad (28)$$

$$d_1 + d_2 \leq 1 \quad (29)$$

$$(\alpha_1 + \alpha_2) d_c < 1 \quad (30)$$

$$d_i = \alpha_i d_c \quad (31)$$

$$\Sigma \alpha_i \leq 1 \quad (32)$$

For the proposed DSNIBC, the duty cycle weighting factors are chosen as $\alpha_1 = 0.15$ and $\alpha_2 = 0.7$, thereby switch S_2 assigning the dominant control authority and switch S_1 assigned for supplementary boosting. So, the controller output duty command d_c is distributed as $d_2 = 0.7 d_c$ and $d_1 = 0.15 d_c$. The weighting factor $\alpha_2 = 0.7$ is selected to maintain dominant contribution of switch S_2 while limiting high duty cycle operation that could otherwise increase conduction losses, semiconductor stress and control saturation. The remaining duty cycle command is allocated to switch S_1 based on presented control strategy.

C. Digital Controller Design

A closed-loop controller has been designed to control the output voltage of the DSNIBC and transfer function matrix is presented in equation (33). Among two active switches, switch S_2 shows a dominant effect on output voltage. So, control-to-output transfer function $G_{vd}(s)$ is obtained in equation (34) for operation when $d_2 > d_1$.

A PI controller is designed to ensure stable performance during changes in system dynamics. The Bode plots for the open-loop and closed-loop responses of the converter are compared in Fig. 7. The loop gain has a gain margin (GM) of 26.7 dB and a phase margin (PM) of 62.5°, with a crossover frequency of 514 Hz. To realize the controller on the DSP microcontroller, the controller transfer function is discretized, and the Z-domain representation is given in (35) using the bilinear transform.

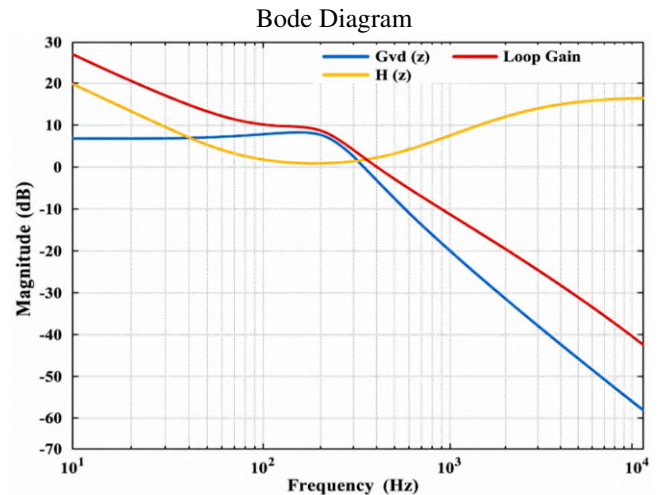


Fig. 7. Frequency response of the proposed DSNIBC.

D. Performance Evaluation Under MPPT Operation

In order to investigate the proposed DSNIBC for application in photovoltaic energy conversion, the converter was studied in combination with the classical Incremental Conductance (INC) MPPT algorithm. The INC algorithm is chosen by reason of its well-established tracking capability, which makes it the most

$$\dot{X} = AX + BV_g \quad \text{Where } X = [I_L \ V_{Co}]^T$$

$$Y = EX$$

$$A = d_m A_1 + (d_2 - d_m) A_2 + (1 - d_1 - d_2 + d_m) A_3 + (d_1 - d_m) A_4 \quad (21)$$

$$B = d_m B_1 + (d_2 - d_m) B_2 + (1 - d_1 - d_2 + d_m) B_3 + (d_1 - d_m) B_4$$

$$E = d_m E_1 + (d_2 - d_m) E_2 + (1 - d_1 - d_2 + d_m) E_3 + (d_1 - d_m) E_4$$

$$x(t) = X + \hat{x}(t) \quad v_o(t) = V_o + \hat{v}_o(t) \quad (22)$$

$$v_g(t) = V_g + \hat{v}_g(t) \quad d(t) = D + \hat{d}(t)$$

$$\hat{x}(t) = (sI - A)^{-1} [B \hat{v}_g(t) + R X_{ss} + S V_g]$$

$$\text{Where } R = \hat{d}_m A_1 + (\hat{d}_2 - \hat{d}_m) A_2 + (1 - \hat{d}_1 - \hat{d}_2 + \hat{d}_m) A_3 + (\hat{d}_1 - \hat{d}_m) A_4$$

$$S = \hat{d}_m B_1 + (\hat{d}_2 - \hat{d}_m) B_2 + (1 - \hat{d}_1 - \hat{d}_2 + \hat{d}_m) B_3 + (\hat{d}_1 - \hat{d}_m) B_4$$

$$X_{ss} = -A^{-1} B V_g$$

$$\begin{aligned} A_1 &= \begin{bmatrix} -\frac{1}{L}(r_L + \frac{r_c R}{(r_c + R)}) & \frac{R}{L(r_c + R)} \\ -\frac{R}{C(r_c + R)} & -\frac{1}{C(r_c + R)} \end{bmatrix} & B_1 &= \begin{bmatrix} 0 \\ 0 \end{bmatrix} & E_1 &= \begin{bmatrix} \frac{r_c R}{(r_c + R)} \\ R \end{bmatrix}^T \\ A_2 &= \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{C(r_c + R)} \end{bmatrix} & B_2 &= \begin{bmatrix} 1 \\ L \end{bmatrix} & E_2 &= \begin{bmatrix} 0 \\ R \end{bmatrix}^T \\ A_3 &= \begin{bmatrix} -\frac{1}{2L}(2r_L + \frac{r_c R}{(r_c + R)}) & -\frac{R}{2L(r_c + R)} \\ \frac{R}{C(r_c + R)} & -\frac{1}{C(r_c + R)} \end{bmatrix} & B_3 &= \begin{bmatrix} 1 \\ 2L \end{bmatrix} & E_3 &= \begin{bmatrix} -\frac{r_c R}{(r_c + R)} \\ R \end{bmatrix}^T \\ A_4 &= \begin{bmatrix} -\frac{r_L}{L} & 0 \\ -\frac{r_c}{C(r_c + R)} & -\frac{1}{C(r_c + R)} \end{bmatrix} & B_4 &= \begin{bmatrix} 0 \\ 0 \end{bmatrix} & E_4 &= \begin{bmatrix} 0 \\ R \end{bmatrix}^T \\ A &= \begin{bmatrix} -\frac{1}{2L}(2r_L + \frac{r_c R}{(r_c + R)})(1 - d_1 - d_2 - d_m) & -\frac{R}{2L(r_c + R)}(1 - d_1 - d_2 - d_m) \\ \frac{R}{C(r_c + R)}(1 - d_1 - d_2) - \frac{r_c}{C(r_c + R)}(d_1 - d_m) & -\frac{1}{C(r_c + R)} \end{bmatrix} \\ B &= \begin{bmatrix} \frac{1}{2L}(1 - d_1 + d_2 - d_m) \\ 0 \end{bmatrix} & E &= \begin{bmatrix} \frac{r_c R}{(r_c + R)}(1 - d_1 - d_2) \\ R \end{bmatrix}^T \end{aligned} \quad (23)$$

$$\frac{\hat{x}(t)}{\hat{d}_2} = (sI - A)^{-1} [(A_2 - A_1) X_{ss} + (B_2 - B_1) V_g] \quad (24)$$

$$\frac{\hat{x}(t)}{\hat{d}_1} = (sI - A)^{-1} [(A_4 - A_1) X_{ss} + (B_4 - B_1) V_g] \quad (25)$$

$$G(s) = \begin{bmatrix} G_{11}(s) & G_{12}(s) \\ G_{21}(s) & G_{22}(s) \end{bmatrix} = \begin{bmatrix} \frac{\hat{I}_L}{\hat{d}_1} & \frac{\hat{I}_L}{\hat{d}_2} \\ \frac{\hat{V}_o}{\hat{d}_1} & \frac{\hat{V}_o}{\hat{d}_2} \end{bmatrix} \quad (33)$$

$$G_{22}(s) = G_{vd}(s) = -0.118 \frac{(s - 98600)(s + 51700)}{(s + 835)(s + 3740)} \quad (34)$$

$$H(z) = 5.84 \frac{(z - 0.9487)(z - 0.9864)}{(z - 1)(z - 0.6688)}, \text{ Loop Gain} = G_{vd}(z) \cdot H(z) \quad (35)$$

used MPPT algorithm in PV power conversion systems. The MPPT controller uses the instantaneous photovoltaic current and voltage as a feedback variable and continuously updates the converter duty ratios so that operation at the maximum power point is maintained under varying irradiance conditions.

To demonstrate the MPPT performance under step reductions in the solar irradiance, Fig. 8 (a) shows the solar irradiance being stepped down from 1000 W/m^2 to 800 , 600 and 400 W/m^2 at 0.3 , 0.4 and 0.5 sec. , respectively. The corresponding photovoltaic power response, illustrated in Fig. 8 (b), the photovoltaic power initially tracks the irradiance profile, dropping from about 30 W to levels of about 24 W , 18 W and 12 W respectively. The operating point moves quickly to the new MPP following each irradiance transition with negligible steady-state oscillation, demonstrating the effective tracking capability of the INC algorithm.

The corresponding duty-cycle responses of switches S_1 and S_2 are presented in Fig. 8 (c). As the irradiance decreases, the

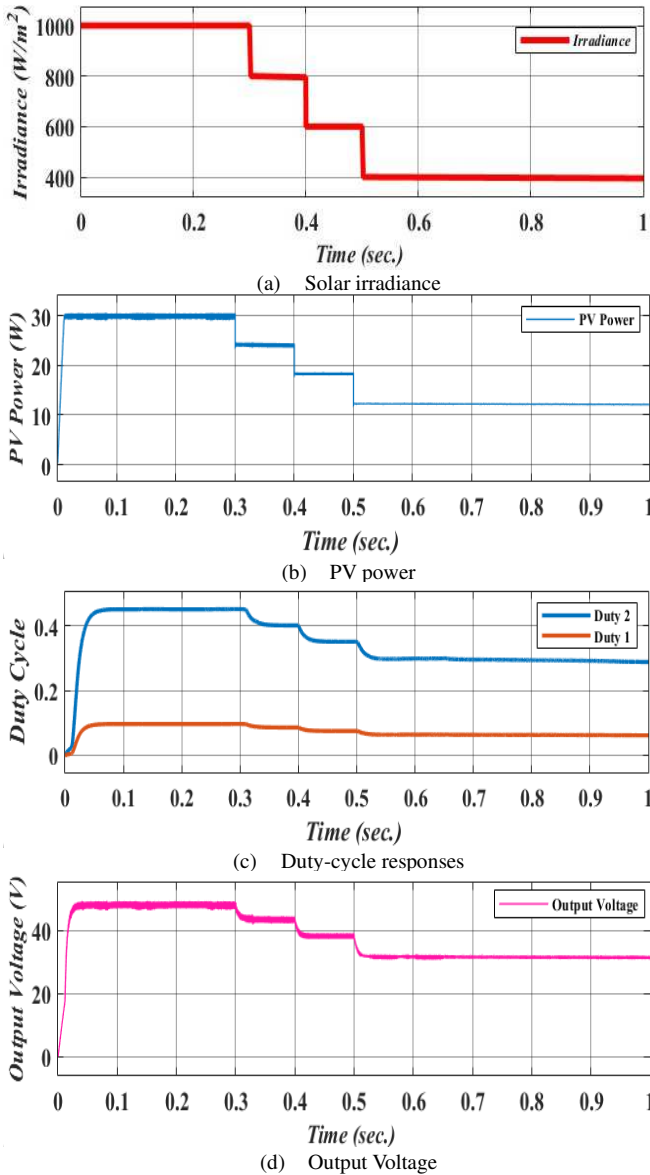


Fig. 8. MPPT performance of proposed DSNIBC under step variation in solar irradiance

decreasing from approximately 0.45 to 0.29 and d_1 from 0.09 to 0.06 , thereby maintaining efficient maximum power point controller adaptively adjusts both duty ratios, with d_2 operation over the entire irradiance range. The corresponding output-voltage response shown in Fig. 8 (d) decreases smoothly from approximately 48 V to 31 V as the available photovoltaic power decreases, while exhibiting fast transient settling and minimal steady-state oscillation. These responses confirm the stable dynamic behaviour of the proposed DSNIBC during MPPT operation.

VII. EXPERIMENTAL HARDWARE RESULTS

A laboratory-scale experimental prototype of the proposed DSNIBC was constructed to provide a regulated output voltage of 48 V at a rated output power of 24 W . The closed-loop control architecture, depicted in Fig. 9, was realized using the *TMS320F28335* microcontroller. A discrete-time voltage control algorithm was implemented to achieve accurate and stable output voltage regulation. The complete experimental setup, shown in Fig. 10, includes the converter prototype, input DC source, load, DSP controller, driver circuit, and measuring instruments. A laboratory-scale prototype was developed to experimentally validate the proposed analytical design and corroborate the corresponding simulation results. The parameter specifications used in the hardware implementation of the DSNIBC are as follows. The power switches are realized using *IRF540* MOSFETs each specified with 100 V and 23 A . The power diodes ($D1$ - $D5$) are implemented using *MUR1560* each specified with 600 V and 15 A to establish required energy transfer within the converter topology. The magnetic energy storage stage is realized using, L_1 and L_2 , each with an inductance of $200 \mu\text{H}$. The output filter employs a $100 \mu\text{F}$ electrolytic capacitor (C_o) to provide smooth output voltage and reduce ripple. The converter was then investigated experimentally, under closed-loop operation, at 50 kHz switching frequency with V_o regulated at 48 V . At the operating point 24 W , the duty ratio d_1 was measured to be 0.12 and d_2 was 0.56 . Fig. 11 (a) shows the controlled output voltage, with less than 5% ripple. Additionally, Fig. 11 (b) shows the inductor current and the experimental results show that the inductor current ripple is less than 20% of the rated current. Voltage stress on the main switch (S_2) and diode (D_2) is shown in Fig. 11 (c) and Fig. 11 (d).

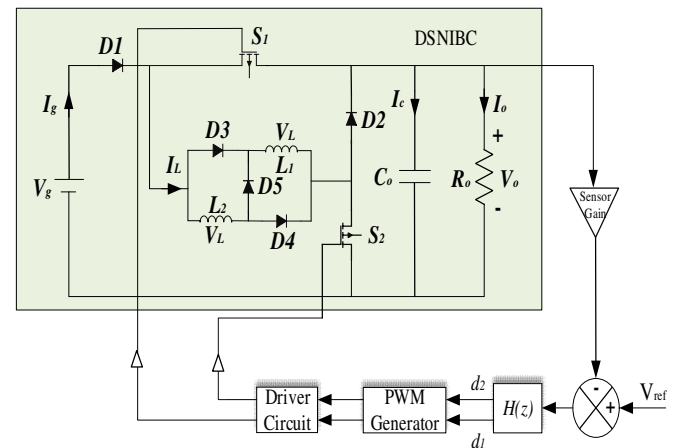


Fig. 9. Closed-loop control architecture of the proposed DSNIBC

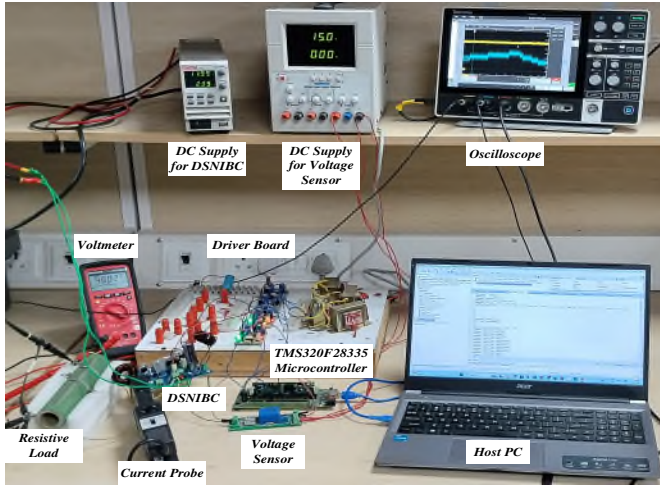


Fig. 10. Hardware prototype setup for proposed DSNIBC

The closed-loop dynamic response of proposed DSNIBC was evaluated by doing load variations to assess output voltage regulation. A decrease in load resistance from $100\ \Omega$ to $50\ \Omega$, causing the output current to increase from 0.5 A to 1 A , so raising the output power from 24 W to 48 W . As exposed in Fig. 12 (a), the output voltage experienced a transient undershoot of approximately 7 V , followed by settling to the reference value within 35 ms . The experimental results verify that presented control strategy maintain precise output voltage regulation under abrupt load variation.

To further investigate the transient regulation capability of controller, experimental tests were conducted under 1 V step source variations to emulate practical operating conditions. For an input-voltage transition from 12 V to 15 V , the controller rejected this input-voltage variation and maintained the output voltage at its reference value of 48 V . Likewise, following an

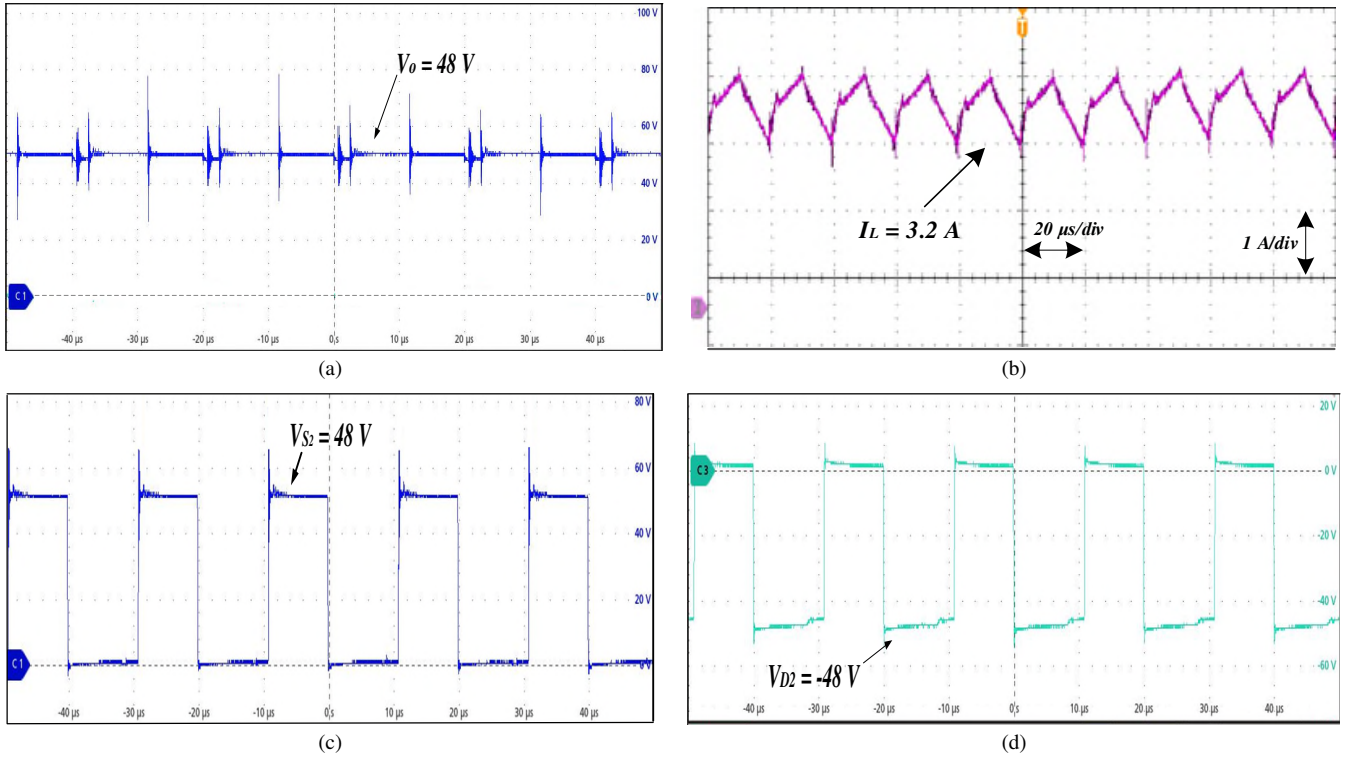


Fig. 11. (a) Regulated output voltage (V_o), (b) Inductor current (I_L), (c) Voltage stress (V_{S2}), (d) Voltage across diode (V_{D2}).

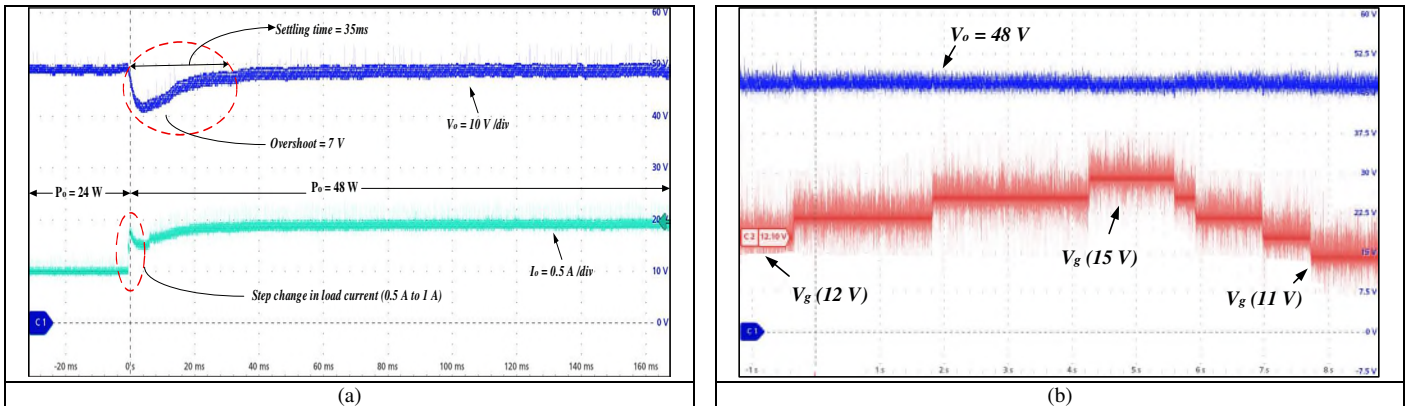


Fig. 12. Dynamic response of the proposed DSNIBC (a) under 50% load variation from 25 W to 48 W (b) under 20% source variation (from 12 V to 15 V and 15 V to 11 V).

input-voltage step from 15 V to 11 V, the controller restores the output voltage back to reference value, as shown in Fig. 12 (b). The obtained experimental results confirm that the presented control strategy achieves stable output voltage regulation under both load and source variation, demonstrating its applicability to low power DC-DC converter.

VIII. CONCLUSION

In this work, proposed DSNIBC is developed to achieve high gain DC-DC conversion. The converter uses two active switches, which operate at different duty ratios. This arrangement achieves much higher voltage gain at moderate duty ratios than a conventional boost converter. Since the two switches (S_1 and S_2) can have either higher or lower duty, the converter operates in three continuous-conduction modes ($d_2 > d_1$, $d_1 > d_2$, and $d_2 = d_1$). The steady-state voltage-gain expressions for all operating modes have been derived, and design equations have been presented to facilitate converter design. Sensitivity analysis and 3D voltage-gain characteristics have been utilized to identify the most suitable operating region for high-voltage-gain operation. Based on this analysis, Case I ($d_2 > d_1$) has been identified as the preferred operating mode owing to its superior voltage-gain characteristics. In addition, a small-signal state-space model of the DSNIBC has been developed to guide the controller design. The dominant duty-cycle control enables the voltage regulation by assigning the primary control to dominant switch. The converter was also evaluated for PV operating condition with INC algorithm, confirming stable MPPT during irradiance variation. The experimental results obtained from a 24 W laboratory-scale prototype confirm the theoretical prediction. The proposed DSNIBC successfully regulated 48 V output under source variation from 12 V to 15 V and from 15 V to 11 V, while maintaining low output voltage ripple. The measured inductor current ripple was maintained below about 20 % of inductor current. During close-loop operation, the converter demonstrated stable output voltage regulation and fast transient response under dynamic operating condition. Compared with reported two-switch high gain converters, the proposed DSNIBC offers a more favorable trade-off between voltage gain, component count, and semiconductor stress without increasing circuit complexity.

In conclusion, the proposed DSNIBC offers a compact, effective design for low power applications. Its design strikes a balance to achieve a high voltage gain, resulting in stable operation. The key contribution of this work is the integration of two-switch operation which provides partial energy transfer, where the inductor is charged by the output capacitor energy, in addition to the input source and dominant duty-cycle control into a switched-inductor boost topology, achieving high gain with a simple, robust structure. In the future, the focus will be on higher-power implementations. This will include soft-switching techniques to further minimize losses as well as multi-input versions for hybrid energy systems.

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