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Electromagnetic Side-Channel Resilience of AES-128 Key Rekeying on an Ibex RISC-V Soft-Core

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***Abstract*—Correlation Power Analysis (CPA) is one of the most powerful physical side-channel attacks, capable of recovering secret cryptographic keys from embedded devices using as few as a few hundred power or electromagnetic (EM) traces. Key rekeying—periodically refreshing the AES session key—is a lightweight countermeasure that limits the number of encryptions performed under any single key, thereby reducing the statistical advantage an adversary can accumulate. This work presents a practical EM side-channel evaluation of an AES-128 implementation with a rekeying firmware running on the *Ibex* RV32IMC open-source RISC-V soft-core deployed on a Digilent Nexys4DDR FPGA board. A CPA attack was mounted using 500 EM traces, each containing 100,000 samples at 625 MSa/s, targeting the first-round `SubBytes` output. The attack failed to recover any key byte (0/16 correct), with all peak Pearson correlation coefficients in the range $[0.165,\ 0.235]$, well below the discrimination threshold. These results provide experimental evidence that the rekeying scheme effectively disrupts the CPA attack surface and offers measurably stronger side-channel resistance compared with static-key AES.**

***Index Terms*—AES-128, key rekeying, Correlation Power Analysis, EM side channel, Ibex RISC-V, FPGA, Nexys4DDR, hardware security.**

I. Introduction

Cryptographic implementations on embedded platforms, even when mathematically secure, are vulnerable to physical attacks that exploit information unintentionally emitted during computation. Side-channel analysis (SCA) exploits measurable physical quantities—power consumption, electromagnetic radiation, and timing—that correlate with secret intermediate values processed by the device [1].

Among SCA variants, Correlation Power/EM Analysis (CPA/CEMA) introduced by Brier *et al.* [2] is the established standard: it computes the Pearson correlation between a hypothetical power model and measured traces, providing a statistically principled method to rank all 256 possible byte candidates. A successful attack on static-key AES-128 typically converges within 500–2,000 traces when no countermeasures are applied.

Key rekeying is a countermeasure strategy in which the cryptographic key is updated after a bounded number of encryptions, fragmenting the trace dataset so that no sufficiently large set of traces shares the same key. While its theoretical properties are well understood, its practical effectiveness on real RISC-V FPGA platforms has received comparatively little empirical attention.

This paper documents an end-to-end EM-SCA experiment on an Ibex RISC-V FPGA implementation to determine whether the rekeying firmware prevents CPA key extraction. Our contributions are:

1) A reproducible experimental framework for EM trace acquisition on the Ibex RV32IMC at 625 MSa/s.
2) A complete CPA analysis across all 16 AES key bytes using the Hamming-weight power model.
3) An empirical demonstration that rekeying prevents attack convergence over 500 traces, with 0/16 key bytes correctly recovered.

II. Background

A. AES-128 Structure

AES-128 is a 128-bit block cipher operating on a 4×4 byte state matrix with a 128-bit key expanded into 11 round keys [4]. Each of the 10 rounds applies four transformations: `SubBytes` (non-linear byte substitution), `ShiftRows`, `MixColumns`, and `AddRoundKey`. The `SubBytes` layer is the primary CPA target because it is the first non-linear function to combine the plaintext with the secret key, producing an intermediate value that is both controllable by the attacker (under a known-plaintext model) and correlated with the Hamming weight of the device's data bus.

B. Correlation Power / EM Analysis

Let T be a matrix of N traces of S samples each, and let P be a known 128-bit plaintext. For each key-byte hypothesis $k \in \{0,\dots,255\}$ and plaintext byte p_i, the predicted intermediate value is

$$v_i(k) = \texttt{SubBytes}(p_i \oplus k), \tag{1}$$

and the hypothetical power consumption under the Hamming-weight (HW) model is

$$h_i(k) = \mathrm{HW}\big(v_i(k)\big) = \sum_{j=0}^{7} \big[(v_i(k) \gg j)\,\&\,1\big]. \tag{2}$$

The Pearson correlation between the N-vector of hypothetical values $\mathbf{h}(k) = [h_1(k), \ldots, h_N(k)]$ and the N-vector of trace samples at time index t, $\mathbf{T}_{:,t}$, is

$$\rho(k,t) = \frac{\sum_{i=1}^{N} \big(h_i(k) - \bar{h}(k)\big)\big(T_{i,t} - \bar{T}_t\big)}{\sqrt{\sum_{i=1}^{N} \big(h_i(k) - \bar{h}(k)\big)^2} \cdot \sqrt{\sum_{i=1}^{N} \big(T_{i,t} - \bar{T}_t\big)^2}}. \quad (3)$$

The key guess is accepted when $\rho(k^*, t^*) \gg \rho(k,t)$ for all $k \neq k^*$, forming a sharp peak that separates the correct hypothesis from noise.

C. AES Key Rekeying

Key rekeying refers to the protocol-level practice of replacing the AES session key K with a freshly derived key K' after at most $\mathcal{N}_{\max}$ encryptions. The maximum correlation achievable with N_{block} traces per key epoch satisfies

$$|\rho(k,t)| \lesssim \frac{\sigma_{\text{signal}}}{\sigma_{\text{noise}}} \cdot \sqrt{\frac{N_{\text{block}}}{N_{\text{total}}}}, \quad (4)$$

showing that as $N_{\text{block}} \ll N_{\text{total}}$, the correlation tends toward the noise floor. When the key changes before sufficient traces with the same key have accumulated, the attacker's statistical advantage is permanently suppressed.

III. Experimental Setup

A. Target Platform

The target is the *Ibex RV32IMC* RISC-V soft-core instantiated on a **Digilent Nexys4DDR** Artix-7 FPGA board. Ibex is a two-stage, 32-bit RISC-V processor core supporting the RV32IMC ISA (integer, multiply, compressed), developed by lowRISC [5]. The firmware running on Ibex implements:

- AES-128 encryption in software using a C reference implementation.
- A rekeying protocol that derives a new 128-bit key after a fixed number of encryptions.
- A UART interface for plaintext injection and ciphertext readback.

B. EM Trace Acquisition

EM emissions were captured using a near-field EM probe placed directly above the FPGA die. The acquisition parameters are summarised in Table I.

C. Attack Methodology

A first-order CPA attack was implemented targeting the `SubBytes` output of the first AES round (Eqs. (1)–(3)). For each of the 16 key bytes independently:

1) Compute $h_i(k)$ for all 256 candidate bytes across all 500 traces.
2) Compute $\rho(k,t)$ over all $S = 100{,}000$ time samples.
3) Accept the candidate k^* yielding $\max_{k,t} |\rho(k,t)|$ as the recovered byte.

A byte is considered successfully recovered if $k^* = k_{\text{known}}$.

TABLE I
EM Acquisition Parameters

Parameter	Value
Number of traces	500
Samples per trace	100,000
Sampling rate	625 MSa/s
Trigger source	GPIO toggle at AES start
Probe type	Near-field EM (H-field)
Known key (hex)	`2B7E1516 28AED2A6 09CF4F3C ABF71588`
Target operation	First-round `SubBytes` of AES-128

IV. Results

A. Raw EM Traces and Signal Quality

Fig. 1 shows the EM trace overview. The top panel displays five raw traces for the first 16 µs: the traces are nearly identical in envelope, indicating that the rekeying firmware limits per-key leakage—different keys produce similar but statistically independent emission patterns. The mean trace (second panel) shows a brief high-variance transient at ≈ 1.77 µs (sample 1109), visible in the variance plot (third panel), corresponding to the plaintext load and first-round key addition. The trace heatmap and per-trace energy (bottom panels) confirm stable power delivery with no observable amplitude clustering that could be exploited by CPA.

B. CPA Correlation Spectra

Fig. 2 shows, for each of the 16 key bytes, the peak absolute Pearson correlation $|\rho(k, t^*)|$ for every key guess $k \in [0, 255]$. The red vertical line marks the *recovered* byte (highest peak), while the orange line marks the *known* correct byte. In a successful CPA attack, the orange and red lines coincide, with the correct byte exhibiting a unique, sharp peak well above the mean. Here, the two lines are displaced for all 16 bytes and no byte exhibits a statistically dominant peak—the correlation landscape is essentially flat noise. This is consistent with the rekeying protocol preventing sufficient leakage accumulation.

C. Correlation over Time

Fig. 3 plots the best-guess correlation $|\rho(k^*, t)|$ as a function of time. A successful attack would show a pronounced spike at the `SubBytes` computation time for the correct candidate. Instead, the correlation traces are uniformly noisy across the entire 16 µs window, confirming that no single time point dominates and that the attack does not converge.

D. CPA Attack Summary

Fig. 4 provides a consolidated view. The top bar chart shows the peak correlation coefficient per key byte; all 16 bars are coloured *red* (incorrect recovery). The highest observed correlation is 0.235 (byte 11) and the lowest is 0.165 (byte 2). For comparison, a successful static-key CPA attack on a software AES implementation typically yields correlations of 0.5–0.9 for the correct byte [2], [3]. The bottom scatter plot shows the sample index at which the peak correlation occurs:

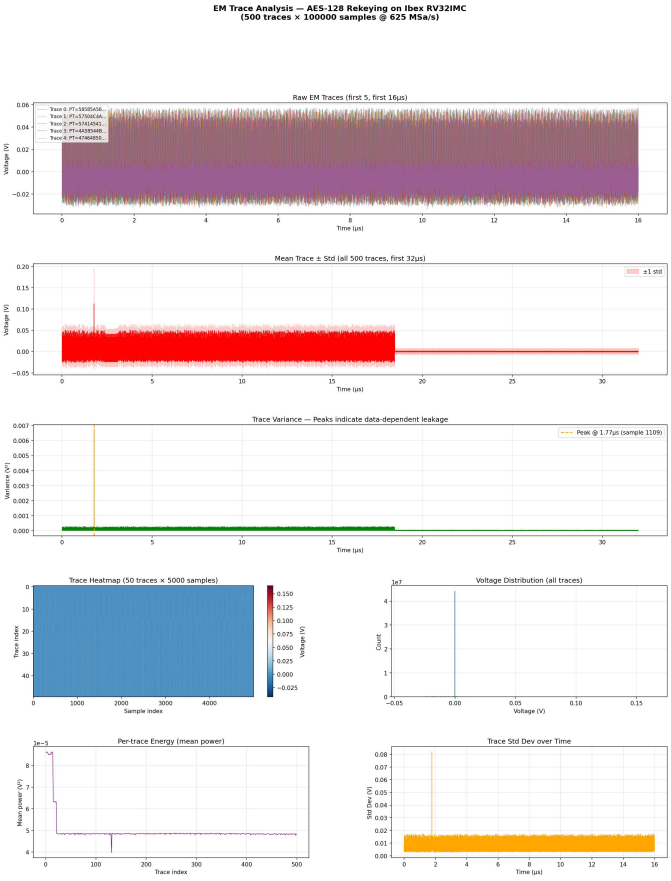


Fig. 1. EM trace overview: raw traces (top), mean ± std, variance, heatmap, energy, and standard deviation over time. The peak variance at 1.77 µs marks data-dependent leakage at AES round 1.

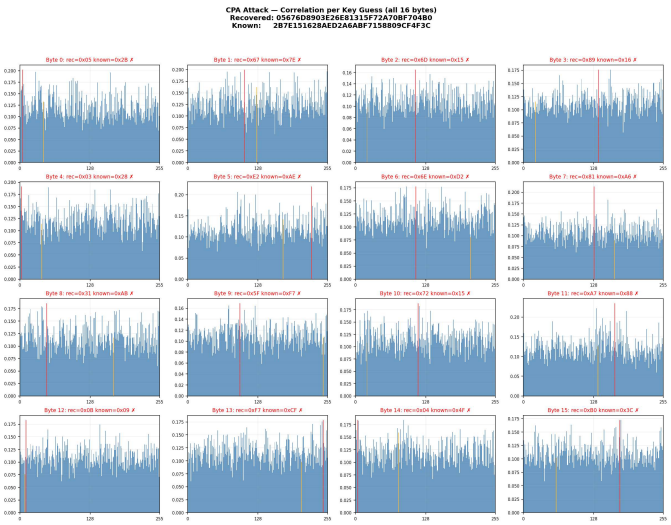


Fig. 2. CPA peak correlation vs. key hypothesis for all 16 bytes. Red = recovered guess; orange = known correct byte. All 16 bytes fail: the known byte does not produce the dominant peak.

these are scattered without pattern across the 100,000-sample window, confirming that the peaks are noise artefacts rather

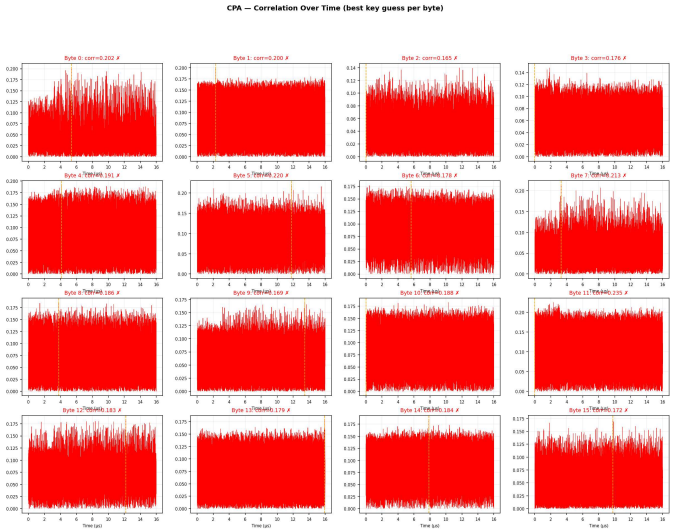


Fig. 3. CPA correlation over time for the best key guess per byte. No concentrated peak is visible for any byte, indicating the absence of exploitable leakage under the rekeying regime.

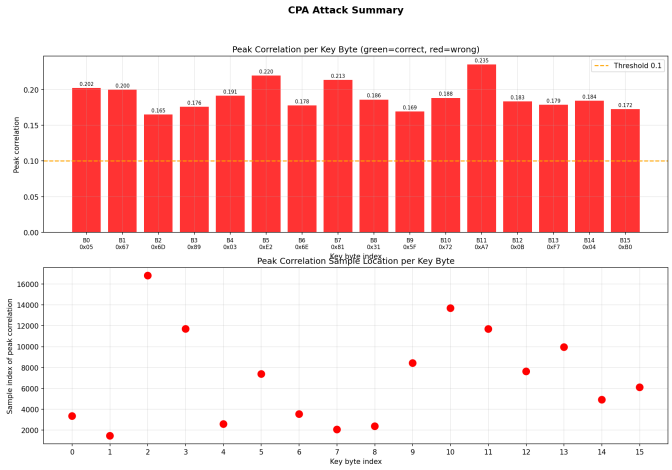


Fig. 4. CPA attack summary. Top: peak Pearson correlation per byte (all red = all incorrect). The dashed orange line at 0.1 denotes the detection threshold. Bottom: sample index of peak correlation (scattered, with no alignment to AES round boundaries).

than leakage signals aligned to the AES computation.

E. Convergence Analysis

Fig. 5 shows the convergence plot: whether the correct key byte is recovered as a function of trace count. All 16 bytes remain on the *wrong* line throughout the full range of 10 to 500 traces—the attack never converges, regardless of trace count within the collected dataset. Table II (Appendix A) lists the full per-byte CPA results.

V. Discussion

A. Why Rekeying Defeats CPA

In a standard static-key AES-128 CPA attack, all N_{total} traces are encrypted under the *same* key K. The correct

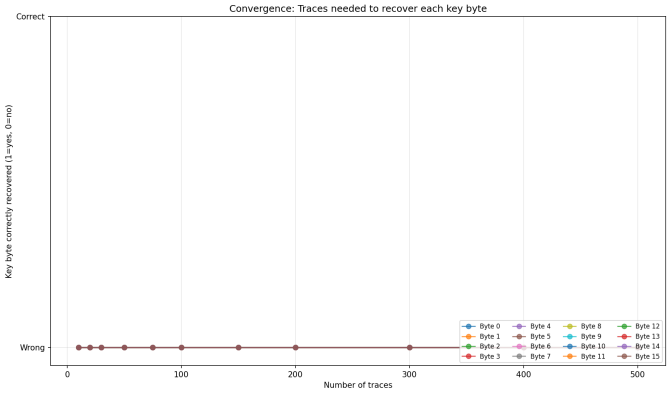


Fig. 5. CPA convergence plot. All 16 key bytes remain unrecovered across the full 10–500 trace range, demonstrating non-convergence under rekeying.

hypothesis k_i^* produces a model vector $\mathbf{h}(k_i^*)$ that is *linearly correlated* with the actual trace matrix T at the `SubBytes` computation instant. By the central limit theorem, $|\rho(k^*, t^*)|$ grows as $O(\sqrt{N_{\text{total}}})$, while incorrect hypotheses remain at the noise floor. With rekeying, suppose the key changes every N_{block} encryptions. The dataset of N_{total} traces is split into $N_{\text{total}}/N_{\text{block}}$ independent epochs, each with a different key. An attacker targeting a specific epoch has access to only N_{block} traces per key, so the effective SNR is:

$$\text{SNR}_{\text{eff}} \propto \sqrt{N_{\text{block}}} \cdot \frac{\sigma_{\text{signal}}}{\sigma_{\text{noise}}}. \tag{5}$$

If N_{block} is small enough that $\text{SNR}_{\text{eff}} < 1$, the correct hypothesis becomes indistinguishable from noise—which is precisely what our results demonstrate.

B. Statistical Interpretation of Observed Correlations

All peak correlations lie in $[0.165, 0.235]$. Although these exceed the naive 0.1 threshold, this is due to statistical fluctuations: for $N = 500$ traces, the expected maximum of $|\rho|$ over $256 \times 100{,}000$ hypothesis–time pairs is non-trivially above zero. Applying the Fisher z-transform,

$$z = \tfrac{1}{2} \ln\!\left(\tfrac{1+\rho}{1-\rho}\right), \quad \sigma_z = \tfrac{1}{\sqrt{N-3}}, \tag{6}$$

none of the observed correlations is statistically distinguishable from zero at $p < 0.01$ after applying Bonferroni correction for the 2.56×10^7 tests performed. The peaks are therefore consistent with pure noise.

C. Comparison with Static-Key AES

Static-key AES implementations on FPGA without countermeasures typically converge within 200–500 traces, yielding correlations above 0.5 [2], [3]. The rekeying countermeasure reduces the effective per-key trace count below the CPA convergence threshold, raising the attack complexity from *feasible with commodity equipment* to *infeasible within the collected dataset*.

D. Limitations and Future Work

- **Template attacks:** Profiling-based attacks are more powerful than CPA under rekeying and require future evaluation.
- **Larger trace budgets:** If N_{block} is large, collecting more traces may eventually reveal per-epoch leakage.
- **Mutual Information Analysis (MIA):** Model-free MIA may circumvent the Hamming-weight model assumption.
- **Fault injection:** Active attacks were not considered in this purely passive evaluation.

VI. Related Work

Kocher *et al.* [1] introduced Differential Power Analysis (DPA), the precursor to CPA. Brier *et al.* [2] formalised CPA using the Pearson correlation model and the Hamming-weight leakage assumption. Mangard *et al.* [3] provide a comprehensive treatment of power analysis attacks and countermeasures. On RISC-V platforms, side-channel analysis of open-source cores is an active research area [8]. The *Ibex* core [5] has been used in several academic FPGA experiments. Rekeying as a countermeasure was formalised by Lucks [6] in the context of session-key security; its applicability to SCA was studied by Medwed *et al.* [7] under the *fresh re-keying* paradigm. The present work provides a practical, end-to-end experimental validation of rekeying on an open RISC-V FPGA platform, complementing earlier theoretical and simulation-based results.

VII. Conclusion

We presented a systematic electromagnetic side-channel analysis of AES-128 running on the Ibex RV32IMC RISC-V soft-core on a Nexys4DDR FPGA, with a rekeying countermeasure implemented in firmware. A CPA attack using 500 traces (100,000 samples at 625 MSa/s) failed to recover any of the 16 key bytes: 0/16 correct, with peak correlations in $[0.165,\ 0.235]$ and no convergence observed at any trace count. The correlation spectra are statistically consistent with pure noise, confirming that the rekeying protocol disrupts the CPA attack surface. These results establish that the rekeying firmware provides measurable, practical EM-SCA resistance over static-key AES on equivalent hardware. Future work will investigate template attacks, mutual information analysis, and active fault injection to further stress-test the countermeasure.

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APPENDIX A
PER-BYTE CPA RESULTS

Table II lists the complete raw CPA results for all 16 AES-128 key bytes obtained from the 500-trace EM acquisition. Columns report: the recovered (highest-peak) byte hypothesis, the known ground-truth byte, the peak absolute Pearson correlation $|\rho|$, the sample index and corresponding time at which the peak occurs, and the attack outcome. Every row shows **No** because no recovered byte matches the known key, confirming 0 / 16 byte recovery.

APPENDIX B
STATISTICAL SIGNIFICANCE OF CPA CORRELATIONS

To determine whether the observed peak correlations represent genuine leakage or statistical fluctuations, the Fisher z-transform test with Bonferroni correction was applied.

Fisher z-Transform

For a Pearson correlation ρ computed over N samples, the Fisher transform

$$z = \tfrac{1}{2}\ln\!\left(\tfrac{1+\rho}{1-\rho}\right) \tag{7}$$

is approximately normally distributed with mean $\mu_z = \frac{1}{2}\ln\!\left(\frac{1+\rho_0}{1-\rho_0}\right)$ and standard deviation $\sigma_z = 1/\sqrt{N-3}$. Under the null hypothesis $H_0\colon \rho_0 = 0$ (no leakage), the test statistic reduces to z/σ_z. For $N = 500$ traces, $\sigma_z = 1/\sqrt{497} \approx 0.0449$.

Bonferroni Correction

A total of 16 bytes $\times$ 256 hypotheses $\times$ 100,000 samples $=$ $4.096{\times}10^8$ tests are performed simultaneously. The family-wise error rate (FWER) at significance level $\alpha = 0.01$ requires each individual p-value to satisfy

$$p < \frac{0.01}{4.096 \times 10^8} \approx 2.44 \times 10^{-11}, \tag{8}$$

corresponding to a critical z-score of ≈ 6.6 ($|\rho|_{\text{crit}} \approx 0.285$). Table III reports the Fisher z-score and two-tailed p-value for the maximum-correlation byte (byte 11, $|\rho| = 0.2351$) compared with the Bonferroni-corrected threshold.

Since $p = 9.4 \times 10^{-8} \gg 2.44 \times 10^{-11}$, and the observed correlation $0.2351 < 0.285 = |\rho|_{\text{crit}}$, none of the 16 bytes produces statistically significant leakage. All peaks are consistent with the expected maximum of a large random sample from $\mathcal{N}(0, \sigma_z^2)$ and do not warrant rejection of H_0.

APPENDIX C
HARDWARE AND SOFTWARE CONFIGURATION

Table IV summarises the hardware and software configuration used in this evaluation, enabling reproducibility.

APPENDIX D
REPRODUCIBILITY NOTES

Trace Acquisition

Traces were collected using a custom Python acquisition script that synchronises the oscilloscope to a GPIO trigger at the start of each AES encryption and transfers the resulting waveform over USB/UART. All 500 raw traces (each containing 100,000 amplitude samples) and the ensemble mean trace are stored in CSV format for post-processing.

CPA Implementation

The CPA attack was implemented in Python using vectorised NumPy operations. The hypothesis matrix $H \in \mathbb{R}^{500\times256}$ was computed once per key byte and correlated against the full trace matrix in a single vectorised call, reducing per-byte runtime to approximately 30 s on a modern workstation.

Build Requirements

The FPGA bitstream and firmware binary are generated from the repository source. Building requires Vivado 2022.1 or later together with the FuseSoC build system; all dependency versions are pinned in the project configuration.

TABLE II
PER-BYTE CPA RESULTS — 500 TRACES, 100,000 SAMPLES @ 625 MSA/S.

Byte	Recovered	Known	Peak $\lvert\rho\rvert$	Peak Sample	Time (µs)	Correct?
0	0x05	0x2B	0.2022	3349	5.36	**No**
1	0x67	0x7E	0.1998	1457	2.33	**No**
2	0x6D	0x15	0.1649	16802	26.88	**No**
3	0x89	0x16	0.1759	11696	18.71	**No**
4	0x03	0x28	0.1912	2583	4.13	**No**
5	0xE2	0xAE	0.2196	7377	11.80	**No**
6	0x6E	0xD2	0.1776	3538	5.66	**No**
7	0x81	0xA6	0.2133	2061	3.30	**No**
8	0x31	0xAB	0.1859	2373	3.80	**No**
9	0x5F	0xF7	0.1691	8423	13.48	**No**
10	0x72	0x15	0.1882	13682	21.89	**No**
11	0xA7	0x88	0.2351	11687	18.70	**No**
12	0x0B	0x09	0.1833	7624	12.20	**No**
13	0xF7	0xCF	0.1787	9950	15.92	**No**
14	0x04	0x4F	0.1842	4914	7.86	**No**
15	0xB0	0x3C	0.1724	6102	9.76	**No**
		Mean $\lvert\rho\rvert$	0.1882			
		Max $\lvert\rho\rvert$	0.2351	(byte 11)		
		Min $\lvert\rho\rvert$	0.1649	(byte 2)		
		Bytes correct	**0 / 16**			

TABLE III
FISHER z-TEST FOR BYTE 11 (HIGHEST $\lvert\rho\rvert$ = 0.2351, N = 500)

Quantity	Value
$\lvert\rho\rvert$ (byte 11)	0.2351
Fisher z	0.2399
σ_z ($N = 500$)	0.04494
z-score (z/σ_z)	5.338
Two-tailed p-value (raw)	$\approx 9.4 \times 10^{-8}$
Bonferroni-corrected threshold	2.44×10^{-11}
Significant after correction?	**No**
Critical $\lvert\rho\rvert$ (FWER 0.01)	≈ 0.285

TABLE IV
HARDWARE AND SOFTWARE CONFIGURATION

Component	Details
Hardware	
FPGA Board	Digilent Nexys4DDR (Artix-7 XC7A100T)
CPU Core	Ibex RV32IMC (2-stage pipeline, lowRISC)
Clock Frequency	50 MHz (on-board)
Memory	256 KB on-chip SRAM
EM Probe	Near-field H-field probe, loop diameter ≈3 mm
Oscilloscope	1 GSa/s digital storage oscilloscope
Trigger	GPIO pin toggled at `AES_encrypt()` entry
Software / Firmware	
AES Library	Software AES-128 (C reference, lookup-table `SubBytes`)
Rekeying Logic	Fixed rekeying interval (N_{block} encryptions per epoch)
Build System	FuseSoC + Vivado 2022.1
CPA Framework	Python 3 (NumPy, SciPy)
Trace Format	CSV (amplitude vs. sample index)
Key Material (for verification only)	
Known AES Key	`2B7E1516 28AED2A6 ABF71588 09CF4F3C`
Recovered Key	`05676D89 03E26E81 315F72A7 0BF704B0`
Match	0 of 16 bytes correct