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Fabrication and Electrical Characterization of AlGaN/GaN HEMTs with BST Gate Dielectric: A Comparative Study of Two- and Three-Terminal Devices

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Abstract

AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising for high-frequency and high-power electronic applications because of their high electron transport capability and polarization-induced two-dimensional electron gas at the AlGaN/GaN heterointerface. In this work, a systematic fabrication and electrical characterization study of AlGaN/GaN HEMT structures incorporating barium strontium titanate (BST) as a gate dielectric is presented. Initially, two-terminal devices were fabricated using photolithographic patterning and Al/Cr/Au metallization with thicknesses of 150/40/250 nm, followed by rapid thermal annealing at 850°C for 40 s to promote low-resistance ohmic contact formation. The two-terminal current-voltage characteristics were investigated before and after annealing over different voltage ranges. Subsequently, a 200-nm-thick BST layer was deposited over the designated gate region by RF sputtering using a commercial 2-inch BST target at an RF power of 100 W, an Ar flow rate of 60 sccm, and a working pressure of 2.0×10^{-2} mbar. The BST-integrated two-terminal devices exhibited predominantly linear and approximately symmetric current-voltage characteristics over the investigated voltage ranges. Finally, a Ni/Au gate electrode with a thickness of 20/100 nm was fabricated over the BST layer to realize a three-terminal BST-gated AlGaN/GaN HEMT. The final device, having a gate length of 14.03 μm and gate width of 1.343 mm, exhibited clear gate-dependent drain-current modulation. The output characteristics showed a maximum drain current of approximately 5.0×10^{-4} A, while the transfer characteristics exhibited drain-current modulation with applied gate voltage. SEM and EDS analyses further verified the fabricated device morphology and elemental distribution of the BST, AlGaN/GaN, and metal-contact regions. The results demonstrate the feasibility of integrating a sputter-deposited BST layer into AlGaN/GaN HEMT structures and establish a systematic electrical comparison from two-terminal contact structures to a three-terminal BST-gated device.

1. Introduction

AlGaN/GaN heterostructures are among the most important III-nitride platforms for high-frequency and high-power electronic devices because of their wide bandgap, high critical electric field, high electron saturation velocity, and the formation of a high-density two-dimensional electron gas (2DEG) at the AlGaN/GaN heterointerface. The 2DEG originates primarily from the strong spontaneous and piezoelectric polarization discontinuities between AlGaN and GaN, enabling high channel conductivity without conventional intentional doping of the channel [1], [2]. These characteristics have established AlGaN/GaN HEMTs as promising devices for microwave power amplification, high-voltage switching, and harsh-environment electronics [3], [4].

Despite these advantages, the practical performance of AlGaN/GaN HEMTs is strongly influenced by the quality of the source/drain contacts and the gate interface. Formation of low-resistance ohmic contacts is particularly important because contact resistance contributes directly to the total device resistance and can limit current conduction. Thermal annealing of metal stacks is therefore commonly employed to modify the metal/AlGaN interface and promote low-resistance contact formation [5]. At the gate, conventional Schottky-gate HEMTs can suffer from relatively high gate leakage and limited gate-voltage

swing. Furthermore, surface states and interface traps can influence threshold voltage, transconductance, current collapse, and long-term device stability [6], [7].

The introduction of an insulating layer between the gate electrode and AlGaN/GaN surface has therefore attracted significant attention. In metal–insulator–semiconductor HEMTs (MIS-HEMTs), an appropriate dielectric can reduce direct gate leakage and provide additional electrostatic control over the channel. High-k dielectrics are particularly attractive because their relatively high permittivity can increase gate capacitance for a given physical thickness, potentially strengthening gate-channel coupling while maintaining a physically thicker insulating layer [6], [8]. A variety of dielectric materials, including Al_2O_3, HfO_2, SiN□, and other high-k oxides, have consequently been investigated for GaN-based MIS structures [6], [8], [9].

However, the incorporation of a dielectric does not automatically guarantee improved device performance. Dielectric/AlGaN interfaces may contain traps and fixed charges that produce threshold-voltage instability, hysteresis, mobility degradation, or dynamic on-resistance effects. Thus, the dielectric material, deposition process, interface quality, and post-deposition treatment must be considered together when developing insulated-gate GaN devices [6], [8].

Barium strontium titanate, commonly expressed as $Ba□Sr_{1-□}TiO_3$ (BST), is a perovskite oxide that has attracted considerable interest for tunable electronic and microwave applications because of its high dielectric permittivity and field-dependent dielectric properties. The composition-dependent electrical response of BST provides an opportunity to engineer its dielectric behavior for device applications [10], [11]. High-k ferroelectric and incipient-ferroelectric oxides have also been investigated for electrostatic control and tunable components, making BST a potentially interesting material for integration with GaN-based electronic structures [10], [12].

The integration of BST with AlGaN/GaN technology is not entirely unexplored. Xu et al. reported the integration of $Ba□Sr_{1-□}TiO_3$ thin films with AlGaN/GaN HEMT circuits, demonstrating the feasibility of incorporating BST into GaN-based microwave device structures [13]. Subsequent studies have also investigated ferroelectric BST-based structures and tunable capacitive devices for high-frequency applications [11], [14]. These studies established the technological feasibility of BST integration with GaN-based platforms and highlighted the potential of high-permittivity ferroelectric oxides for electrically tunable devices.

Nevertheless, the existing literature has predominantly focused on the integration of BST films with AlGaN/GaN microwave circuits, tunable capacitors, or specialized ferroelectric structures [11], [13], [14]. A systematic experimental comparison of the electrical response of the same AlGaN/GaN device platform before and after thermal treatment, followed by localized BST deposition and subsequent conversion into a three-terminal BST-gated HEMT, is comparatively less addressed. In particular, the relationship between the initial Al/Cr/Au contact characteristics, post-annealing electrical response, BST-deposited two-terminal behavior, and the gate-controlled transfer/output characteristics of the final

Ni/Au/BST/AlGaN/GaN structure has not been sufficiently established in a single experimental sequence.

Accordingly, this work investigates the fabrication and electrical characteristics of AlGaN/GaN HEMT structures incorporating a sputter-deposited BST layer as the gate dielectric. First, two-terminal Al/Cr/Au contacts are fabricated on the AlGaN/GaN wafer using photolithographic patterning, thermal evaporation, and lift-off, followed by rapid thermal annealing to establish the contact condition. The two-terminal I–V characteristics are examined before and after annealing to evaluate the influence of thermal treatment on electrical transport. Subsequently, a 200-nm-thick BST layer is deposited over the designated gate/channel region, and the resulting two-terminal I–V characteristics are investigated. Finally, a Ni/Au gate electrode is fabricated over the BST layer to realize a three-terminal BST-gated AlGaN/GaN HEMT. The resulting transfer and output characteristics are evaluated to assess gate-controlled drain-current modulation.

The fabricated structures are further examined using scanning electron microscopy and energy-dispersive X-ray spectroscopy to verify the device morphology and elemental distribution. Through this sequential approach, the work establishes a direct experimental correlation between metal-contact processing, thermal annealing, BST integration, and the electrical behavior of the resulting AlGaN/GaN HEMT structures.

The primary objective of this study is therefore not merely to demonstrate BST deposition on AlGaN/GaN, but to experimentally correlate the evolution of device electrical behavior from the initially metallized two-terminal structure through annealed contacts and BST integration to the final three-terminal BST-gated HEMT architecture.

2. Experimentation

2.1 Device Fabrication

AlGaN/GaN HEMT wafers were commercially procured and diced into smaller pieces prior to device fabrication. The diced wafer pieces were sequentially cleaned in acetone using ultrasonication for 10 min to remove organic contaminants and processing residues, followed by rinsing in isopropyl alcohol (IPA) to remove residual acetone. The samples were subsequently rinsed with deionized (DI) water and dried using nitrogen gas. A photoresist layer was then deposited by spin coating at 2000 rpm, followed by a soft-baking step to obtain a suitable resist profile for contact patterning. The source and drain contact patterns were defined using photolithography with a photomask. An image-reversal photolithography process was employed to obtain the desired resist profile for subsequent lift-off metallization. The patterned samples were developed to selectively remove the exposed/reversed photoresist regions, thereby defining the contact areas.

An Al/Cr/Au metal stack with thicknesses of 150/40/250 nm, respectively, was subsequently deposited by thermal evaporation. The metal contacts were formed using a lift-off process, resulting in the two-

terminal Al/Cr/Au device structure. The fabricated devices were then subjected to rapid thermal annealing (RTA) at 850°C for 40 s to modify the metal/AlGaN interface and promote the formation of low-resistance ohmic contacts. The annealing treatment facilitates interfacial reactions and alloying within the metal/semiconductor contact region, thereby improving carrier transport between the metal electrode and the conducting channel. Following annealing, the device morphology was examined using scanning electron microscopy (SEM), and the two-terminal current–voltage (I–V) characteristics were measured to evaluate the electrical behavior of the fabricated contacts.

For the BST-integrated two-terminal devices, the annealed Al/Cr/Au-contacted AlGaN/GaN structures were used as the starting devices. A 200-nm-thick barium strontium titanate (BST) layer was deposited selectively over the designated gate/channel region using a sputtering system. A commercially available 2-inch BST target was employed as the sputtering source, with argon (Ar) used as the working gas. Following BST deposition, the devices were subjected to two-terminal I–V measurements to investigate the electrical response of the BST-integrated device structure.

Finally, three-terminal BST-gated AlGaN/GaN HEMTs were fabricated by introducing a gate electrode over the previously deposited BST layer. The gate region was defined using a second photolithography step, followed by deposition of a Ni/Au metal stack with thicknesses of 20/100 nm, respectively. The Ni/Au gate metal was deposited by thermal evaporation and subsequently patterned by lift-off to form the gate electrode over the BST layer. The resulting three-terminal device consisted of Al/Cr/Au source and drain contacts and a Ni/Au gate electrode separated from the AlGaN/GaN surface by the 200-nm-thick BST layer. The fabricated devices were characterized by SEM to verify the device morphology, followed by transfer (I_{DS}–V_{GS}) and output (I_{DS}–V_{DS}) measurements to evaluate the gate-controlled electrical characteristics of the BST-gated AlGaN/GaN HEMT.

The metal contacts and BST dielectric layer were deposited under controlled vacuum conditions. For the deposition of the 200-nm-thick BST layer, a sputtering system equipped with a commercial 2-inch BST target was employed. Prior to deposition, the chamber was evacuated to a base pressure of approximately 2×10^{-6} mbar. During sputtering, Ar gas was introduced at a flow rate of 60 sccm, and the chamber was maintained at a working pressure of 2.0×10^{-2} mbar with an RF power of 100 W. The BST film was deposited selectively over the designated gate region of the AlGaN/GaN HEMT structure.

The Al/Cr/Au source and drain contacts and the Ni/Au gate electrode were deposited by thermal evaporation. During thermal evaporation, the chamber working pressure was maintained at approximately 2.3×10^{-6} mbar. The Al/Cr/Au and Ni/Au metal stacks were deposited with nominal thicknesses of 150/40/250 nm and 20/100 nm, respectively. These controlled deposition conditions were used to obtain well-defined metal contacts and the BST dielectric layer for subsequent electrical characterization of the fabricated devices.

2.2 Device Structure

The fabricated devices were based on an AlGaN/GaN HEMT heterostructure with laterally defined source and drain electrodes. For the two-terminal device configuration, the source-to-drain separation was maintained at 100 μm, with the Al/Cr/Au metallization serving as the two electrical contacts. For the three-terminal configuration, a gate electrode was introduced in the region between the source and drain contacts, resulting in a metal–insulator–semiconductor HEMT (MIS-HEMT)-type architecture in which the BST layer acts as the gate dielectric. The gate length and gate width were 14.03 μm and 1.343 mm, respectively. A 200-nm-thick BST layer was deposited over the designated gate region prior to formation of the Ni/Au gate electrode. Thus, the final three-terminal device consisted of Al/Cr/Au source and drain contacts and a Ni/Au gate electrode separated from the underlying AlGaN/GaN surface by the BST dielectric layer. The resulting device geometry was used for the subsequent transfer and output characteristic measurements. The defined gate dimensions and dielectric thickness provide the geometrical parameters required for evaluating the gate-controlled electrical behavior of the BST-integrated AlGaN/GaN HEMT.

2.3 Device Characterization

The morphology and elemental composition of the fabricated AlGaN/GaN HEMT devices were characterized using a Zeiss EVO 18 Special Edition scanning electron microscope (SEM). SEM imaging was performed to examine the surface morphology, device geometry, fabricated metal contacts, BST-coated gate region, and Ni/Au gate structure. Energy-dispersive X-ray spectroscopy (EDS/EDX) was performed using the SEM-integrated EDX system to identify the constituent elements present in the selected regions of the devices. In addition to point EDX spectra, elemental mapping was performed to investigate the spatial distribution of the relevant elements, including Ba, Sr, Ti, O, Al, Cr, Ga, and Au, in the BST-deposited and metal-contact regions. The EDX spectra and elemental maps were acquired from the corresponding regions examined by SEM to correlate the device morphology with its elemental composition.

The electrical characteristics of the fabricated devices were measured using a Keithley 2634B SourceMeter Unit (SMU). The measurements were performed in DC voltage-sweep mode using a linear voltage sweep and a two-wire sensing configuration. The measurement setup employed 150 source/sweep points, a source-to-measure delay of 5 ms, and a measurement window of 20 ms. The current was measured using the automatic current-range setting with a minimum current range of 1×10^{-10} A, while the auto-zero function was enabled. The voltage sweep was applied according to the measurement range specified for each device structure. Two-terminal I-V measurements were performed over the selected bipolar and unipolar voltage ranges for the as-fabricated, annealed, and BST-integrated devices. For the final three-terminal BST-gated AlGaN/GaN HEMT, transfer characteristics (I_{DS}-V_{GS}) and output characteristics (I_{DS}-V_{DS}) were measured by controlling the gate-source and drain-source voltages, respectively. The electrical measurements were used to evaluate the current transport behavior of the fabricated devices and to investigate the effect of thermal annealing and BST integration on the gate-controlled electrical characteristics of the AlGaN/GaN HEMT.

Figure 1 illustrates the sequential fabrication process and corresponding device architectures of the AlGaN/GaN HEMT structures investigated in this work. Initially, the AlGaN/GaN HEMT wafer was subjected to a standard cleaning procedure to remove surface contaminants. Photolithography was then employed to define the contact pattern, followed by deposition of an Al/Cr/Au metal stack with thicknesses of 150/40/250 nm, respectively, using thermal evaporation. A lift-off process was subsequently performed to realize the two-terminal metal contacts. The fabricated devices were cleaned with deionized (DI) water and dried using nitrogen gas prior to rapid thermal annealing (RTA) at 850°C for 40 s. The annealing treatment was employed to improve the metal–semiconductor contact properties and facilitate the formation of ohmic contacts. The resulting two-terminal devices were electrically characterized by current–voltage (I–V) measurements [15]–[17].

To investigate the effect of the BST layer, a second device configuration was fabricated using the two-terminal Al/Cr/Au device as the starting structure. A 200-nm-thick BST (barium strontium titanate) layer was deposited selectively over the central gate/channel region by sputtering. In this configuration, the BST layer was evaluated without introducing a separate gate electrode, and the corresponding two-terminal I–V characteristics were measured to examine its electrical behavior.

For the three-terminal HEMT structure, the BST layer was subsequently integrated as the gate dielectric. Following BST deposition, a second photolithography step was used to define the gate electrode region, and a Ni/Au metal stack with thicknesses of 20/100 nm, respectively, was deposited by thermal evaporation. A subsequent lift-off process produced the Ni/Au gate contact over the BST layer, resulting in the final three-terminal AlGaN/GaN HEMT structure with Al/Cr/Au source and drain contacts and a Ni/Au gate electrode. This device architecture enabled the investigation of the gate-controlled electrical characteristics, including the transfer and output characteristics of the BST-gated AlGaN/GaN HEMT [22]–[24].

3. Result and Discussion

Figure 2 presents the SEM characterization of the fabricated AlGaN/GaN HEMT devices and confirms the formation of the designed device geometries. As shown in Fig. 2**(a)**, the two-terminal device consists of two patterned Al/Cr/Au metal contacts formed on the AlGaN/GaN heterostructure, with the region between the contacts defining the active channel for two-terminal electrical characterization. The magnified SEM image in Fig. 2**(b)** provides a closer view of the channel region and the separation between the metal contacts, indicating a well-defined device geometry. Figure 2**(c)** shows the complete three-terminal AlGaN/GaN HEMT structure, where the Al/Cr/Au source and drain contacts are laterally separated and a centrally located Ni/Au gate electrode is introduced over the gate region following BST deposition. The higher-magnification image in Fig. 2**(d)** provides a detailed view of the gate region and the gate–channel configuration. The SEM images therefore verify the successful realization of both the two-terminal and three-terminal device architectures used for subsequent electrical characterization [15], [16].

Figure 3 presents the EDS elemental mapping of the BST-deposited region of the two-terminal AlGaN/GaN HEMT device. The elemental maps show the spatial distribution of Ba, Sr, Ti, and O, which are the principal constituent elements of the deposited BST layer. The presence and distribution of these elements across the selected region provide evidence for the incorporation of the BST layer over the intended device area. In addition, the EDS maps of Al and Ga correspond to the underlying AlGaN/GaN heterostructure, while the detected Cr and Au signals are associated with the underlying Al/Cr/Au metallization. The spatially resolved distribution of the constituent elements indicates that the BST deposition was successfully realized over the targeted gate/channel region while retaining the characteristic elemental signatures of the underlying AlGaN/GaN device and metal contacts. These EDS results, together with the SEM observations, support the successful integration of the BST layer with the AlGaN/GaN HEMT structure [18], [19].

Figure 4 presents the SEM images and corresponding EDX spectra obtained from two different regions of the fabricated three-terminal AlGaN/GaN HEMT. Figure 4**(a)** shows the SEM image of the complete device region containing the Al/Cr/Au source and drain contacts, the BST-coated gate region, and the Ni/Au gate electrode. The corresponding EDX spectrum in Fig. 4**(b)** exhibits characteristic signals from Ga and Al originating from the underlying AlGaN/GaN heterostructure, together with Cr and Au associated with the metallization. Additional signals corresponding to O, Sr, and Ti are also observed, which are consistent with the presence of the BST layer in the analyzed region. The spectrum therefore provides qualitative evidence for the coexistence of the semiconductor, metal-contact, and BST-related elemental signatures within the selected device area **(**Table 1**).**

In contrast, Fig. 4**(c)** represents the upper device region where the Al/Cr/Au metallization is directly patterned on the AlGaN/GaN surface without the BST-coated gate region. The corresponding EDX spectrum in Fig. 4**(d)** is dominated by the characteristic Ga and Al signals of the AlGaN/GaN heterostructure, along with Cr and Au peaks associated with the metal contacts. Importantly, the BST-related elemental signatures observed in Fig. 4**(b)**, particularly Sr and Ti, are not evident in the spectrum obtained from the region shown in Fig. 4**(c).** This difference between the two spectra provides qualitative evidence that the BST deposition is localized to the intended gate region rather than being uniformly present over the upper device surface [18], [19].

Table 1
Characteristic EDS X-ray peak energies and corresponding elemental assignments observed in the BST-coated and Al/Cr/Au-metallized regions of the AlGaN/GaN HEMT device.

Element	Approx. characteristic energy	Interpretation
O	~ 0.52 keV	BST-related oxygen
Al	~ 1.49 keV	AlGaN barrier
Sr	~ 1.8–2.0 keV region	BST
Au	~ 2.1 keV and higher-energy Au lines	Au metallization
Ti	~ 4.5 keV	BST-related Ti*
Cr	~ 5.4 keV	Cr metallization
Ga	~ 9.25 and ~ 10.26 keV	GaN/AlGaN
Au	~ 9.7, ~ 11.4, ~ 13.4 keV	Au metallization

Figure 5 presents the EDS elemental mapping of the upper region of the fabricated three-terminal AlGaN/GaN HEMT, where the Al/Cr/Au metallization is patterned on the AlGaN/GaN heterostructure. The elemental maps clearly reveal the spatial distribution of Al, Cr, Ga, and Au within the analyzed region. The Ga map represents the underlying GaN layer, while the Al distribution is associated primarily with the AlGaN barrier layer. The Cr and Au maps correspond to the respective layers of the Al/Cr/Au metallization used for the source and drain contacts. The localized distribution of Cr and Au along the patterned contact regions, together with the presence of Al and Ga across the semiconductor region, is consistent with the designed device architecture. The EDS mapping therefore provides spatially resolved qualitative evidence for the presence and distribution of the constituent elements of both the AlGaN/GaN heterostructure and the Al/Cr/Au metal contacts [18], [19].

Figure 6 shows the two-terminal current–voltage characteristics of the AlGaN/GaN HEMT structures measured before post-deposition rapid thermal annealing (RTA). The measurements were performed over progressively wider voltage ranges to evaluate the pre-annealing electrical response of the Al/Cr/Au metal–semiconductor contacts and the underlying AlGaN/GaN heterostructure. As shown in Fig. 6**(a)**, for a voltage sweep from − 1 to + 1 V, the device exhibits a nonlinear and asymmetric current response, with the current increasing from approximately $-(5–8) \times 10^{-9}$ A at negative bias to ~ 2×10^{-8} A at + 1 V. Small fluctuations in the current near the central voltage region are also observed, which may be associated with measurement instability, localized trapping, or the initial non-ideal contact behavior [16], [17], [20].

With increasing voltage range, the nonlinear character of the I–V response becomes more pronounced. In Fig. 6**(b)**, the current remains close to zero over an intermediate voltage range and then increases rapidly above approximately 3–4 V, reaching ~ 2×10^{-4} A at + 6 V. Figure 6**(c)** shows a similar strong nonlinear response, with the current increasing sharply around 3–5 V and reaching a maximum of

approximately (1.6–1.8) × 10^{-4} A near 5 V. Beyond this point, the current gradually decreases with increasing voltage, reaching approximately 1.1 × 10^{-4} A at + 15 V. This post-peak reduction in current may indicate the influence of device self-heating, charge trapping, or field-dependent transport effects; however, further temperature-dependent or pulsed measurements would be required to identify the dominant mechanism conclusively [16].

The positive-bias characteristics in Figs. 6**(d)–(f)** further demonstrate the strongly nonlinear transport behavior of the as-fabricated contacts. In Fig. 6**(d)**, the current remains very low at low voltage and increases rapidly above approximately 3 V, reaching ~ 1.5–1.6 × 10^{-5} A near 4.7–5 V. Figures 6**(e) and 6(f)** exhibit a similar turn-on/knee-like behavior at approximately 4–5 V, followed by a maximum current of ~ 1.3 × 10^{-4} A near 5 V. The current subsequently decreases gradually with increasing applied voltage, reaching approximately (8–9) × 10^{-5} A at 12 V in Fig. 6**(e)** and ~ 8 × 10^{-5} A at 16 V in Fig. 6**(f)** [17], [20], [21]. Summary of result is present in Table 2.

Table 2
Summary of Quantitative summary

Panel	Voltage range	Approx. maximum current	Important observation
(A)	−1 to + 1 V	~ 2 × 10^{-8} A	Low-current, nonlinear response
(B)	−6 to + 6 V	~ 2 × 10^{-4} A	Sharp current increase above ~ 3–4 V
(C)	−20 to + 20 V	~ 1.7 × 10^{-4} A	Peak near ~ 5 V followed by current decrease
(D)	0 to + 5 V	~ 1.6 × 10^{-5} A	Strong nonlinear increase above ~ 3 V
(E)	0 to + 10 V	~ 1.3 × 10^{-4} A	Peak near ~ 5 V followed by gradual decrease
(F)	0 to + 16 V	~ 1.3 × 10^{-4} A	Similar peak near ~ 5 V and subsequent decrease

Figure 7 presents the two-terminal I–V characteristics of the AlGaN/GaN HEMT device after thermal annealing of the Al/Cr/Au contacts. Compared with the pre-annealing characteristics shown in Fig. 6, the post-annealing device exhibits a substantially modified electrical response, indicating the influence of the thermal treatment on the metal–semiconductor interface and carrier transport. For the low-voltage sweep in Fig. 7**(a)**, the current initially increases rapidly with applied voltage and then approaches a nearly saturated value of approximately 1.5–1.6 × 10^{-11} A over the positive-voltage region. The response is considerably more stable at higher positive bias than that observed before annealing [16].

For the wider bipolar sweep shown in Fig. 7**(b)**, the current increases from the low-current regime and reaches approximately 8.5–8.8 × 10^{-11} A, after which the current remains nearly constant over the higher positive-voltage region. Figure 7**(c)**, measured over − 20 to + 20 V, exhibits a similar trend, with the current increasing to approximately 3.4–3.5 × 10^{-10} A and subsequently approaching a quasi-saturated regime. The reproducibility of the nearly saturated current at higher positive bias suggests a stabilized post-annealing electrical response [17].

The positive-bias characteristics in Figs. 7**(d)** and **7(e)** show a substantially higher current level. In Fig. 7**(d)**, the current remains very small below approximately 2–3 V and then increases rapidly, reaching approximately 6.0×10^{-5} A at 5 V. Figure 7**(e)** shows a similar sharp increase beginning at approximately 3–4 V, with the current reaching a maximum of approximately $7.8–8.0 \times 10^{-4}$ A near 5 V. Beyond the peak, the current gradually decreases with increasing voltage and reaches approximately $6.5–6.8 \times 10^{-4}$ A at 10 V. The post-peak decrease may be associated with field-dependent transport, trapping, or self-heating effects; however, identification of the dominant mechanism would require additional temperature-dependent or pulsed I–V measurements [20], [21]. Summary of results present in Table 3.

Table 3
Summary of Quantitative summary

Panel	Voltage range	Approx. current response	Main observation
(A)	−1 to + 1 V	~ $1.5–1.6 \times 10^{-11}$ A	Rapid initial increase followed by quasi-saturation
(B)	−6 to + 6 V	~ $8.5–8.8 \times 10^{-11}$ A	Current reaches a stable quasi-saturated region
(C)	−20 to + 20 V	~ $3.4–3.5 \times 10^{-10}$ A	Similar saturation-like behavior at high bias
(D)	0 to + 5 V	~ 6.0×10^{-5} A	Sharp current increase above ~ 2–3 V
(E)	0 to + 10 V	~ $7.8–8.0 \times 10^{-4}$ A	Peak near ~ 5 V followed by gradual current decrease

Figure 8 presents the two-terminal current–voltage (I–V) characteristics of the AlGaN/GaN HEMT structure after deposition of a 200-nm-thick BST layer over the designated gate/channel region. The measurements were performed over different voltage ranges to investigate the electrical response of the BST-integrated two-terminal structure. In contrast to the nonlinear characteristics observed for the as-deposited Al/Cr/Au-contacted device before annealing, the BST-deposited structure exhibits an approximately linear and symmetric I–V response over the investigated voltage ranges. The nearly linear dependence of current on applied voltage indicates an approximately constant effective conductance within the measured bias range, with no pronounced threshold-like or rectifying behavior [22].

At low bipolar bias, Fig. 8**(a)** shows an approximately linear response from − 1 to + 1 V, with the current varying from approximately − 4.3×10^{-5} to + 4.3×10^{-5} A. A similar linear behavior is observed in Fig. 8(b), where the current reaches approximately ±$(8–9) \times 10^{-5}$ A over the − 2 to + 2 V range. In Fig. 8**(c)**, the current increases almost linearly from approximately − 2.6×10^{-4} A at − 6 V to + 2.6×10^{-4} A at + 6 V. These results indicate a relatively symmetric current response with respect to voltage polarity [23].

The wider bipolar sweep in Fig. 8**(d)**, extending from − 15 to + 15 V, also exhibits a linear I–V dependence; however, the current magnitude is comparatively lower, reaching approximately −$(5.5–6.0) \times 10^{-5}$ A and +$(6.0–6.5) \times 10^{-5}$ A at the corresponding voltage limits. The reduced slope in this

measurement compared with the other panels suggests a lower effective conductance under this particular measurement condition. This difference may arise from device-to-device variation, measurement history, or voltage-dependent effects and should not be attributed solely to the BST layer without further controlled measurements [24].

For the unipolar measurements, Fig. 8**(e)** shows a nearly linear increase in current from approximately 0 A at 0 V to ~ 2.2–2.3 × 10^{-4} A at 5 V, whereas Fig. 8**(f)** shows an increase to approximately 4.3–4.5 × 10^{-4} A at 10 V. The absence of an obvious current saturation or sharp nonlinear transition in these measurements further indicates approximately ohmic-like two-terminal transport in the investigated bias range [25], [26]. Summary of results present in Table 4.

Table 4
Summary of Quantitative interpretation

Panel	Voltage range	Approx. current range	Approx. slope, (G = dI/dV)	Approx. (R = 1/G)
A	−1 to + 1 V	−4.3 to + 4.3 ×10^{-5} A	~ 4.3 × 10^{-5} S	~ 23 kΩ
B	−2 to + 2 V	−8 to + 8.5 ×10^{-5} A	~ 4.1 × 10^{-5} S	~ 24 kΩ
C	−6 to + 6 V	−2.6 to + 2.6 ×10^{-4} A	~ 4.3 × 10^{-5} S	~ 23 kΩ
D	−15 to + 15 V	−(5.5–6.0) to +(6.0–6.5) ×10^{-5} A	~ 4.0 × 10^{-6} S	~ 250 kΩ
E	0 to + 5 V	0 to ~ 2.3 ×10^{-4} A	~ 4.6 × 10^{-5} S	~ 22 kΩ
F	0 to + 10 V	0 to ~ 4.4 ×10^{-4} A	~ 4.4 × 10^{-5} S	~ 23 kΩ

Figure 9 presents the electrical characteristics of the fabricated three-terminal BST-gated AlGaN/GaN HEMT. The transfer characteristics (I_{DS}–V_{GS}) shown in Fig. 9**(a)** were measured at different drain voltages (V_D = 0, 1, 2, and 4 V), while the output characteristics (I_{DS}–V_{DS}) in Fig. 9**(b)** were obtained at different gate-source voltages (V_{GS} = − 2, − 1, 0, + 1, and + 2 V). These measurements demonstrate the gate-voltage-dependent modulation of the drain current and confirm the three-terminal operation of the fabricated BST-gated HEMT [22].

In Fig. 9**(a)**, the transfer characteristics exhibit a strong dependence of the drain current on the applied gate voltage. At negative gate voltages, the drain current reaches a magnitude of approximately 1.4–1.9 × 10^{-4} A, whereas the current approaches nearly zero as the gate voltage is increased toward approximately − 2 to − 1 V. The transition from the high-current to the low-current state occurs mainly in the V_{GS} range of approximately − 4 to − 2 V. The transfer curves also show a systematic dependence on the drain voltage, indicating that the channel current is influenced by both gate and drain bias. The maximum drain-current magnitude observed in the investigated transfer characteristics is approximately 1.9 × 10^{-4} A [23].

The output characteristics in Fig. 9**(b)** further demonstrate the modulation of the drain current by the gate-source voltage. At low drain voltages, the drain current initially increases rapidly with increasing V_{DS}. With further increase in V_{DS}, the current gradually approaches a saturation-like regime. For V_{GS} = + 2 V, the drain current reaches a maximum value of approximately 5.0×10^{-4} A at $V_{DS} \approx 5–6$ V and subsequently decreases gradually to approximately $4.2–4.3 \times 10^{-4}$ A at V_{DS} = 20 V. When V_{GS} is reduced from + 2 to − 2 V, the drain current decreases systematically. At V_{DS} = 20 V, the drain current is approximately $3.8–3.9 \times 10^{-4}$ A for V_{GS} = + 1 V, $3.7–3.8 \times 10^{-4}$ A for V_{GS} = 0 V, $3.5–3.6 \times 10^{-4}$ A for V_{GS} = − 1 V, and $3.4–3.5 \times 10^{-4}$ A for V_{GS} = − 2 V [24].

Quantitatively, changing the gate-source voltage from − 2 to + 2 V results in an increase in the high-drain-voltage current from approximately 3.4×10^{-4} A to 4.2×10^{-4} A, corresponding to an increase of approximately 0.8×10^{-4} A, or about 24%. This systematic change in drain current with gate bias demonstrates effective electrostatic modulation of the conducting channel by the gate electrode through the BST-containing gate structure. The output curves also exhibit a clear high-field current reduction after the maximum current near $V_{DS} \approx 5–6$ V. This behavior may be associated with self-heating, charge trapping, or other high-field transport effects; however, additional temperature-dependent or pulsed measurements would be required to identify the dominant mechanism conclusively **[27].**

Overall, the transfer and output characteristics demonstrate that the fabricated three-terminal BST-gated AlGaN/GaN HEMT exhibits clear gate-controlled drain-current modulation. The observation of a maximum drain current of approximately 5.0×10^{-4} A and systematic current variation with V_{GS} confirms the electrical functionality of the fabricated gated structure. The results also indicate that the incorporation of BST in the gate region enables effective gate-field coupling to the AlGaN/GaN channel, providing the basis for further investigation of BST as a gate dielectric in AlGaN/GaN HEMT devices [27–29].

4. Conclusion

This work demonstrated the fabrication and electrical characterization of AlGaN/GaN HEMT structures with a BST-based gate dielectric using a systematic two-terminal-to-three-terminal device fabrication approach. Al/Cr/Au source and drain contacts with thicknesses of 150/40/250 nm were initially fabricated by photolithography, thermal evaporation, and lift-off. The electrical characteristics measured before annealing showed a pronounced nonlinear response, indicating non-ideal transport through the as-deposited metal/AlGaN/GaN contact structure. Following rapid thermal annealing at 850°C for 40 s, a substantial modification of the two-terminal electrical response was observed, demonstrating the influence of thermal treatment on the metal/semiconductor contact interface.

A 200-nm-thick BST layer was subsequently deposited over the designated gate region using RF sputtering. The BST-integrated two-terminal devices exhibited predominantly linear and approximately symmetric I-V characteristics over most of the investigated voltage ranges. This behavior indicates

stable two-terminal electrical transport after BST integration. SEM and EDS characterization further supported the successful fabrication of the device structures and the presence and spatial distribution of the constituent elements associated with BST, the AlGaN/GaN heterostructure, and the Al/Cr/Au metallization.

For the final three-terminal device, a Ni/Au gate electrode with a thickness of 20/200 nm was fabricated over the BST layer, forming a BST-gated AlGaN/GaN HEMT. The device exhibited clear gate-dependent drain-current modulation in the transfer characteristics and a pronounced drain-current response in the output characteristics. A maximum drain current of approximately 5.0×10^{-4} A was obtained at a positive gate bias, while systematic variation of the drain current with V_GS confirmed the electrical functionality of the gate-controlled structure. The fabricated device therefore demonstrates the feasibility of using a sputter-deposited BST layer as the gate dielectric in an AlGaN/GaN HEMT architecture.

Overall, the comparative investigation establishes a clear experimental sequence from the initial Al/Cr/Au two-terminal contact structure, through thermal annealing and BST integration, to the final Ni/Au/BST/AlGaN/GaN three-terminal HEMT. The results provide a basis for further optimization of BST thickness, interface quality, deposition conditions, and gate geometry to improve the electrical performance and reliability of BST-gated AlGaN/GaN HEMTs.

Declarations

Conflict of Interest:

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

AI Declaration Statement

Artificial intelligence tools were used only for language improvement and editing purposes in this manuscript.

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Figures

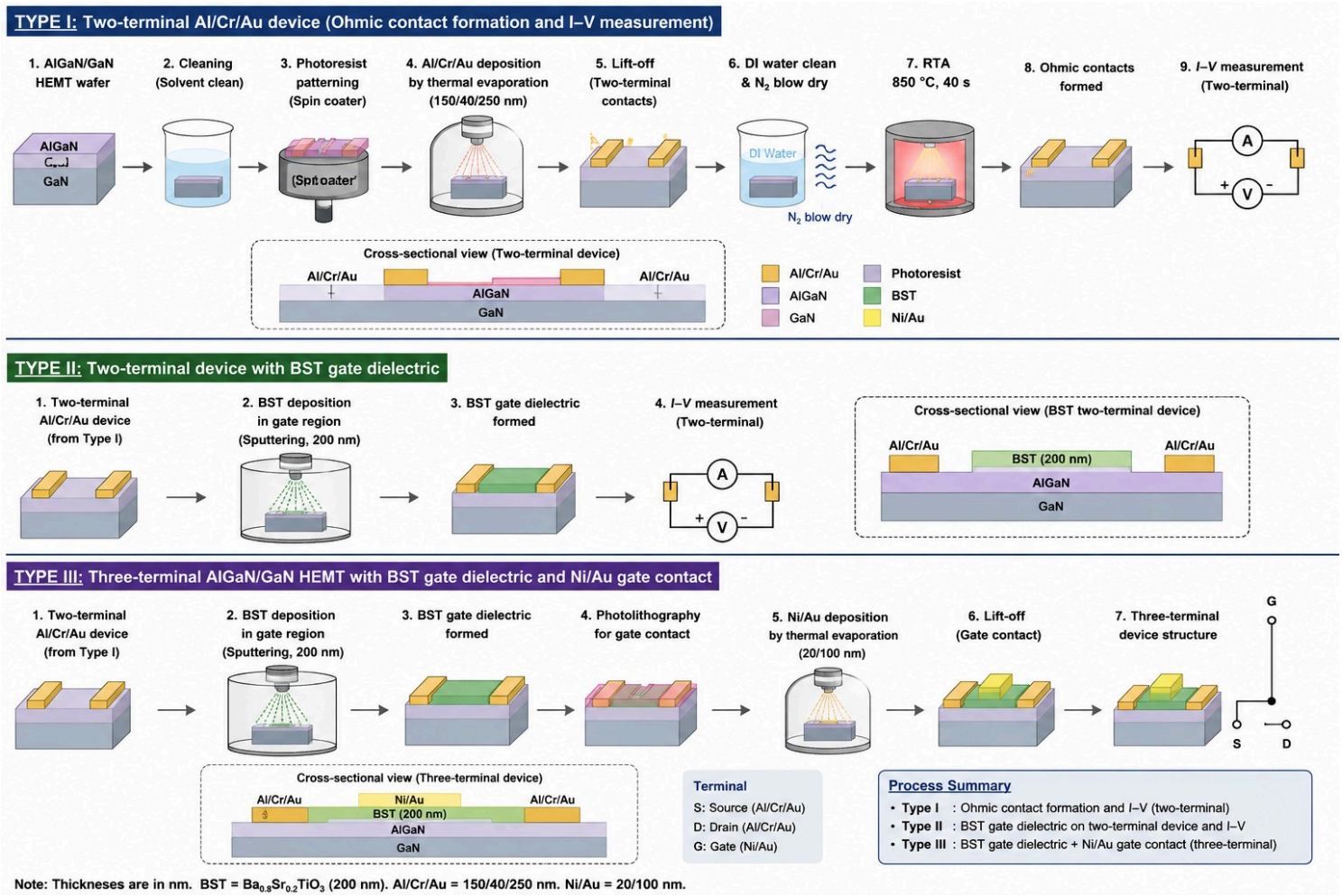


Figure 1

Schematic illustration of the fabrication process flow and device structures of the AlGaN/GaN HEMT devices. The process involves wafer cleaning, photolithographic patterning, Al/Cr/Au (150/40/250 nm) metallization by thermal evaporation and lift-off to form two-terminal contacts, followed by DI-water cleaning, N_2 drying, and rapid thermal annealing (RTA) at 850 °C for 40 s to form ohmic contacts. For the BST-based devices, a 200-nm-thick BST layer is deposited in the gate region by sputtering, followed by two-terminal I–V characterization. For the three-terminal device, a Ni/Au (20/100 nm) gate contact is

subsequently defined and deposited over the BST layer to realize the final gated AlGaN/GaN HEMT structure.

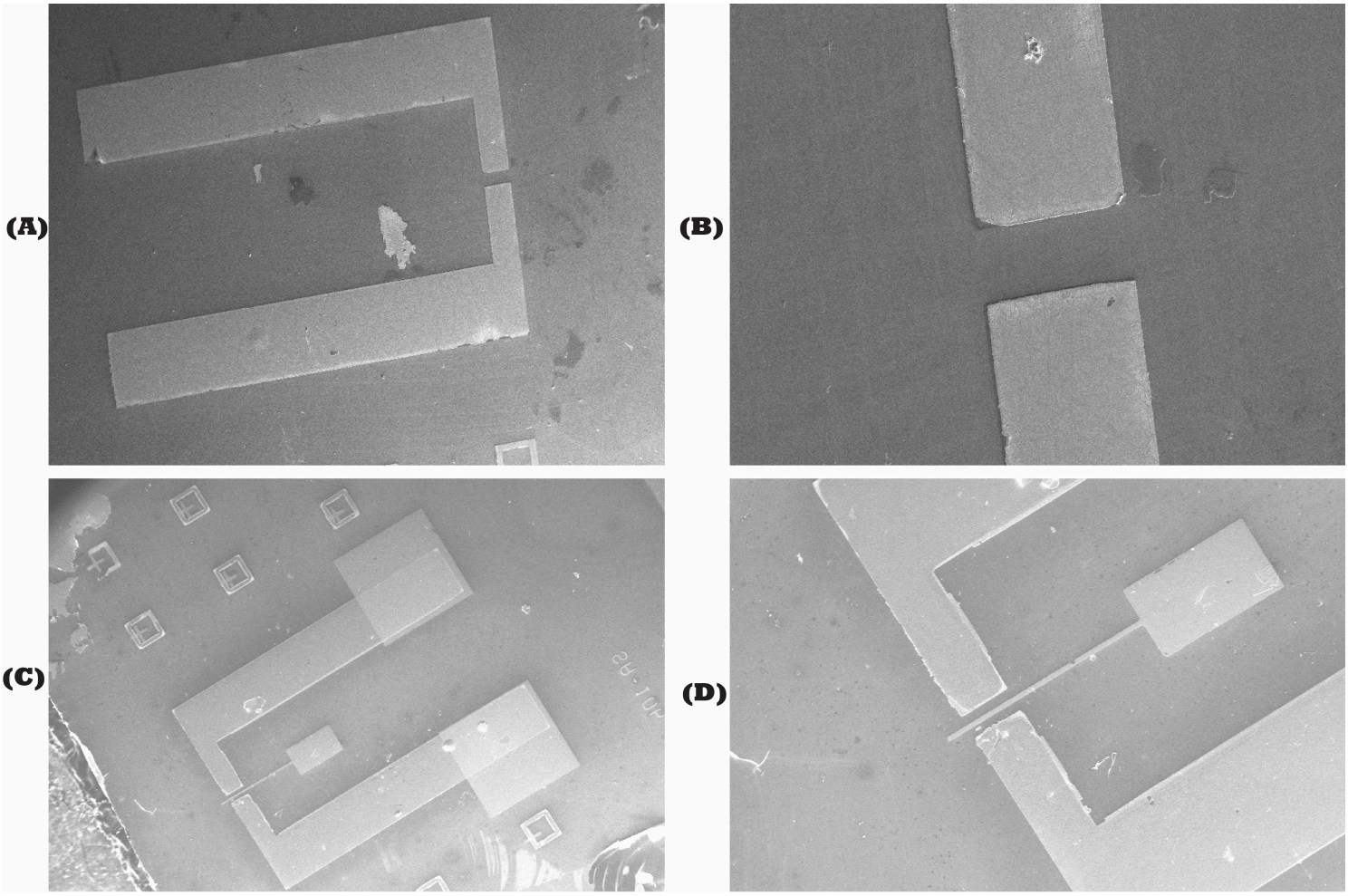


Figure 2

SEM images of the fabricated AlGaN/GaN HEMT devices: **(A)** two-terminal device structure with Al/Cr/Au metal contacts defined by photolithography and deposited by thermal evaporation; **(B)** magnified view of the active channel region; **(C)** complete three-terminal HEMT structure comprising Al/Cr/Au source and drain contacts and a Ni/Au gate contact defined by a second photolithography and metallization step; and **(D)** higher-magnification SEM image of the gate region shown in **(B).**

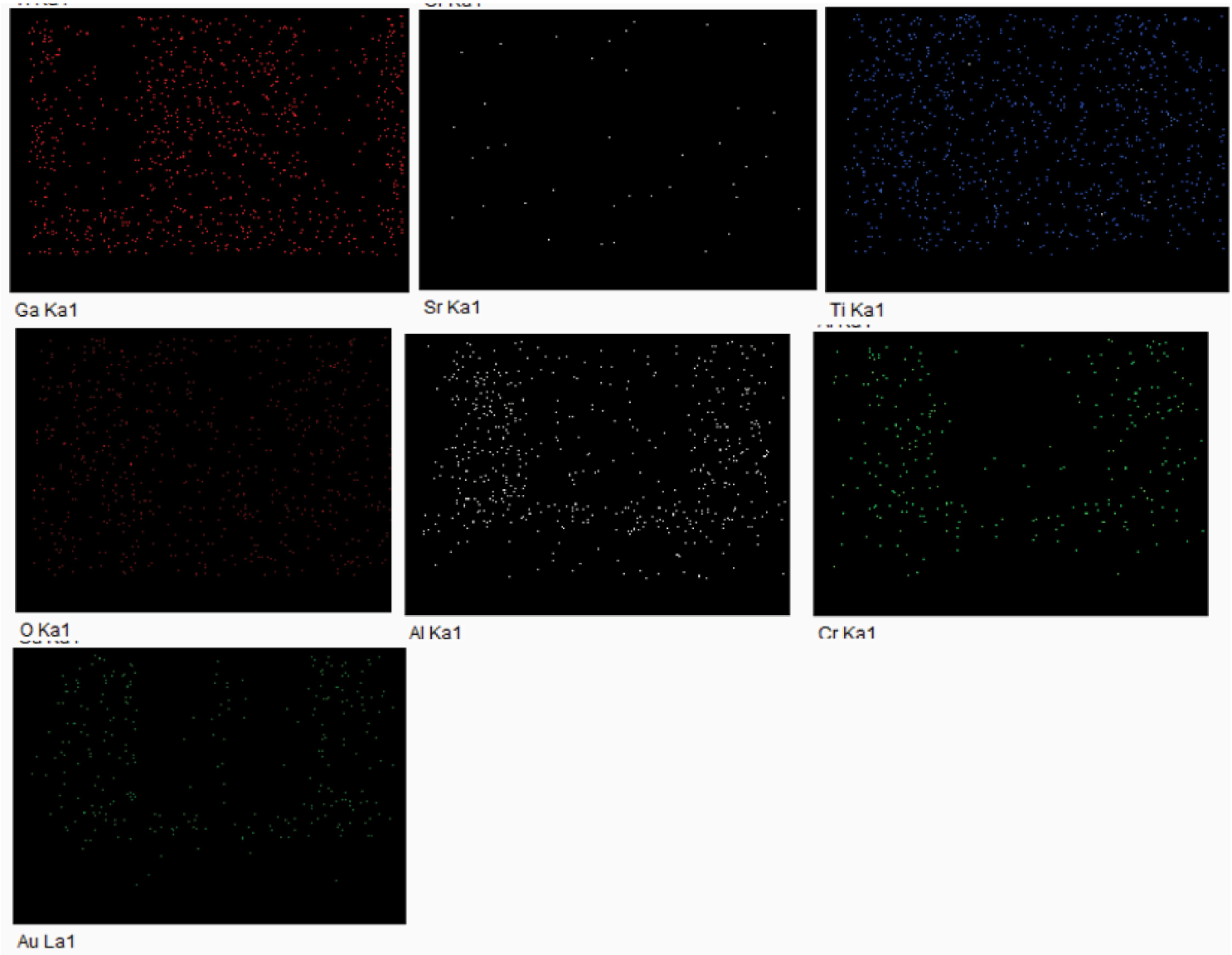


Figure 3

EDS elemental mapping of the BST-deposited gate region of the AlGaN/GaN HEMT two-terminal device, showing the spatial distribution of **Ba, Sr, Ti, O, Al, Cr, and Au** elements within the selected gate region, confirming the elemental composition of the deposited BST layer and underlying device structure.

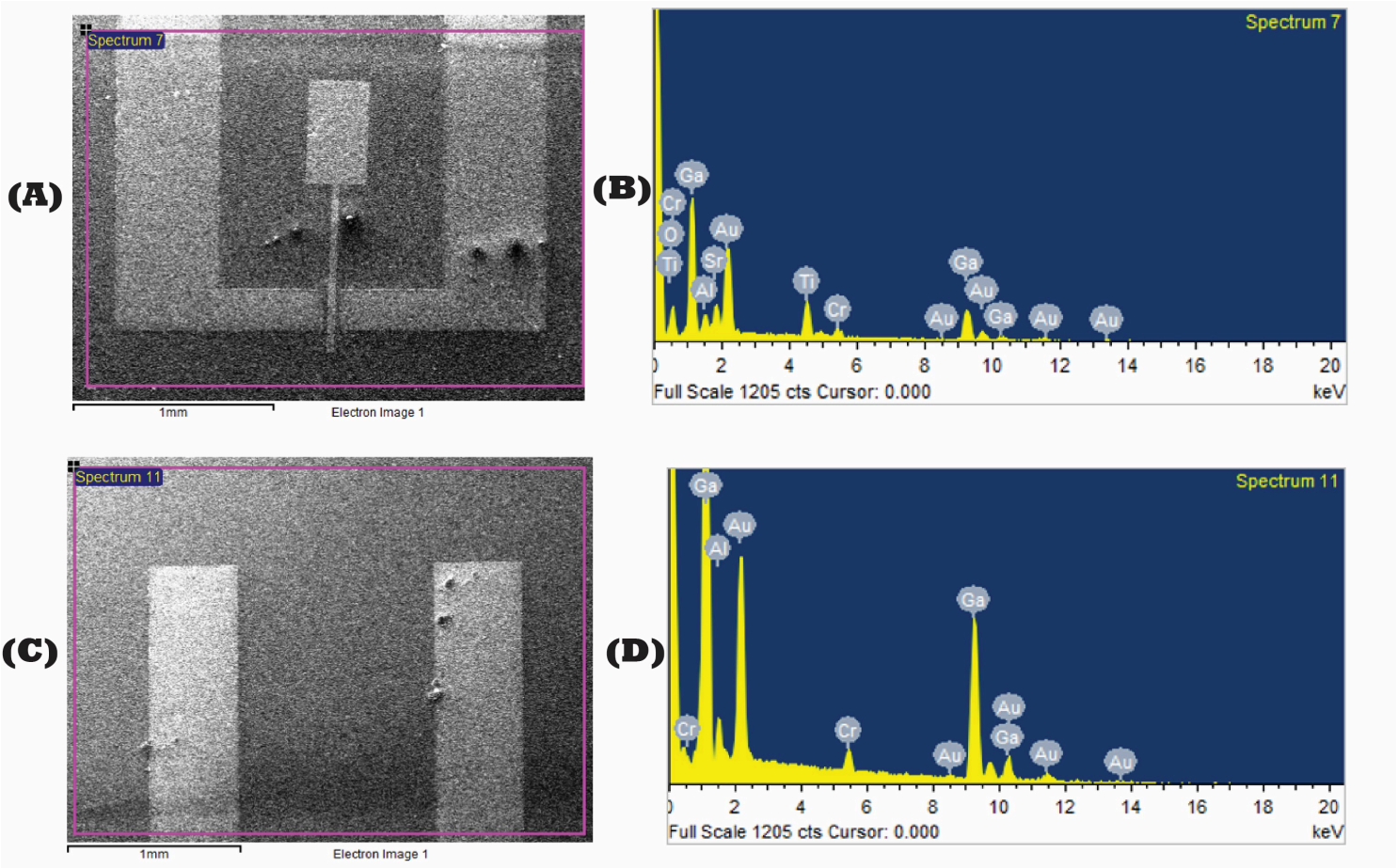


Figure 4

SEM images and corresponding EDX spectra of the fabricated three-terminal AlGaN/GaN HEMT device: **(A)** SEM image of the device showing Al/Cr/Au source and drain contacts, BST deposited in the gate region, and the subsequently fabricated Ni/Au gate contact; **(B)** corresponding EDX spectrum of the region shown in (A), revealing the elemental composition associated with the BST-coated gate region and device structure; **(C)** SEM image of the upper device region showing the Al/Cr/Au metallization on the AlGaN/GaN surface; and **(D)** corresponding EDX spectrum of the region shown in (C), confirming the presence of the constituent elements of the metal contacts and underlying AlGaN/GaN structure.

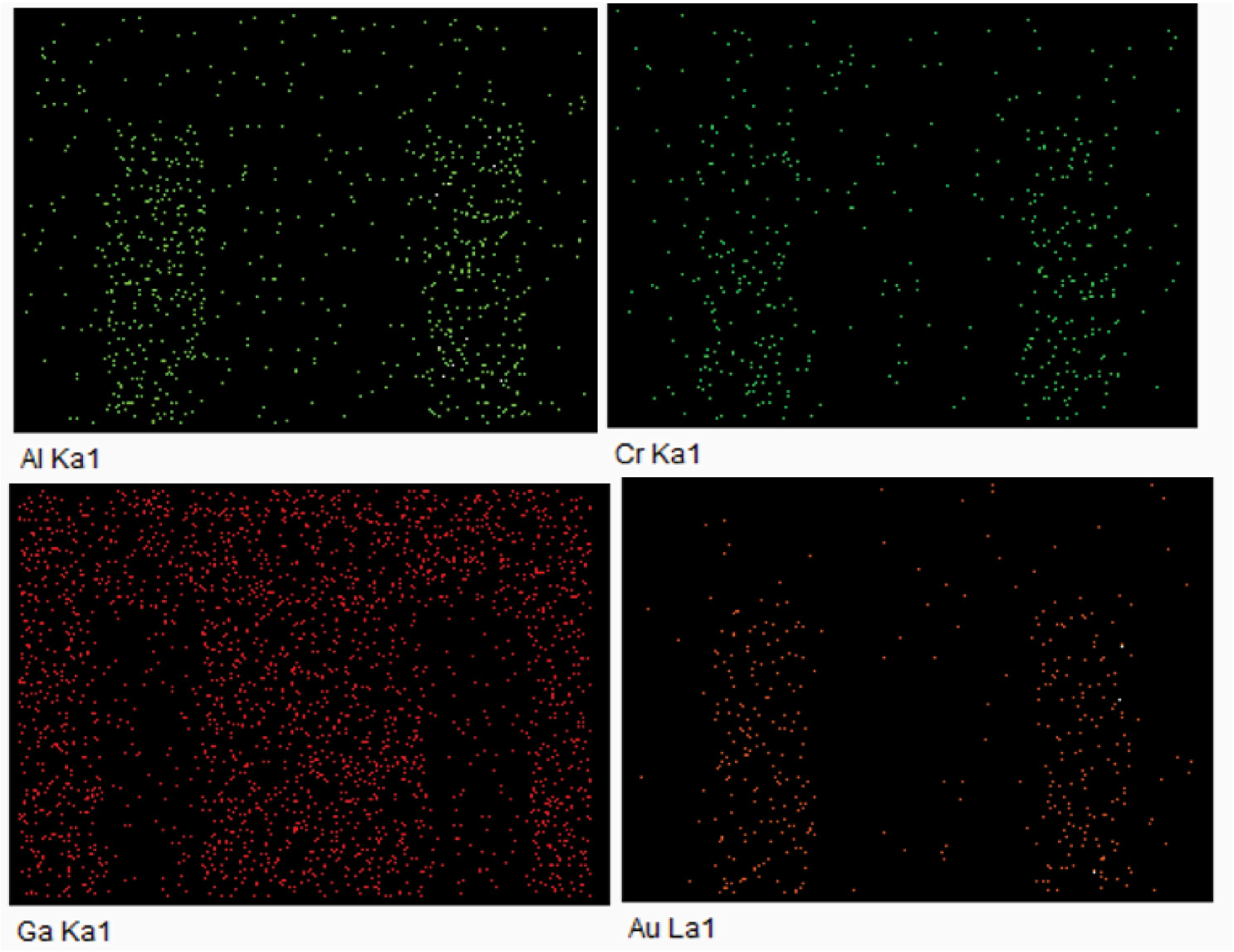


Figure 5

EDS elemental mapping of the upper region of the three-terminal AlGaN/GaN HEMT device, showing the spatial distribution of **Al, Cr, Ga, and Au** associated with the AlGaN/GaN heterostructure and the patterned Al/Cr/Au metal contacts.

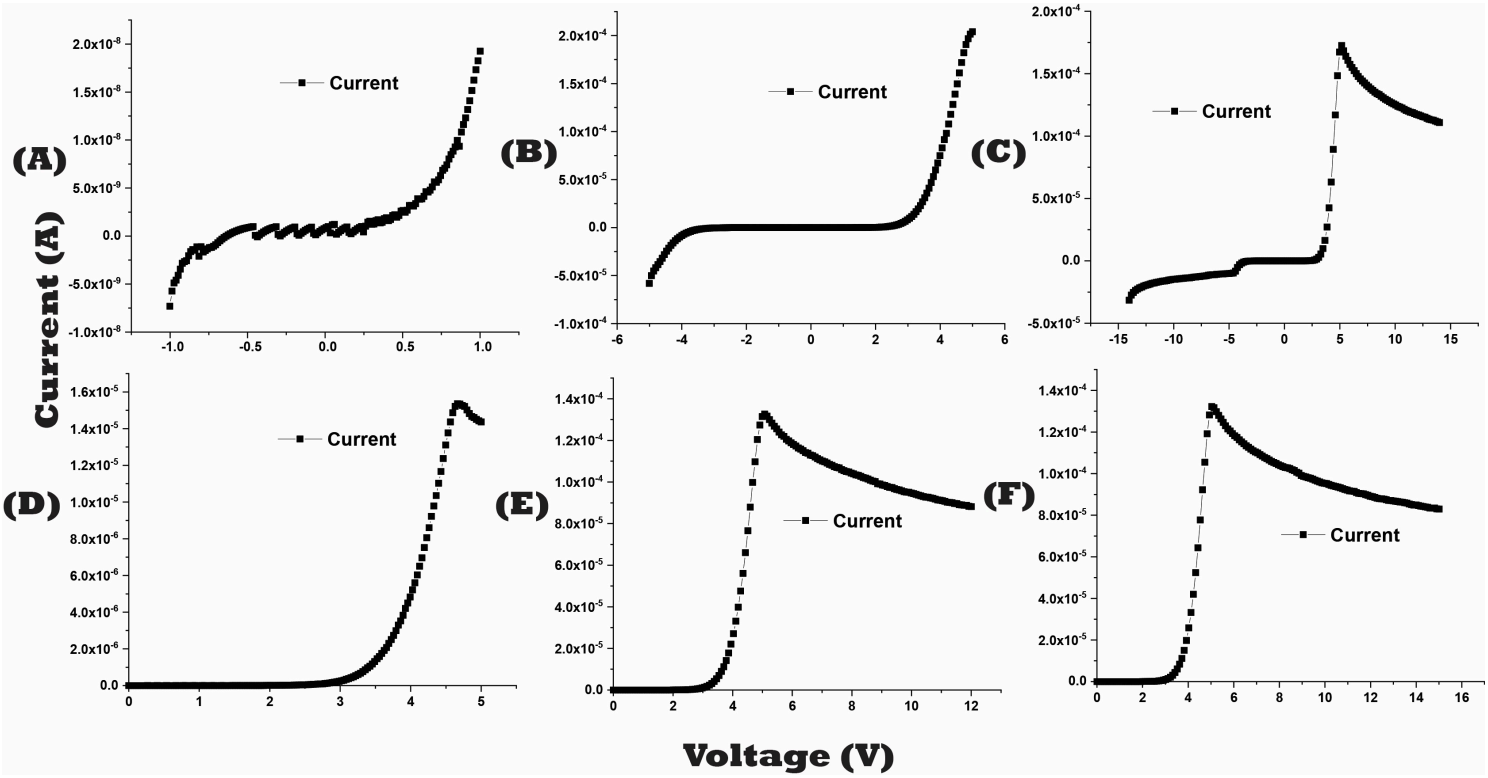


Figure 6

Two-terminal current–voltage (I–V) characteristics of AlGaN/GaN HEMT devices with photolithographically patterned Al/Cr/Au contacts deposited by thermal evaporation, measured prior to post-deposition annealing at different voltage sweep ranges: **(A)** −1 to +1 V, **(B)** −6 to +6 V, **(C)** −20 to +20 V, **(D)** 0 to +5 V, **(E)** 0 to +10 V, and (F) 0 to +16 V.

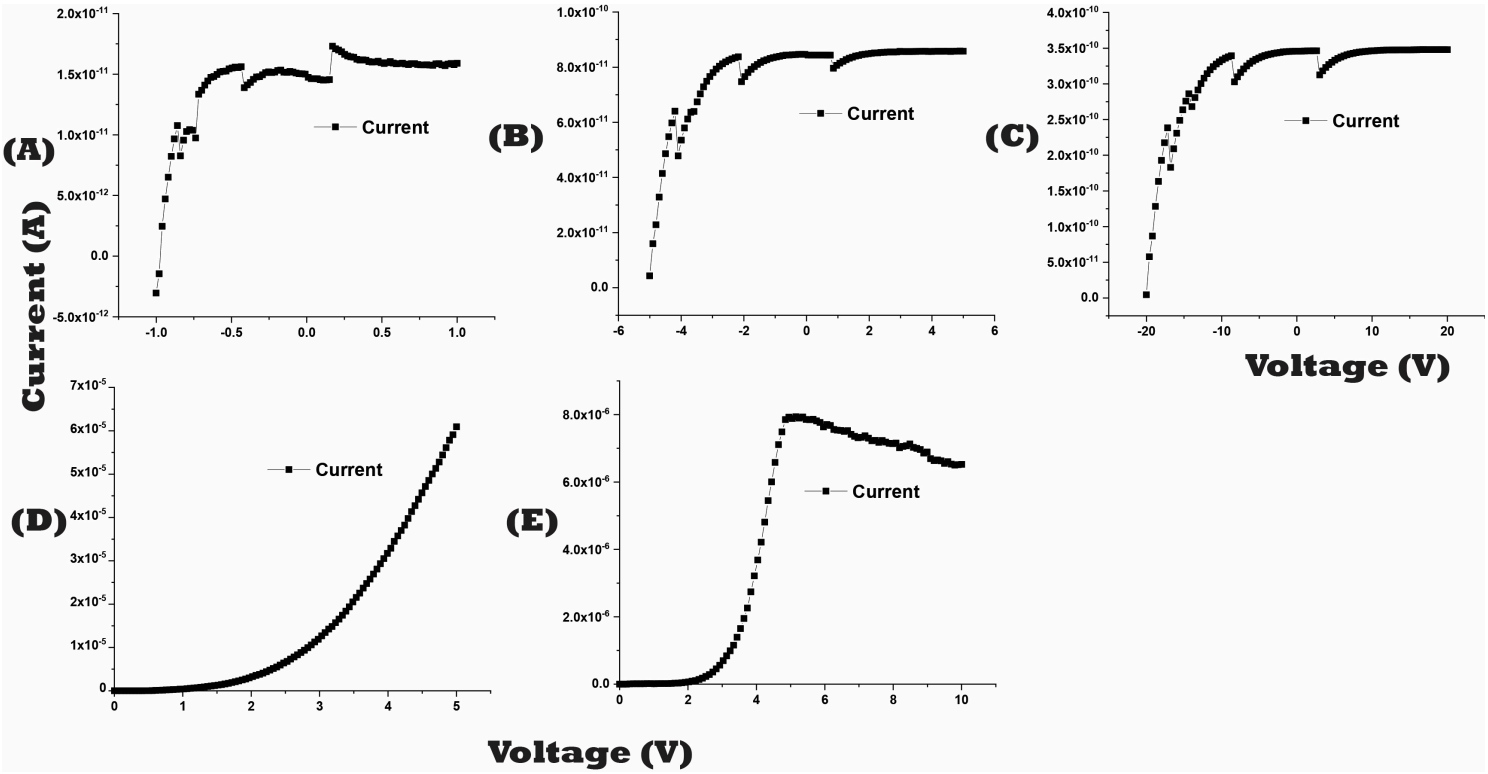


Figure 7

Two-terminal current–voltage (I–V) characteristics of AlGaN/GaN HEMT devices with Al/Cr/Au metal contacts patterned by photolithography and deposited by thermal evaporation, followed by thermal annealing. The I–V characteristics were measured over different voltage sweep ranges: **(A)** −1 to +1 V, **(B)**−6 to +6 V, **(C)** −20 to +20 V, **(D)** 0 to +5 V, and **(E)** 0 to +10 V.

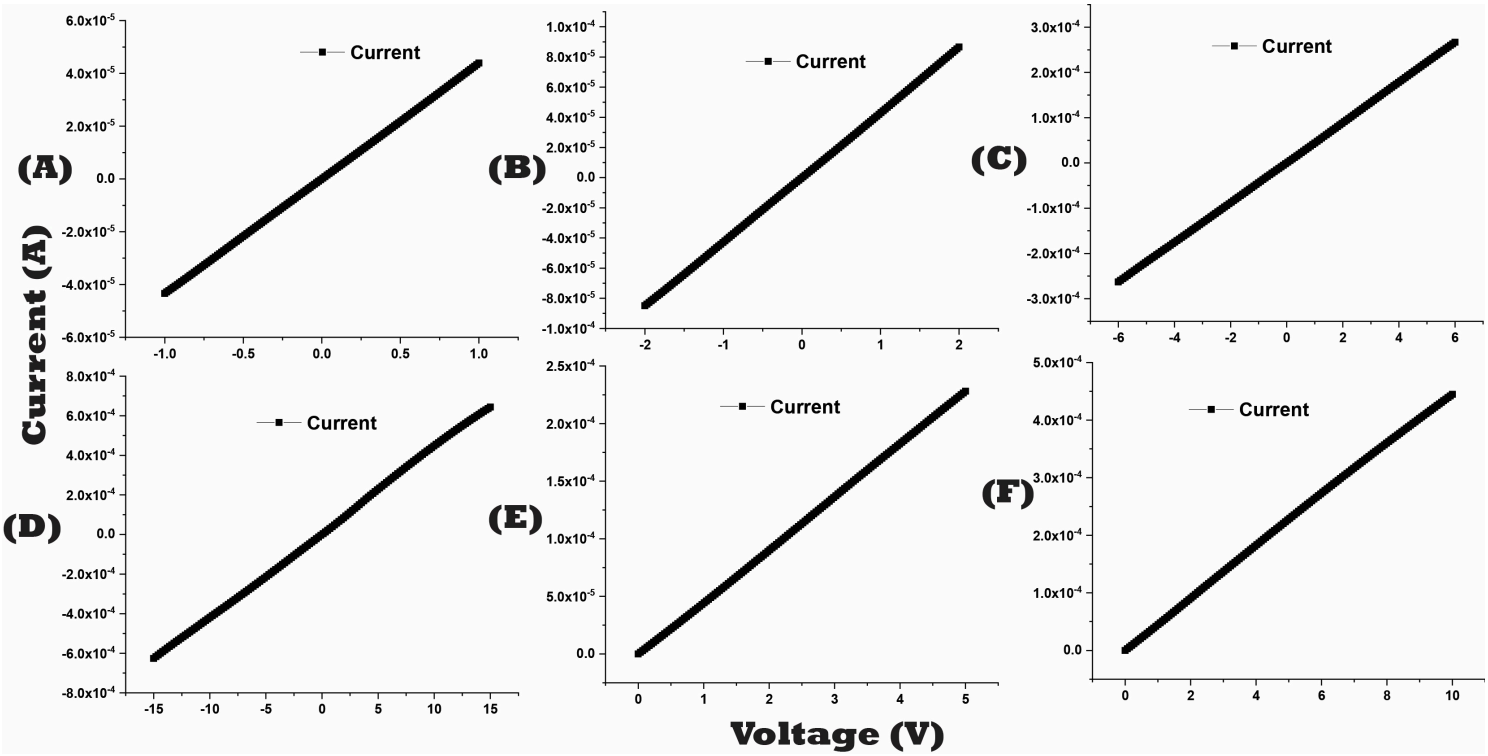


Figure 8

Two-terminal current–voltage (I–V) characteristics of BST-deposited AlGaN/GaN HEMT structures, measured over different applied voltage ranges: **(A)** −1 to +1 V, **(B)** −2 to +2 V, **(C)** −6 to +6 V, **(D)** −15 to +15 V, **(E)** 0 to +5 V, and **(F)** 0 to +10 V.

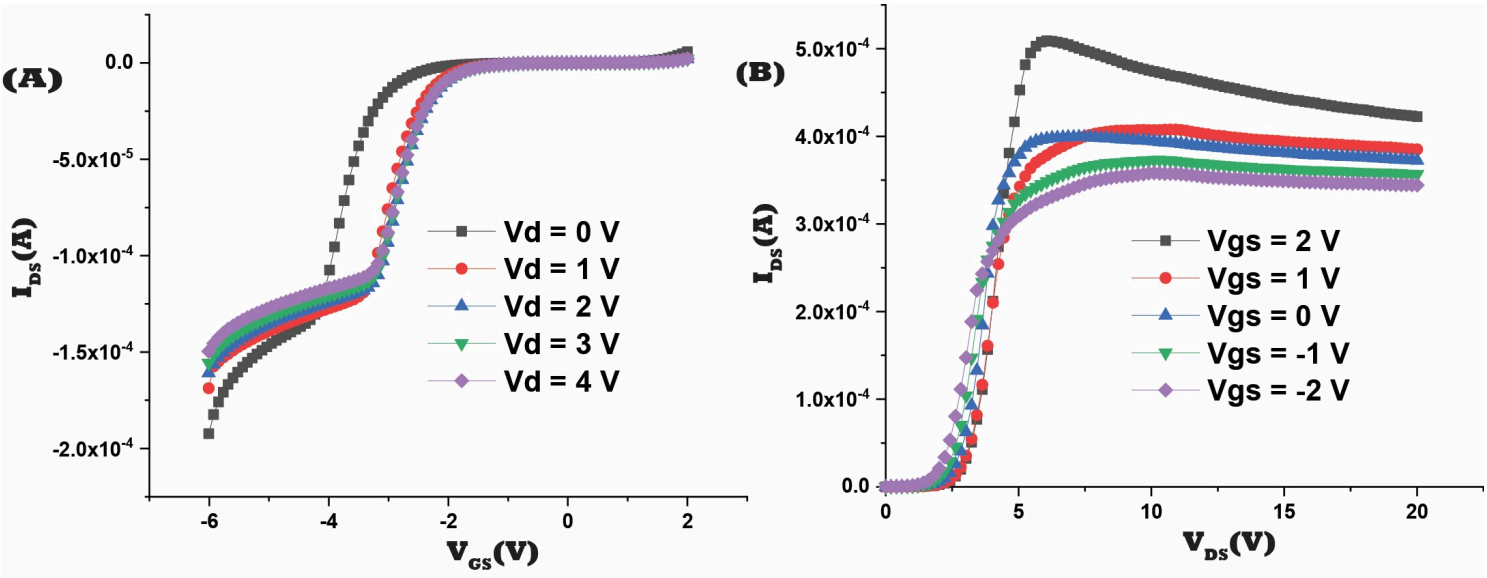


Figure 9

Transfer and output characteristics of the two-terminal AlGaN/GaN HEMT device: **(A)** transfer characteristics measured at different drain voltages , and **(B)** output characteristics measured at different gate-source voltages.