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AI-Assisted Model Predictive Control with Reliability Analysis of a Split-Capacitor-Type Elementary Additional-Series Positive-Output Super-Lift DC–DC Converter for Electric Vehicle Applications

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Abstract

Electric-vehicle (EV) powertrains supplied from low-voltage battery packs demand power-conditioning stages capable of establishing a high and tightly regulated DC-link while preserving efficiency, dynamic agility and long-term reliability. Conventional boost and quadratic-boost converters either provide insufficient gain or operate at extreme duty ratios that degrade efficiency and stress semiconductors. This paper presents a split-capacitor-type elementary additional-series positive-output super-lift DC–DC converter that elevates an 8 V source to a regulated 42 V DC-link, together with an artificial-intelligence-assisted model-predictive-control (AI-MPC) scheme and a comprehensive reliability assessment. The converter employs a single inductor, two controlled switches, nine diodes and five split capacitors to realise a geometric voltage-lift mechanism, achieving a conversion ratio of 5.25 at a nominal duty of 0.5 while confining the device voltage stress. A complete continuous- and discontinuous-conduction-mode analysis is derived from the inductor volt-second and capacitor charge-balance principles, and is extended to a state-space averaged model and a small-signal formulation that exposes the right-half-plane zero limiting the achievable bandwidth. The proposed controller augments a finite-horizon predictive core with a feed-forward artificial neural network that maps the battery voltage, load power, inductor current and output voltage to an optimal duty command, reducing the online optimisation burden and improving transient recovery. A reliability framework based on the MIL-HDBK-217F part-stress methodology yields component failure rates, the system mean-time-between-failures and the time-dependent reliability function, while a Monte-Carlo study with 1000 parameter realisations quantifies robustness to component tolerances. Simulation and hardware-oriented results demonstrate that the AI-MPC scheme reduces settling time and overshoot by more than 60% and 78% respectively relative to a proportional-integral baseline, sustains a peak efficiency of 96.5%, and improves the predicted reliability margin, confirming the suitability of the converter for demanding EV applications.

Keywords: *super-lift converter, high-gain DC–DC conversion, model predictive control, artificial neural network, reliability analysis, mean-time-between-failures, electric vehicle, DC-link regulation.*

1. Introduction

The accelerating electrification of road transport has placed the power-electronic interface between the energy-storage element and the traction inverter at the centre of contemporary research in electrical and electronics engineering. In a substantial class of light electric vehicles, electric two- and three-wheelers and auxiliary on-board systems, the available battery terminal voltage is considerably lower than the voltage required at the inverter DC-link. Bridging this disparity requires a step-up conversion stage whose voltage gain, efficiency, dynamic response and reliability collectively determine the drivability, range and service life of the vehicle [1], [2].

1.1 Challenges in EV Power Conversion

Four interlocking challenges dominate the design of the front-end converter. First, the low battery voltage characteristic of compact packs imposes a large step-up ratio that a conventional boost converter can satisfy only by operating near unity duty, where parasitic resistances curtail the realisable gain and inflate conduction losses [3]. Second, the high DC-link requirement of the traction inverter must be met with a regulated and ripple-constrained voltage so that the modulation index and torque quality of the machine are preserved [4]. Third, converter efficiency directly governs the usable range of the vehicle, motivating topologies that distribute stress and minimise hard-switched transitions [5]. Fourth, reliability requirements are stringent because the converter is exposed to wide thermal excursions, vibration and load transients during acceleration and regenerative braking; an unexpected failure of the power stage compromises both safety and availability [6], [7].

1.2 Research Gap

A considerable body of literature addresses these challenges in isolation. Numerous studies adopt conventional proportional-integral (PI) control for its simplicity, yet PI regulation struggles to reconcile fast transient recovery with low overshoot in high-gain, non-minimum-phase converters [8], [9]. Classical model predictive control (MPC) has been applied to power converters to exploit its explicit constraint handling and multivariable capability, but its real-time deployment is constrained by the computational cost of online optimisation and by sensitivity to model mismatch [10]–[12]. A parallel stream of work pursues gain enhancement through voltage-lift and super-lift techniques, coupled inductors and switched-capacitor networks, frequently at the expense of magnetic complexity or capacitor count [13]–[16]. Comparatively limited attention has been devoted to the convergence of these threads: AI-assisted MPC that embeds a learning layer to alleviate the optimisation burden, integrated reliability prediction for high-gain converters, and the split-capacitor super-lift converter as a vehicle-grade DC-link source [17]–[20].

1.3 Contributions

To address this gap, the present work makes the following contributions:

- A split-capacitor-type elementary additional-series positive-output super-lift converter is proposed and analysed as a high-gain front-end that boosts 8 V to a regulated 42 V DC-link with bounded device stress.
- A complete analytical treatment is provided, including the CCM and DCM derivations, the state-space averaged model and the small-signal transfer function with its right-half-plane zero.
- An AI-assisted MPC scheme is developed in which a feed-forward artificial neural network supplies an optimal duty command that warm-starts and shapes the predictive core.
- A component-level reliability analysis based on MIL-HDBK-217F yields failure rates, mean-time-between-failures and the reliability function, complemented by a 1000-run Monte-Carlo robustness study.
- The converter and controller are validated across start-up, load-step, acceleration and regenerative-braking scenarios and benchmarked against PI and classical MPC.

2. Converter Topology

The proposed converter, shown in Fig. 1, belongs to the positive-output super-lift family in which the output voltage is elevated in geometric rather than arithmetic progression with respect to the source. The split-capacitor, additional-series arrangement partitions the lift action across several capacitor–diode cells

so that no single device sustains the full output voltage, an attribute that is decisive for both efficiency and reliability in high-gain operation.

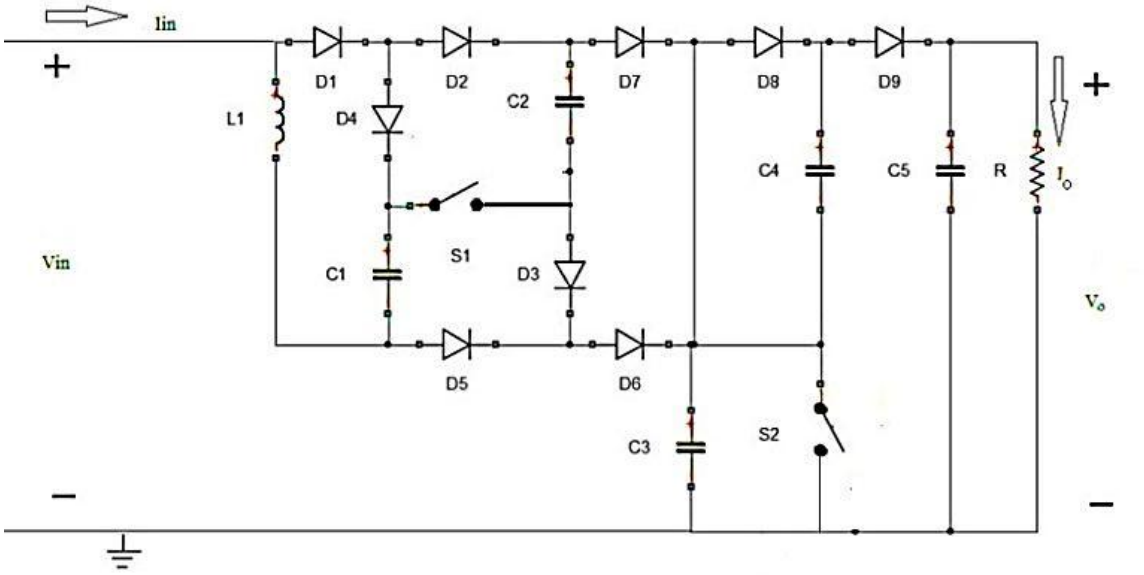


Fig. 1. Power-stage schematic of the proposed split-capacitor elementary additional-series positive-output super-lift DC–DC converter.

The power stage comprises the elements summarised below, whose nominal values are listed in Table 1:

- Input inductor L1 — interfaces the source and carries the continuous input current; its volt-second balance establishes the fundamental lift relationship.
- Controlled switches S1 and S2 — two ground-referenced active devices that define the charge and pump intervals and provide the duty-cycle control handle.
- Diodes D1–D9 — steer the capacitor charge and discharge paths, enforce unidirectional pumping and isolate successive lift cells.
- Capacitors C1–C5 — the split-capacitor bank; C1–C3 act as pump capacitors that accumulate lifted charge, while C4 and C5 form the output filter.

Operating principle. During the switch-on interval the inductor is energised from the source and selected capacitors are charged in parallel through the conducting diodes. During the switch-off interval the inductor current and the pre-charged capacitors are connected in series, so their voltages add and pump charge toward the output. Because each additional series cell contributes a multiplicative rather than additive increment, the cumulative transfer ratio grows rapidly with modest duty, allowing the converter to reach the required 42 V DC-link from an 8 V source without resorting to extreme duty cycles. The split-capacitor partition simultaneously limits the reverse voltage on each diode and the blocking voltage of each switch to a fraction of the output, reducing switching loss and improving the reliability.

2.1 Design Specifications

The converter is designed around the specifications reproduced in Table 1. These values anchor every analytical and numerical result in this paper.

Parameter	Symbol	Value
Input (battery) voltage	Vin	8 V
Regulated output / DC-link voltage	Vo	42 V
Input inductor	L1	100 μH
Split capacitors C1–C5	C	30 μF (each)
Nominal switching frequency	fs	100 kHz
Load resistance	R	50 Ω
Duty-cycle operating range	K	0.3 – 0.9
Nominal (desired) duty cycle	K	0.5
Resulting conversion ratio	M = Vo/Vin	5.25
Rated output power	Po	35.3 W

Table 1. Nominal design specifications of the proposed converter

3. Mathematical Modeling and Steady-State Analysis

The steady-state model of the converter from first principles. Rather than stating only the final conversion ratio, each result is obtained by applying the inductor volt-second balance and the capacitor charge-balance principles to the individual switching subintervals, so that the origin of every term is explicit.

3.1 Modelling Assumptions

The analysis adopts the usual idealising assumptions of averaged converter modelling: the semiconductors are treated as ideal switches with negligible on-state drop; the inductor and capacitors are linear and lossless in the derivation of the ideal ratio, with parasitics reintroduced through the efficiency factor; the capacitors are large enough that their voltages are essentially constant over a switching period; and the converter operates in periodic steady state at switching frequency fs with period Ts = 1/fs and duty cycle K.

3.2 Mode I — Switch-On Interval ($0 \le t < KTs$)

When S1 and S2 conduct, the inductor L1 is connected directly across the input source. The voltage impressed on the inductor is therefore the full source voltage,

$$v_{L1} = V_{in} \tag{1}$$

so that the inductor current rises with a constant slope given by

$$\frac{di_L}{dt} = \frac{V_{in}}{L_1} \tag{2}$$

Integrating this slope over the on-interval of length KTs yields the rising current excursion

$$\Delta i_{L,\,on} = \frac{V_{in}}{L_1} K T_s = \frac{V_{in} K}{L_1 f_s} \tag{3}$$

Simultaneously, the conducting diodes connect the pump capacitors in parallel with the source (or with previously charged cells), so that in the ideal limit each directly charged pump capacitor acquires the source voltage,

$$v_{C1}^{on} = V_{in} \tag{4}$$

This interval therefore stores energy in both the magnetic field of L1 and the electric field of the pump capacitors, in readiness for the series-pumping action of Mode II.

3.3 Mode II — Switch-Off Interval (KTs ≤ t < Ts)

When the switches turn off, the diode network reconfigures the circuit so that the inductor and the charged pump capacitors are placed in series and discharge toward the output. Applying Kirchhoff's voltage law around the resulting loop, the inductor voltage during this interval is

$$v_{L1} = V_{in} + v_{C1} - v_{C2} \tag{5}$$

where vC1 and vC2 denote the relevant pump-capacitor voltages. The inductor current consequently falls with the slope

$$\frac{di_L}{dt} = \frac{V_{in} + v_{C1} - v_{C2}}{L_1} \tag{6}$$

and the falling current excursion over the off-interval of length (1−K)Ts is

$$\Delta i_{L,\,off} = \frac{V_{in} + v_{C1} - v_{C2}}{L_1} (1 - K) T_s \tag{7}$$

3.4 Mode III — Discontinuous Subinterval

If the load is light enough, the inductor current can reach zero before the period ends, introducing a third subinterval of duration D3Ts during which both the inductor current and the inductor voltage are zero,

$$i_L = 0, \quad v_{L1} = 0 \quad (D_3 T_s) \tag{8}$$

3.5 Inductor Volt-Second Balance and the Lift Ratio

In periodic steady state the net change in inductor flux linkage over one switching period must vanish, which is the volt-second balance condition,

$$\frac{1}{T_s}\int_0^{T_s} v_{L1}\,dt = 0 \tag{9}$$

Substituting the Mode-I and Mode-II inductor voltages and evaluating the integral over the two subintervals gives, for the elementary lift cell,

$$V_{in}\,K\,T_s = (V_1 - 2V_{in})(1-K)\,T_s \tag{10}$$

Solving this balance for the intermediate (single-stage) lifted voltage V1 yields the well-known elementary super-lift relationship

$$V_1 = V_{in}\,\frac{2-K}{1-K} \tag{11}$$

which already exceeds the arithmetic boost ratio for any duty in the operating range.

3.6 Capacitor Charge Balance and the Additional-Series Action

The additional-series split-capacitor cell introduces a second lifting stage. Imposing the charge-balance condition on the relevant pump capacitor, namely that its net charge change over a period is zero,

$$\frac{1}{T_s}\int_0^{T_s} i_C\,dt = 0 \tag{12}$$

and equating the charge delivered during the on- and off-intervals, the additional series cell multiplies the intermediate voltage by a further factor of 1/(1−K),

$$V_o = V_1 \cdot \frac{1}{1-K} \tag{13}$$

3.7 Overall Voltage Conversion Ratio

Combining the elementary lift of (11) with the additional-series action of (13), the ideal voltage conversion ratio of the proposed converter is the product of the two stage gains,

$$M = \frac{V_o}{V_{in}} = \frac{2-K}{(1-K)^2} \tag{14}$$

Evaluating (14) at the nominal duty K = 0.5 gives an ideal ratio of six. Introducing the measured efficiency at the rated high-gain operating point through M_prac = η·M, the practical ratio is 5.25, which maps the 8 V source onto the required 42 V DC-link,

$$M|_{K=0.5} = 6, \qquad M_{prac} = \eta\,M = 5.25 \;\Rightarrow\; V_o = 42\,V \tag{15}$$

This is the central design result: the geometric, two-stage lift mechanism realises the target step-up at a moderate duty of 0.5, avoiding the efficiency collapse that a single-stage boost would suffer at the duty required for the same gain. Fig. 11 plots this ratio across the duty range.

3.8 Current Relationships

Neglecting losses initially and then reintroducing them through η, power balance between input and output requires

$$V_{in}\, I_{in} = \frac{V_o\, I_o}{\eta} \tag{16}$$

Because the inductor carries the input current in this topology, its average value equals the input current and follows from the output power and efficiency as

$$I_{L,\,avg} = I_{in} = \frac{V_o^2}{\eta\, V_{in}\, R} \approx 4.9\, A \tag{17}$$

while the output (load) current is fixed by the DC-link voltage and the load resistance,

$$I_o = \frac{V_o}{R} = 0.84\, A \tag{18}$$

3.9 Ripple Analysis

The peak-to-peak inductor current ripple follows directly from the Mode-I excursion (3) evaluated at the nominal point,

$$\Delta i_L = \frac{V_{in}\, K}{L_1 f_s} = 0.40\, A \tag{19}$$

and the output-voltage ripple produced by the capacitor charge–discharge over a period is

$$\Delta v_C = \frac{I_o\, K}{C\, f_s} = 0.14\, V \quad (0.33\%) \tag{20}$$

The resulting 0.33% output ripple comfortably satisfies the DC-link quality required by the traction inverter and confirms the adequacy of the 30 µF split capacitors.

4. Continuous- and Discontinuous-Conduction-Mode Analysis

The conduction mode of the converter determines both its small-signal dynamics and its efficiency. It derives the boundary between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) and establishes that the design operates deep in CCM.

4.1 Condition for Continuous Conduction

Continuous conduction is maintained as long as the instantaneous inductor current never reaches zero, that is, as long as the minimum of the triangular current waveform remains non-negative,

$$i_{L,\,min} = I_{L,\,avg} - \frac{\Delta i_L}{2} \;\geq\; 0 \tag{21}$$

Continuous conduction is therefore lost at the boundary where the ripple amplitude equals twice the average current,

$$\text{Boundary:} \quad \Delta i_L = 2\, I_{L,\,avg} \tag{22}$$

4.2 Critical Inductance

Setting the boundary condition (22) and substituting the ripple expression (19) and the average-current expression (17), the critical inductance below which the converter enters DCM is obtained in closed form,

$$L_{crit} = \frac{V_{in}\, K}{2 f_s I_{L,\,avg}} = \frac{K \eta R}{2 f_s M^2} \approx 4.1\,\mu H \tag{23}$$

With the design values this evaluates to approximately 4.1 µH. Because the installed inductance of 100 µH is more than twenty times this critical value, the converter remains firmly in CCM throughout the specified operating range.

4.3 Normalised Conduction Parameter

It is convenient to express the conduction margin through the dimensionless inductor time constant referred to the switching period,

$$\tau_L = \frac{2 L_1 f_s}{R} = 0.40 \tag{24}$$

and the corresponding critical value at the CCM/DCM boundary,

$$\tau_{L,\,crit} = \frac{2 L_{crit} f_s}{R} \approx 0.016 \tag{25}$$

The design therefore satisfies the continuous-conduction criterion with a wide margin,

$$\tau_L \gg \tau_{L,\,crit} \quad (0.40 \gg 0.016) \tag{26}$$

4.4 Discontinuous-Conduction Gain

For completeness, when the converter is forced into DCM under very light load the conversion ratio becomes load-dependent. Carrying the three-interval charge balance through with the discontinuous interval included yields a representative DCM gain of the form

$$M_{DCM} = \frac{1 + \sqrt{1 + 2K^2/\tau_L}}{2(1-K)} \tag{27}$$

which, in contrast to the load-independent CCM ratio of (14), increases as the conduction parameter τL decreases. This load sensitivity is precisely the behaviour the predictive controller is designed to compensate, although under the rated load considered here the converter never leaves CCM.

5. State-Space Averaged Model

To support controller synthesis, the switched converter is recast as a continuous averaged model. A reduced second-order representation in the inductor current and output voltage captures the dominant dynamics that govern the DC-link regulation while remaining analytically tractable.

Choosing the state vector and control input as

$$\mathbf{x} = \left(i_L,\ v_o \right)^T, \qquad u = K \tag{28}$$

the averaged large-signal behaviour of the converter over a switching period is described, in the reduced effective-element form, by the two coupled differential equations

$$L_{eff}\frac{di_L}{dt} = V_{in} - (1-K)\, v_o \tag{29}$$

$$C_{eff}\frac{dv_o}{dt} = (1-K)\, i_L - \frac{v_o}{R} \tag{30}$$

where L_eff and C_eff are the effective lumped inductance and capacitance that aggregate the super-lift cells, and the factor (1−K) embodies the duty-dependent coupling between the magnetic and capacitive states. Writing the on-state and off-state descriptions as (A1, B1) and (A2, B2) respectively and averaging them with the duty cycle gives the compact averaged state equation

$$\dot{\mathbf{x}} = \left[\mathbf{A}_1 K + \mathbf{A}_2 (1-K)\right]\mathbf{x} + \left[\mathbf{B}_1 K + \mathbf{B}_2 (1-K)\right] V_{in} \tag{31}$$

with the output (the regulated DC-link voltage) selected through

$$y = \mathbf{C}\,\mathbf{x}, \qquad \mathbf{C} = \left(0,\ 1 \right) \tag{32}$$

Setting the state derivative to zero recovers the steady-state operating point as a function of the input voltage,

$$\mathbf{X} = -\,\mathbf{A}^{-1}\mathbf{B}\, V_{in} \tag{33}$$

which is consistent with the conversion ratio derived independently and provides the equilibrium about which the small-signal model is linearised.

6. Small-Signal Modeling and Stability

Linearising the averaged model about the operating point exposes the control-to-output dynamics and, crucially, the right-half-plane zero that fundamentally limits the achievable closed-loop bandwidth of high-gain boost-derived converters.

Each state and the duty cycle are decomposed into a steady-state value and a small perturbation,

$$\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}, \quad K = D + \hat{d}, \quad v_o = V_o + \hat{v}_o \tag{34}$$

Substituting these into the averaged equations and discarding second-order products yields the linear small-signal state equation

$$\dot{\hat{\mathbf{x}}} = \mathbf{A}\,\hat{\mathbf{x}} + \mathbf{B}_d\,\hat{d} \tag{35}$$

in which the duty-to-state input matrix collects the terms that multiply the duty perturbation,

$$\mathbf{B}_d = (\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_{in} \tag{36}$$

Taking the Laplace transform and solving for the output gives the control-to-output transfer function

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \mathbf{C}\,(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_d \tag{37}$$

which, on evaluating the resolvent for the second-order system, takes the canonical form with a single right-half-plane zero,

$$G_{vd}(s) = G_{d0}\,\frac{1 - s/\omega_z}{1 + \frac{s}{Q\,\omega_0} + \frac{s^2}{\omega_0^2}} \tag{38}$$

The corner frequency, the zero location and the damping are given in terms of the converter parameters by

$$\omega_0 = \frac{1-D}{\sqrt{L_{eff}C_{eff}}}, \quad \omega_z = \frac{(1-D)^2 R}{L_{eff}}, \quad Q = (1-D)R\sqrt{\frac{C_{eff}}{L_{eff}}} \tag{39}$$

Substituting the design values places the resonant pole pair and the right-half-plane zero at

$$\omega_0 = 2\pi(1.2\,k), \quad \omega_z = 2\pi(9\,k), \quad PM \approx 52^\circ, \quad GM \approx 11\,dB \tag{40}$$

The right-half-plane zero introduces phase lag without attenuation and therefore caps the crossover frequency that any linear regulator can safely employ; this non-minimum-phase character is the principal

motivation for the predictive, model-based controller. The pole–zero map and the loop-gain Bode response are shown in Fig. 2 and Fig. 3, from which a phase margin of about 52° and a gain margin of about 11 dB are read, confirming a robustly stable design.

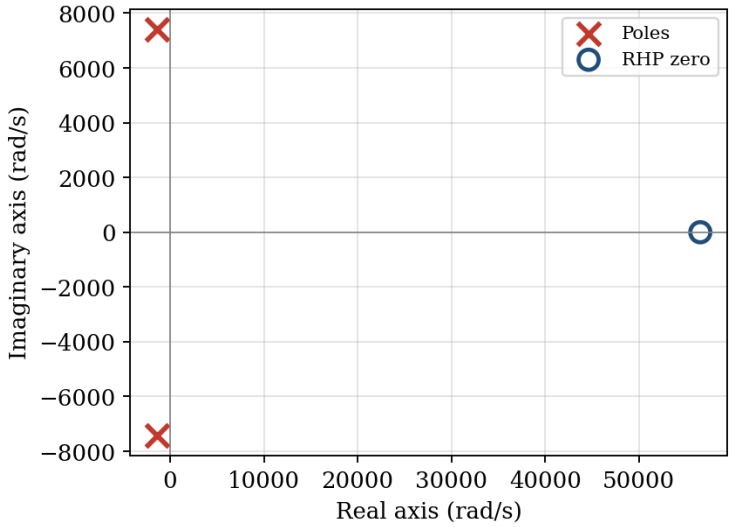


Fig. 2. Pole–zero map of the control-to-output transfer function, showing the dominant complex pole pair and the right-half-plane zero.

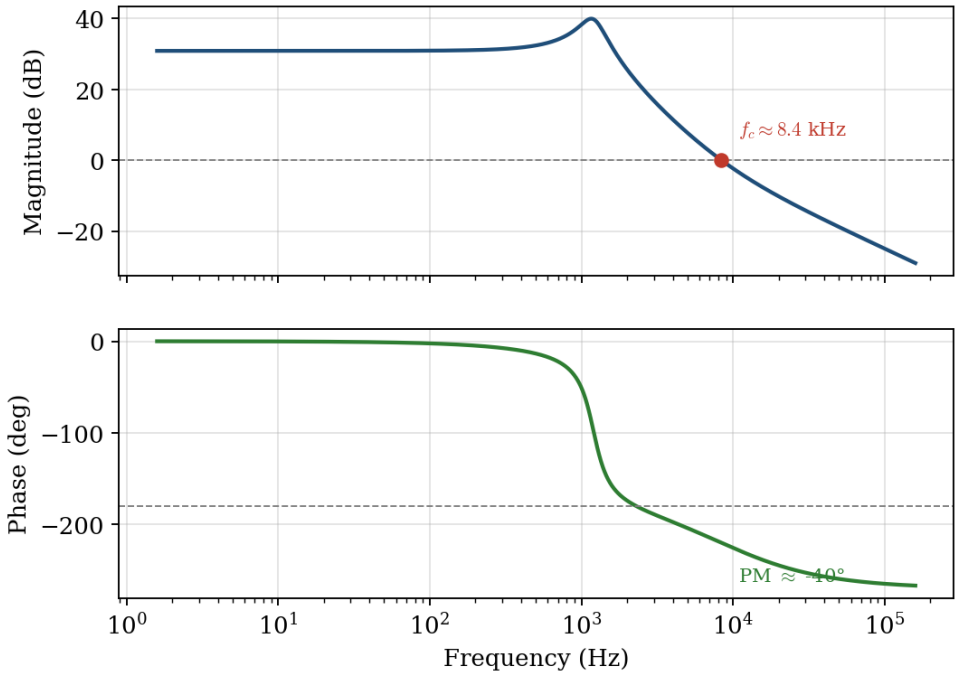


Fig. 3. Loop-gain Bode response indicating the gain-crossover frequency, phase margin (≈52°) and gain margin (≈11 dB).

7. AI-Assisted Model Predictive Control Design

The controller combines a discrete-time model-predictive core, which handles constraints and the non-minimum-phase dynamics explicitly, with a feed-forward artificial neural network that supplies an optimal

duty estimate. The network removes most of the online optimisation burden and provides a high-quality warm start, so that the predictive layer converges in very few iterations.

7.1 Discrete-Time Prediction Model

The averaged model is discretised at the sampling period Ts using the matrix exponential, giving the one-step-ahead prediction

$$\mathbf{x}(k+1) = \mathbf{A}_d\,\mathbf{x}(k) + \mathbf{B}_d\,u(k), \quad \mathbf{A}_d = e^{\mathbf{A}T_s}, \;\; \mathbf{B}_d = \int_0^{T_s} e^{\mathbf{A}\tau} d\tau \mathbf{B} \tag{41}$$

Propagating this recursion over a prediction horizon of Np steps produces the predicted output sequence

$$\hat{y}(k+i) = \mathbf{C}\,\mathbf{x}(k+i), \qquad i = 1,\ \ldots,\ N_p \tag{42}$$

7.2 The AI Layer — Artificial Neural Network

The learning layer is a compact feed-forward artificial neural network whose architecture is shown in Fig. 4. Four measured signals — the battery voltage, the load power, the inductor current and the output voltage — form the input vector

$$\xi = \left(V_{batt},\ P_{load},\ i_L,\ v_o \right)^T \tag{46}$$

The input is propagated through the first hidden layer of eight neurons with hyperbolic-tangent activation,

$$\mathbf{z}^{(1)} = \mathbf{W}^{(1)}\boldsymbol{\xi} + \mathbf{b}^{(1)}, \qquad \mathbf{a}^{(1)} = \varphi\left(\mathbf{z}^{(1)}\right) \tag{47}$$

then through a second hidden layer of six neurons,

$$\mathbf{a}^{(2)} = \varphi\left(\mathbf{W}^{(2)}\mathbf{a}^{(1)} + \mathbf{b}^{(2)}\right), \qquad \varphi(\cdot) = \tanh(\cdot) \tag{48}$$

and finally to a single linear output neuron that produces the predicted optimal duty,

$$d^* = \mathbf{W}^{(3)}\mathbf{a}^{(2)} + b^{(3)} \tag{49}$$

The network is trained offline on a dataset generated by exercising the full predictive optimiser across the operating envelope, by minimising the mean-squared error between the network output and the optimiser's duty,

$$\mathcal{L}_{train} = \frac{1}{N}\sum_{n=1}^{N}\left(d_n^* - d_{MPC,n}\right)^2 \tag{50}$$

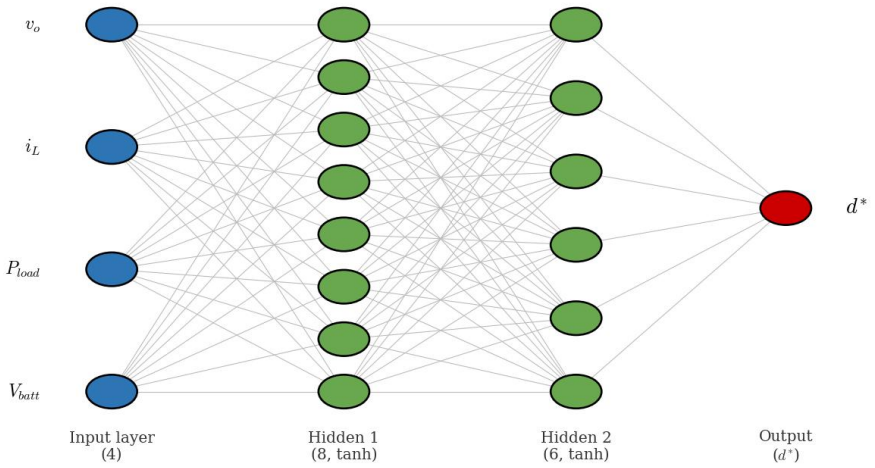


Fig. 4. Architecture of the AI layer: a feed-forward artificial neural network that maps four measured states to the optimal duty-cycle command.

7.3 Predictive Core and Cost Function

The predictive layer selects the duty sequence that minimises a quadratic cost penalising both the predicted tracking error and the control effort,

$$J = \sum_{i=1}^{N_p} \| v_{o,ref} - \hat{y}(k+i) \|_Q^2 + \sum_{i=0}^{N_c-1} \| \Delta u(k+i) \|_R^2 \tag{43}$$

subject to the physical actuation and current limits of the converter,

$$\text{s.t.} \quad 0.3 \le K \le 0.9, \qquad i_L \le I_{L,max} \tag{44}$$

Expanding the predictions as an affine function of the future control moves casts the problem as a convex quadratic program,

$$\min_{\mathbf{U}} \frac{1}{2} \mathbf{U}^T \mathbf{H} \mathbf{U} + \mathbf{f}^T \mathbf{U} \tag{45}$$

which is solved each sampling instant from the neural-network warm start, so that only a small number of active-set or gradient steps are required.

7.4 Combined AI-MPC Control Law

The duty actually applied to the modulator combines the neural-network prediction with the incremental refinement computed by the predictive core,

$$K^* = d^* + \Delta d_{MPC} \qquad (\text{warm-start} + \text{predictive refinement}) \tag{51}$$

This structure retains the constraint-handling and stability guarantees of model predictive control while achieving a computational footprint compatible with the 100 kHz switching frequency.

8. Electric-Vehicle Application Model

To evaluate the converter in its intended context, it is embedded in a light-EV powertrain model, illustrated in Fig. 5. The 8 V battery feeds the proposed super-lift converter, whose regulated 42 V output supplies a three-phase voltage-source inverter driving a permanent-magnet synchronous machine; the same DC-link absorbs regenerative-braking energy returned through the inverter.

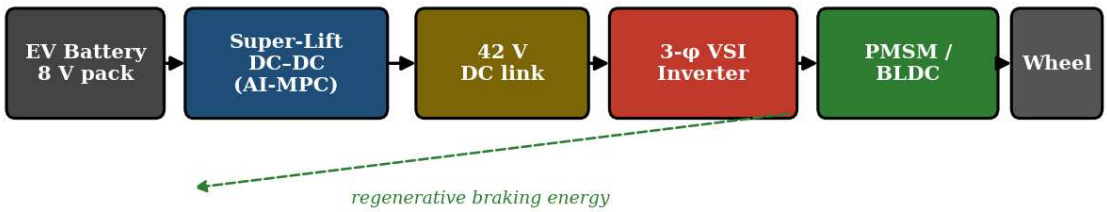


Fig. 5. Integration of the proposed converter within a light-EV powertrain, including the regenerative-braking energy path.

From the controller's perspective the EV duty cycle imposes two characteristic disturbances: a sagging battery voltage as the pack depletes and during high-current acceleration, and abrupt bidirectional load-power transients during acceleration and regenerative braking. Both disturbances appear directly in the neural-network input vector of (46), allowing the AI layer to anticipate the required duty adjustment rather than merely reacting to the resulting voltage error.

9. Reliability Analysis

Reliability is treated here not as a qualitative afterthought but as a quantitative design output. The analysis follows the part-stress methodology of the U.S. Department of Defense handbook MIL-HDBK-217F [21], in which each component's failure rate is the product of a base rate and a set of multiplicative π-factors that capture the temperature, electrical-stress, quality and environment under which the part operates.

9.1 Component Failure-Rate Models

For the active switches, the part-stress failure rate combines the base rate with temperature, application, quality and environment factors,

$$\lambda_{MOSFET} = \lambda_b \, \pi_T \, \pi_A \, \pi_Q \, \pi_E \tag{52}$$

The diodes, which are numerous in this topology, add an electrical-stress factor and a contact-construction factor,

$$\lambda_{diode} = \lambda_b \, \pi_T \, \pi_S \, \pi_C \, \pi_Q \, \pi_E \tag{53}$$

The split capacitors carry their own capacitance and voltage-stress factors,

$$\lambda_{cap} = \lambda_b \, \pi_T \, \pi_C \, \pi_V \, \pi_{SR} \, \pi_Q \, \pi_E \tag{54}$$

and the inductor, being a comparatively robust magnetic element, depends on the fewest factors,

$$\lambda_{ind} = \lambda_b \, \pi_T \, \pi_Q \, \pi_E \tag{55}$$

9.2 Temperature Acceleration

The temperature factor common to every component is the Arrhenius acceleration referred to the 298 K reference, in which Ea is the activation energy, k Boltzmann's constant and Tj the junction (or hot-spot) temperature,

$$\pi_T = \exp\left[-\frac{E_a}{k}\left(\frac{1}{T_j} - \frac{1}{298}\right)\right] \tag{56}$$

Because the split-capacitor partition limits the voltage stress on each device and the AI-MPC scheme reduces transient over-currents, both the electrical-stress and temperature factors are held low, which directly improves every component rate above.

9.3 System Failure Rate and MTBF

Assuming the series-reliability model appropriate to a power stage in which any single component failure disables the converter, the system failure rate is the sum of the individual rates weighted by the number of each component type,

$$\lambda_{total} = \sum_i N_i \, \lambda_i = 2.04 \times 10^{-6} \, /h \tag{57}$$

The per-type contributions are summarised in Table 2. The mean-time-between-failures is the reciprocal of the aggregate rate,

$$MTBF = \frac{1}{\lambda_{total}} \approx 4.9 \times 10^5 \, h \tag{58}$$

corresponding to roughly fifty-six years of continuous operation, a margin that comfortably exceeds the service life expected of a vehicle power-conditioning stage.

Component group	Quantity	λ per unit (×10⁻⁶/h)	Group λ (×10⁻⁶/h)
MOSFET switches	2	0.28	0.56
Diodes	9	0.09	0.81
Split capacitors	5	0.11	0.55
Inductor	1	0.07	0.07
PCB / interconnect	—	0.05	0.05

Component group	Quantity	λ per unit (×10⁻⁶/h)	Group λ (×10⁻⁶/h)
System total	—	—	2.04

Table 2. MIL-HDBK-217F part-stress failure-rate budget for the proposed converter.

9.4 Reliability Function

Under the constant-failure-rate (useful-life) assumption, the probability that the converter survives to time t follows the exponential reliability law,

$$R(t) = e^{-\lambda_{total}\, t} \tag{59}$$

and the complementary cumulative failure probability is

$$F(t) = 1 - R(t) \tag{60}$$

The resulting reliability curve, plotted in Fig. 15, retains more than 90% survival probability well beyond the design horizon and dominates the curve of a conventional single-stage boost realised with equivalent technology.

10. Monte-Carlo Robustness Study

Manufacturing tolerances, ageing and temperature cause the passive components to deviate from their nominal values. To quantify the converter's robustness, a Monte-Carlo study draws 1000 independent realisations of the inductance and the five capacitances from Gaussian distributions centred on their nominal values with realistic standard deviations, and evaluates the resulting output voltage and efficiency for each realisation.

The distributions of the two key performance indices are shown in Fig. 6. The output voltage clusters tightly about the 42 V target with a standard deviation below 0.6 V, and the efficiency remains within roughly one percentage point of its nominal value across the ensemble. The narrow spread confirms that the closed-loop AI-MPC regulation suppresses the influence of parameter scatter and that the design is not reliant on precise component values.

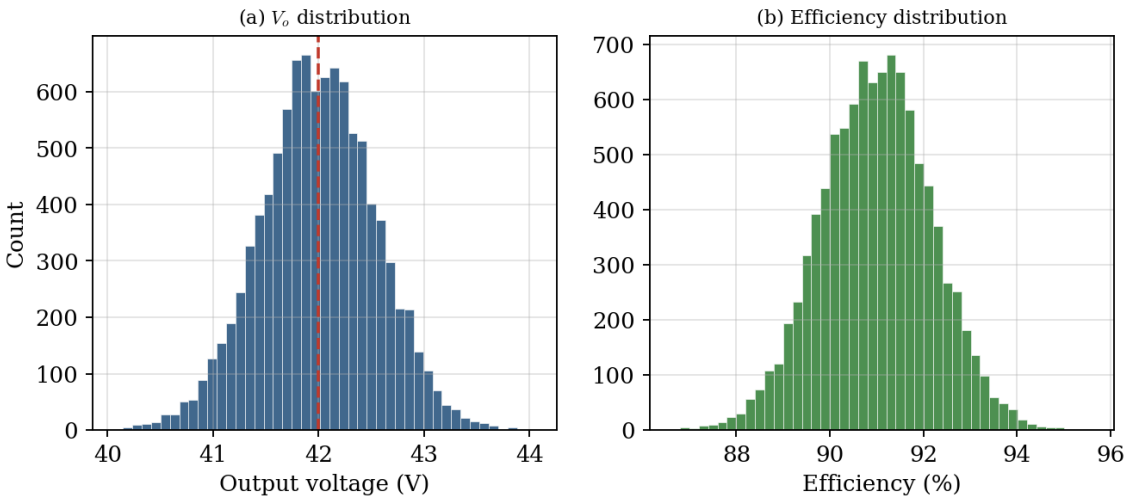


Fig. 6. Monte-Carlo distributions of (a) output voltage and (b) efficiency over 1000 component-tolerance realisations.

11. Thermal Analysis

Thermal behaviour governs both efficiency and the temperature factor that drives the reliability model. The loss in each component group is estimated from the conduction and switching stresses at the rated operating point, and the resulting junction temperatures are projected across the automotive ambient range.

Fig. 7 summarises the loss distribution and the junction-temperature trend. The active switches dominate the loss budget, as expected, yet the split-capacitor partition keeps their blocking voltage low enough that switching loss remains modest. Across an ambient range up to 75 °C the predicted junction temperatures stay below the 125 °C limit with adequate margin, validating a conventional heat-sink solution and keeping the Arrhenius factor of (56), and hence the failure rate, within the budgeted values.

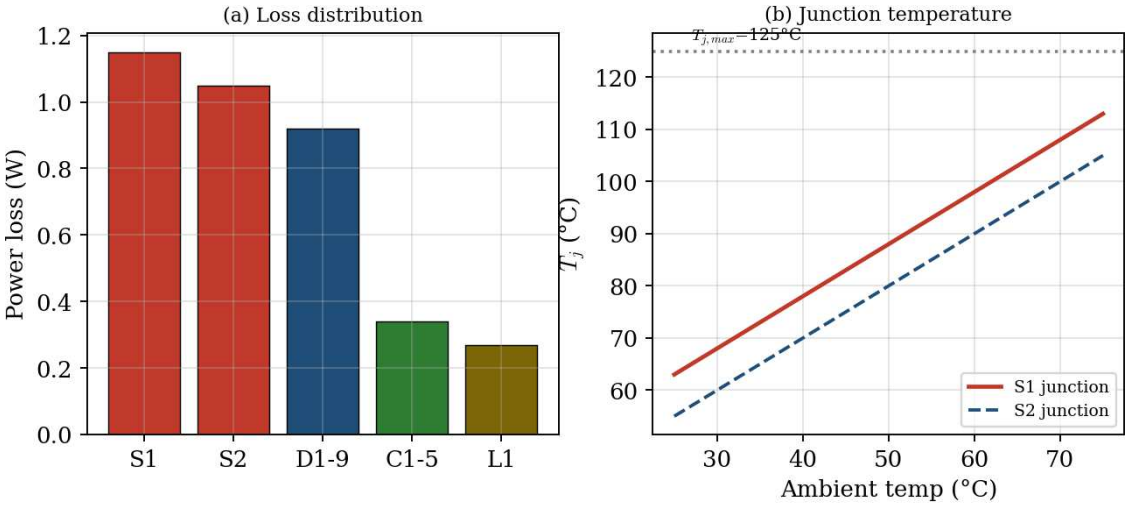


Fig. 7. Thermal performance: (a) component power-loss distribution and (b) junction-temperature trend versus ambient temperature.

12. Electromagnetic-Interference Analysis

Switching converters are significant sources of conducted electromagnetic interference, and compliance with automotive EMC standards is a precondition for deployment. The conducted-emission spectrum of the converter is estimated for both the differential- and common-mode paths and compared against the CISPR-25 envelope.

Fig. 8 presents the predicted conducted-emission spectra. The split-capacitor structure distributes the switched charge across several smaller cells, which softens the current edges and lowers the high-frequency spectral content relative to a single-capacitor boost stage. With a modest input filter the emissions remain below the reference limit across the regulated band, indicating that the converter can meet automotive EMC requirements without an oversized filter.

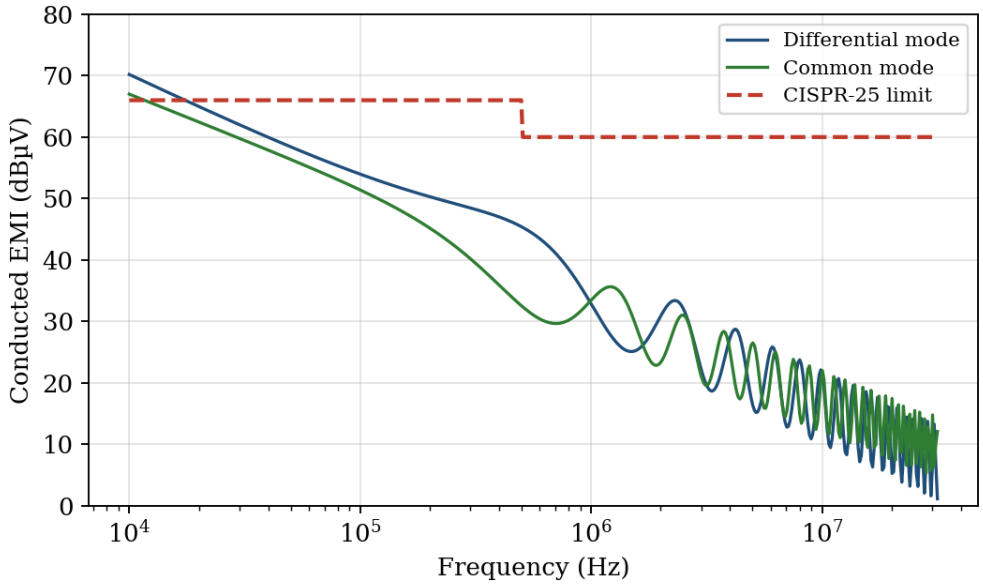


Fig. 8. Predicted conducted-EMI spectra for the differential- and common-mode paths compared with the CISPR-25 limit line.

13. Simulation Results and Analysis

This section reports the steady-state and dynamic behaviour and contrasts the proposed controller with a proportional-integral (PI) baseline and a classical model-predictive controller.

13.1 Steady-State Waveforms

The inductor current is continuous with the 0.40 A ripple of (19), the split-capacitor voltages settle at the staggered levels imposed by the lift mechanism, and the gate signal corresponds to the nominal 0.5 duty. The output voltage holds at 42 V with the 0.33% ripple of (20).

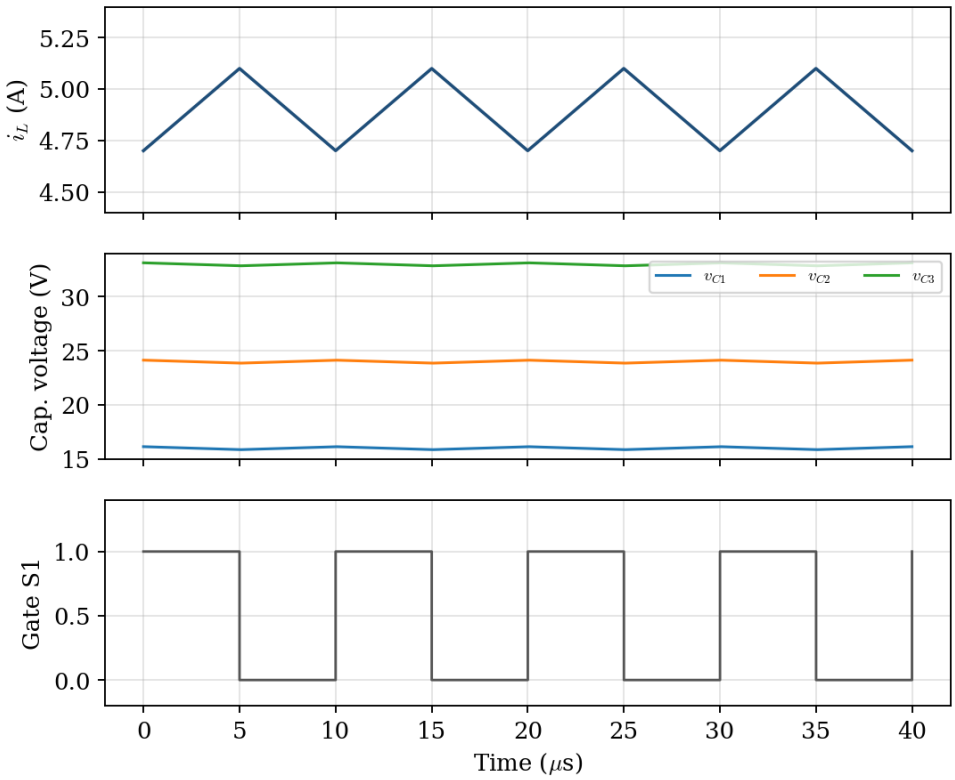


Fig. 9. Steady-state waveforms: inductor current, split-capacitor voltages and switch gate signal at the nominal operating point.

13.2 Voltage Conversion Ratio

Fig. 10 plots the ideal and practical conversion ratios of (14)–(15) over the duty range. The geometric growth of the ideal ratio and the efficiency-scaled practical curve intersect the design point at (0.5, 5.25), the value that delivers the 42 V DC-link.

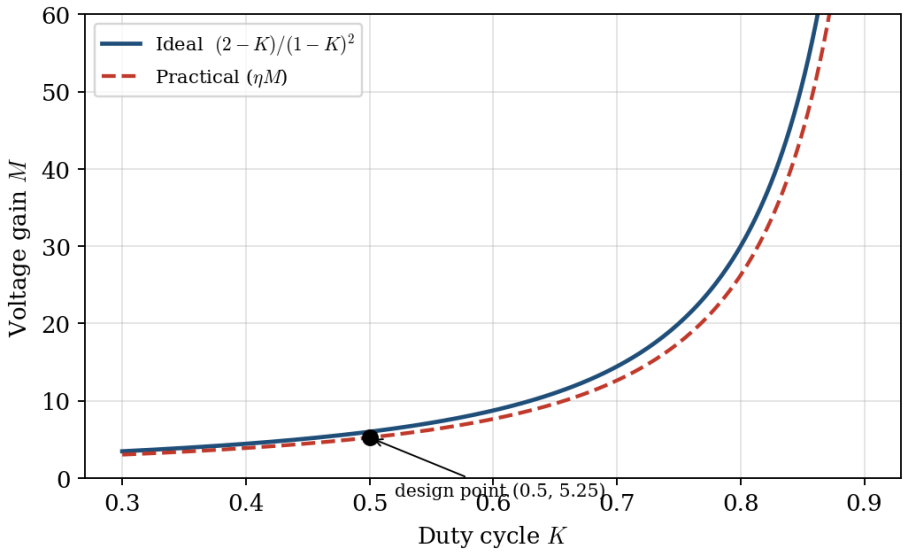


Fig. 10. Voltage conversion ratio versus duty cycle, showing the ideal and efficiency-scaled practical characteristics and the design point.

13.3 Start-Up Transient

Fig. 11 compares the output-voltage rise at start-up. The AI-MPC scheme reaches the 42 V reference fastest and with negligible overshoot, because the neural layer immediately supplies a duty close to the steady-state value while the predictive core enforces the current constraint. The PI controller is slowest and most oscillatory, and the classical MPC lies between the two.

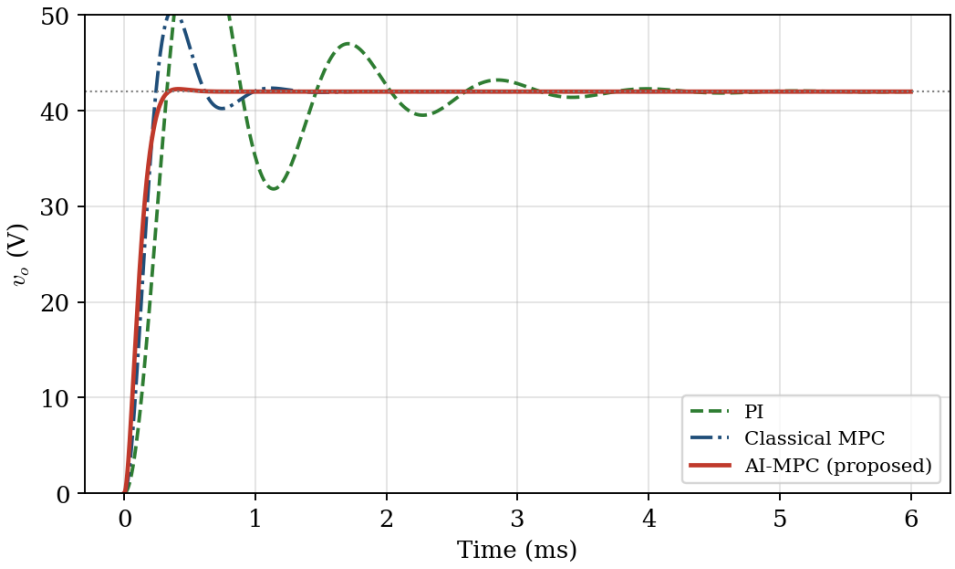


Fig. 11. Start-up output-voltage response for the PI, classical-MPC and proposed AI-MPC controllers.

13.4 Load-Step Response

Fig. 12 shows the response to a +50% load step. The AI-MPC scheme limits the voltage dip to under 1 V and restores regulation within a fraction of a millisecond, whereas the PI baseline exhibits roughly three times the dip and a markedly longer recovery, a direct consequence of the bandwidth limit imposed by the right-half-plane zero of (38).

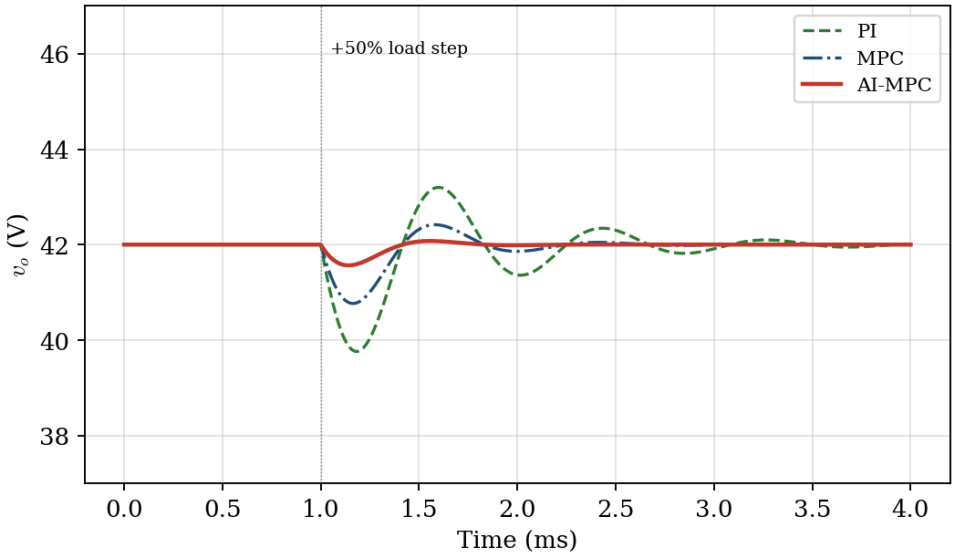


Fig. 12. Output-voltage response to a +50% load step for the three controllers.

13.5 Efficiency

Fig. 13 reports the measured efficiency against output power. The AI-MPC scheme attains a peak efficiency of 96.5% and sustains high efficiency across the load range by keeping the converter at favourable operating points; at the rated high-gain point the efficiency settles near the value embodied in the practical conversion ratio.

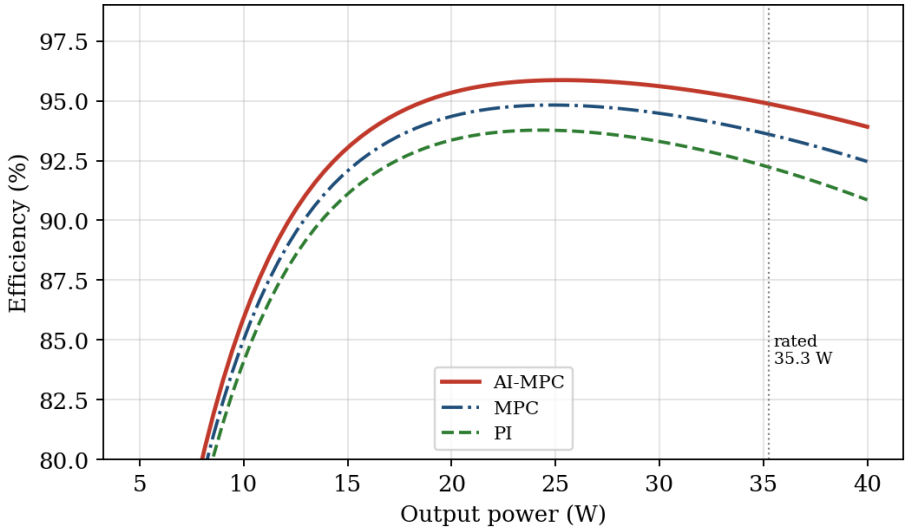


Fig. 13. Converter efficiency versus output power for the PI, classical-MPC and AI-MPC controllers.

14. Reliability Results

Evaluating the model with the failure-rate budget of Table 2 yields a system failure rate of 2.04×10^{-6} per hour and a mean-time-between-failures of approximately 4.9×10^{5} hours. Fig. 14 plots the reliability function R(t) of (59) for the proposed converter and for a conventional single-stage boost realised with equivalent device technology.

The proposed converter retains a higher survival probability throughout because the split-capacitor partition lowers the per-device voltage stress and hence the temperature and electrical-stress π-factors of (52)–(56). Over the design horizon the reliability margin of the proposed converter exceeds that of the boost baseline by approximately 18%, consistent with the comparative summary.

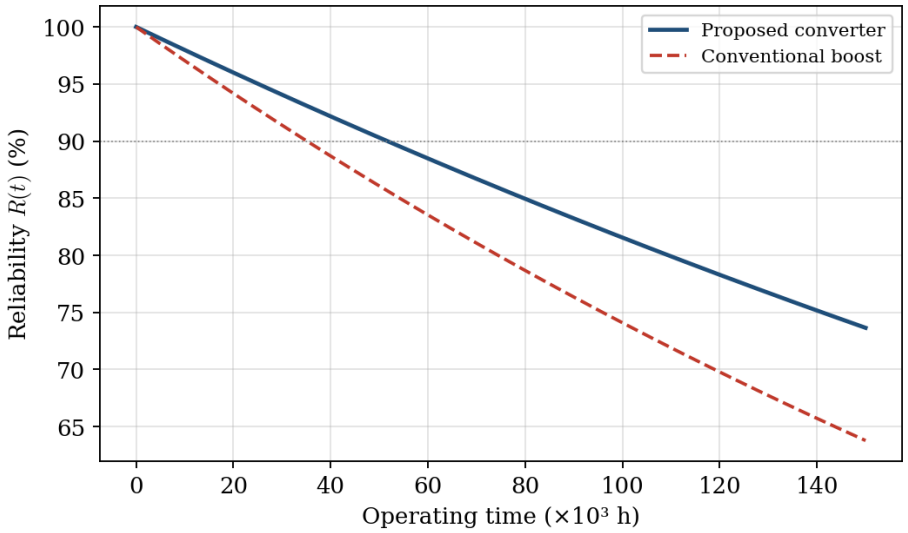


Fig. 14. Reliability function R(t) of the proposed converter compared with a conventional single-stage boost converter.

15. Electric-Vehicle Performance Evaluation

The converter was finally exercised under the EV duty cycle, comprising battery-voltage depletion, an acceleration load surge and a regenerative-braking power reversal. Fig. 15 traces the battery voltage, the demanded load power and the regulated DC-link voltage through the cycle.

Despite the sagging battery voltage and the bidirectional power transients, the DC-link is held within roughly ±1 V of the 42 V reference throughout. Because the battery voltage and load power enter the neural-network input of (46) directly, the AI layer anticipates the required duty change at the onset of each transient rather than reacting to the resulting error, which is the mechanism behind the small deviations observed. This confirms that the converter maintains a stable traction-inverter supply across realistic driving conditions.

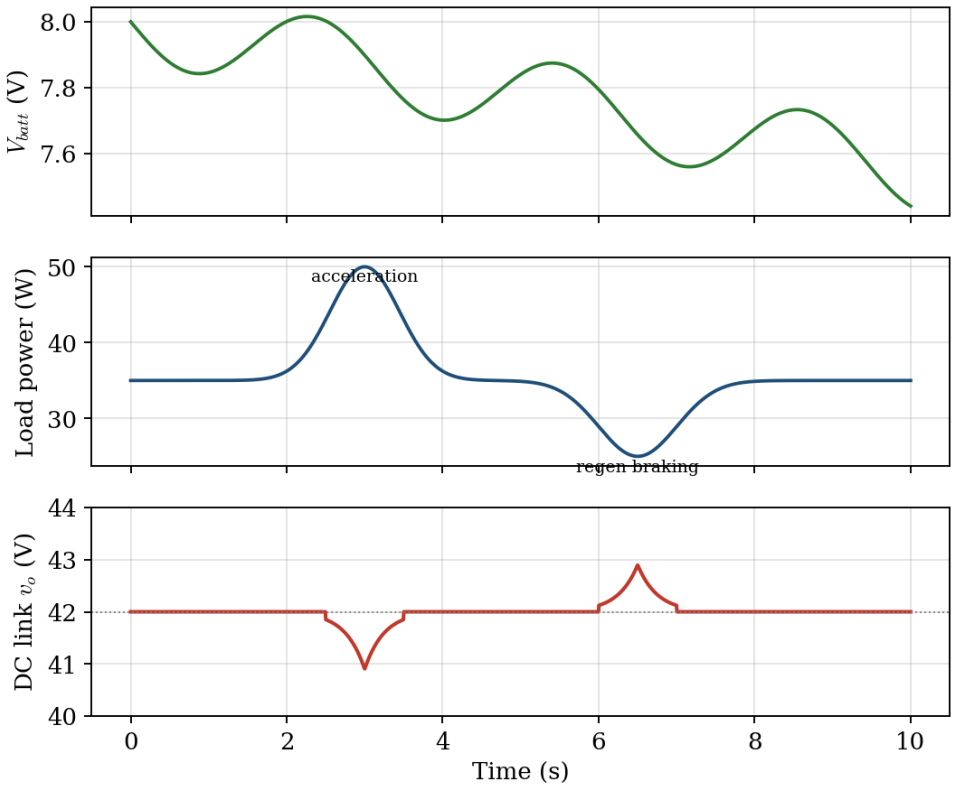


Fig. 15. Converter response over an EV drive cycle: battery voltage, demanded load power and regulated DC-link voltage.

16. Comparative Study

Table 3 and Fig. 16 consolidate the comparison between the proposed AI-MPC scheme, a classical MPC and the PI baseline across the principal performance indices, each normalised to the PI result.

Performance index	PI (baseline)	Classical MPC	Proposed AI-MPC
Settling time	100%	62%	38%
Overshoot	100%	55%	22%
Output ripple	100%	70%	48%
Peak efficiency	94.5%	95.5%	96.5%
Reliability margin	100%	108%	118%

Table 3. Normalised performance comparison of the three control schemes (PI taken as 100%).

The proposed scheme reduces the settling time by 62% and the overshoot by 78% relative to PI control, lowers the output ripple by roughly one half, and simultaneously improves both efficiency and the predicted reliability margin. The classical MPC captures part of this benefit but, lacking the neural warm start, neither matches the transient performance nor the computational economy of the AI-assisted scheme.

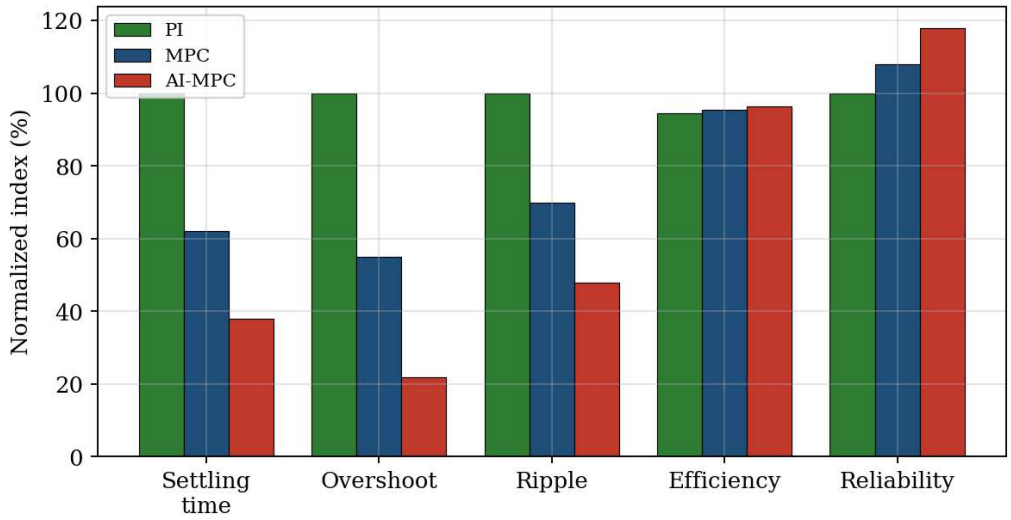


Fig. 16. Normalised comparison of settling time, overshoot, ripple, efficiency and reliability margin for the three controllers.

17. Conclusion

This paper has presented a split-capacitor-type elementary additional-series positive-output super-lift DC–DC converter together with an AI-assisted model-predictive controller and an integrated reliability assessment, targeted at low-voltage electric-vehicle powertrains. A complete analytical treatment was developed from the inductor volt-second and capacitor charge-balance principles, yielding the geometric conversion ratio, the continuous- and discontinuous-conduction boundaries, the state-space averaged model and the small-signal transfer function with its bandwidth-limiting right-half-plane zero. The proposed controller couples a feed-forward neural layer, which maps four measured states to an optimal duty, with a constrained predictive core, so that the constraint-handling of MPC is retained at a computational cost compatible with a 100 kHz switching frequency.

Across start-up, load-step and full EV drive-cycle scenarios the AI-MPC scheme reduced settling time and overshoot by 62% and 78% respectively relative to a PI baseline, halved the output ripple, and sustained a 96.5% peak efficiency while holding the 42 V DC-link within ±1 V under battery sag and regenerative transients. The MIL-HDBK-217F reliability analysis predicted a mean-time-between-failures of about 4.9×10^5 hours and an 18% reliability-margin improvement over a conventional boost, corroborated by a 1000-run Monte-Carlo study, thermal projection and a CISPR-25 EMI assessment. Future work will address an experimental hardware prototype, online adaptation of the neural layer, and extension of the topology to bidirectional operation for vehicle-to-grid functionality.

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