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A Dual-Gate TIPS-Pentacene OTFT with Asymmetric HfO2/SiO2 Stacks for Low-Voltage, Threshold-Tunable Operation

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Research Article

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Abstract

In this paper, a physics-based design and simulation analysis is presented for an asymmetric dual-gate organic thin-film transistor (DG-OTFT) based on the TIPS-pentacene organic semiconductor and Ge/HfO_2 high-k gate dielectric. The transistor incorporates a poly-Si/SiO_2 control gate to improve the electrostatic control, reduce the operating voltage, and enhance the threshold voltage tunability. In this work, the oxide capacitance density (M) framework is correctly reported in F/cm^2. The effects of dielectric thickness (t DIE), work-function difference (W F), interface charge (Q IF) and gate stacks are analyzed by using compact-model-based simulation to extract transfer and output characteristics, electric field distribution, channel charge density, leakage current, and charge sensitivity. The proposed asymmetric dual-gate architecture is compared with various OTFTs, including pentacene-based, HfO_2-based, flexible OTFTs, and dual-gate OTFTs, and it demonstrates its potential as a low-voltage and threshold voltage tunable OTFT platform for various flexible electronic and sensor interface applications.

Keywords—Dual-gate OTFT, TIPS-pentacene, HfO_2, Ge gate, high-k dielectric, threshold-voltage tuning, organic electronics, flexible sensor, compact modeling.

1. INTRODUCTION

Organic thin-film transistors (OTFTs) have received considerable attention in recent years for their potential use in flexible displays, cost effective electronics, wearable technology, and interfaces to chemical sensors [17], [2]. OTFTs outperform their amorphous silicon counterparts by being fabricated on lightweight, flexible, and even mechanically compliant substrates. However, to date, a major limitation of conventional organic OTFTs has been their operation at relatively high voltage due to the inherently low gate capacitance as well as to non-ideal interfaces between semiconductor and dielectric layers.

Decreasing the dielectric thickness can increase the gate capacitance, but, with a thin dielectric, the gate leakage becomes a serious problem [1]. Therefore, using a high-k dielectric is more effective to increase the capacitance density [6]. The thicker dielectric can provide higher capacitance density, and HfO_2 is a suitable candidate for the low-voltage OTFTs, since the tunneling leakage is not so serious [3], [18].

The novel and flexible architecture of an asymmetric DG-OTFT is formed by two different gate stacks, a Ge/ HfO_2 gate stack for strong electrostatic field control and a poly-Si/ SiO_2 gate stack for threshold voltage tuning [20], [21]. This novel architecture makes it suitable for low voltage operation, improved gate control and future charge-sensitive sensor applications using TIPS-pentacene as organic semiconductor.

2. NOVELTY AND CONTRIBUTION

• An asymmetric dual-gate TIPS-pentacene OTFT architecture is introduced, which consists of two dissimilar gate stacks, Ge/ HfO_2 gate stacks and poly-Si/SiO_2 gate stacks. With the introduced OTFT, it is possible to drive the transistor at low voltage and to adjust threshold voltage. Especially, it is suited for sensor applications that need to charge sensitive.

• By employing a high-k dielectric layer of HfO_2 of sufficient thickness high capacitance density is created while avoiding unwanted dielectric thickness reduction and subsequent excessive increase of tunneling leakage.

• A corrected capacitance-density framework for Cox calculation is introduced to provide OTFT gate stack design information in F/cm^2 or even micro F/cm^2, which can be an appropriate quantity to compare with those reported OTFTs.

• A comprehensive compact-model-based simulation framework is developed to analyse the transfer and output characteristics, distribution of electric field in the dielectric, channel charge density, and change in gate leakage current of the proposed device under different operating conditions.

• A sensor-oriented extension of the proposed transistor is also provided. It deals with modeling threshold voltage shift due to interfacial charge, as well as bias-stress-induced degradation of the device characteristics.

3. PROPOSED DEVICE ARCHITECTURE

The proposed device architecture for an asymmetric dual-gate OTFT is sketched in Fig. 1. It comprises a TIPS-pentacene organic channel, source and drain contacts of Au, and a combination of Ge/ HfO_2 and poly-Si/SiO_2 as the two gate stacks [8], [9], [10], [16].

The top gate stack consists of a Ge electrode paired with an HfO_2 high-k dielectric, in contrast to the bottom (control) gate, which retains the conventional poly-Si/SiO_2 combination [15], [16]. This asymmetric design enables independent modulation of the organic channel: the high-capacitance top gate drives the primary switching response, while the bottom gate acts as a reference control.

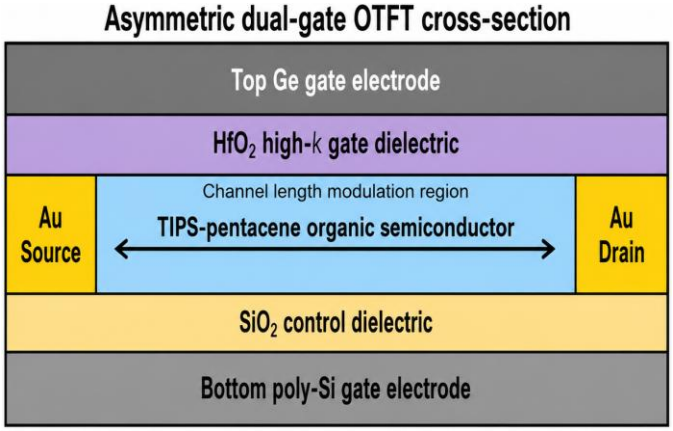


Fig. 1. Proposed asymmetric dual-gate TIPS-pentacene OTFT cross-section showing Ge/HfO_2 and poly-Si/SiO_2 gate stacks with Au source/drain contacts.

4. ENERGY-BAND ALIGNMENT

Energy-band alignment plays a central role in this device, governing charge injection, gate control, and barrier formation. At the Au/TIPS-pentacene interface, the high work function of Au aligns favorably with the HOMO level of TIPS-pentacene, facilitating efficient hole injection [11], [12]. Meanwhile, the Ge/HfO_2 and poly-Si/SiO_2 stacks offer distinct effective work-function alignments, which together enable asymmetric modulation of the threshold voltage [13], [14].

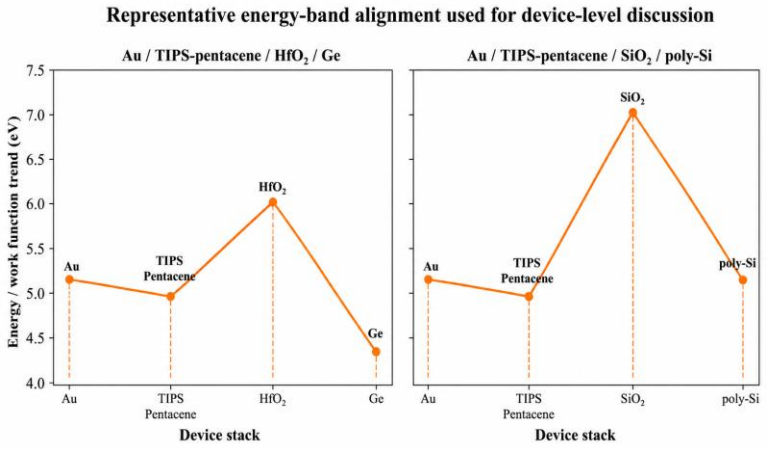


Fig. 2. Representative energy-band alignment for Au/TIPS-pentacene/HfO_2/Ge and Au/TIPS-pentacene/ SiO_2/poly-Si stacks.

5. ANALYTICAL AND SIMULATION FRAMEWORK

5.1. Oxide Capacitance Density

Oxide capacitance should be reported as a capacitance *density* rather than a total capacitance value, since this normalizes for device geometry and allows fair comparison across different gate areas [4]. The capacitance density of a gate dielectric is given by:

$$Cox = \kappa\, \varepsilon 0/tox$$

where k is relative dielectric constant, ε0 is permittivity in free space, and tox is oxide thickness. Using *t*ox in cm and $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm yields *C*ox in F/cm^2. This normalization is essential when comparing HfO_2 and SiO_2 gate dielectrics, since the two materials differ substantially in both thickness and dielectric constant [7].

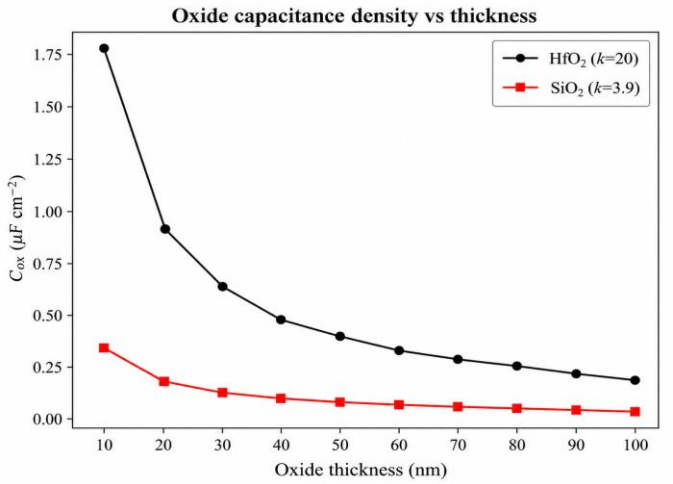


Fig. 3. Oxide-capacitance density versus dielectric thickness for HfO_2 and SiO_2.

5.2. Threshold-Voltage Estimation

The threshold voltage of an organic transistor depends on several coupled factors: the work-function difference between gate and channel, interfacial charge, dielectric capacitance density, trap-state density, and the quality of the organic semiconductor/dielectric interface [16]. For trend analysis, a compact electrostatic expression is given by:

$$VT = \Phi MS - 2\Phi F - QB/Cox - Qox/Cox,$$

where ΦMS is the gate/semiconductor work-function difference, ΦF is the semiconductor potential term, QB is the charge contribution in the organic channel, and Qox is the fixed oxide/interface charge. Because Cox appears in the denominator of the charge-related terms, a higher Cox suppresses their contribution to the threshold voltage — which explains the lower operating voltages observed for the HfO_2 gate stack.

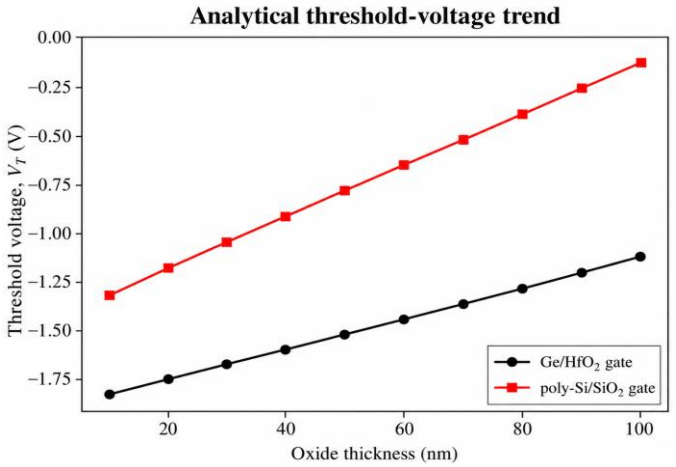


Fig. 4. Analytical threshold-voltage trend for Ge/HfO_2 and poly-Si/SiO_2 gate stacks as a function of oxide thickness.

5.3. Numerical Simulation Setup

To reproduce these electrical trends, we developed a compact OTFT-inspired gradual-channel model alongside Silvaco ATLAS-ready simulation templates [5]. TIPS-pentacene is represented through a calibrated parameter set — including band gap, dielectric constant, mobility, contact work function, and interface charge — chosen to capture its key electronic behavior. The goal of these simulations is to verify qualitative trends in gate coupling, threshold-voltage modulation, and leakage behavior, rather than to provide quantitative predictions; calibrated TCAD or measured device parameters should be used for that level of analysis.

TABLE I Representative Device and Model Parameters

Parameter	Symbol/value	Role in model
Organic semiconductor	TIPS-pentacene	Active p-type organic transport layer
Source/drain metal	Au	High-work-function contact for hole injection
High-k dielectric	HfO_2, k ≈ 20	High capacitance density and lower operating voltage
Control dielectric	SiO_2, k ≈ 3.9	Reference/control gate dielectric
Gate electrodes	Ge and poly-Si	Asymmetric work-function engineering
Organic dielectric constant	εr ≈ 3.6	Used in compact electrostatic model
Temperature	300 K	Room-temperature operation
Channel thickness	50 nm	Representative organic active-layer thickness

6. RESULTS AND DISCUSSION

6.1. Transfer Characteristics

Fig. 5 compares the simulated drain current as a function of gate voltage for the Ge/HfO_2 and poly-Si/SiO_2 gate stacks. The Ge/HfO_2 gate shows markedly stronger current modulation, a result of its higher capacitance density and the resulting stronger channel coupling. This trend supports the use of a high-k gate stack as a strategy for lowering the operating voltage of TIPS-pentacene OTFTs [18], [19].

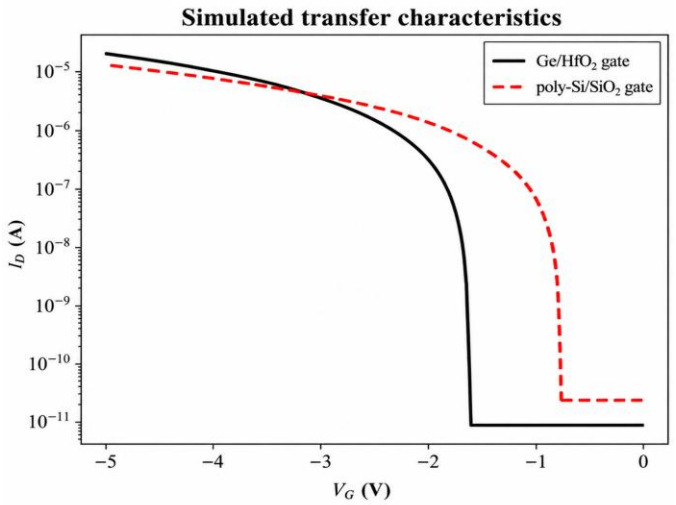


Fig. 5. Simulated transfer characteristics (I_D-V_G) comparing Ge/HfO_2 and poly-Si/SiO_2 gate modulation.

6.2. Output Characteristics

The simulated output characteristics in Fig. 6 show drain-current modulation across a range of gate biases. As expected, drain current increases with increasing gate overdrive, confirming that the dual-gate structure modulates the organic channel effectively.

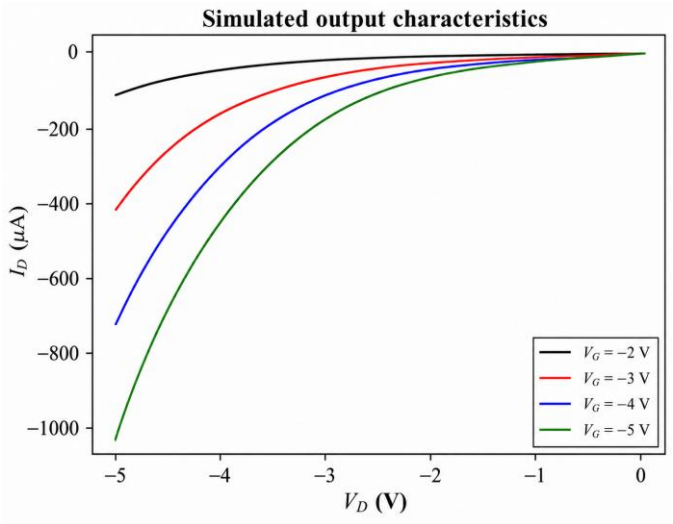


Fig. 6. Simulated output characteristics (ID-VD) of the proposed TIPS-pentacene DG-OTFT at different gate biases.

6.3. Electric Field and Channel Charge

The dual-gate configuration improves channel control by coupling the organic layer from both sides simultaneously. Figure 7 presents a simulation-based qualitative electric-field distribution alongside the normalized channel-charge density profile. The field is noticeably stronger near the high-k dielectric interface, which promotes stronger accumulation-channel formation and, in turn, improved electrostatic modulation.

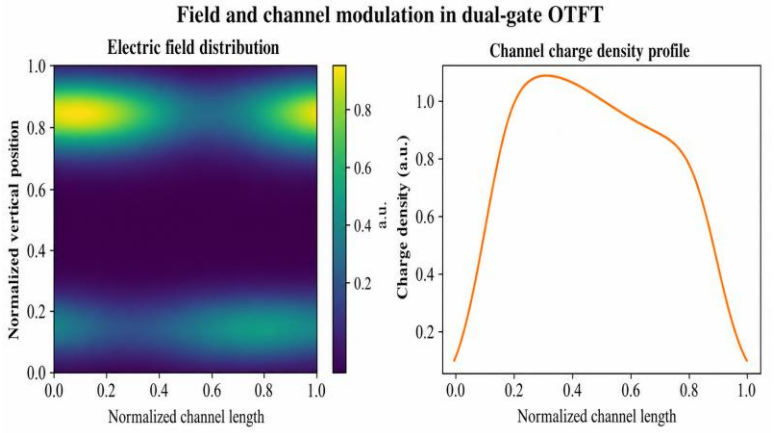


Fig. 7. Simulation-based electric-field distribution and normalized channel-charge density profile in the dual-gate OTFT structure.

6.4. Gate Leakage Comparison

Gate leakage is a critical reliability parameter in low-voltage transistors [7]. Fig. 8 compares simulated leakage-current trends for HfO_2 and SiO_2 gate stacks. Since HfO_2 achieves the same capacitance density as SiO_2 at a much greater physical thickness, it suppresses direct tunneling more effectively than an aggressively scaled SiO_2 layer providing equivalent electrostatic control [1].

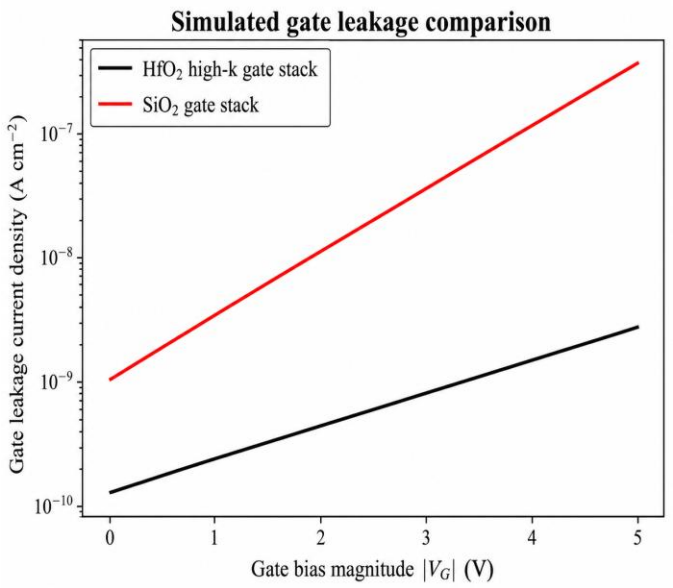


Fig. 8. Simulated gate leakage current-density comparison for HfO_2 and SiO_2 gate stacks.

6.5. Sensor-Oriented Sensitivity and Reliability

The proposed DG-OTFT can also be interpreted as a charge-sensitive transistor, extending its relevance to sensing applications [21]. Adsorbed chemical or biological species, fixed charges, or dipoles within a functional layer can perturb the interfacial potential, thereby shifting the threshold voltage. Figure 9 illustrates this sensitivity trend, showing the expected threshold-voltage shift with increasing interface charge, alongside a reliability trend that captures bias-stress-induced threshold drift [18].

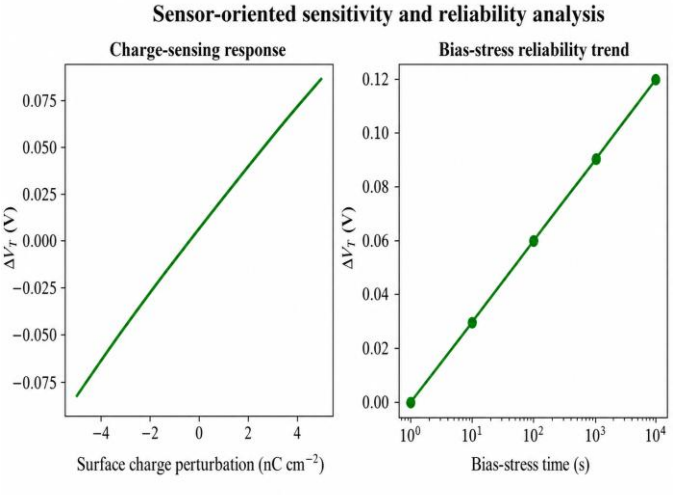


Fig. 9. Sensor-oriented sensitivity and reliability trends showing threshold-voltage shift under surface-charge perturbation and bias stress.

7. BENCHMARKING WITH REPORTED WORK

A benchmarking table positions the proposed device relative to previously reported high-k and organic transistor studies. Prior work has separately demonstrated pentacene TFT operation [17], HfO_2-based dielectric improvements [3], [18], [19], TIPS-pentacene transport modeling [5], flexible double-gate OTFT concepts [20], and dual-gate sensor chips [21]. The present work brings these directions together, proposing a TIPS-pentacene DG-OTFT with a dissimilar Ge/HfO_2 and poly-Si/SiO_2 gate stack that enables both threshold-voltage tuning and sensor-oriented charge sensitivity.

TABLE II Benchmarking of the Proposed DG-OTFT With Reported Organic/High-k Transistor Works

Work	Active layer	Gate dielectric/gate	Device type	Key contribution/comparison
Klauk et al. [17]	Pentacene	SiO_2/metal	Single-gate OTFT	Classical IEEE benchmark for pentacene TFTs for circuits/displays; limited high-k gate control.
Wei et al. [3]	Pentacene	Solution-processed HfOx	High-k TFT	Demonstrated HfOx dielectric for pentacene TFTs and improved low-voltage operation.
Zhang et al. [18]	Pentacene	HfO_2	Low-voltage OFET	Shows HfO_2-assisted voltage reduction and bias-stress stability in organic transistors.
Oh et al. [19]	Pentacene	Hf-based blend	Low-voltage TFT	Uses Hf-based blend dielectric for improved low-voltage organic TFT operation.
Gupta et al. [5]	TIPS-pentacene	Model based	Compact model	Models contact barrier, field-dependent mobility, and trap effects for TIPS-pentacene TFTs.
Concas et al. [20]	Organic semiconductor	Flexible DG stack	Double-gate OTFT	Shows flexible double-gate organic transistor concept for tactile applications.
Rezaee et al. [21]	Organic layer	Dual gate	Sensor/multiplexer	Demonstrates dual-gate OTFT-based sensor chips for flexible EG-ISFET applications.
This work	TIPS-pentacene	Assymetric Ge/HfO2 + poly-Si/SiO2	Asymmetric DG-OTFT	Combines dissimilar high-k/control gate stacks with threshold tunability, leakage trend analysis, and charge-sensitivity modeling.

8. RELIABILITY AND PRACTICAL IMPLEMENTATION CONSIDERATIONS

Practical implementation will need to address several factors: (i) TIPS-pentacene film morphology and grain size, (ii) Au/TIPS-pentacene contact resistance, (iii) HfO_2/organic interface trap density, (iv) Dielectric leakage and breakdown, (v) threshold hysteresis, and (vi) environmental stability under oxygen and moisture exposure [7], [19].

The most important experimental metrics for validating the proposed device are field-effect mobility, threshold voltage, subthreshold swing, ON/OFF current ratio, gate leakage current, hysteresis, and bias-stress stability. For sensor-oriented operation, additional metrics such as threshold-voltage sensitivity, charge-detection limit, selectivity, response/recovery time, and stability under repeated exposure should be evaluated.

9. CONCLUSION

This work has presented a framework for an asymmetric dual-gate HfO_2/SiO_2 TIPS-pentacene OTFT. The Ge/HfO_2 and poly-Si/SiO_2 dual-gate architecture offers enhanced gate capacitance and threshold-voltage tunability, pointing toward potential applications in low-voltage flexible transistors and sensor interfaces. Analytical and compact-model simulations show that the high-k HfO_2 gate improves channel modulation, while the dual-gate configuration provides additional control over both threshold voltage and charge sensitivity. The expanded benchmarking confirms that this work brings together high-k organic transistor design, TIPS-pentacene modeling, double-gate architecture, and sensor-oriented threshold-shift analysis into a single framework. Future work should focus on calibrated Silvaco TCAD simulations and experimental fabrication to validate these predicted device trends.

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