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An Improved Switched-Inductor-Capacitor Z-Source Inverter with Enhanced Boost Capability and Reduced Voltage Stress

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Abstract: This paper proposes an improved switched-inductor/capacitor Z-source inverter (ISLC-ZSI) with enhanced boosting capability for single-stage DC–AC conversion in low-voltage renewable energy systems. The impedance network is derived from the improved switched-inductor Z-source inverter by replacing the central diode of the switched-inductor cell with a capacitor and reconfiguring the network to maintain continuous input current. This modification provides a high boost factor at a relatively small shoot-through interval, enabling operation over a wider modulation range. In addition, the ISLC-ZSI alleviates the electrical stress imposed on capacitors, diodes, and active switches compared with representative high-gain Z-source and switched-inductor-based topologies a unified ground path between the DC input source and the DC-link stage is also preserved, providing an advantageous feature for renewable-energy interfaces. The operating modes and steady-state characteristics are analyzed, and analytical expressions for the boost factor, voltage gain, and component voltage stresses are established. A comprehensive comparison with recently reported impedance-source inverters is conducted in terms of component count, boosting performance, voltage gain, input-current continuity, and device stresses. Finally, simulation and prototype experimental results validate the theoretical findings and confirm the effective operation and practical feasibility of the proposed ISLC-ZSI topology under representative operating conditions.

Keywords: Impedance-Source Inverter, Switched-Inductor Cell, High boosting Capability, Shoot-Through Interval, Continuous Input Current, Electrical Stress, PWM method control, Improved Z-Source Inverter.

1. Introduction

The growing demand for clean, reliable, and highly efficient energy-conversion systems has significantly accelerated the integration of renewable and distributed power sources, including photovoltaic modules, fuel cells, and other low-voltage DC energy resources [1-7]. These sources are attractive because of their low environmental impact, modularity, and suitability for decentralized generation. However, many renewable DC sources, particularly photovoltaic modules and fuel-cell stacks, provide a relatively low and widely varying output voltage. Therefore, an efficient power-conversion interface with voltage-boosting capability is required to supply AC loads or grid-connected inverters [8-9].

Conventional voltage-source inverters are widely used for DC-AC conversion. Consequently, the obtainable AC-side voltage is restricted by the DC-link voltage supplied to the inverter stage, while the input voltage cannot be inherently boosted without additional conversion stages or auxiliary circuitry. Therefore, in systems where the available DC input voltage falls below the required AC output level, an additional front-end step-up DC-DC conversion stage is typically introduced. However, this two-stage configuration increases component count, cost, system volume, and control complexity while reducing the overall conversion efficiency. Furthermore, a key limitation of conventional voltage-source inverters is their exposure to shoot-through faults, where simultaneous conduction of the upper and lower switches in the same phase leg can impose destructive short-circuit conditions on the inverter bridge [10-11].

Originally developed by Peng, the Z-source inverter (ZSI) enables integrated single-stage DC-AC power conversion with voltage buck-boost functionality through the integration of an X-type impedance network between the DC supply and the inverter-bridge stage [12]. In contrast to traditional voltage-source inverter structures, the ZSI exploits controlled shoot-through intervals as part of its normal operation to achieve DC-link voltage boosting, thereby enhancing system reliability and eliminating the requirement for dead time. Owing to these advantages, Z-source and other impedance-source inverter topologies have been extensively investigated for renewable-energy systems, including photovoltaic generation [13-15], fuel-cell systems [1] and refernce [4], wind-energy conversion [16], and uninterruptible power supplies [17].

Despite these advantages, the classical ZSI suffers from several drawbacks, including discontinuous input current, limited boost capability, and relatively high voltage stress on passive and semiconductor components. To address these limitations, various modulation-based switching control strategies considerable research efforts have focused on to improve the boost factor, mitigate voltage stress on power devices, and achieve more effective regulation of the shoot-through interval [18-23]. Although these modulation techniques address the performance of the classical ZSI to some extent, the achievable voltage gain remains limited. This feature is especially advantageous in operating conditions that require a high modulation index while maintaining a low shoot-through interval [24-25].

To address the input-current discontinuity associated with the classical ZSI, the quasi-Z-source inverter was introduced as an improved impedance-source configuration [26]. Compared with the classical ZSI, the qZSI offers continuous current flow at the input side and alleviates the electrical stress across one of its capacitors without compromising the attainable boost factor. Several modified qZSI-based structures have subsequently been reported to improve voltage gain, reduce inrush current, and enhance the suitability associated with impedance-source inverter configurations for clean-energy applications [27-30]. In addition, advanced Z-source inverter variants, including enhanced Z-source, switched inductor-based Z-source, improved switched-inductor cells Z-source, and LC-network-assisted Z-source topologies have been developed to enhance the boosting factor and mitigate electrical stress [31-33]. However, many of these topologies still require a relatively large shoot-through interval to obtain high voltage capability, or they impose high electrical stress on capacitors, diodes, and switches. In certain configurations, the enhanced voltage-boosting capability is obtained albeit with added circuit components and increased implementation complexity, discontinuous input current, or the elimination of the unified ground reference linking the input side to the inverter-bridge stage.

To address these limitations, a modified switched-inductor-capacitor cells Z-source inverter configuration with enhanced voltage-boosting capability is introduced in this work. The proposed topology is obtained by replacing the middle diode of the improved switched-inductor based cell with a capacitor and rearranging the impedance network. This simple structural modification leads to a considerably improved boost capability while maintaining a low shoot through interval. Furthermore, with the proposed configuration, continuous input current operation is achieved, while the electrical stress across the capacitors and diodes is reduced and the topology is maintained ground-reference continuity with the input DC source.

The primary technical contributions presented in this work can be summarized as follows:

✓This work introduces an enhanced switched-inductor/capacitor-based Z-source impedance network aimed at achieving high voltage-boosting capability in a single-stage DC–AC conversion structure;

✓Using the proposed topology, a small shoot-through duty ratio results in enhanced boost gain, allowing a high modulation index to be achieved;

✓The continuous input-current feature of the proposed topology enables it to be suitable for low voltage clean-energy sources, including photovoltaic modules and fuel cells;

✓Comparable to high-boost impedance-source topologies, capacitors, diodes, and inverter bridge switches suffer less voltage stress;

✓The DC-link and input DC source operate on common ground in the proposed inverter.
A comprehensive validation framework, including analytical derivations, comparative benchmarking, simulation investigations, and experimental testing, is contributed to substantiate the validity and operational capability of the developed topology.

The remaining sections of this paper are structured as follows. Section 2 presents a detailed description of the proposed ISLC-ZSI topology and its operating principles, including the boost factor, voltage gain, and voltage stresses. Section 3 designs the passive components, inductors and cpapacitors. Section 4 provides a comparative study with existing impedance-source inverter topologies. The simulation-driven and prototype-based assessments are discussed in Section 5, and the main conclusions are drawn in Section 6.

2. The Proposed structure

This proposed structure integrates two designs: the SL-IZSI [26] and the new q-ZSI [29], as shown in Fig. 1. The power-circuit architecture of the proposed structure is illustrated in Fig. 2.a. The proposed structure consists of six diodes, three capacitors, and four inductors. As depicted in Fig. 1, this structure is based on the improved switched-inductor-cell Z-source inverter configuration [32] and the recently presented q-ZSI [36]. In the proposed design, the middle diode in improved switched ZSI [32] is replaced with a capacitor in one of the switched inductor cells, based on the concept of switched capacitors discussed in the reference [36]. This modification results in an enhanced boosting coefficient. It is assumed that the inductors have equal values, while the capacitors have unequal values.

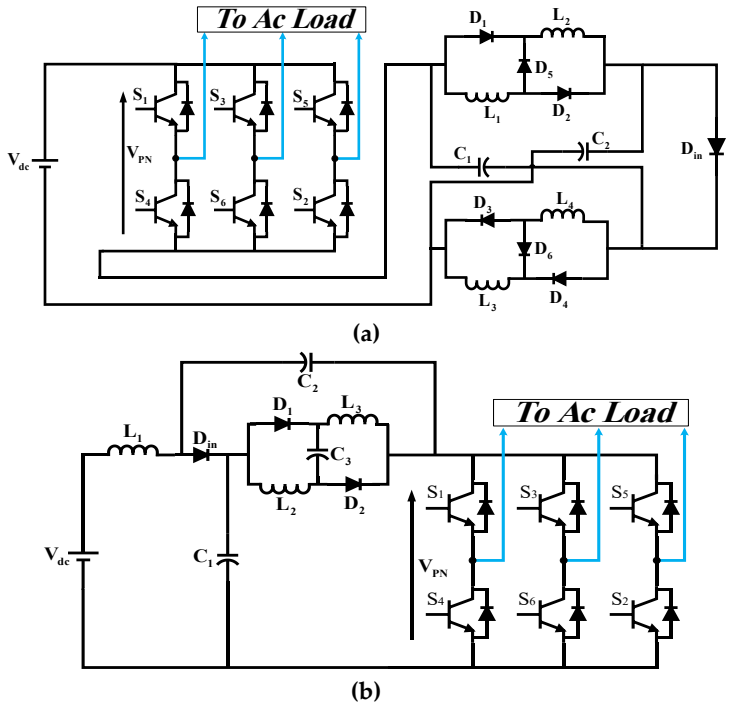


Figure 1. Basic structures (a) SL-IZSI [32], (b) recently presented qZSI [36]

Fig. 2.a depicts the power-stage configuration of the switched-inductor-capacitor cells Z-source inverter configuration. The topology is developed by the single switched-inductor ZSI presented in reference15 and incorporates 3 inductors, 4 capacitors, and 2 diodes. Compared with earlier impedance-source inverter structures, the proposed configuration offers enhanced voltage boosting capability and lower component-level voltage stress. The suggested switched capacitor inductor cells q-ZSI is depicted in Fig 2.a. The control method of a simple boost is used to control this inverter based on usual modulation strategies [30]. In addition, the capacitors' capacities and inductors' inductances are considered equal.

2.1. Operating analysis

Analyzing the operational modes of the suggested inverter is in the form of a classic Z-source inverter. To analyze the operating states, they are streamlined into two categories: ST and Non ST modes. The proposed inverter configuration in states of ST and non-ST is demonstrated in Figs 2.b and 2.c.

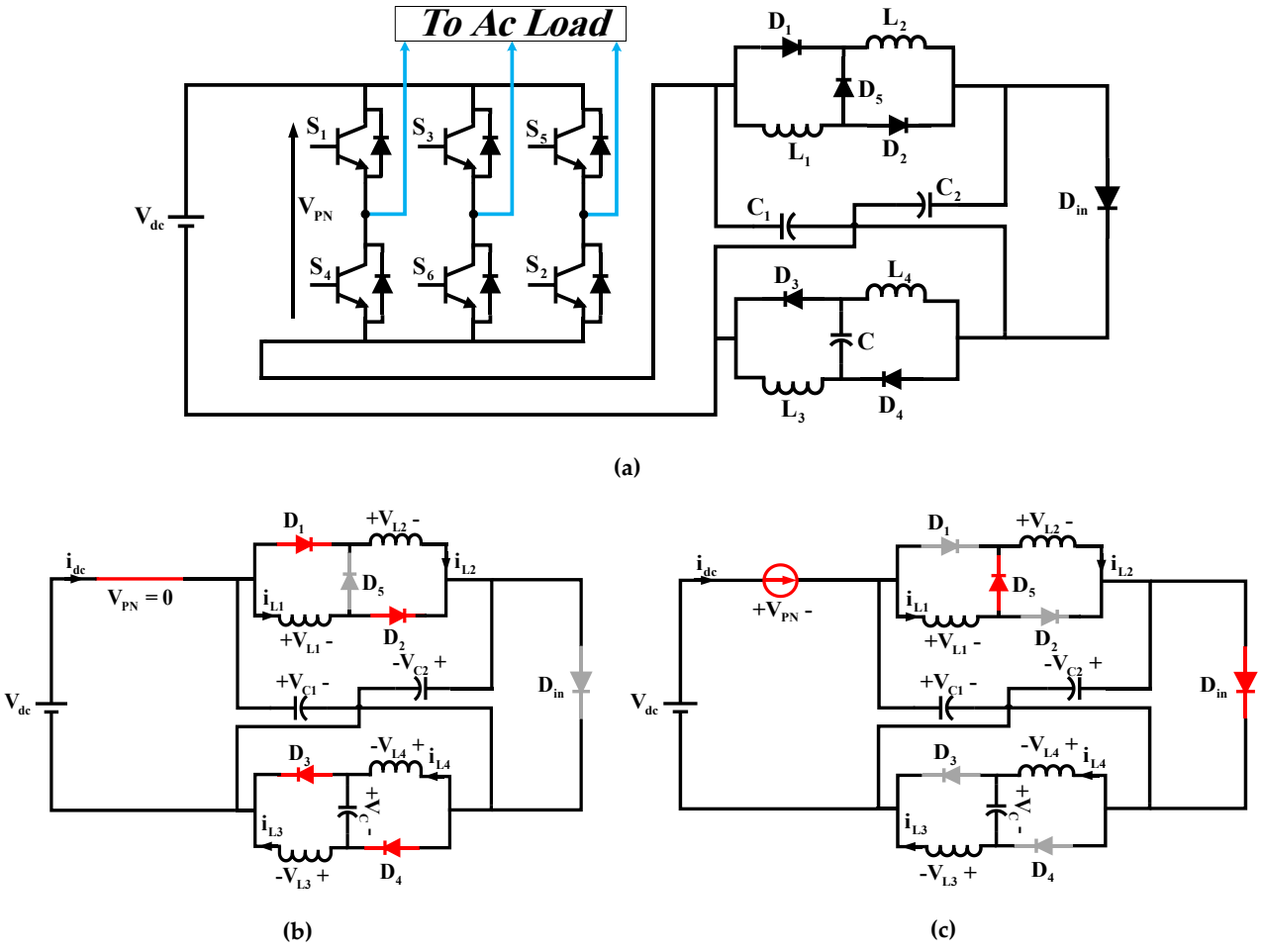


Figure 2. a) Topology of the proposed inverter and its equivalent circuit model under (b) ST state, and (c) Non-ST state

2.1.1. ST state

In ST mode, the switches on each leg (phase) are turned on simultaneously. As illustrated in Figure 2.b, the DC-link is short-circuited. In this case, the diodes D_{in} and D_2 energy are transferred from the capacitors to the inductors. Assuming v_{L1} and v_{L3} are equal to v_{L2} andv_{L4}, respectively. In this case, we obtain four voltage values for the inductors (v_{L1}, v_{L2}, v_{L3}, and v_{L4}) and three voltage values for the capacitors:

$$v_{L1-ST} = V_{C2} + V_{dc} \quad (1)$$

$$v_{L3-ST} = V_C \quad (2)$$

$$v_{L3-ST} + v_{L4-ST} = V_C + V_{C1} - V_{dc} \quad (3)$$

$$i_{C1} = 2I_L - I_{in} \tag{4}$$

$$i_{C2} = -2I_L \tag{5}$$

$$i_C = 2I_{L1} - 2I_L + I_{in} \tag{6}$$

Where I_L and I_{L1} are the average current of inductors (L_1, L_3).

In this case, the corresponding DC-link voltage is derived as:

$$V_{PN} = V_i = 0 \tag{7}$$

2.1.2. Non-ST state

Fig. 2.c illustrates the simplified circuit model of the proposed inverter under the non-shoot through operating condition. Under this condition, D_{in} and D_2 conduct. Under this condition, simultaneous conduction of the two switches in a given phase leg is avoided. Accordingly, the capacitors are energized during this interval, while the inductors release part of their stored energy. The dynamic equations of the inverter in this condition are written as below:

$$v_{L1-nST} + v_{L2-nST} = -V_{C1} \tag{8}$$

$$v_{L3-nST} + v_{L4-nST} = V_{C2} + V_C \tag{9}$$

$$v_{L3-nST} + v_{L4-nST} = V_i - V_{C1} - V_{dc} \tag{10}$$

$$i_{C1} = I_L - I_{PN} \tag{11}$$

$$i_{C2} = I_{L1} - I_{PN} \tag{12}$$

$$i_C = I_{L1} \tag{13}$$

$$V_{PN} = V_i \tag{14}$$

2.2. Boosting factor calculation

Based on the volt–second balance criterion for the inductors implies that the net inductor voltage averaged over a complete switching cycle must be zero, which yields:

$$v_{L-ST} DT_s + v_{L-nST} (1-D)T_s = 0 \tag{15}$$

Based on the equations (1) and (8) for inductors of L_1 and L_2, we have:

$$2(V_{C2} + V_{dc})DT_s - V_{C1}(1-D)T_s = 0 \tag{16}$$

Based on the equations (2), (3), and (9) for inductors of L_3 and L_4, we have:

$$(2V_C)DT_s + (V_{C2} + V_C)(1-D)T_s = 0 \tag{17}$$

$$(V_C + V_{C1} - V_{dc})DT_s + (V_{C2} + V_C)(1-D)T_s = 0 \tag{18}$$

Thus, by solving equations (16), (17), and (18):

$$V_{C1} = \frac{(1+D)^2}{1-4D-D^2} V_{dc} \tag{19}$$

$$V_{C2} = \frac{4D}{1-4D-D^2} V_{dc} \tag{20}$$

$$V_C = \frac{(1-D^2)}{1-4D-D^2}V_{dc} \tag{21}$$

Consequently, the DC-link voltage (V_i) is:

$$V_i = \frac{2(1+D)}{1-4D-D^2}V_{dc} \tag{22}$$

Subsequently, the boosting coefficient (B) of the suggested ZSI is able to be calculated as below:

$$B = \frac{V_i}{V_{dc}} = \frac{2(1+D)}{1-4D-D^2} \tag{23}$$

Moreover, the AC voltage phase and the AC voltage line-to-line are expressed by:

$$V_{AC-Phase} = B\left(\frac{MV_{dc}}{2}\right) = \frac{(1+D)MV_{dc}}{1-4D-D^2} \tag{24}$$

$$V_{AC-Line} = \sqrt{3}V_{AC-Phase} = \frac{\sqrt{3}(1+D)MV_{dc}}{1-4D-D^2} \tag{25}$$

Accordingly, the boosting voltage capability (G) achieved by the proposed Z-source inverter is derived as follows:

$$G = M.B = \frac{2(1+D)M}{1-4D-D^2} \tag{26}$$

2.3. Current ripple analysis

The voltage applied to the inductor L is determined by:

$$v_L = L\frac{di_L}{dt} \tag{27}$$

$$\frac{di_{L1-ST}}{dt} = \frac{V_{C2}+V_{dc}}{L_1} \tag{28}$$

Two ST modes are produced by the control technique of the simple boost during each switching cycle T_s, and the inductor current increases at interval ($\frac{DT_s}{2}$). Hence, the ripple of the current during the ST state is able to be found as follows:

$$di_{L1-ST} \approx \left(\frac{V_{C2}+V_{dc}}{L_1}\right)\frac{DT_s}{2}$$

$$\Delta i_{L1-ST} = \Delta i_{L2-ST} = \frac{D(1-D^2)T_s}{2(1-4D-D^2)L_1}V_{dc} \tag{29}$$

Furthermore, in the non-ST mode, the ripple of current of the inductor is able to be calculated using equations (8), (19), and (27):

$$\Delta i_{L1-nST} = \Delta i_{L2-nST} = \frac{-D(1-D^2)T_s}{2(1-4D-D^2)L_1}V_{dc} \tag{30}$$

Using the same method, the ripple of the current of the other inductors in both the ST and non-ST states is obtained as below:

$$\Delta i_{L3-ST} = \Delta i_{L4-ST} = \frac{(1-D^2)T_s}{2(1-4D-D^2)L_3}V_{dc} \tag{31}$$

$$\Delta i_{L3-nST} = \Delta i_{L4-nST} = \frac{-(1-D^2)T_s}{2(1-4D-D^2)L_3} V_{dc} \tag{32}$$

2.4. Voltage ripple analysis

The current flowing through a capacitor C can be written as below:

$$i_C = C\frac{dv_C}{dt} \tag{33}$$

From equations (8) and (33):

$$\frac{dv_{C1-ST}}{dt} = \frac{2I_L - I_{dc}}{C_1} \tag{34}$$

According to the control technique of the simple boost, the capacitor voltage ripple in the ST state is obtained as below:

$$dv_{C1-ST} = \frac{(2I_L - I_{dc})}{C_1}\frac{DT_2}{2} \tag{35}$$

Applying the charge-balance condition to the capacitors requires the net capacitor current averaged over a complete switching cycle to be zero, which gives:

$$i_{C-ST}DT_s + i_{C-nST}(1-D)T_s = 0 \tag{36}$$

From (4) and (11):

$$(2I_L - I_{dc})DT_s - 2I_L(1-D)T_s = 0 \tag{37}$$

According to the relationships (5), (6), and (12):

$$-2I_L DT_s + (I_{L1} - I_{PN})(1-D)T_s = 0 \tag{38}$$

Therefore, the average current of the inductors can be calculated by solving (37) and (38) as follows:

$$I_L = \frac{2(1-D)}{1-5D^2} I_{PN} \tag{39}$$

$$I_{L1} = \frac{(1+5D)(1-D)}{1-5D^2} I_{PN} \tag{40}$$

And,

$$I_{PN} = \frac{I_{dc}}{G} \tag{41}$$

From equations (35), (39), and (41), the ripple of the voltage of the C_1 during ST mode is expressed by:

$$\Delta v_{C1-ST} = \frac{D(1-9D+3D^2+5D^3)T_s}{2C_1(1-5D^2)(1+D)} I_{dc} \tag{42}$$

Taking R as output load, we have:

$$I_{dc} = G.I_{PN} = \frac{G(1-D)V_i}{R} \tag{43}$$

Moreover, the voltage ripple of C_1 during non-ST mode is derived using (14), (35), and (41):

$$\Delta v_{C1-nST} = \frac{-D(1-9D+3D^2+5D^3)T_s}{2C_1(1-5D^2)(1+D)} I_{dc} \tag{44}$$

Using the same technique, the voltage ripple of the other capacitors during the ST and non-ST states is obtained as follows:

$$\Delta v_{C2-ST} = \frac{-D(1-D)(1-4D-D^2)T_s}{C_2(1-5D^2)(1+D)} I_{dc} \tag{45}$$

$$\Delta v_{C2-nST} = \frac{D(1-D)(1-4D-D^2)T_s}{C_2(1-5D^2)(1+D)} I_{dc} \tag{46}$$

$$\Delta v_{C-ST} = \frac{D(1+5D)(1-D)(1-4D-D^2)T_s}{2C(1-5D^2)(1+D)} I_{dc} \tag{47}$$

$$\Delta v_{C-nST} = \frac{-D(1+5D)(1-D)(1-4D-D^2)T_s}{2C(1-5D^2)(1+D)} I_{dc} \tag{48}$$

3. Design considerationsfor inductors and capacitors

In the proposed ZSI, the capacitors are sized by considering the allowable voltage ripple across each capacitor, which can be formulated as follows:

$$v_C\,\% = \frac{\Delta v_C}{V_C} \times 100 \tag{49}$$

Accordingly, from (23), (42), (43), and (49), the value of C_1 is obtained as follows:

$$C_1 = \frac{D(1-9D+3D^2+5D^3)}{2f_s v_C\,\%(1-5D^2)(1+D)V_{C1}} I_{dc} \times 100 \tag{50}$$

In the same way, the values of C_2 and C are derived as follows:

$$C_2 = \frac{D(1-D)(1-4D-D^2)}{f_s v_{C\%}(1-5D^2)(1+D)V_{C2}} I_{dc} \times 100 \tag{51}$$

$$C = \frac{D(1+5D)(1-D)(1-4D-D^2)}{2f_s(1-5D^2)(1+D)} I_{dc} \times 100 \tag{52}$$

Also, the inductors are sized by considering the permissible current ripple in each inductor, which can be formulated as follows:

$$i_L\,\% = \frac{\Delta i_L}{I_L} \times 100 \tag{53}$$

From (29), (31), (39), (40), (43), and (53), accordingly, the inductance required for each inductor is determined by:

$$L_1 = L_2 = \frac{D(1-5D^2)}{4f_s i_L\,\%(1-D)^2 I_{dc}} \times 100 \tag{54}$$

$$L_3 = L_4 = \frac{D(1-5D^2)}{4f_s i_L\,\%(1+5D)(1-D) I_{dc}} \times 100 \tag{55}$$

4. Comparison evaluation

In this section, the impedance network of the proposed structure is compared with seven previous topologies: SLZSI [34], SL-IZSI [32], EBZSI [37], EB-QZSI [38], embedded dual switched-capacitor ZSI [40], voltage-lift-type ZSI [41], and a novel topology of switched-inductor/capacitor ZSI [42]. Table 1 presents a comprehensive comparison of the suggested topology characteristics with recently reported structures in terms of the quantity of elements, the capacitor's voltage stress, gain voltage, input current, and boosting capability. As can be seen, the total quantity of both passive and active elements in the suggested topology is identical to most of the previous structures, except for structures reported in the references [40] and [42]. It is also deduced from Table 1 that the proposed topology configuration is able to contribute a continuous current in the input. The evaluation of the proposed topology's performance relies heavily on the boosting factor. Fig. 3 visualizes the comparison of different topologies. As illustrated in Fig. 3.a, the boosting factor of the proposed topology is significantly more extensive than other structures. Hence, it is a suitable candidate for interfacing the renewable energy sources with low output voltage. The variation of buck-boost factor versus M in different topologies is illustrated in Fig. 3.b. As can be observed, the suggested topology has surpassed voltage gain. As shown in Fig.3.c, the proposed strategy offers lower electrical stress on the diodes compared to the other structures, with the exception of SL-ZSI [34]. Based on Fig. 3.d, the suggested topology exhibits much lower overall voltage stress on capacitors compared to structures EB-QZSI [38], [41], and [42]. Nevertheless, the voltage stress across capacitors EBZSI [37], SL IZSI [32], and SL-ZSI [34] is lower than the proposed configuration.

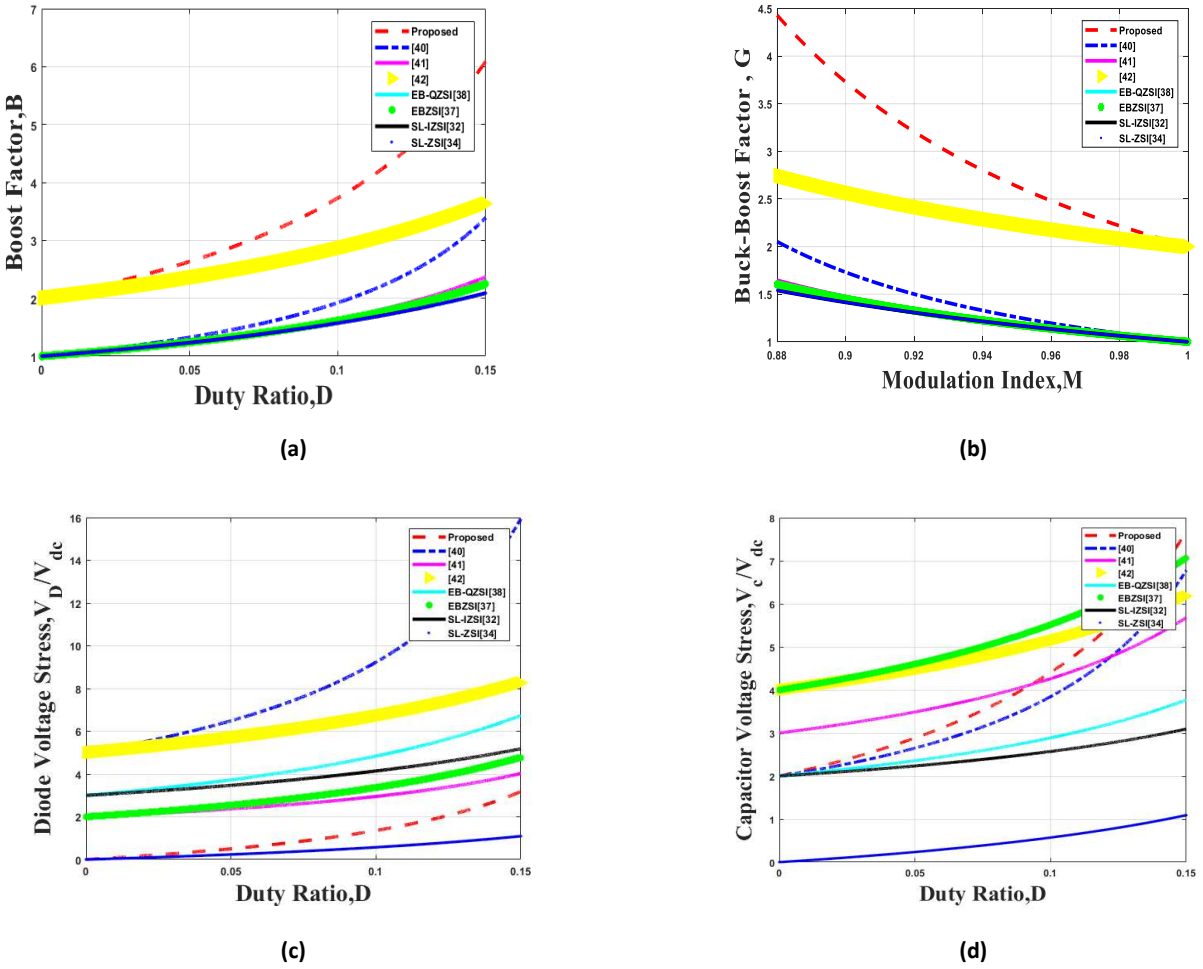


Figure 3. A performance comparison between the proposed topology and representative existing structures, (a) the boosting coefficient, (b) the gain voltage, (c) electrical stress across diodes, and (d) electrical stress on capacitors

5. Power-conversion efficiency analysis

To accurately determine the energy-conversion efficiency achieved by the proposed configuration, a comprehensive evaluation of all loss mechanisms is essential. Given that parasitic resistances have a substantial impact on the performance and overall efficiency of power converters, each component of power loss within the converter must be rigorously identified, considered, and quantified. The total power loss of a converter comprises several components, including switch losses (consisting of both conduction and switching losses), diode losses, inductor losses, and capacitor losses. By adding up all these individual contributions, aggregate power dissipation can be calculated. In the following sections, each category of loss is examined in detail, and the corresponding calculation procedures are presented.

Switching losses are able to be categorized into two distinct types: Conduction-related losses and switching losses. Using expressions (56) and (57) we can calculate these losses.

Table 1. Comparative analysis of the proposed topology with structures reported in the literature

Parameter	SL-ZSI [27]	SL-IZSI [26]	EB-ZSI [30]	EB-QZSI [31]	Ref [42]	Ref [41]	Ref [40]	Proposed
L	4	4	4	4	3	4	2	4
C	2	2	4	4	3	5	3	3
Diodes	7	7	5	5	3	4	4	6
Switches	0+6	0+6	0+6	0+6	0+6	0+6	2+6	0+6
Input current	Discontinuous	Continuous	Continuous	Continuous	Discontinuous	Continuous	Continuous	Continuous
Boost factor	$\frac{1+D}{1-3D}$	$\frac{1+D}{1-3D}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{2}{1-3D}$	$\frac{1}{1-4D+D^2}$	$\frac{1}{1-5D+2D^2}$	$\frac{2(1+D)}{1-4D-D^2}$
Voltage gain	$\frac{M(2-M)}{3M-2}$	$\frac{M(2-M)}{3M-2}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{2M}{3M-2}$	$\frac{M}{M^2+2M-2}$	$\frac{M}{M^2+M-2}$	$\frac{2(M-2)}{M^2-6M+2}$
$\frac{V_{C1}}{V_{dc}}$	$\frac{2D}{1-3D}$	$\frac{1-D}{1-3D}$	$\frac{(1-D)^2}{1-4D+2D^2}$	$\frac{(1-D)^2}{1-4D+2D^2}$	$\frac{1-D}{1-3D}$	$\frac{1-2D}{1-4D+D^2}$	$\frac{2D}{1-5D+2D^2}$	$\frac{(1+D)^2}{1-4D-D^2}$
$\frac{V_{C2}}{V_{dc}}$	$\frac{2D}{1-3D}$	$\frac{1-D}{1-3D}$	$\frac{(1-D)^2}{1-4D+2D^2}$	$\frac{D(1-D)}{1-4D+2D^2}$	$\frac{2(1-D)}{1-3D}$	$\frac{1-2D}{1-4D+D^2}$	$\frac{1-2D}{1-5D+2D^2}$	$\frac{4D}{1-4D-D^2}$
$\frac{V_{C3}}{V_{dc}}$	------	------	$\frac{1-D}{1-4D+2D^2}$	$\frac{1-3D+D^2}{1-4D+2D^2}$	$\frac{1-D}{1-3D}$	$\frac{D}{1-4D+D^2}$	$\frac{1}{1-5D+2D^2}$	$\frac{1-D^2}{1-4D-D^2}$
$\frac{V_{C4}}{V_{dc}}$	-----	-----	$\frac{1-D}{1-4D+2D^2}$	$\frac{D(2-D)}{1-4D+2D^2}$	-----	$\frac{1-D}{1-4D+D^2}$	-------	-------

$$P_{SW} = \frac{1}{2} f_s V_i I_{sh} (t_r + t_f) \quad (56)$$

$$P_{Cond} = R_s I_{sh}^2 D \quad (57)$$

The on-state resistance, shoot-through current, as well as the rise and fall times of the switch, can be represented mathematically by R_s, I_{sh}, t_r, and t_f.

The diode power losses in the proposed structure comprise conduction losses and reverse-recovery-associated losses. The conduction loss is able to be represented as follows:

$$P_{Cond-D} = V_F I_{D(avg)} + R_D I_{D(rms)}^2 \quad (58)$$

$$P_{rr-D} = Q_{rr} f_s V_D \quad (59)$$

$I_{D1} = I_{D2}$ and $I_{D3} = I_{D4}$, we have:

$$\begin{cases} I_{Din(rms)} = \sqrt{1-D}\,(I_L + I_{L1} - I_{PN}) \\ I_{Din(avg)} = (1-D)(I_L + I_{L1} - I_{PN}) \end{cases} \tag{60}$$

$$\begin{cases} I_{D1(rms)} = \sqrt{D}\,I_L \\ I_{D1(avg)} = DI_L \end{cases} \tag{61}$$

$$\begin{cases} I_{D3(rms)} = \sqrt{D}\,(I_{dc} - 2I_L - I_{L1}) \\ I_{D3(avg)} = D(I_{dc} - 2I_L - I_{L1}) \end{cases} \tag{62}$$

$$\begin{cases} I_{D5(rms)} = \sqrt{1-D}\,I_L \\ I_{D5(avg)} = (1-D)I_L \end{cases} \tag{63}$$

And,

$$V_{Din} = V_{dc} \tag{64}$$

$$V_{D1} = V_{D2} = \frac{1-D^2}{2(1-4D-D^2)}V_{dc} \tag{65}$$

$$V_{D3} = V_{D4} = \frac{1}{2}V_{dc} \tag{66}$$

$$V_{D5} = \frac{1-D^2}{1-4D-D^2}V_{dc} \tag{67}$$

The capacitor's power loss can be calculated as follow:

$$P_C = r_C I_{C(rms)}^2 \tag{68}$$

$I_{C(rms)}$ denotes the calculated RMS current through the capacitor, while r_C represents the capacitor's equivalent series resistance (ESR):

$$I_{C-RMS} = \sqrt{i_{C-ST}^2 D + i_{C-nST}^2 (1-D)} \tag{69}$$

Also, the inductor's power loss is able to be measured as below:

$$P_L = r_L I_{L-RMS}^2 \tag{70}$$

r_L corresponds to the equivalent series resistance (ESR) of the inductor, accounting for its resistive losses.

Accordingly, the aggregate power dissipation in the proposed converter is as follows:

$$P_{Loss} = P_{Loss-S} + P_{Loss-D} + P_{Loss-C} + P_{Loss-L} \tag{71}$$

Efficiency of the proposed structure can be calculated as below:

$$\eta\% = \frac{P_o}{P_o + P_{Loss}} \times 100 \tag{72}$$

The parameter values employed in the power loss calculations are used from Table 3. The detailed power losses among the various components in the proposed topology are presented in Fig. 4. As observed, the losses associated with the switches, diodes, capacitors, and inductors are 0.7 W (7.1%), 6.05 W (62.3%), 0.75 W (7.6%), and 2.23 W (23%), respectively.

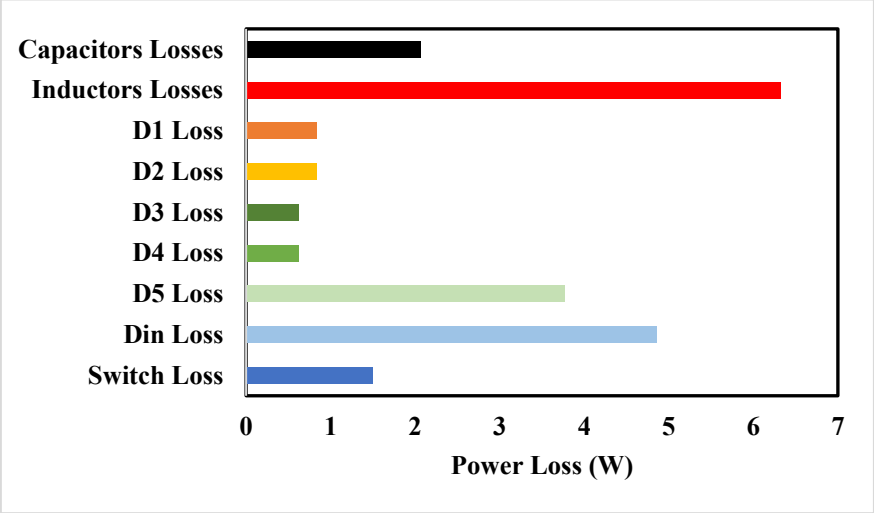


Figure 4. Detailed characterization of aggregate power dissipation associated with the proposed topology

Fig. 5, in order to further analyze, illustrates the variation of the efficiency of the suggested topology versus output power for two duty ratios, 0.1 and 0.15. It is observed that the efficiency for duty ratio of 0.15 is higher than 0.1.

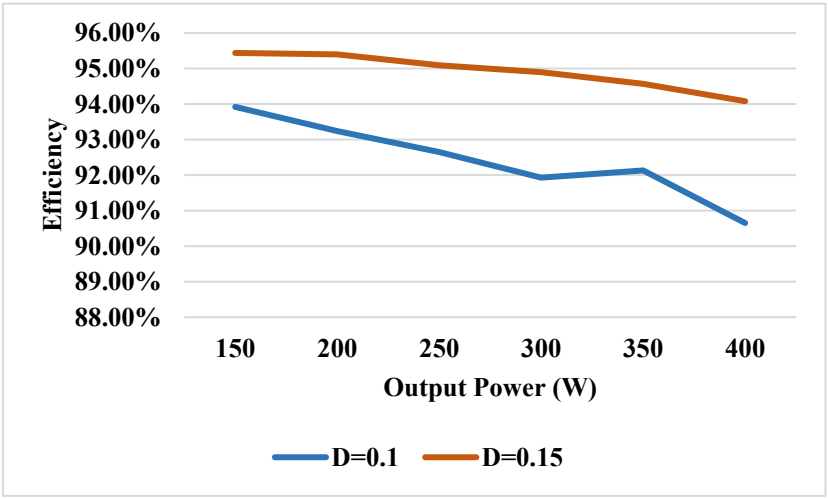


Figure 5. The variation efficiency of the proposed topology

5. Performance verification through simulation and experimental studies

In order to assess the effectiveness of the suggested structure, the proposed topology is evaluated through both simulation and experimental investigations. For clarity, the circuit parameters applied in the simulations and experiments are listed in Table 2.

Table 2. Parameters for simulation and experimental

Parameter	Description
Input voltage	40 V
Nominal output power	250 W
Switches	STT2002
Diodes	MUR860
Capacitors C_1,C_2&C	470 µF
Inductors L_1,L_2,L_3&L_4	1 mH
Filter C_f & L_f	33 µF & 1 mH
Switching frequency	20 kHz

5.1. Results of simulation analysis

To assess the efficacy of the suggested structure, MATLAB-based simulations are carried out using ideal components, which are represented in Table 2. The simulation findings of the proposed structure are illustrated in Fig. 6 by the simple boost method19, with values $D = 0.1$ and $M = 0.9$.

Regarding Fig.s 6.a and 6.b, the DC-link and the output voltage, V_i and V_{L-L}, in the non-shoot-through state are approximately 142 V and 110 V, respectively. These values align with the mathematical calculations based on equations (16) and (18). The boost coefficient in this mode is 3.72, which agrees with (17). Also, the input and output currents are 50 A and 2 A, respectively, which are displayed in Fig. 6.d and Fig. 6.e. Based on Fig. 6.c, the voltages of the capacitors C_1, C_2, and C are equal to 76 V, 23 V, and 61 V, respectively, which is in agreement with (12), (13), and (14). The inverter exhibits a total harmonic distortion (THD) of about 1.33%, as illustrated in Figure 6.f.

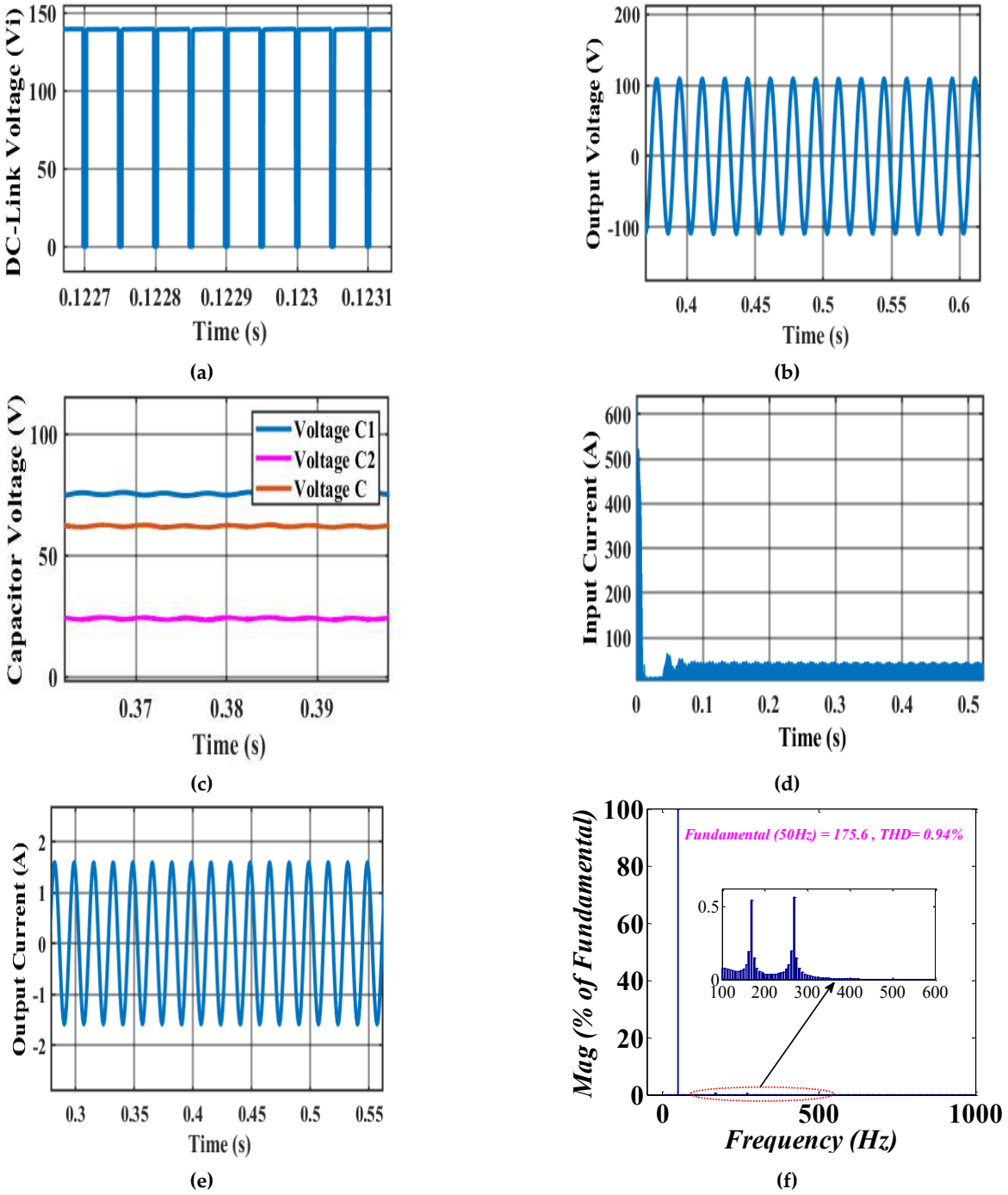


Figure 6. Simulation results for $\mathbf{D = 0.1}$, $\mathbf{M = 0.9}$. (a) DC-link voltage, (b) output AC line-line voltage, (c) voltage across capacitors $\mathbf{C_1}$, $\mathbf{C_2}$, and $\mathbf{C}$, (d) input current, (e) load current, and (f) output voltage THD

5.2. Results of experimental analysis

The laboratory-scale experimental platform employed for the validation of the proposed structure is presented in Fig. 7. A TMS320F28377s processor is utilized for the purpose of controlling the inverter. The practical parameters are chosen to be identical to those utilized in the simulation. The prototype-based experimental findings of the proposed inverter are indicated in Fig. 8 when $D = 0.1$ and $M = 0.9$. In Fig. 8.a, the DC-link voltage is raised to 139 V from the input voltage of 40 V. As shown in Fig. 8.b, the voltages across C_1 and C_2, denoted as V_{C1} and V_{C2}, are measured to be 76 V and 21 V respectively. Additionally, the voltage of C (V_C) is measured to be 58V. Fig. 8.c shows that the voltage across diode D_1, D_2, and D_{in} are equal to 29 V and 36 V, which are in agreement with theoretical calculations. Also, the voltage of diodes D_3, D_4, and D_5 are depicted in Fig. 8.d. Additionally, Figure 8.e depicts the current passing through inductors. The output voltage and current are illustrated in Fig. 8.f. The deviation from the simulation results is 10% due to the non-ideal nature of the elements.

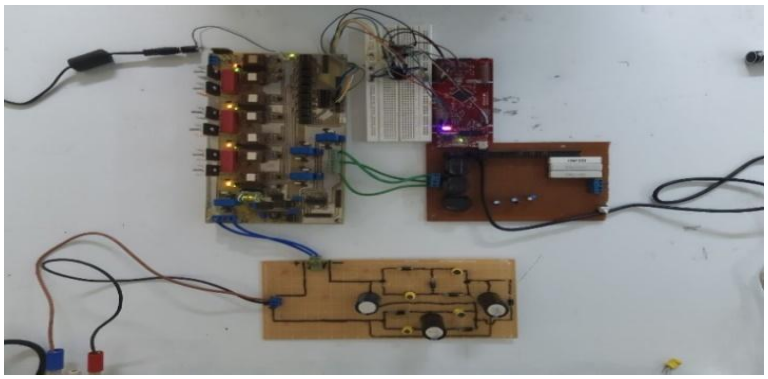
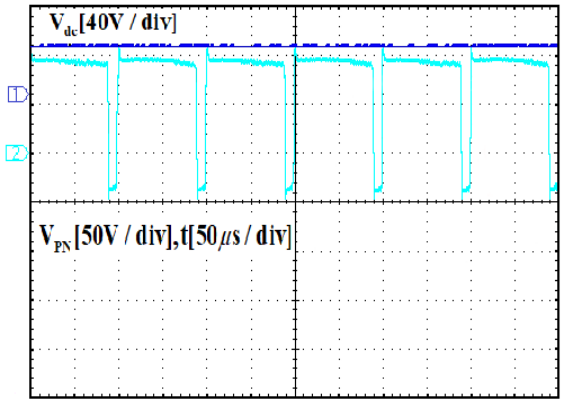
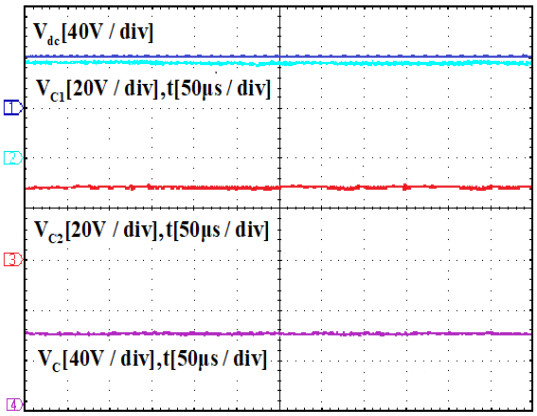


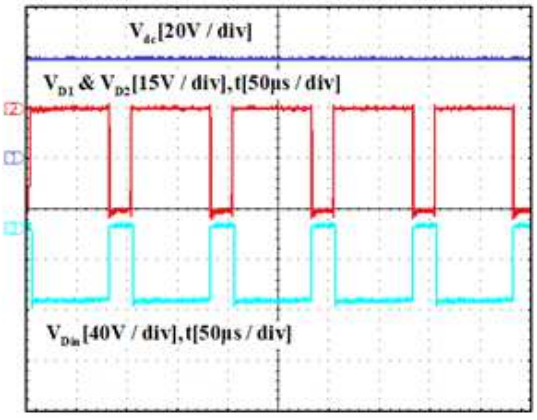
Figure 7. Experimental configuration of the suggested inverter



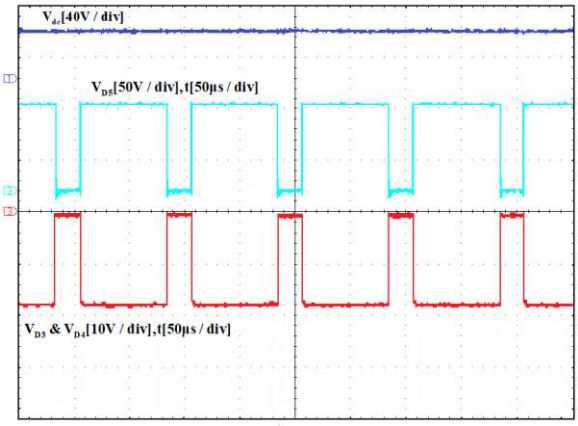
(a)



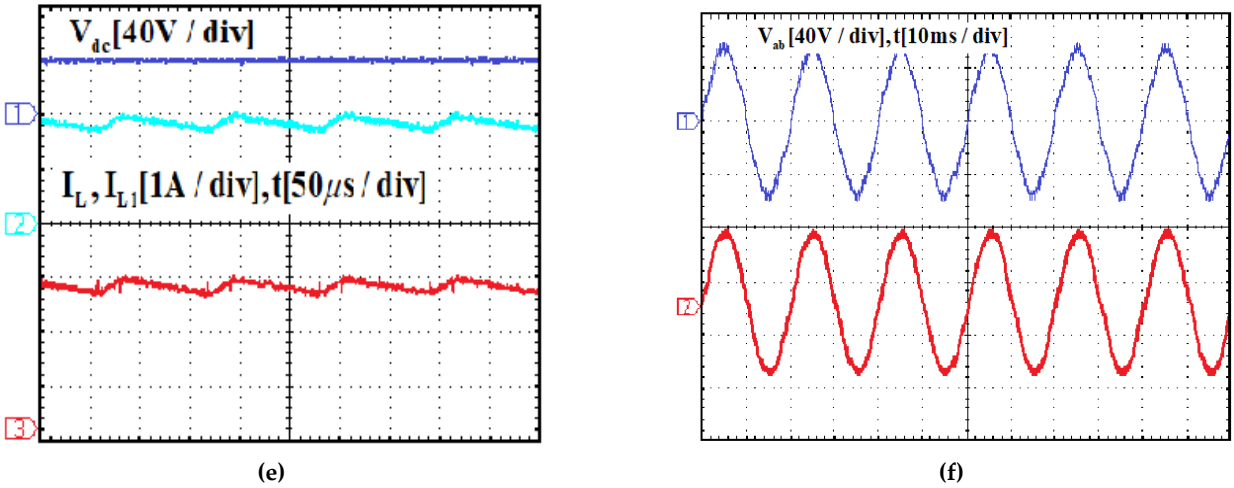
(b)



(c)



(d)



(e) (f)

Figure 8. Results of experimental for $\mathbf{D = 0.1}$ and $\mathbf{M = 0.9}$, (a) The input voltage, DC-link voltage, (b) the capacitors voltage, (c) The diodes $\mathbf{V_{D1}, V_{D2}}$ & $\mathbf{V_{Din}}$, (d) The diodes $\mathbf{V_{D3}, V_{D4}}$ & $\mathbf{V_{D5}}$, (e) The inductors current, and (f) The line-to-line voltage, and the load current

5. Conclusion

This paper presented a high boosting capability improved switched-inductor-capacitor cells Z source inverter for single-stage DC-AC power conversion. The proposed topology was derived by modifying the improved switched-inductor-based Z-source network through the replacement of the middle diode with a capacitor and the rearrangement of the impedance network. This modification enables the proposed inverter to achieve a high boosting factor at a relatively small shoot-through interval while maintaining a large modulation-index range. The steady-state analysis shown that the proposed ISLC ZSI enables continuous current at the input side, reduced electrical stress on capacitors and active components, diodes, and semiconductors, compared with relevant high-boost Z-source and switched-inductor based topologies. In addition, the proposed structure offers a unified ground reference operation between the input side and the DC-link, which is particularly beneficial for clean-energy applications. Compared with recently reported impedance-source inverters, the proposed topology achieves improved boost capability and voltage gain without requiring a significant increase in component count. Simulation results generated from the MATLAB/Simulink environment together with laboratory prototype measurements verified the theoretical analysis, operating principles, boost factor, voltage gain, and electrical stress characteristics of the proposed inverter. Therefore, the proposed ISLC-ZSI is a suitable candidate for low-voltage clean-energy systems, including photovoltaic and fuel cell applications, where high boosting capability, low shoot-through interval, continuous input current, and reduced component voltage stress are required.

Data availability statement:

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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Competing interests:
The author declare no competing interests.

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