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Fast-Switching Monolayer $MoSiGeN_4$ Transistors: Device Performance at Sub-5 nm High-Performance Nodes

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Abstract

The scaling limits of silicon-based transistors have driven the search for two-dimensional field-effect transistors capable of high-speed and energy-efficient operation at sub-5-nm gate lengths. This work presents a double-gated n-type field-effect transistor built from monolayer Janus $MoSiGeN_4$, a two-dimensional semiconductor, evaluated using first-principles density functional theory combined with the non-equilibrium Green's function formalism. On-state current, subthreshold swing, intrinsic delay, and power-delay product are examined across gate lengths from 2 to 5 nm. Without any source or drain underlap, the device satisfies International Technology Roadmap for Semiconductors high-performance targets projected for the year 2028, down to a 4-nm gate length. Introducing a modest underlap restores electrostatic control at shorter channels, extending compliant scaling to a 2-nm gate length while boosting the on-state current to the roadmap target. Most notably, the intrinsic delay and power-delay product remain far below roadmap limits across every gate length studied, falling as low as 0.006 ps and 0.004 fJ/μm, respectively, well over an order of magnitude below the corresponding 2028 targets. To our knowledge, this is the first demonstration of such switching speed and energy-efficiency potential in this material, with performance metrics substantially exceeding roadmap requirements. These findings establish the double-gated monolayer $MoSiGeN_4$ field-effect transistor as a compelling device for next-generation high-speed, energy-efficient logic beyond the 5-nm node.

Keywords: 2-D materials, ON–OFF ratio, ballistic transport, subthreshold swing (SS), delay, power-delay product (PDP).

1 Introduction

To sustain Moore's Law, continuous miniaturization of transistor dimensions is essential. However, conventional bulk-Si scaling is fundamentally constrained by short-channel effects (SCEs), drain-induced barrier lowering, and increased gate leakage, limiting further performance improvements[1–3]. Although SOI, FinFET, and GAAFET architectures have extended CMOS scaling primarily by improving gate electrostatics[4, 5], these innovations do not eliminate the scaling constraints of silicon. As gate length approaches the few-nanometer regime, short-channel effects, source-to-drain tunneling,

and the inability to further reduce silicon body thickness impose limits on silicon-based devices[6–8].

Two-dimensional (2D) semiconductors have emerged as promising alternatives to overcome these limitations, owing to their atomically thin, dangling-bond-free surfaces that enable superior carrier transport and electrostatic control[9, 10]. Graphene, the first-discovered 2D material[11], remains the most widely studied. Despite its high mobility and atomic smoothness, the absence of a bandgap[12] prevents its use as a semiconductor in transistor applications.

Transition metal dichalcogenides (TMDs) have attracted significant attention following the successful fabrication of the first monolayer MoS_2 transistor[13]. Extensive research continues to explore the potential of TMDs as channel materials for nanoscale transistors owing to their excellent electrostatic control and high I_{ON}/I_{OFF} ratios[14]. MoS_2-based field-effect transistors (FETs) have been experimentally demonstrated with gate lengths scaled down to a few nanometers[15, 16], highlighting their scalability beyond the limits of silicon technology. However, the relatively low carrier mobility restricts their suitability for high-performance (HP) applications[17]. Black Phosphorus (BP) transistors, with their superior hole mobility[18], provide a promising p-type counterpart, but suffer from poor environmental stability[19].

Recently, a new family of 2D semiconductors, MA_2N_4 (where M denotes an early transition metal, and A represents Si or Ge), has emerged as a higher-mobility alternative to the TMD channels. This family has attracted significant attention because of its high carrier mobility[20] and the successful chemical vapor deposition (CVD) synthesis of $MoSi_2N_4$ with excellent environmental stability[21, 22]. Double-gated (DG) monolayer $MoSi_2N_4$ MOSFETs meet the International Roadmap for Semiconductors (ITRS) requirements for high-performance (HP) devices[23] for p-type operation down to a 3 nm gate length[24], however, the corresponding n-type devices fail to satisfy the HP requirements below 5 nm. ML WSi_2N_4 MOSFETs have shown improvement, with both p-type FETs and n-type FETs meeting the ITRS HP standards in the sub-5 nm regime[25]. However, their applicability is limited to gate lengths $\geq$ 3 nm, leaving device performance below 3 nm an open question.

A new Janus 2D material, $MoSiGeN_4$, inspired by the successful synthesis of $MoSi_2N_4$, has been predicted to exhibit high carrier mobility and excellent dynamical, thermal, and mechanical stability, making it a promising channel material for next-generation nanoelectronic devices[26, 27]. The structural asymmetry of $MoSiGeN_4$ breaks the vertical mirror symmetry, inducing an out-of-plane polarization and a built-in electric field that enhances electrostatic gate control. Consequently, $MoSiGeN_4$ transistors are expected to achieve a higher I_{ON}/I_{OFF} ratio, a steeper subthreshold swing (SS), and lower power consumption. Similar advantages have been reported for other Janus materials, including enhanced carrier mobility in Janus TMDs[28, 29] and promising sub-10-nm device performance in Janus Ga_2SSe[30]. These characteristics, along with a predicted electron mobility of approximately 5200 $cm^2V^{-1}s^{-1}$[26], make $MoSiGeN_4$ a compelling candidate for ultra-scaled transistors, motivating a theoretical investigation of its MOSFET performance at sub-5-nm gate lengths.

In this work, we demonstrate that sub-5-nm n-type DG MOSFETs based on monolayer $MoSiGeN_4$ exhibit fast switching and low power dissipation, as evaluated using first-principles density functional theory (DFT) combined with the non-equilibrium Green's function (NEGF) formalism along the zigzag and armchair transport directions. Key performance parameters such as the on-state current (I_{on}), subthreshold swing (SS), intrinsic delay (τ), and power-delay product (PDP) are analyzed. The results show that the $MoSiGeN_4$ FETs satisfy the ITRS HP 2028 targets when scaled down to 4 nm gate length, and that employing a small underlap (UL) structure extends this scaling down to a 2 nm gate length while achieving an on-state current near 1.5 times the ITRS target. The device also exhibits intrinsic delay and power-delay product well below the ITRS requirements even at a 2 nm gate length, consistent with the enhanced electrostatic gate control provided by the built-in polarization of the Janus structure. These results establish monolayer $MoSiGeN_4$ as a promising channel material for next-generation high-speed, energy-efficient transistor applications.

2 Device Structures and Methods

To evaluate the ballistic performance limits of monolayer $MoSiGeN_4$ at the sub-5 nm node, we constructed a symmetric double-gate field-effect transistor architecture. As shown in Fig.1, the device structure has four distinct regions along the transport direction: a central channel region of length L_g; two equal underlap regions on each side of the channel having a total length of UL; a semi-infinite source; and a semi-infinite drain region. The total channel length is the summation of gate length and underlap length (L_{ch} = L_g + UL). The device width (W) is taken to be 10.23 Å and the channel region (L_{ch}) is varied to calculate the transport properties at different channel lengths. The source and drain regions are n-type doped, whereas the channel region is intrinsic. This allows us to assess the performance of monolayer $MoSiGeN_4$ as the channel of FETs. Electrostatic doping is exploited to reversibly shift the Fermi level and realize effective n-type behavior and abrupt, junction-free profiles without introducing chemical impurities. Two symmetric dielectric slabs of 0.41 nm thick and with a dielectric constant of 3.9 (SiO_2) are placed on top and bottom of the channel material. The dielectric width equals the device width and extends across the channel region. The van der Waals gap between the semiconductor channel and the dielectric is automatically optimized during simulation. The dielectric thickness is chosen to meet the ITRS criterion of equivalent oxide thickness (EOT) of 0.41 nm[23]. On top of the dielectric slabs, two symmetrical metal gates of thickness 0.40 nm and width 10.23 Å are placed.

The methodology combines two complementary computational techniques: the density functional theory (DFT) and the non-equilibrium Green's function (NEGF) formalism. The drain current under a given bias voltage V_{dd} and gate voltage V_g is obtained through the Landauer-Büttiker formula[31],

$$I_{ds}(V_{dd},V_g) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E,V_{dd},V_g) \times [f_s(E-\mu_s) - f_d(E-\mu_d)]\}dE \quad (1)$$

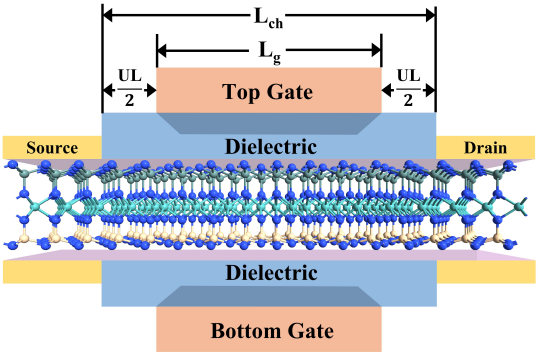


Fig. 1 Device model of the double-gated monolayer $MoSiGeN_4$ FET. The gate oxide is SiO_2. The gate length (L_g), underlap length (UL), and channel length (L_{ch} = L_g + UL) are indicated. The source and drain regions are heavily n-type doped to a concentration of 1×10^{13} cm^{-2}, while the channel region is intrinsic (undoped)

where $T(E,V_{dd},V_g)$ is the transmission coefficient, f_s/f_d is the Fermi-Dirac distribution function for source/drain electrodes, and μ_s/μ_d is the electrochemical potential of the source/drain electrodes. The transmission coefficient is obtained by:

$$T(E) = \mathrm{T_r}[\Gamma^L(E)G(E)\Gamma^R(E)G^\dagger(E)] \quad (2)$$

where $\Gamma^{L/R}(E)$ represents the broadening function of the right/left contacts and $G(E)$ is the retarded Green's function of the central region. The Green's function is obtained using the formula:

$$G(E) = [(E+i\delta_+)S - H - \Sigma^L(E) - \Sigma^R(E)]^{-1} \quad (3)$$

where i is the imaginary number unit, δ_+ is an infinitesimal positive number, S and H are the overlap and Hamiltonian matrices, respectively. $\Sigma^{L(R)}(E)$ is the self-energy of the left(right) electrode, which describes the effect of electrode states on the electronic structure of the central region. The Hamiltonian is formed as a function of electron density n(r):

$$H(n) = -\frac{\hbar^2}{2m}\nabla^2 + V^H(n) + V^{\mathrm{XC}}(n) + V^{\mathrm{ext}} \quad (4)$$

where $V^H(n)$ is the Hartree potential due to the mean-field electrostatic interaction between the electrons, $V^{\mathrm{XC}}(n)$ is the exchange-correlation

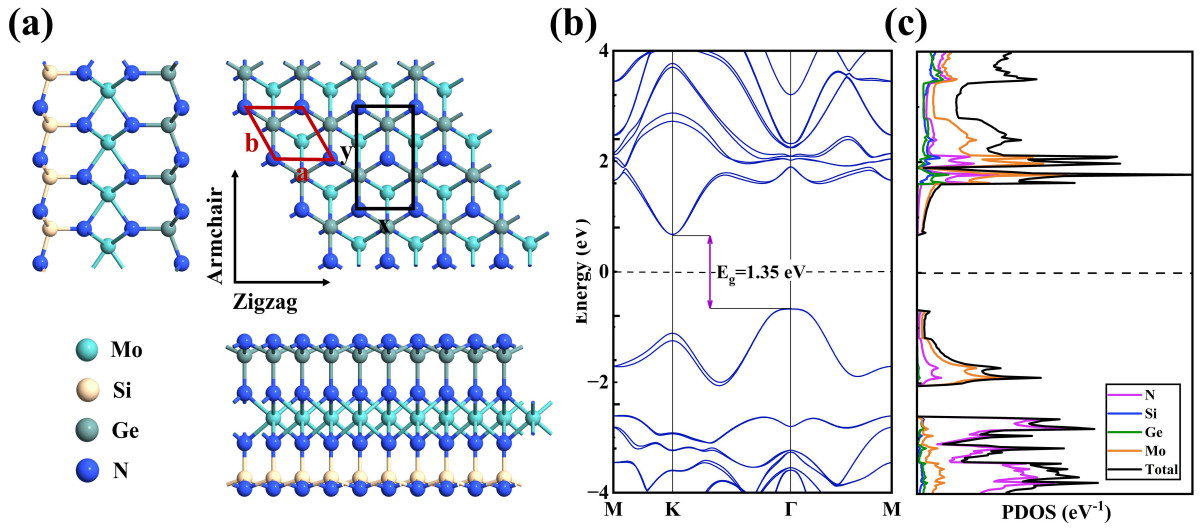


Fig. 2 (a) Top and side view of the optimized monolayer $MoSiGeN_4$, showing the rhombus primitive cell (red lines) and rectangular supercell (black lines). (b) Electronic band structure using spin-orbit coupling (SOC). (c) Projected density of states (PDOS) of monolayer $MoSiGeN_4$

potential due to the electron's quantum mechanical nature and V^{ext} represents any other electrostatic fields in the system. The Hartree potentials $V^H(n)$ of the electrodes are aligned through their chemical potentials (μ_s/μ_d), hence it depends on the bias voltage by,

$$\mu_s - \mu_d = eV_{dd} \tag{5}$$

However, the Hartree potential in the central region is determined by solving the Poisson equation, using bulk-like electrode Hartree potentials as boundary conditions at the electrode-central region interfaces. The external potential V^{ext} is given by:

$$V^{\text{ext}} = \sum_{\mu} V_{\mu}^{\text{pseudo}} + V^{\text{gate}} \tag{6}$$

The first term is the pseudopotential due to the electrostatic potential of ions, and the second term V^{gate} is the applied gate voltage (V_g).

The geometric optimizations, electronic properties, and energy band calculations are performed based on DFT. To avoid interactions between neighboring atoms due to the periodic boundary conditions, a 20 Å vacuum layer is added on both sides of the unit cell's 'c' direction. The LCAO (Linear Combination of Atomic Orbitals) calculator is used to perform geometric optimization of the unit cell. The exchange-correlation effects are described by generalized gradient approximation (GGA) and the Perdew–Burke–Ernzerhof (PBE) functional potential[32]. Van der Waals correction is set to Disabled, and PseudoDojo Pseudopotential with High basis set is used. The density mesh cutoff is set to 105 Ha, and the Fermi-Dirac occupation method with 300 K broadening temperature is used. The Monkhorst-Pack k-point sampling of 33 × 33 × 1 is set in the Brillouin zone integration[33]. The maximum energy and force for convergence are 5×10^{-7} eV and 5×10^{-3} eV/Å, respectively. DiagonalizationSolver is used as the eigenvalue solver, and Poisson Solver is set to FFT. Due to the presence of a transition metal, SOC (Spin-Orbit Coupling) influences the band structure of $MoSiGeN_4$, the band structure is calculated with SOC taken into account.

The transport properties of the device are computed using the DFT combined with the NEGF formalism. The Device LCAO calculator is used with the exchange-correlation functional set to GGA-PBE and Fritz Haber Institute (FHI) pseudopotential with a DoubleZetaPolarized basis set. A density mesh cut off of 75 Ha and a broadening temperature of 300 K are set. To

Table 1 Structural and Electrical Properties of Monolayer $MoSiGeN_4$ [26, 36]

Parameter	Simulation	Literature
Band Gap	1.3496 eV	1.35 eV
a	2.954 Å	2.96 Å
b	2.954 Å	2.96 Å
$\mathbf{m_e^*}$ (AM)	$0.374\,m_0$	$0.392\,m_0$
$\mathbf{m_e^*}$ (ZZ)	$0.374\,m_0$	$0.409\,m_0$
$\mathbf{m_h^*}$ (AM)	$-9.172\,m_0$	$-10.845\,m_0$
$\mathbf{m_h^*}$ (ZZ)	$-9.369\,m_0$	$-10.908\,m_0$

calculate the electronic transport characteristics of the device, Monkhorst-Pack k-point sampling of $3 \times 1 \times 320$ and $3 \times 1 \times 50$ are applied in the channel and electrode region, respectively. Periodic, Neumann, and Dirichlet boundary conditions are applied to the transverse, vertical, and transport directions, respectively. The Poisson equation is solved self-consistently using a multigrid solver with a tolerance of 1×10^{-4} eV for the potential. The Landauer-Büttiker formalism is implemented through a weighted contour integral. An equilibrium contour with a 50-point semi-circle is applied. All the simulations are executed in the Quantum Atomistic Tool Kit (ATK) 2019 package[34, 35].

3 Results and Discussion

The structural and electrical properties of ML $MoSiGeN_4$ are first investigated using the DFT framework to evaluate its transport behavior. The Janus structure of monolayer $MoSiGeN_4$ can be regarded as a MoN_2 sublayer sandwiched between Si-N and Ge-N sublayers. As shown in Fig. 2(a), the relaxed structure of monolayer $MoSiGeN_4$ has a hexagonal lattice structure with lattice parameters of the unit cell found as a = b = 2.954 Å, which is in good agreement with the previously found theoretical data[26, 36]. The electronic band structure of monolayer $MoSiGeN_4$ was obtained using the GGA+SOC method and calculated along the high-symmetry path M-K-Γ-M within the first Brillouin Zone. The resulting band

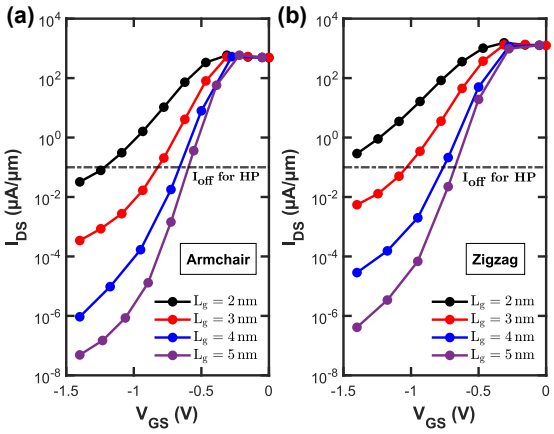


Fig. 3 Log-scale transfer characteristics (I_D–V_{GS}) for $MoSiGeN_4$ MOSFETs without underlap for (a) armchair-n and (b) zigzag-n directed devices at L_g = 2–5 nm. The dashed line indicates the I_{off} target for high-performance (HP) applications. All results are obtained at a fixed carrier density of 1×10^{13} cm^{-2}

structure in Fig. 2(b) indicates an indirect band gap of 1.35 eV, with the conduction band minimum (CBM) located at the K point, consistent with previous reports[36]. The calculated electron effective mass is 0.374 m_0 along both armchair and zigzag transport directions, while the hole effective masses are 9.369 m_0 and 9.172 m_0 along the zigzag and armchair directions, respectively, listed and compared in Table 1, where m_0 denotes the rest mass of a free electron. These values indicate a significantly higher electron mobility compared to hole mobility. The projected density of states (PDOS), illustrated in Fig. 2(c), reveals that the CBM and VBM are dominated by Mo-d and N-p orbitals, indicating strong orbital hybridization.

We calculate the transport properties for gate lengths of 2 nm – 5 nm. According to ITRS HP specifications, off current is $I_{off} = 0.1\ \mu A/\mu m$. On current ($I_{on}$) is calculated at a gate-source voltage $V_{gs(on)} = V_{gs(off)} + V_{dd}$, where V_{dd} is the bias voltage (0.64 V in ITRS HP requirement) and $V_{gs(off)}$ is the gate-source voltage corresponding to I_{off}. Subthreshold swing (SS) is a key parameter that measures how effectively a transistor can switch from the OFF state to the ON state. It is defined as the required change in gate voltage to increase the drain current by one decade (tenfold) in the subthreshold region, typically expressed in mV/dec. To identify the optimum doping level

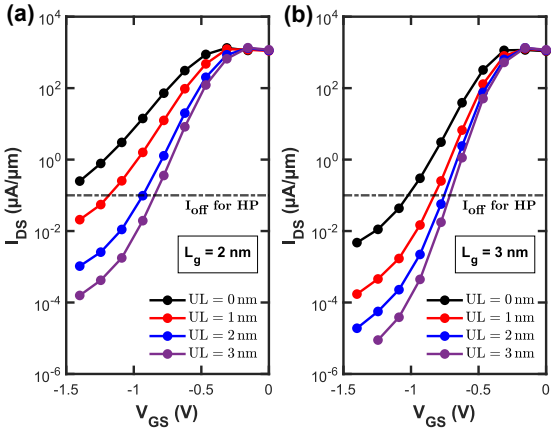


Fig. 4 Log-scale transfer characteristics (I_D–V_{GS}) for zigzag directed $MoSiGeN_4$ MOSFETs for different underlap (UL) lengths for (a) L_g = 2 nm and (b) L_g = 3 nm devices. The dashed line indicates the I_{off} target for high-performance (HP) applications

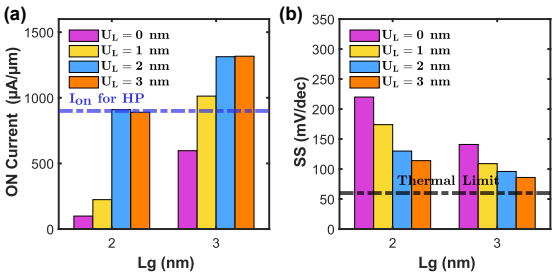


Fig. 5 Effect of underlap (UL) on (a) ON current and (b) subthreshold swing (SS) for N-FETs at L_g = 2 and 3 nm. The dashed line in (a) denotes the ITRS 2028 high-performance (HP) I_{on} target (900 μA/μm), while the dashed line in (b) marks the thermal limit of SS (60 mV/dec at 300 K)

of drain/source, transport characteristics are evaluated at four doping concentrations (5×10^{12} cm^{-2}, 1×10^{13} cm^{-2}, 5×10^{13} cm^{-2} and 7×10^{13} cm^{-2}). Doping level of 1×10^{13} cm^{-2} provides the best balance between on current and subthreshold swing: I_{on} exceeds the ITRS 2028 HP target of 900 μA/μm while maintaining an acceptable SS of 95 mV/dec. Lower doping provides low SS but fails the on current target, while higher doping degrades SS severely. Also, at 1×10^{13} cm^{-2} doping level, transport in the zigzag direction is superior compared to the armchair direction. Consequently, doping concentration of 1×10^{13} cm^{-2} along the zigzag direction is adopted for subsequent analysis.

We benchmark the transport characteristics at different gate lengths against the ITRS 2028 HP targets: I_{off} = 0.1 μA/μm, $I_{on} \geq$ 900 μA/μm, and $I_{on}/I_{off} \geq 9 \times 10^3$. Transfer characteristics at different gate lengths are shown in Fig. 3(a) and Fig. 3(b) for armchair and zigzag directed n-type FETs, respectively. At L_g = 5 nm and 4 nm, the device meets ITRS requirements, achieving an I_{on} of 1064 μA/μm and 1042 μA/μm, and an SS of 77 mV/dec and 95 mV/dec, respectively. As L_g is reduced to 3 nm and 2 nm, the device fails to satisfy the ITRS requirements. For 3 nm and 2 nm L_g, the I_{on} drops to 597 μA/μm and 99 μA/μm, and SS becomes 141 mV/dec and 220 mV/dec, respectively (Table 2). The device fails to meet the requirements at shorter gate length due to significant source-to-drain tunneling, which degrades I_{on} and SS.

To improve the device performance, one practical approach is to add an underlap (UL) structure between the source/drain and the gate which improves gate electrostatic control and reduces source-to-drain tunneling. The transfer characteristics for L_g = 2 nm and 3 nm with UL = 0-3 nm are shown in Fig. 4(a) and Fig. 4(b), respectively and the effects of UL on I_{on} and SS is summarized in Fig. 5. For L_g = 3 nm, I_{on} significantly increases from 597 μA/μm to 1013 μA/μm with the introduction of 1 nm UL, meeting the ITRS requirement, and reaches 1317 μA/μm for 3 nm UL. Likewise for L_g = 2 nm, I_{on} increases from 99 μA/μm to 910 μA/μm with the addition of a 2 nm UL, meeting ITRS standard. However, increasing UL beyond 2 nm for L_g = 2 nm decreases the I_{on} value (890 μA/μm at UL = 3 nm). This is because the gate controllability at the UL region is weaker than the gate region; hence, too long UL reduces the device performance. So, there is an optimum UL length beyond which the device performance degrades. A noticeable improvement in SS is observed with the addition of UL. When a 3 nm UL is added to L_g = 3 nm, the SS improves from 141 mV/dec to 86 mV/dec. Similarly, for L_g = 2 nm, a reduction in SS from 220 mV/dec to 114 mV/dec is observed upon introducing a 3 nm UL. This clearly indicates that the addition of UL effectively reduces short-channel effects and enhances device performance.

Table 2 Performance Metrics of n-Type ZZ-Directed $MoSiGeN_4$ FETs

L_g (nm)	UL (nm)	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}	SS (mV/dec)	τ (ps)	PDP (fJ/μm)
5	0	1064	0.1	1.06×10^4	77	0.014	0.009
4	0	1042	0.1	1.04×10^4	95	0.016	0.010
3	0	597	0.1	5.97×10^3	141	0.017	0.006
	1	1013	0.1	1.01×10^4	109	0.010	0.006
	2	1313	0.1	1.31×10^4	96	0.007	0.006
	3	1317	0.1	1.32×10^4	86	0.006	0.005
2	0	99	0.1	0.99×10^3	220	0.073	0.005
	1	224	0.1	2.24×10^3	174	0.026	0.004
	2	910	0.1	9.10×10^3	130	0.007	0.004
	3	890	0.1	8.90×10^3	114	0.006	0.004
ITRS HP 2028	–	900	0.1	9.00×10^3	–	0.423	0.240

The effects of underlap are illustrated in Fig. 6 using PLDOS and current spectrum in both on and off states for $L_g = 2$ nm having 4 different ULs. The energy barrier height (Φ_B), defined as the maximum difference in the CBM between channel and source, decreases as UL is applied. The thermal current refers to the current spectra above the energy barrier, and the tunneling current corresponds to the current spectra below the barrier. Without UL, the off state has a large energy barrier of 0.47 eV, and only the tunneling current (I_{tunnel}) contributes to the current spectra. A barrier of 0.09 eV exists in the on state, resulting in a small on current of 99 μA/μm. This is because the drain to source voltage of 0.64 V is insufficient to drive a significant number of carriers over the barrier, as observed in the current spectra (low $I_{thermal}$). When 1 nm UL is added, the off-state barrier height reduces by 0.09 eV to become 0.38 eV, and the on-state barrier reduces to 0.04 eV from 0.09 eV. As the barrier is reduced, the total on-current increases to 224 μA/μm, indicating an increase of nearly 126%. Similarly, for 2 nm UL, the off-state barrier becomes 0.31 eV and most importantly, the on-state barrier vanishes to become 0 eV, and a large thermal current ($I_{thermal}$) is observed. The total on-state current ($I_{thermal} + I_{tunnel}$) increases significantly to become 910 μA/μm, meeting the ITRS requirements. The reduction of source-drain tunneling is also evident in the current spectra, resulting in a lower SS as the UL length increases. However, for 3 nm UL, the off-state barrier increases to become 0.33 eV due to reduced gate controllability over the UL regions resulting in a reduced on-state current of 890 μA/μm.

Besides I_{on} and SS, we calculated intrinsic delay time (τ) and power delay product (PDP), two crucial performance parameters. Intrinsic delay time signifies the switching speed of the FETs: a lower τ represents faster switching. It is defined as

$$\tau = \frac{Q_{on} - Q_{off}}{I_{on}} \tag{7}$$

where Q_{on} and Q_{off} represents the total charge in the channel when the device is in the on and off states, respectively. Without UL, τ ranges from 0.014 ps at $L_g = 5$ nm to 0.073 ps at $L_g = 2$ nm; outperforming the ITRS requirement (Table 2). Adding UL further reduces τ: for $L_g = 2$ nm, it decreases from 0.073 ps (UL = 0) to 0.006 (UL = 3 nm) and for $L_g = 3$ nm, from 0.017 ps (UL = 0) to 0.006 (UL = 3 nm). PDP measures energy per switching event and is obtained from

$$\text{PDP} = \frac{(Q_{on} - Q_{off})V_{dd}}{W} \tag{8}$$

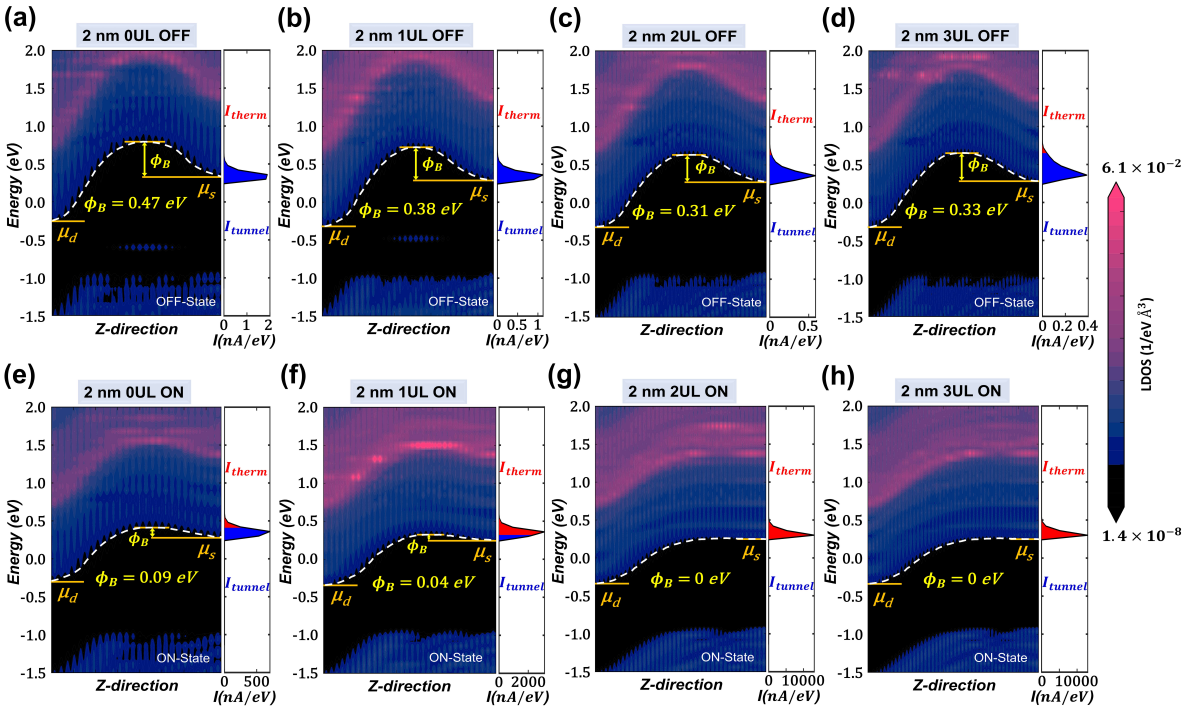


Fig. 6 Position-resolved local density of states (PLDOS) and spectral current for n-type high-performance (HP) monolayer (ML) $MoSiGeN_4$ MOSFETs at $L_g = 2$ nm. (a) 0-nm UL at the OFF-state. (b) 1-nm UL at the OFF-state. (c) 2-nm UL at the OFF-state. (d) 3-nm UL at the OFF-state. (e) 0-nm UL at the ON-state. (f) 1-nm UL at the ON-state. (g) 2-nm UL at the ON-state. (h) 3-nm UL at the ON-state

where W is the width of the channel and V_{dd} is the supply voltage. As shown in Table 2, PDP remains between 0.004 fJ/μm and 0.010 fJ/μm across all nodes: outperforming the ITRS requirement. Similar to τ, PDP decreases with the introduction of ULs for both $L_g = 2$ nm and 3 nm FETs.

A comparison against leading 2D materials [37], presented in Table 3, highlights the strong performance of $MoSiGeN_4$. The results in Table 3 show that n-type monolayer $MoSiGeN_4$ FETs, with a gate length (L_g) of 3 nm, stand out as a strong performance contender across the key parameters evaluated, outperforming other 2D channel materials such as MoS_2, InSe, Silicene, Arsenene, $MoSi_2N_4$, α-CS, WGe_2N_4, and $MoTe_2$. This comparison is carried out against other monolayer, dual-gate FETs with the same gate length ($L_g = 3$ nm), ensuring a consistent benchmarking framework across all candidate materials. Furthermore, Fig. 7(a) and Fig. 7(b) provide a visual comparative analysis of

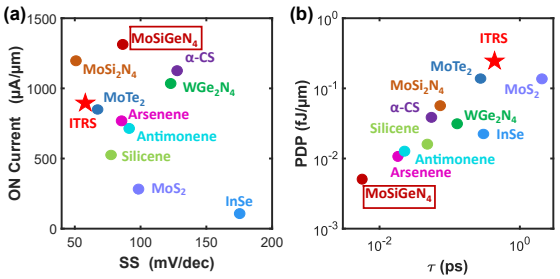


Fig. 7 (a) ON current (I_{on}) versus subthreshold swing (SS) and (b) power-delay product (PDP) versus delay (τ) for $MoSiGeN_4$ FETs compared with other 2D FETs, all considered as monolayers, at $L_g = 3$ nm

I_{on} and PDP between our results and the best-performing materials reported in the literature. Notably, $MoSiGeN_4$ combines a remarkably low PDP and switching delay with a high ON-state current (I_{on}) – attributes essential for high-speed, energy-efficient logic devices at sub-5 nm nodes.

Table 3 Comparison of Performance Parameters for Different Monolayer n-Type Materials [37]

Parameter	**$MoSiGeN_4$**	**MoS_2**	**InSe**	**Silicene**	**Arsenene**	**$MoSi_2N_4$**	**α-CS**	**WGe_2N_4**	**$MoTe_2$**	**Antimonene**
L_g**(nm)**	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
EOT(nm)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
V_{DD}**(V)**	0.64	0.64	0.64	0.64	0.64	0.64	0.64	0.64	0.64	0.64
SS(mV/dec)	86	98	176	77	87	52	128	123	67	91
I_{on}**(**μ**A/**μ**m)**	1317	267.78	107	527	757	1206	1110	1046	858.19	728
τ**(ps)**	0.006	2.052	0.294	0.047	0.020	0.074	0.057	0.130	0.260	0.022
PDP(fJ/μ**m)**	0.005	0.135	0.022	0.016	0.011	0.057	0.040	0.030	0.140	0.012

4 Conclusion

In conclusion, the DFT-NEGF study shows that monolayer $MoSiGeN_4$ double-gate FETs sustain fast switching and low power dissipation in the sub-5 nm gate length regime, meeting ITRS high-performance targets across all evaluated metrics. Without underlap, the FETs meet ITRS HP drive-current targets down to 4 nm gate length; introducing symmetric source/drain underlap restores electrostatic control and enables robust scaling down to a 2 nm gate length, delivering I_{on} exceeding 9.00×10^2 μA/μm. Both intrinsic delay and power-delay product (PDP) comfortably remain within ITRS requirements, and improve further with underlap, with delay as low as 0.006 ps and PDP within 0.004-0.010 fJ/μm across all gate lengths studied. Together, these results demonstrate that monolayer $MoSiGeN_4$ FETs achieve high switching speed and energy efficiency at gate lengths as short as 2 nm, positioning Janus $MoSiGeN_4$ as a strong candidate channel material for next-generation high-speed, low-power transistor applications, warranting further experimental investigation to confirm the observed performance gains.

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5 Statements & Declarations

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Data Availability. The data that support the findings of this study are available within the article.

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