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# *High Gain Low Elements Counts Switched Capacitor based Multi-Level Inverter*

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*Abstract:* The proposed switched capacitor multi-level inverter can be utilized in photovoltaic, fuel cell, and battery systems to generate low harmonic content at output voltage. This topology, with the help of two sources, 9 switches, 9 drivers, 2 capacitors, and 2 diodes, can produce 11 voltage levels at its output. The advantages include voltage boosting, self-balancing of the capacitors, and higher voltage levels relative to components compared to similar structures. Furthermore, having switches that work at the low frequency of 50 Hz is an important advantage that can reduce switching losses. Due to the usage of the "nearest level" modulation scheme, the switches work at 50 Hz, which can lead to low total losses. In the proposed configuration, DC energy sources, such as photovoltaics and batteries, will be utilized as input sources. A comparison between the proposed topology and similar schemes has been made in terms of the number of levels, the number of switches, voltage gain, the ratio of voltage gains to the number of switches, and the ratio of voltage levels to all device numbers. The simulation results and experimental prototype of the proposed circuit have been practically implemented to prove the effectiveness of the proposed scheme.

*Keywords:* Multi-level inverters, capacitor switching inverters, voltage stress, renewable energies, voltage boosting.

## 1. Introduction

Every year, several inverters are presented; among them, the most basic inverters can be considered classic models [1], and with the help of these basic inverters and the passage of time and increasing human knowledge, new inverters with better features have been provided. There are different types of classic multi-level inverters (MLIs); three of the most important and widely used of them are the neutral point clamped (NPC), the flying capacitor (FC), and the cascade H-bridge (CHB) [2-4].

To reduce the harmonics of the output voltage, the multi-level converters that generate step voltage can be utilized. In these inverters, a high number of output voltage levels will lead to total harmonic distortion (THD) content reduction and an increase in output voltage quality. MLIs have less voltage stress on components than traditional converters, which leads to higher efficiencies. Furthermore, due to the high-level numbers and the low harmonic content, the size of the output inductor is drastically reduced, which will reduce the weight, size, and overall cost of the inverter. The existence of such benefits will lead to the utilization of these inverters in many applications such as photovoltaics [5], hybrid energy (HES) [6], and HVDC systems [7, 8].DC sources, switches, and diodes are the basic elements of these converters. Many research studies, such as [9, 10] proposed new circuits with a low number of elements to decrease the price and sizes of the converter. Papers [11, 12] have provided topologies with fewer switches, which leads to a reduction in the number of driver circuits and, therefore, to a reduction in the price and sizes of the inverter. Because the cost, size, and weight of batteries, fuel cells, and photovoltaics are high compared to other elements, it should provide circuits with a low source number [12-14].

One way to decrease source numbers in multilevel converters is to utilize a capacitor(s), which are usually referred to as switching capacitor multilevel inverters (SCMLIs). SCMLIs, besides having the advantages of conventional MLIs, also can increase the output voltage gain of the converter [15-18]. Although many topologies use capacitors in the circuit, they do not result in a gain boost in the output voltage, as seen in the

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circuits referenced in [19] and [20]. Having the voltage balance of capacitors is the major challenge for these kinds of inverters.

The main goal in SCMLIs is to decrease the number of sources and replace them with the capacitor(s), which will lead to a reduction in size, weight, and cost of the converter with high voltage gain. In these inverters, it is possible to naturally achieve charge balance without the necessity of external auxiliary circuits. These features can decrease the cost and size of the circuit and reduce the complexity of the control strategy. It is necessary to note that the capacitance of the capacitors should be selected large enough that the voltage ripple during their longest discharge interval does not exceed an accepted value. Capacitive switching topologies have a higher number of levels compared to topologies without capacitive switching, which means they do not require an output filter, providing an advantage for this type of topology. This paper proposes an SCMLI topology that combines an MLI and an H-bridge to achieve better output voltage quality. The major goal of the presented circuit is to achieve more levels by reducing the number of switches and DC sources. Increasing the output voltage levels will result in a lower THD compared to previous articles. In this topology, the nearest-level (NL) scheme will be utilized, which causes the circuit elements (switches and diodes) to work at a low frequency. The major contributions of this article are as follows:

- Low component (switches, diodes, capacitors, drivers, sources) numbers compared to recently published articles.
- Higher ratio of output voltage levels to component numbers
- Higher ratio of output voltage gain to switch numbers compared to most of the new topologies
- Natural self-balancing of capacitors.

## 2. Proposed Topology

The proposed topology presented in this research work is depicted in Fig.1. In the proposed circuit, 9 IGBT switches are used, 8 of which are unidirectional, and $S_{1a}$ is a bidirectional power switch. In addition to 9 switches, 2 DC input voltage sources, 2 diodes, and 2 capacitors are used in the topology so that this circuit can produce voltage levels of 11 at its output voltage. The output voltage peak value is $5V_{DC}$, and since the sum of the voltages of the two input sources is $3V_{DC}$ ($V_{s0} = 2V_{DC}$, $V_{s1} = V_{DC}$), the gain of the converter will be approximately 1.66. The proposed scheme can be used for pure resistive R loads as well as for inductive R-L loads.

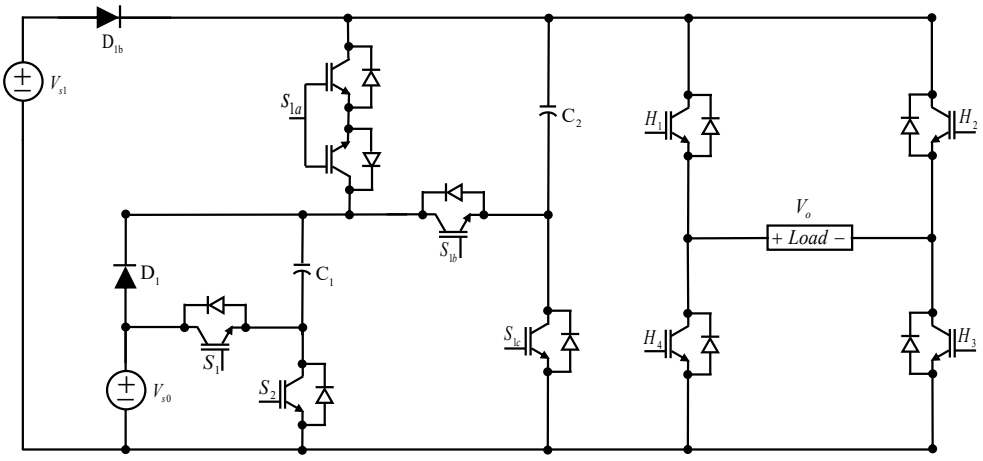



Figure 1. Proposed multilevel inverter topology

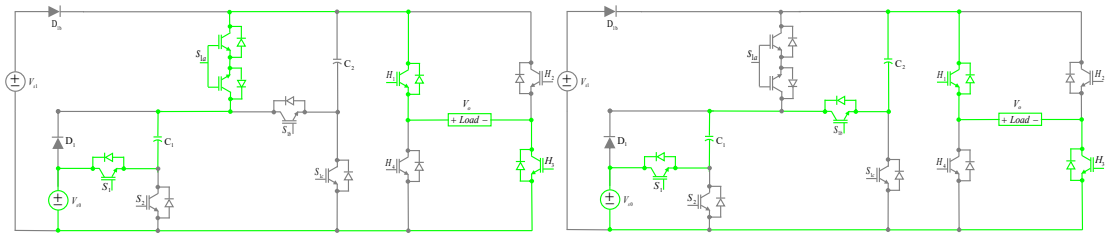
### *A. Operating modes*

Table 1 shows the different switching modes. Table 1 describes the ON or OFF states of each diode and switch, besides the charging/discharging states of the capacitors at each voltage level. Fig. 2 displays only the positive working modes of the proposed circuit. The voltage magnitudes of two power supplies are shown in equation (1).

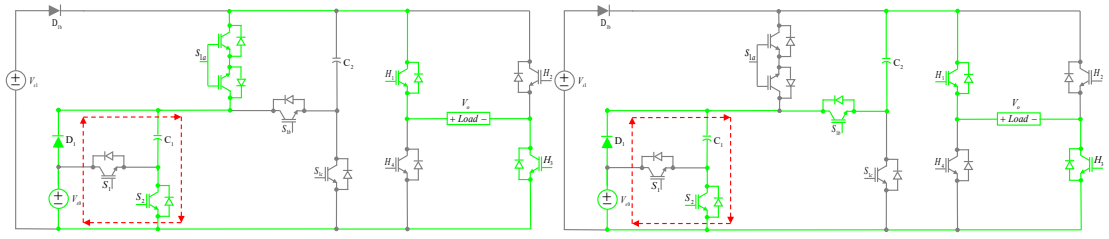
$$V_{s0} = 2V_{DC},\ V_{s1} = V_{DC}. \tag{1}$$

Table 1. Switching table of the proposed converter.

| $C_2$ | $C_1$ | $D_{1b}$ | $D_1$ | $H_4$ | $H_3$ | $H_2$ | $H_1$ | $S_{1c}$ | $S_{1b}$ | $S_{1a}$ | $S_2$ | $S_1$ | Output Voltage |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | D | OFF | OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | $V_{s0}+V_{C1}+V_{C2}$ |
| - | D | OFF | OFF | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $V_{s0}+V_{C1}$ |
| D | C | OFF | ON | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | $V_{s0}+V_{c2}$ |
| - | C | OFF | ON | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | $V_{s0}$ |
| C | C | ON | ON | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | $V_{s1}$ |
| C | C | ON | ON | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| C | C | ON | ON | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $-(V_{s1})$ |
| - | C | OFF | ON | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | $-(V_{s0})$ |
| D | C | OFF | ON | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | $-(V_{s0}+V_{c2})$ |
| - | D | OFF | OFF | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | $-(V_{s0}+V_{C1})$ |
| D | D | OFF | OFF | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | $-(V_{s0}+V_{C1}+V_{C2})$ |




a b




c d

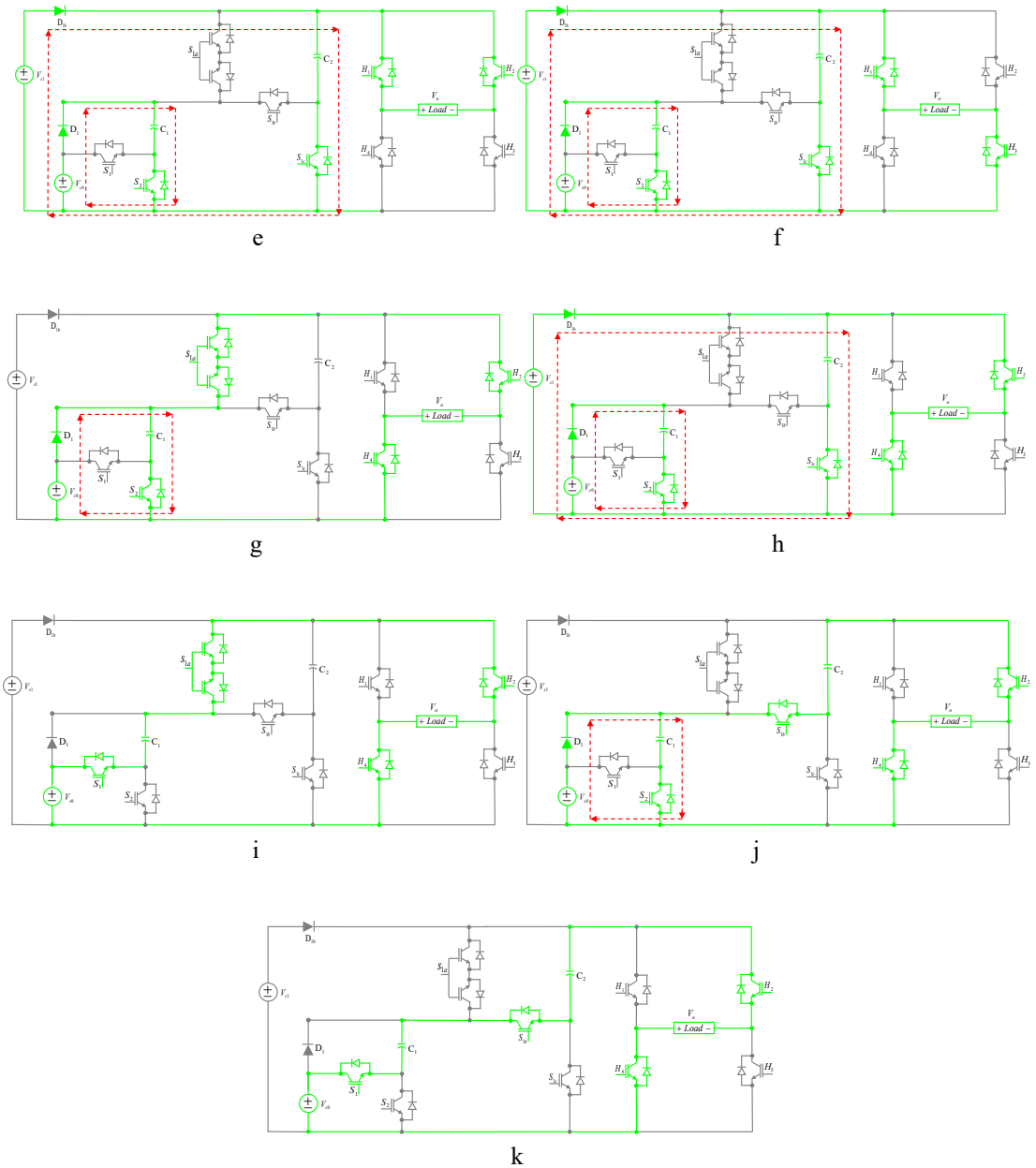



Figure 2. Operating modes of the proposed 11-level structure and mode a [$V_o$=5$V_{DC}$], b [$V_o$=4$V_{DC}$], c [$V_o$=3$V_{DC}$], d [$V_o$=2$V_{DC}$], e [$V_o$=$V_{DC}$], f [$V_o$=0], g [$V_o$=-$V_{DC}$], h [$V_o$=-2$V_{DC}$], i [$V_o$=-3$V_{DC}$], j [$V_o$=-4$V_{DC}$] and k [$V_o$=-5$V_{DC}$].

Switches $S_1$ and $S_2$ should not be turned on at the same time. If these two switches are turned on at the same time, the input source $V_{s0}$ will be short-circuited. Also, the H-bridge switches on one leg should not be on at the same time. Therefore, care must be taken in switching and applying the signal to the switches that can be short-circuited in the topology, and a dead time must be given between the two switches to prevent unwanted short-circuiting.

## B. *Comparative analysis*

Table 2 compares the proposed converter in terms of level numbers, semiconductors, drivers, input voltage sources, capacitors, diodes, ratio of voltage gain to switch numbers, ratio of levels to devices (switches, diodes, sources, capacitors, and drives), and voltage gain with topologies based on capacitive switching. Compared to [21], the proposed circuit has higher-level numbers with a reduced number of input sources, which enables the reduction of

THD as well as fewer solar cells (photovoltaics). Furthermore, the topology [21] has a lower voltage gain despite the use of more capacitors than the proposed topology. The topology [22] has a better number of levels than the proposed topology, but the production of these levels is done with the help of more input voltage sources, which increases the final construction cost. Additionally, this topology, which uses 4 capacitors, is unable to produce a voltage gain greater than one. Topologies [23], [24], [25], [26] have equal or lower levels than the proposed topology, while they produced lower levels with a higher switch number than the proposed circuit.

The ratio of voltage gain to switch numbers (*GS*) at all the topologies, except the topology [27], which used more switches than our proposed topology, is higher than the proposed schemes. Although the Structure [28] generates a higher number of output voltage levels, it exhibits a lower *GS* compared to the proposed topology. Schemes [27], [29] and [30] have lower levels with a higher number of switches. Furthermore, our scheme has a higher ratio of level numbers to components than all other topologies in Table 2. Based on this table, our proposed circuit has lower component (switches, diodes, capacitors, drivers, and sources) numbers compared to other topologies.

To provide a fair comparison of voltage stress among different topologies, the Total Blocking Voltage (*TBV*) and the Normalized Total Blocking Voltage (*NTBV*) are considered. The *NTBV* is calculated as:

$$NTBV = \frac{TBV}{V_{o,\max}} \tag{2}$$

where $V_{o,max}$ denotes the maximum obtainable output voltage. This normalization enables a meaningful comparison between topologies with different voltage gains and output voltage levels.

In this study, a modified cost function is proposed to simultaneously account for the number of switches, gate drivers, voltage stress, passive components, DC sources, and component utilization efficiency. The proposed cost function is expressed as equation (3).

$$CF = \frac{\left(N_{SW} + N_{Dr} + \alpha NTBV + \beta\left(N_{Ca} + N_{SO} - 1\right)\right)\left(1 - RLD\right)}{N_L} \tag{3}$$

where $\alpha$ and $\beta$ are weighting coefficients associated with the normalized voltage stress and the passive/source-related complexity, respectively. In this work, $\beta$ is fixed at 2, while two different values of $\alpha$ (0.5 and 1.5) are considered to investigate the sensitivity of the cost function to voltage stress. The inclusion of the factor ($1 - RLD$) allows the cost function to penalize topologies with poor level density, thereby rewarding structures capable of generating a larger number of voltage levels with fewer components. The term ($N_{Ca} + N_{SO} - 1$) is used to avoid penalizing the existence of the mandatory first DC source, while additional sources and capacitors contribute to the overall implementation complexity.

Table 2**.** Comparison of proposed topology components with recently published papers.

| Parameter | [21](a) | [22](b) | [23](c) | [24](d) | [25](e) | [26](f) | [27](g) | [28](h) | [29](i) | [30](j) | Proposed |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_L$ | 9 | 13 | 11 | 9 | 9 | 7 | 9 | 13 | 9 | 9 | 11 |
| $N_{SW}$ | 8 | 12 | 11 | 14 | 10 | 10 | 11 | 12 | 10 | 11 | 9 |
| $N_{Dr}$ | 8 | 12 | 11 | 14 | 10 | 10 | 11 | 12 | 10 | 11 | 9 |
| $N_{SO}$ | 4 | 3 | 2 | 2 | 1 | 1 | 1 | 2 | 1 | 1 | 2 |
| $N_{Ca}$ | 4 | 4 | 1 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | 2 |
| $N_d$ | 2 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 2 | 2 |
| *G* | 1 | 1 | 1.5 | 2 | 0.5 | 1.5 | 4 | 2 | 1.5 | 1 | 1.67 |
| *RLD* | 0.37 | 0.42 | 0.44 | 0.28 | 0.37 | 0.29 | 0.34 | 0.46 | 0.36 | 0.37 | 0.5 |
| *GS* | 0.16 | 0.08 | 0.13 | 0.14 | 0.05 | 0.18 | 0.36 | 0.16 | 0.1 | 0.09 | 0.18 |
| $N_C$ | 24 | 31 | 25 | 32 | 24 | 24 | 26 | 28 | 25 | 24 | 22 |
| *CF* $\alpha$=0.5, $\beta$=2 | 1.65 | 1.66 | 1.43 | 2.93 | 1.96 | 3.04 | 2.08 | 1.35 | 2.15 | 2.34 | 1.29 |
| *CF* | 2.67 | 1.78 | 1.65 | 3.37 | 2.52 | 4.26 | 2.45 | 1.55 | 2.49 | 2.81 | 1.69 |

| $\alpha$=1.5, $\beta$=2 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| *TBV* | 5.5$V_{DC}$ | 16$V_{DC}$ | 22$V_{DC}$ | 22$V_{DC}$ | 4$V_{DC}$ | 18$V_{DC}$ | 20$V_{DC}$ | 20$V_{DC}$ | 7$V_{DC}$ | 6.75$V_{DC}$ | 15$V_{DC}$ |
| *NTBV* | 5.5 | 2.67 | 4.4 | 5.5 | 8 | 12 | 5 | 5 | 4.67 | 6.75 | 8.9 |

*$N_L$=Number of levels, $N_{SW}$=Number of switches, $N_{Dr}$=Number of drivers, $N_{SO}$=Number of Sources, $N_{Ca}$= Number of capacitors and $G$=Gain, $RLD$=($N_L/N_C$): Relative Level Density, $GS$=($G/N_{SW}$), $N_C$= Number of Components, $CF$=Cost Function, $TBV$=Total Blocking Voltage, $NTBV$=Normalized Total Blocking Voltage: $NTBV$=($TBV/V_{o,max}$)

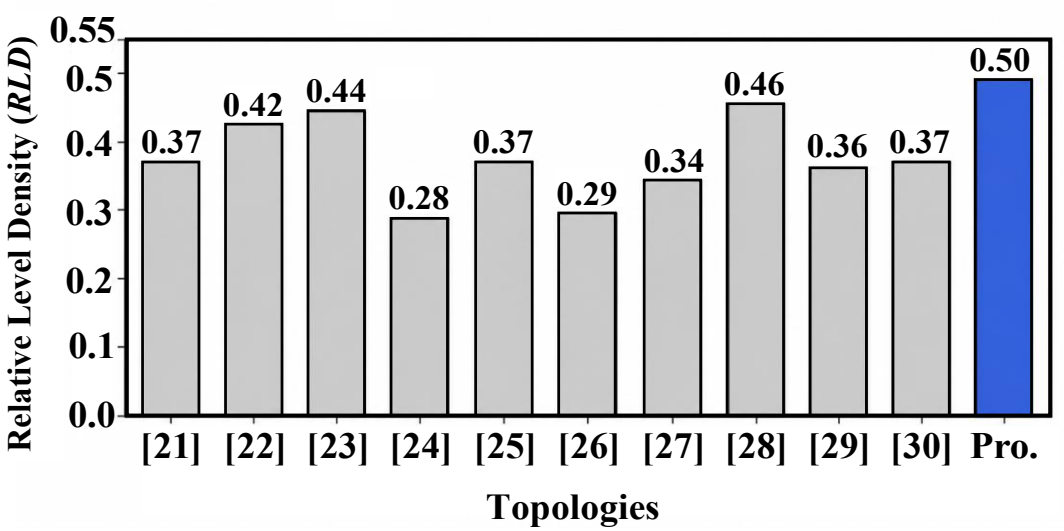
According to Table 2, the proposed topology achieves the highest *RLD* value of 0.5 among all compared structures, indicating superior component utilization efficiency. Furthermore, despite generating 11 output voltage levels using only two DC sources and two capacitors, the proposed inverter requires a relatively low number of components ($N_C$ = 22). For both weighting scenarios ($\alpha$ = 0.5 and $\alpha$ = 1.5), the proposed topology exhibits the lowest cost function values of 1.29 and 1.69, respectively. These results demonstrate that the proposed inverter maintains an effective trade-off between component count, voltage stress, voltage gain, and level generation capability, making it a competitive candidate for medium-voltage switched-capacitor multilevel inverter applications.

Table 2 presents a comprehensive comparison between the proposed topology and recently reported multilevel inverters in terms of the number of output levels, semiconductor switches, gate drivers, DC sources, capacitors, voltage gain, relative level density (*RLD*), gain-to-switch ratio (*GS*), component count, normalized total blocking voltage (*NTBV*), and the proposed cost function (*CF*). Unlike conventional comparisons that mainly rely on the number of components or voltage gain, the adopted evaluation incorporates multiple structural and electrical indices to provide a more balanced assessment of converter performance.

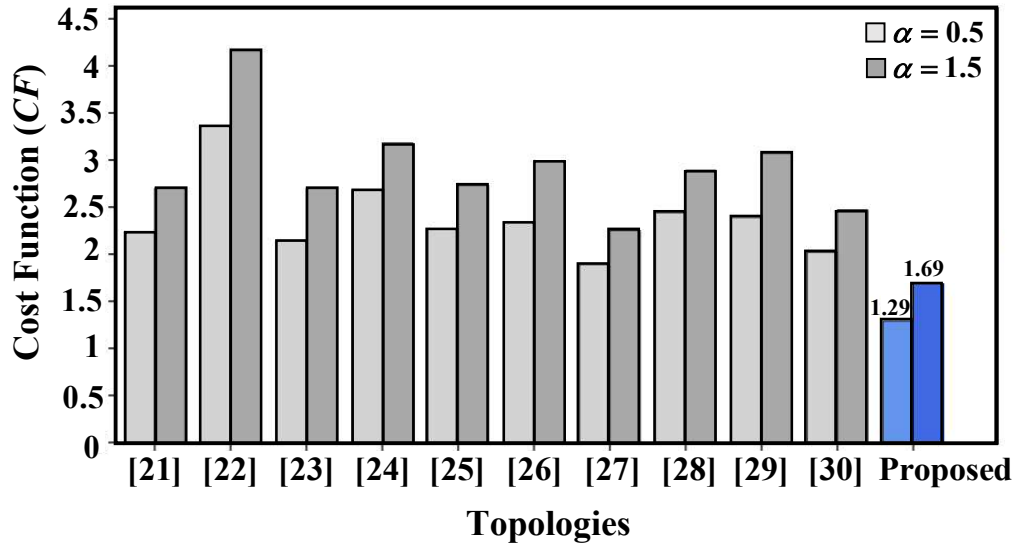
As can be observed, the proposed topology generates 11 output voltage levels using only two isolated DC sources and two switched capacitors while requiring only 22 components, resulting in the highest *RLD* value (0.5) among all compared topologies. This indicates a superior utilization of hardware resources for generating output voltage levels.

To further highlight the comparative performance, the *RLD* and *CF* values are illustrated in Fig. 3(a) and (b) respectively. The *RLD* comparison confirms that the proposed converter achieves the highest level density, whereas the *CF* comparison demonstrates the lowest cost function under both weighting scenarios ($\alpha$=0.5 and $\alpha$=1.5). These results verify that the proposed topology provides an improved balance between hardware complexity, voltage stress, and output performance.

Furthermore, the multidimensional comparison shown in Fig. 4 simultaneously visualizes the component count, cost function, output levels, and *RLD* using a bubble chart. The proposed topology is clearly positioned in the desirable lower-left region of the diagram, corresponding to fewer components and a lower cost function, while its larger *RLD* further emphasizes its structural efficiency. This graphical representation confirms that the proposed converter offers a favorable trade-off between hardware utilization and electrical performance compared with recently published counterparts.




(a)




(b)

**Figure 3. Comparison results: a) Relative Level Density (*RLD*) bar chart of proposed converter and other topologies, b) Cost Function (*CF*) bar chart for different values of *α***

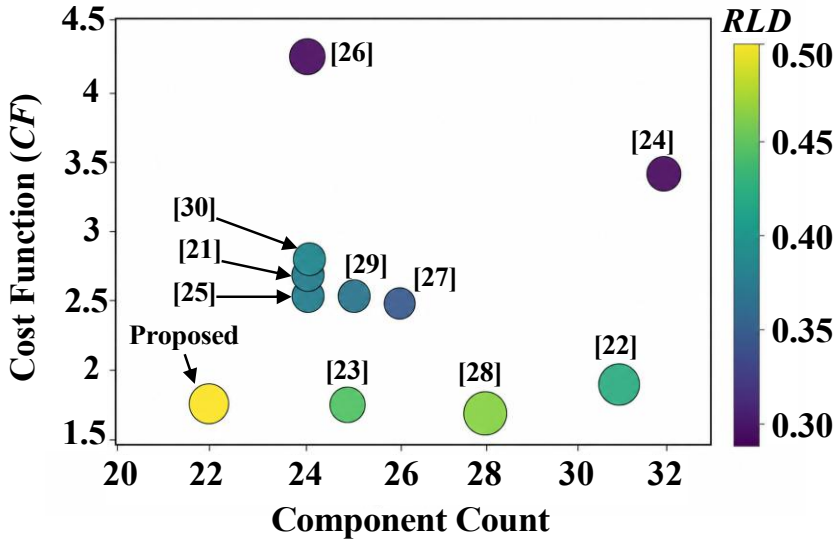



**Figure 4. Comparison of proposed converter with other topologies in terms of Cost Function (*CF*), Component Count and Relative Level Density (*RLD*), presented as a bubble chart**

## 3. Results and Discussion

### *A. Simulation results*

To evaluate the proposed 11-level topology feasibility, the topology is simulated with the help of PSCAD/EMTDC software. Simulation results for input sources $V_{s0}$=122 V and $V_{s1}$=61 V, R-L load (R=180 Ω, L=600 mH), and $C_1$=2000 µF and $C_2$=1500 µF are provided. Fig. 5 depicts the 11-level output voltage of the proposed circuit with the help of the NL switching method. The peak values of the output voltage and load current are approximately equal to 305 volts and 1.27 A, respectively. Therefore, the output voltage gain is 1.66.

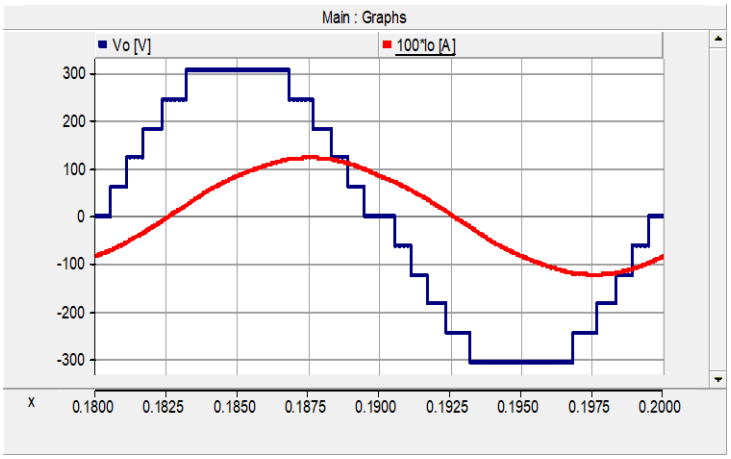



Figure 5. 11 level output voltage and current, simulation

### *B. Experimental results*

To evaluate the performance and effectiveness of the proposed 11-level topology with two sources, an experimental prototype has been made that is depicted in Fig. 6. In this prototype, two DC sources, 8 unidirectional and one bidirectional switches, 9 driver circuits, 2 capacitors, and 2 diodes are used. The elements of the proposed circuit have been shown in Table 3. Fig. 7 shows the output current and voltage waveforms of the proposed circuit. Input sources in this topology are provided 61 and 122 volts, and according to the voltage gain of 1.66 for the proposed scheme, the voltage generated at the output of the topology should be 305 volts, but because of voltage drop at the parasitic elements of switches, diodes, and capacitors, the output voltage is less than the 305 volts that we obtain in the

simulation results of Fig. 5. The maximum value of output current is approximately equal to 1.2 amps under inductive load. So the output power is 190 W (225*1.2/1.41).

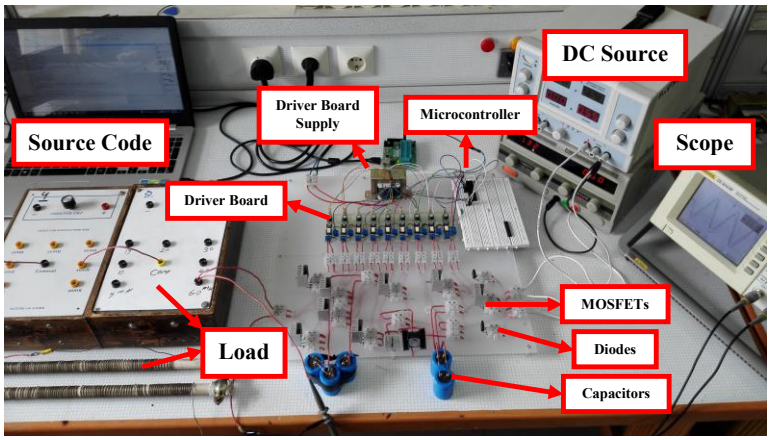



Figure 6. Laboratory prototype of the proposed topology

Table 3. Elements of proposed circuit

| Parameter | Value/Type |
|---|---|
| Input DC Source | $V_{S0}$=122[V], $V_{S1}$=61[V] |
| Frequency | $f_o$=50 [Hz] |
| MOSFETs | IRFP450APBF |
| Diodes | SFAF1606G |
| Optocoupler-Drivers | TLP250 |
| Capacitances | $C_1$= 2000[µF], $C_2$= 1500[µF] |
| Microcontroller | ATmega16 |

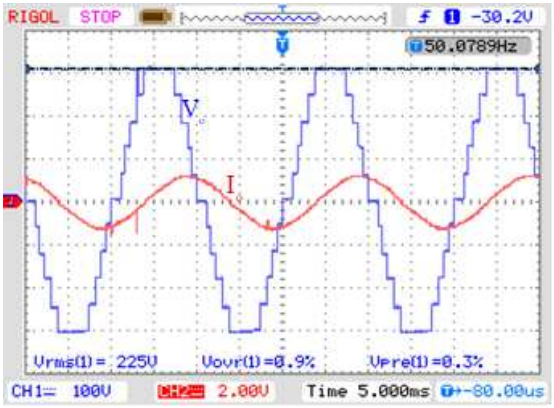
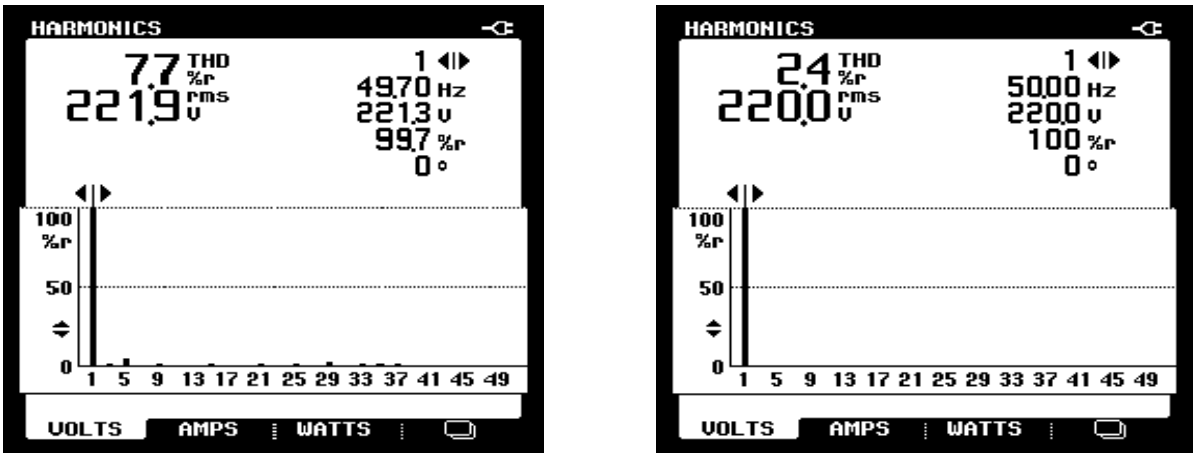



Figure 7. Depicts of current and voltage, experimental

The output voltages' harmonic content of the proposed 11-level structure is depicted in Fig. 8. In Fig. 8(a) the THD is more than the acceptable level of 5% based on standards of IEEE & IEC. This figure shows the result without utilizing the output filter [20]. With a small inductive (L) filter, the THD can be reduced to less than 3%, as can be seen in Fig. 8(b). Based on IEEE and IEC standards, the acceptable THD is less than or equal to 5%. Fig. 9 depicts the experimental results under a high inductive load of R = 110 Ω, L = 60 mH. These experimental results verify that the presented circuit can be utilized in industrial applications. Waveforms are depicted in Fig. 10 under a pure resistive load of R = 270 Ω.




(a) (b)

Figure 8. a) THD of output voltage without output filter, b) Output voltage THD with output filter

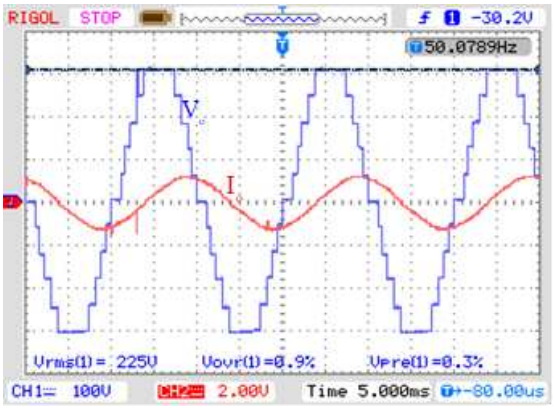



Figure 9. Output current and voltage waveforms under R= 110 and L = 60 mH

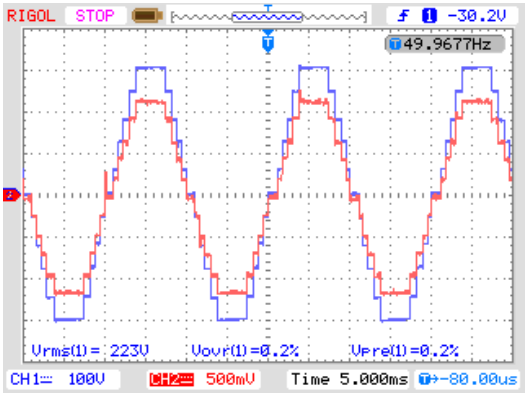



Figure. 10. Output current and voltage waveforms under pure resistance of R = 270 ohm

## 4. PWM strategy

The PWM signals for IGBTs are generated by the nearest level method. The nearest level method for the proposed 11-level inverter has been demonstrated in Fig. 11. As shown in Fig. 10, in this PWM strategy the sinusoidal reference wave has been compared with multi-level output voltage and the required pulses produced.

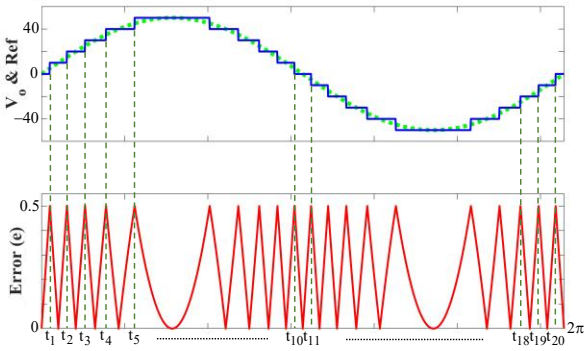



Figure 11. Nearest level PWM

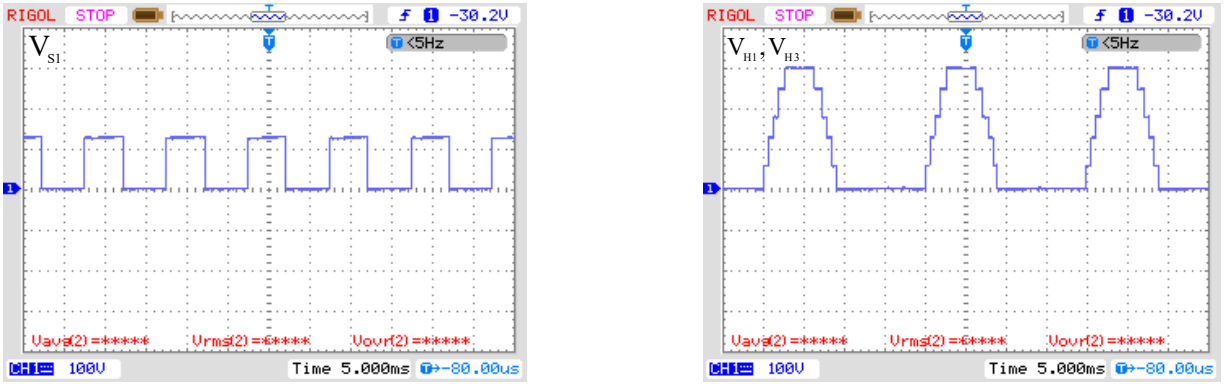
## 5. Voltage stress of switches

Voltage stress of switches is depicted in Fig. 10. As we can see from Fig. 12, the $S_1$ voltage stress is only 2 $V_{DC}$, but for $H_1$ and $H_3$ it is 5 $V_{DC}$ ($V_{s0} = 2V_{DC}$, $V_{DC} = 61$ V, $V_{s1} = V_{DC}$ ). Table 4 demonstrates the voltage stress of all diodes and switches. For better comparison, another characteristic for measuring the *VS* of the elements is defined, which is known as the normalized blocking voltage (*NBV*). The normalized blocking voltage (*NBV*) is calculated by equation (4). The *NBV* is equal to the ratio of the blocking voltage (*BV*) of each semiconductor to the peak value of output voltage. According to Table 4, except for H-bridge switches whose voltage stress is equal to output voltage, the voltage stress of other switches ($S_1$, $S_2$, $S_{1a}$, $S_{2b}$, $S_{3c}$) is less than output voltage.

$$NBV = \frac{BV_{Semiconductor}}{V_{o,\max}} . \tag{4}$$

Table 4. *BV*, *NBV* of all switches and diodes

| Switch | *BV* | *NBV* [%] | Switch | *NBV* [%] | Diode | *BV* |
|---|---|---|---|---|---|---|
| $S_1$ | $2V_{DC}$ | 40 | $H_1$ | 100 | $D_1$ | 2 $V_{DC}$ |
| $S_2$ | 2 $V_{DC}$ | 40 | $H_2$ | 100 | | |
| $S_{1a}$ | 1 $V_{DC}$ | 20 | $H_3$ | 100 | $D_{1b}$ | 4 $V_{DC}$ |
| $S_{1b}$ | 2 $V_{DC}$ | 40 | $H_4$ | 100 | | |
| $S_{1c}$ | 4 $V_{DC}$ | 80 | | | | |




(a) (b)

Figure. 12. Voltage stress of switches(a) $S_1$ and (b) $H_1$, $H_3$

## 6. Capacitor voltage balancing

The voltage waveforms of capacitors $C_1$ and $C_2$ are presented in Fig. 13. The results show that the capacitors' voltages of $C_1$ and $C_2$ are normally set to 122 $V_{dc}$ and 61 $V_{dc}$, respectively. It is also evident from these results that both charge/discharge processes of the two capacitors are uniformly distributed during the switching period. Thus,

without utilizing the extra circuitry, the self-balancing of two capacitors is confirmed. The voltage ripples of $C_1$ & $C_2$ are depicted on Fig. 14 (a) & (b), respectively. The voltage ripple for $C_1$ is around 1% and for $C_2$ is around 5%.

*A. Capacitor selection*

Based on Table 1 and Figs. 2 & 10, the capacity $C_1$ has a longer discharging interval compared to $C_2$. During $V_4$ and $V_5$ intervals, capacitor $C_1$ is discharging, but capacitor $C_2$ is discharging only in the $V_5$ interval. It should be mentioned that the $V_5$ interval has the longest duration (almost 4 times longer than the other intervals). The charge value that discharged from $C_1$ during the $V_4$+$V_5$ interval can be obtained by:

$$\Delta Q_1 = 6\int_{t_4}^{t_5} i_L(t)\, dt \tag{5}$$

And for $C_2$ is:

$$\Delta Q_2 = 3\int_{t_4}^{t_5} i_L(t)\, dt \tag{6}$$

where $\Delta Q_1$ is the discharge value of $C_1$, $i_L$ is maximum load current under pure resistive load, and $\Delta Q_2$ is discharge value of capacitor $C_2$.

So, the capacitors $C_1$ and $C_2$ can be selected by (7) and (8), respectively.

$$C_1 \geq \frac{\Delta Q_1}{\Delta v} \tag{7}$$

$$C_2 \geq \frac{\Delta Q_2}{\Delta v} \tag{8}$$

where, $\Delta v$ is the acceptable voltage ripple that is between 5% and 10% .

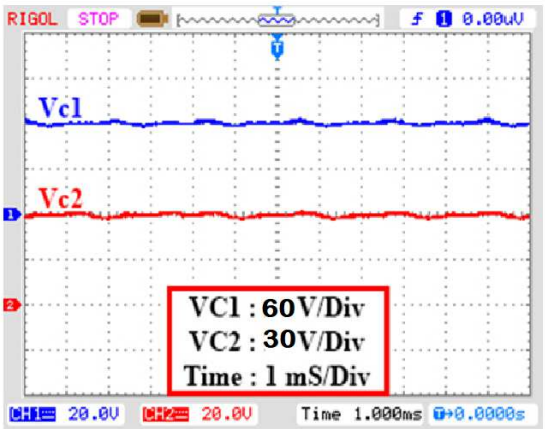
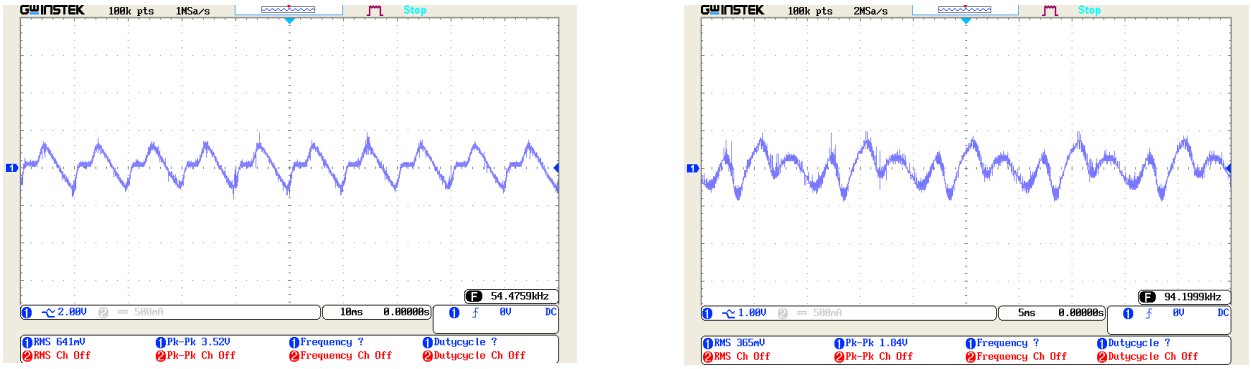



Figure. 13 The voltage depicts of $V_{C1}$ & $V_{C2}$




(a) (b)

Figure. 14. Voltage ripples of (a) $C_1$, and (b) $C_2$

## 7. Efficiency

By measuring the input and output powers with a power analyzer (Fluke 43B), the efficiency can be calculated, and the results under various loads are shown in Fig. 15. Based on the scope of Fig. 7, for the rated condition, the RMS value of output voltage of 225 V and maximum current of 1.2, the output power is 190 W (= 225*(1.2/1.41)= 190W). Input power equals the sum of two sources' power (almost equal to 196 W), so efficiency under rated conditions is 97%. Furthermore, the power analyzer can be utilized to measure both input powers and output power. Fig. 13 shows that the proposed topology gives a maximum efficiency of 97.2% at an output power of 200 W (almost the rated power of 190 W) and provides an efficiency value of 96% at an output power of 300 W. The detailed analysis of power losses is as follows.

### *A. Power Loss Analysis*

There are several types of losses in the proposed topology, which include conductor losses, switching losses, and capacitor voltage ripple losses. The reasons for the losses are the parasitic effects of all elements (such as voltage drops of switches and diodes) and the voltage ripple of the capacitors. By reducing these three losses, the converter can be turned into higher efficiency and be more ideal. From equation (9), the total loss can be calculated with a small approximation.

$$P_{Loss}^{Total} = \sum (P_{Loss}^{Conduction} + P_{Loss}^{Switching} + P_{Loss}^{Ripple}) . \tag{9}$$

### *B. Conductive losses*

Conductive losses occur in power switches, power diodes, anti-parallel diodes, and capacitors. Power switches and power diodes have conductive resistance, and power diodes have a voltage forward drop (VFD), and capacitors also have an equivalent series resistance (ESR), which causes conduction losses. The total conduction losses of the proposed topology can be obtained.

$$\begin{aligned} P_{Loss,cond} &= P_{cond,switch} + P_{cond,Diode} + P_{cond,capacitors} \\ &= \mathrm{R}_{on}^{switch} I_{rms,switch}^2 + (\frac{1}{T}\int_0^T V_{DF} i_{out}(t)dt) + R_{ESR} I_{rms,capacitor}^2 \end{aligned} \tag{10}$$

### *C. Switching losses*

In power converters, when a switch changes from off to on or vice versa, the non-ideal nature of the switches means that there is a delay in turning on ($t_{on}$) and turning off ($t_{off}$), collectively referred to as "switching time". During these switching times, some losses occur in the switches, which are known as switching losses. Switching losses can be evaluated in one working period. For example, for the Kth switch, the switching losses, besides the switching times, are related to the current stress of the switch ($I_k$), the voltage stress of the switch ($V_{swk}$), and the number of switchings on and off ($N_{on,k}$, $N_{off,k}$) in each working period.

$$P_{Loss,switching} = \frac{1}{6T} V_{swk} I_k (N_{on,k} t_{on} + N_{off,k} t_{off}) \tag{11}$$

*D. Voltage ripple losses of capacitors*

Due to the difference between the input voltage of the power supply ($V_{dc}$) and the capacitor voltage ($V_C$), capacitor voltage ripple losses occur. If the voltage ripple of the capacitor is higher than the standard value when supplying the load, more current is drawn from the capacitor to supply the load, which has almost constant power. As a result, with the increase in capacitor current, the conductivity loss of the converter increases. This type of loss can be calculated from equation (12), so the capacitor voltage ripple loss depends on capacitor capacity ($C_P$) and capacitor voltage ripple ($\Delta V$).

$$P_{ripC_P} = \frac{1}{2T} C_P (\Delta V_{CP})^2 \tag{12}$$

The efficiency of the converter is obtained according to Fig. 13 by measuring the powers and applying the relation in equation (13). It should be noted that, due to laboratory limitations, the topology has been tested with low input voltage and low power.

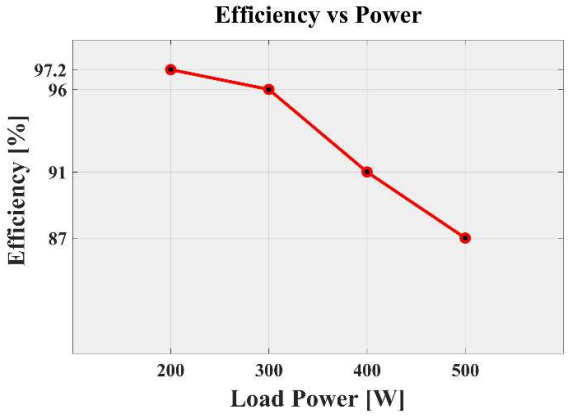



Figure 15. Experimental efficiency under different loads

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \tag{13}$$

## 8. Conclusion

The proposed topology utilizes two isolated DC sources, nine power switches, nine gate drivers, two switched capacitors, and two diodes to generate an 11-level output voltage waveform while achieving a voltage gain of 1.67. Owing to the switched-capacitor structure, the converter provides natural capacitor voltage self-balancing without requiring additional control circuitry. The proposed converter operates properly under both resistive and R-L loads, and the experimental results confirm satisfactory output voltage and current waveforms with acceptable harmonic performance without using an output filter. To provide a comprehensive evaluation, the proposed converter is compared with recently published multilevel inverter topologies using several structural and electrical performance indices, including the relative level density (*RLD*), gain-to-switch ratio (*GS*), normalized total blocking voltage (NTBV), and a modified cost function (*CF*). The comparative results indicate that the proposed topology achieves the highest RLD among the considered converters while maintaining the lowest cost function under different weighting factors. In addition, the proposed converter requires only 22 components, resulting in a favorable balance between hardware complexity, voltage stress, and output voltage capability. The accompanying comparative bar and bubble

charts further illustrate these characteristics and provide a clear visualization of the performance–complexity trade-off achieved by the proposed topology.

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The authors declare that no external funding was received for this study.

## 10. Data availability

All data generated or analyzed during this study, including simulation results, experimental waveforms, measurement results, and photographs of the experimental implementation of the proposed converter, are included in this published article.

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