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Amorphous High-κ Dielectrics for Top-Gate Integration in 2D Semiconductor Transistors

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High-κ dielectrics compatible with two-dimensional (2D) semiconductors and their reliable integration remain key bottlenecks limiting the development of 2D semiconductor electronics. Here, we introduce a room-temperature fabrication strategy that combines magnetron sputtering with a van der Waals assembly process to form amorphous high-κ top-gate dielectrics on 2D semiconductors. Amorphous dielectric materials feature no grain boundaries, atomically smooth surfaces, and uniform dielectric properties. Magnetron sputtering is demonstrated as a general deposition approach for various amorphous high-κ dielectrics, including $CaCu_3Ti_4O_{12}$ (CCTO), $BaTiO_3$ (BTO), and Ga_2O_3. To avoid direct sputter-induced damage to the 2D semiconductor channel, an efficient transfer strategy is developed that exploits the strong hydrophilicity of freshly deposited SiO_x (contact angle of ~0°) and the extremely weak adhesion of the SiO_x-Au interface (adhesion strength of ~0.14 MPa). Top-gate MoS_2 transistors incorporating such amorphous high-κ dielectrics exhibit excellent electrical characteristics. In particular, the top-gate MoS_2 transistor with the CCTO dielectric (relative dielectric constant κ of ~46 as the maximum value) achieved a near-Boltzmann-limit subthreshold swing of 60 mV/decade and an on/off ratio exceeding 10^6. Our work identifies amorphous high-κ dielectrics as a new material system for 2D semiconductor-compatible top-gate dielectrics in future nanoelectronics.

Introduction

Two-dimensional (2D) semiconductors demonstrate significant potential for enabling low power consumption, large-scale integration, and continued device scaling following the Moore's law, owing to their atomically thin thickness and dangling-bond-free surfaces[1, 2]. In company with the 2D semiconductor channel, the gate dielectric is also an essential component in transistors for charge accumulation to realize switching[3, 4]. However, the absence of a dielectric layer that simultaneously provides high capacitance and low leakage current often limits the performance of 2D transistors below theoretical expectations[5]. Furthermore, searching for materials with high dielectric constants (κ) and integrating the dielectric layers onto 2D semiconductor channel surfaces remain critical challenges in the fabrication of 2D transistors[6-8].

High-κ oxide dielectrics synthesized via atomic layer deposition (ALD), such as Al_2O_3, HfO_2, and ZrO_2, are usually considered as superior alternatives to conventional SiO_2 gate dielectric[9-12]. However, a significant challenge remains in the ALD of dielectric materials directly deposited onto the 2D semiconductor channels, because the dangling-bond-free surfaces of 2D semiconductors lack the nucleation sites required for the chemical reactions involved in the ALD processes[13]. Considerable efforts have been dedicated to overcoming this limitation, including the introduction of seeding or buffer layers[14-16] and the transfer strategies[17, 18]. Nevertheless, the reliance of ALD on highly reactive precursors restricts the variety of dielectric materials that can be prepared, and conventional ALD-compatible oxides, including HfO_2 and Al_2O_3, exhibit relatively low dielectric constants. Additionally, the elevated temperatures and reactive substances involved in the ALD process may degrade the electrical properties of the underlying 2D semiconductor channels.

Native oxides fabricated through oxidation are also promising candidates for high-performance gate dielectrics. Inspired by the Si/SiO_2 system, Lai et al. demonstrated the partial oxidation of the 2D semiconductor HfS_2 into HfO_2, achieving high-quality gate dielectrics and enabling high-performance transistors[19]. And the synthesis of Bi_2SeO_5, a native oxide with a dielectric constant of approximately 22, has been achieved by oxidizing Bi_2O_2Se, which simultaneously serves as the channel[7, 20, 21]. In addition, some other oxides can also be obtained as the top-gate dielectrics by direct oxidation of their corresponding metals, including Ga_2O_3[22], Al_2O_3[23], and Y_2O_3[24].

Other crystalline dielectric flakes, fabricated by exfoliation, chemical vapor deposition (CVD), pulsed laser deposition (PLD) or chemical vapor transport (CVT), offer a rich material palette for gate dielectric applications, including van der Waals layered materials (hBN[25]), perovskite oxide ($SrTiO_3$[26, 27]), perovskite-like niobates ($MgNb_2O_6$[28], $CaNb_2O_6$[29], $Sr_2Nb_3O_{10}$[30]), rare earth compounds (Gd_2O_5[31], GdOCl[32], $Sm_2O_2SO_4$[33]), transition metal oxides (Mn_3O_4[34], MoO_3[35]), and transition metal thiophosphates ($Cu_{0.8}Ag_{0.2}InP_2S_6$[36]). Recently, $KBe_2BO_3F_2$ has also been exfoliated as a top-gate dielectric, simultaneously achieving a high bulk dielectric constant and a wide bandgap[37].

To meet the demands of integrated circuit applications, large-scale high-quality dielectric films have been realized through diverse synthesis routes. Representative examples include CaF_2 grown by molecular-beam epitaxy (MBE)[38], single-crystalline Al_2O_3 obtained via intercalative oxidation[23], Sb_2O_3 prepared by thermal evaporation[39] or CVD[40], Y_2O_3 formed through thermal evaporation followed by oxidation[24], MoO_3 derived from the direct oxidation of a monolayer MoS_2 film[41], and $CaCu_3Ti_4O_{12}$ (CCTO) synthesized using wet-chemistry method[42]. Supplementary Table S1 summarizes representative studies on high-κ dielectrics fabricated by various methods.

Compared with ALD, CVD, PLD, CVT, and MBE, etc., magnetron sputtering offers distinct advantages as an industrially compatible technique, including high deposition rates, low process temperatures, excellent scalability, and broad material versatility (A detailed comparison of the advantages and limitations of each method is provided in Supplementary Table S2). However, research on the utilization of magnetron sputtering for gate dielectrics in 2D semiconductor transistors remains limited[43], particularly for top-gate architectures, due to the damage effects of energetic ion bombardment on the 2D channels. On the other hand, in comparison with crystalline dielectrics, amorphous high-κ dielectrics offer the advantage of eliminating adverse effects associated with grain boundaries and defects as demonstrated in silicon transistors[44, 45]. Efficiently introducing compatible amorphous high-κ dielectric materials, especially materials with dielectric constants exceeding those of conventional ALD-fabricated dielectrics (e.g., HfO_2, ZrO_2, typically $\kappa < 20$), into 2D semiconductor transistors remains a challenge.

Here, we propose a general fabrication strategy that integrates magnetron-sputtered amorphous high-κ dielectrics with 2D semiconductors for top-gate transistor fabrication. And a transfer technique that

established a van der Waals interface between the dielectric and the channel was applied to address the damage issue in conventional sputtering processes. Our strategy is compatible with sputtered amorphous high-κ dielectric films, including copper calcium titanate ($CaCu_3Ti_4O_{12}$, CCTO), barium titanate ($BaTiO_3$, BTO), and gallium oxide (Ga_2O_3), as well as ALD-deposited hafnium oxide (HfO_2) films. Utilizing this method, top-gate transistors were fabricated, with CVD-grown MoS_2 and exfoliated $MoTe_2$ as the channels and the emerging amorphous high-κ materials (CCTO, BTO, and Ga_2O_3) as the dielectrics, achieving a minimum subthreshold swing (*SS*) approaching 60 mV/decade.

Results

Fabrication and integration of the sputtered amorphous high-κ dielectrics

The fabrication strategy for the stacked top gate on the 2D semiconductor channel, consisting of a sputtered amorphous high-κ dielectric and a metal gate electrode, is outlined in Fig. 1. The processes commence with the sequential deposition of a fresh SiO_x layer, an Au film and a dielectric layer on a SiO_2/Si substrate, as shown in Fig. 1a. The dielectric can be selected from magnetron-sputtered Ga_2O_3, $CaCu_3Ti_4O_{12}$ (CCTO), $BaTiO_3$ (BTO), etc., as well as ALD-deposited HfO_2, as shown in Fig. 1b. The architecture of the completed top-gate transistor is presented in Fig. 1c.

Figure 1d illustrates the magnetron sputtering mechanism, where energetic ions from a radio-frequency plasma bombard the target, sputtering the target atoms that are subsequently deposited onto the substrate. However, direct sputtering onto a 2D semiconductor channel could induce significant damage to the channel, as demonstrated in Supplementary Figs. 1 and 2. To circumvent this issue, we proposed an approach in which the dielectric was first deposited onto a metal film and then transferred onto the channel, thereby eliminating the exposure of the 2D semiconductor to the sputtering process. To achieve the exfoliation of the amorphous dielectric and metal film, a water-assisted exfoliation and transfer method was developed, leveraging the superhydrophilic nature of the freshly deposited SiO_x and the weak adhesion between SiO_x and Au. In Supplementary Fig. 3, contact-angle comparisons show that the freshly deposited SiO_x is superhydrophilic (contact angle ~0°), in contrast to commercial SiO_2/Si substrate. The adhesion measurements (Supplementary Fig. 4) reveal an Au-SiO_x adhesion strength of 0.143 MPa, which is even

111 weaker than the interlayer van der Waals interaction strength of mica (~0.150 MPa as measured), indicating
112 the feasibility of exfoliation. The transfer procedures for the Au films and the hybrid dielectric/Au films are
113 detailed in Supplementary Figs. 5 and 6. Following exfoliation, the top-gate film was retrieved using a
114 glass-supported polydimethylsiloxane (PDMS) stamp and transferred onto the semiconductor channels. A
115 more detailed fabrication process for the top-gate transistors is presented in Supplementary Fig. 7a, and this
116 method is also applicable to fabricating FET arrays, as shown in Supplementary Figs. 7b-d.

117 Top-view and cross-sectional structural characterizations of a completed amorphous top-gate transistor
118 are presented in Figs. 1e-k. Optical micrographs of the device before and after top-gate film transfer are
119 displayed in Figs. 1e and 1f, respectively. Cross-sectional transmission electronic spectroscopy (TEM)
120 images (Figs. 1g and 1h) show the overall device structure and a magnified view of the Au/CCTO/MoS_2
121 layer stack. The higher-magnification TEM image in Fig. 1i clearly reveals the ordered atomic arrangement
122 of Au, whereas the underlying CCTO layer appears as an amorphous disordered phase. Fast Fourier
123 transform (FFT) analysis of the high-resolution images of the Au and CCTO layers in Fig. 1i yields distinct
124 diffraction features. The FFT pattern of Au (Fig. 1j) shows sharp bright spots, confirming its long-range
125 crystalline order, while that of CCTO (Fig. 1k) exhibits diffuse halos, consistent with an amorphous
126 structure lacking atomic periodicity (see also Supplementary Fig. 8 for the Au/BTO cross-sectional TEM
127 image).

128 In this work, we successfully combined magnetron sputtering with a transfer technique to fabricate
129 amorphous top-gate 2D semiconductor transistors. Magnetron sputtering is suitable for depositing various
130 high-κ amorphous dielectric materials, providing an alternative route to enhance top-gate performance. To
131 verify the compatibility of this transfer method with conventional processes, HfO_2 layers deposited by ALD
132 on Au films were also exfoliated and transferred.

133

134 **Characteristics of the sputtered amorphous high-κ dielectric films**

135 Good uniformity and flatness are critical to achieving excellent insulation in the dielectric layer. The
136 morphologies of the CCTO, BTO, and HfO_2 layers were characterized using atomic force microscope
137 (AFM) and transmission electron microscope (TEM), as shown in Fig. 2. The successful transfer of all four

dielectric films and high-κ/metal stacks, including sputtered BTO, CCTO, Ga_2O_3 and ALD-deposited HfO_2, onto the target substrate is demonstrated in Supplementary Fig. 9. Moreover, the Au films, as well as the four dielectric films mentioned above, were transferred onto Cu meshes for TEM characterization (Supplementary Figs. 10 and 11).

To clearly observe the morphologies of the dielectric films, we removed the metal layers via wet etching (note that in the actual device fabrication for top-gate structures, the metal layer serves as the gate electrode and does not need to be removed). The optical micrographs are shown in Figs. 2a, 2e, and 2i, and the AFM measurements were conducted on these dielectric films to assess their roughness and thickness (Figs. 2b, 2f, and 2j). Among them, the CCTO layer exhibits a thickness of approximately 25 nm and demonstrates good uniformity, as reflected by its low root-mean-square (RMS) roughness of 0.926 nm. Similarly, the BTO film has a thickness of 55 nm and an RMS roughness of 1.132 nm. The HfO_2 layer measures 23 nm in thickness and achieves a lower surface roughness of 0.437 nm. Furthermore, we characterized the thickness and roughness of the high-κ/metal stacks by AFM. CCTO, BTO, and Ga_2O_3 films with various thicknesses deposited on the metal layers consistently exhibit low roughness values below 1 nm (Supplementary Figs. 12 and 13).

To verify the amorphous nature of the dielectric layers, we characterized the sputtered CCTO and BTO films using TEM, with ALD-deposited HfO_2 as a reference. The TEM images of the CCTO, BTO, and HfO_2 layers are shown in Figs. 2c, 2g, and 2k, respectively, with insets providing low-magnification overviews. In Figs. 2c and 2g, no oriented domains with regular lattice are observed in the CCTO and BTO films, in contrast to the ALD-deposited HfO_2 (Fig. 2k), which exhibits distinct lattice fringes and grain boundaries. The selected-area electron diffraction (SAED) patterns of CCTO and BTO (Figs. 2d and 2h) display diffuse halos, confirming their amorphous structures. In comparison, the SAED pattern of ALD-HfO_2 (Fig. 2l) exhibits discrete, irregular diffraction spots, consistent with a polycrystalline structure. Additionally, optical transmittance measurements on the above-mentioned films were used to determine their optical bandgaps. The results revealed wide bandgaps, which accounted for the good insulating properties of all the fabricated amorphous dielectric films (Supplementary Fig. 14).

High-κ top-gate 2D transistors with the subthreshold swing approaching the Boltzmann limit

Utilizing the proposed method, we fabricated CVD-grown MoS_2 transistor incorporating sputtered CCTO and BTO as top-gate dielectrics. For comparison, we also constructed a transistor using exfoliated $MoTe_2$ as the channel and conventional ALD-deposited HfO_2 as the top-gate dielectric. Figure 3 presents the electrical characteristics of representative transistors, with insets displaying the images of the devices before and after the top-gate films transfer. The performance of the MoS_2 transistor with a 33 nm CCTO dielectric is presented in Figs. 3a-c, achieving an on/off ratio of 10^6 and a minimum subthreshold swing of 60 mV/dec (average *SS* over four orders of magnitude ~ 76 mV/dec). In Figs. 3d-f, the MoS_2 transistor employing a 55 nm BTO dielectric layer also exhibits high performance, characterized by a switching ratio of 10^8 and a minimum *SS* of 100 mV/dec (average *SS* over four orders of magnitude ~ 123 mV/dec). The reduced subthreshold swing observed in these devices indicates lower power consumption, resulting from the improved gate controllability enabled by the high-κ dielectric materials. More detailed TEM images are provided in Supplementary Fig. 15. More MoS_2 FETs were constructed using CCTO dielectrics of various thicknesses (22, 16, and 15 nm), and their transfer characteristics are presented in Supplementary Fig. 16. These devices consistently achieved a low *SS* of approximately 80 mV/dec, representing a substantial improvement over back-gated configurations using 300 nm SiO_2 (*SS* ~ 5 V/dec). Furthermore, the top-gate transfer curves exhibit minimal hysteresis, as illustrated in Supplementary Fig.17.

The electrical performance of exfoliated $MoTe_2$ transistor is demonstrated in Figs. g-i. The on/off ratio of the $MoTe_2$ transistors exceeded 10^5, with a minimum *SS* near 70 mV/dec and an average *SS* of approximately 95 mV/dec over four orders of magnitude. We also integrated ALD-deposited HfO_2 on MoS_2 to fabricate top-gate transistors, and the optical and cross-sectional TEM images are provided in Supplementary Fig. 18. The MoS_2/HfO_2 transistor also achieves a minimum subthreshold swing of 83 mV/dec, as reflected in the transfer characteristic curves (Supplementary Fig. 19).

Beyond CVD-MoS_2, oriented carbon nanotube (CNT) quasi-2D films have also been used to fabricate sputtered top-gate field-effect transistors, with CCTO, BTO, and Ga_2O_3 films as top gate dielectrics. The SEM image and Raman spectrum of the CNTs are presented in Supplementary Fig. 20. To highlight the enhanced gate controllability offered by the high-κ top gate, we conducted comparative measurements

between the top-gate and back-gate operations of carbon nanotube devices (Supplementary Fig. 21). Using the sputtered amorphous top gate, a gate voltage variation of below 1 V is sufficient to achieve a switching ratio of one order of magnitude, whereas the back gate (300 nm SiO_2) requires a voltage swing twenty times larger to accomplish the same function.

Sputtered amorphous dielectrics with κ values exceeding 40

Transistors operate as switches based on the capacitor formed by the gate electrode, dielectric layer, and channel. Therefore, the gate capacitance serves as a direct metric for evaluating dielectric performance. To this end, metal-insulator-metal (MIM) capacitors were fabricated using the dielectric materials described above (CCTO, BTO, HfO_2), as illustrated in Fig. 4a. The fabrication procedures for the capacitors are detailed in the Methods section, and the optical images of the capacitors are presented in Supplementary Fig. 22.

Capacitance-voltage (*C*-*V*) measurements were conducted using a semiconductor analyzer to extract the dielectric capacitance. The relative dielectric constant was then calculated using the following formula:

$$\varepsilon_r = \frac{C \cdot d}{\varepsilon_0 \cdot S}$$

where C is the capacitance measured by the *C*-*V* test, d is the thickness of the dielectric layer, S is the capacitor area, and ε_0 is the vacuum permittivity. Figure 4b summarizes the dielectric constants extracted from all capacitors measured across a range of frequencies. The highest relative dielectric constants achieved by CCTO and BTO are approximately 46 and 93, respectively, with average values of 42 and 47. And the ALD-deposited HfO_2 showed a dielectric constant of ~11. Several representative capacitors were selected, and their relative dielectric constants are shown in Fig. 4c. Corresponding *C*-*V* curves measured at multiple frequencies for these capacitors are presented in Figs. 4d–f. The 55 nm-thick BTO layer yielded a maximum capacitance of 1.50 μF/cm², followed by the CCTO capacitor with a maximum capacitance of 1.24 μF/cm². HfO_2 capacitor exhibited a capacitance of 0.42 μF/cm².

As shown in Fig. 4g, the electric breakdown characteristics were also investigated. All capacitors exhibited low leakage currents, remaining below the low-power limit of 1.5×10^{-2} A/cm² and far below complementary metal-oxide-semiconductor gate limit (10 A/cm²)[28, 46].

To evaluate the performance of the fabricated dielectric layers, we benchmarked the transistors in Fig. 3 against state-of-the-art high-κ devices reported in the literature, with a focus on dielectric constant (κ) and subthreshold swing (*SS*) (Fig. 4h)[2, 13-19, 23, 47-68]. The $MoTe_2$ transistor employing transferred ALD-HfO_2 as the top-gate dielectric performs on par with previously reported HfO_2-based devices. The BTO-based transistor achieves a substantially higher κ of ~93 while maintaining an *SS* comparable to advanced counterparts. Moreover, the CCTO-gated transistor exhibits a κ of ~46 and a minimum *SS* approaching 60 mV/dec, positioning it among the leading high-κ devices.

Conclusions

In conclusion, we have reported a general fabrication strategy for 2D semiconductor top-gate transistors that integrates magnetron-sputtered amorphous high-κ dielectrics with an efficient film-transfer technique, achieving high relative dielectric constants exceeding 40 and low subthreshold swings approaching 60 mV/dec. This approach provides a general pathway and an expanded material platform for integrating high-κ dielectrics into top-gate architectures. Adjusting the sputtering conditions could further improve the film quality and reduce leakage currents, while transfer-technique optimization would enable wafer-scale integration of high-κ/metal gate stacks. The demonstrated amorphous high-κ dielectric films also exhibit good mechanical flexibility, indicating their potential for use in flexible electronics and related applications.

Methods

Fabrication of the high-κ/metal gate stacks.

The high-κ/metal gate stacks were fabricated via a continuous deposition process. First, electron-beam evaporation was used to deposit a thin SiO_x buffer layer onto a commercial SiO_2/Si substrate. A gold layer (30–60 nm) was then deposited onto the SiO_x surface under high vacuum to preserve its hydrophilicity for subsequent exfoliation in water. The dielectric films (including CCTO, BTO, and Ga_2O_3) were subsequently deposited by magnetron sputtering (MSP-300B, Beijing Chuangshi Weina Technology Co., Ltd.) at room temperature, with thicknesses precisely controlled by sputtering power and time. The chamber base pressure was below 8×10^{-4} Pa, and the working pressure was maintained at 0.5 Pa–2 Pa with an Ar flow of 40 sccm. HfO_2 layers were alternatively deposited by atomic layer deposition (ALD) via Suzhou Research Materials Microtech Co., Ltd.

Transfer of the high-κ/metal gate films

Following the gate stack preparation, the sample was immersed in deionized (DI) water, enabling the gate film to detach from the substrate and float freely on the DI water surface. The free-standing film was subsequently retrieved with a polydimethylsiloxane (PDMS) stamp and transferred onto the predefined region over the channel and source/drain electrodes.

Prefabrication of the channels and electrodes

The MoS_2 channels were grown by chemical vapor deposition (CVD), whereas the $MoTe_2$ channels were mechanically exfoliated onto a SiO_2/Si substrate. For the transistor arrays, the semiconductor channels were also synthesized via CVD, and the large-area 2D semiconductor films were patterned into strip-shaped arrays by electron beam lithography (EBL) combined with SF_6 plasma etching. The source and drain electrodes were defined by either EBL or UV photolithography, followed by electron-beam evaporation for metal deposition.

Fabrication of the capacitors

Bottom electrodes were deposited by electron-beam evaporation through a custom-designed ultrathin metal shadow mask, avoiding the sharp edges or burrs often introduced by photolithographic patterning. The dielectric/metal stack was subsequently transferred onto the bottom electrodes using the procedure

described above. Photoresist was then applied to protect the top electrodes, and the exposed regions were treated with Au etchant for ~10 s to remove excess gold, thus finalizing the capacitor fabrication

Characterizations and electrical measurements

Atomic force microscopy (AFM; NT-MDT) was employed to determine the root mean square (RMS) roughness and film thickness. Contact angle measurements were performed using an SDC-200s contact angle meter, and the adhesion strengths were quantified with a digital adhesion tester. Electrical characteristic curves were acquired with a probe station system equipped with a Keithley 2636B source measure unit under high vacuum (~10^{-6} Torr). Capacitance–voltage (C–V) measurements were carried out using a semiconductor parameter analyzer (Keithley 4200A). High-resolution transmission electron microscopy (HRTEM) and selected-area electron diffraction (SAED) were performed on an FEI Tecnai F20 or a Thermo Spectra 200 microscope. Focused ion beam (FIB) was applied to fabricate the cross-sectional TEM samples with a Thermo Scientific Scios 2 DualBeam system. Raman spectroscopy was performed using a Bruker SENTERRA II Raman system.

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Author contributions

Y.W., J.J. and Z.Z. conceived and designed the project. Y.W., J.J. and F.X. fabricated the devices. Y.W. and J.J. performed the OM, AFM and electrical characterizations. Y.W. and J.J. obtained and analyzed the TEM data. C.L. contributed to the contact angles and adhesion strengths characterizations. J.Z. and B.Z provided the 2D semiconductors materials synthesized by CVD. Y.H., H.L., S.Q., and C.G. commented on the manuscript and helped analyze the data. Y.W., J.J. and Z.Z. co-wrote the manuscript. All authors discussed the results and reviewed the manuscript.

Competing interests

The authors declare no competing interests.

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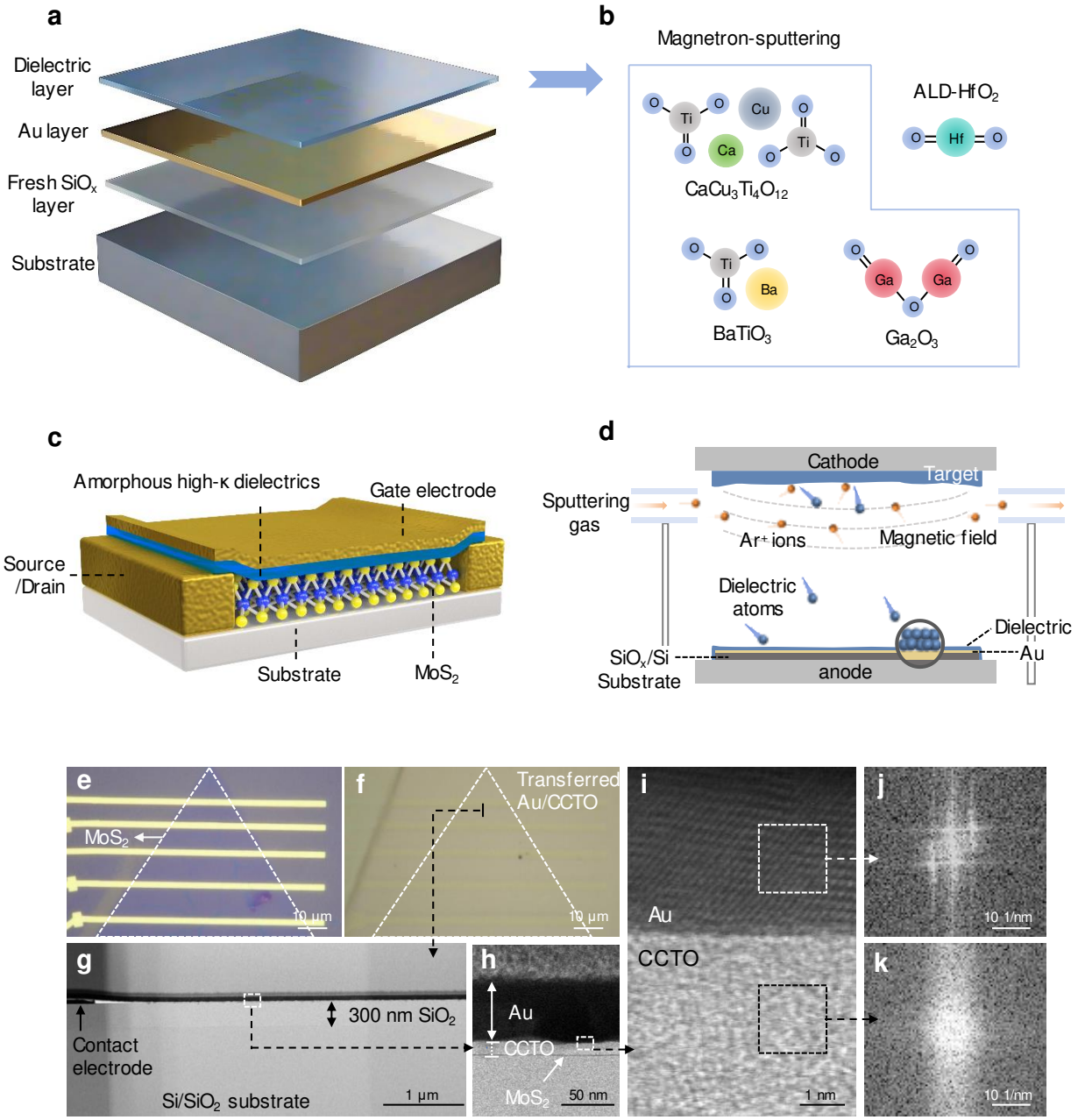


Fig. 1 | Fabrication process and mechanism of the amorphous dielectrics and top-gate transistors. a, Schematic diagram of the top-gate stack structure, consisting of a dielectric layer and a gold (Au) layer, with a thin hydrophilic SiO_x layer pre-deposited beneath the Au. **b,** Chemical structures of the dielectric materials employed. $CaCu_3Ti_4O_{12}$ (CCTO), $BaTiO_3$ (BTO) and Ga_2O_3 are prepared using magnetron sputtering, whereas HfO_2 is deposited by atomic layer deposition (ALD). **c,** Schematic of the completed top-gate transistor. **d,** Schematic illustration of the magnetron sputtering process for dielectric deposition. **e,f,** Optical micrographs of a typical CVD-grown MoS_2 transistor before (**e**) and after (**f**) the integration of the amorphous high-κ dielectric/Au top-gate stack. **g,** Cross-sectional transmission electron microscopy (TEM) image of the amorphous top-gate transistor. **h,** Magnified TEM image of the white-boxed region in **g**, showing the stacking of the metal, dielectric and 2D semiconductor. **i,** Magnified TEM image of the white-boxed region in **h**, revealing the distinctly different crystallinity of Au and CCTO. **j,k,** FFT patterns confirming the crystalline nature of Au (**j**) and the amorphous state of CCTO (**k**).

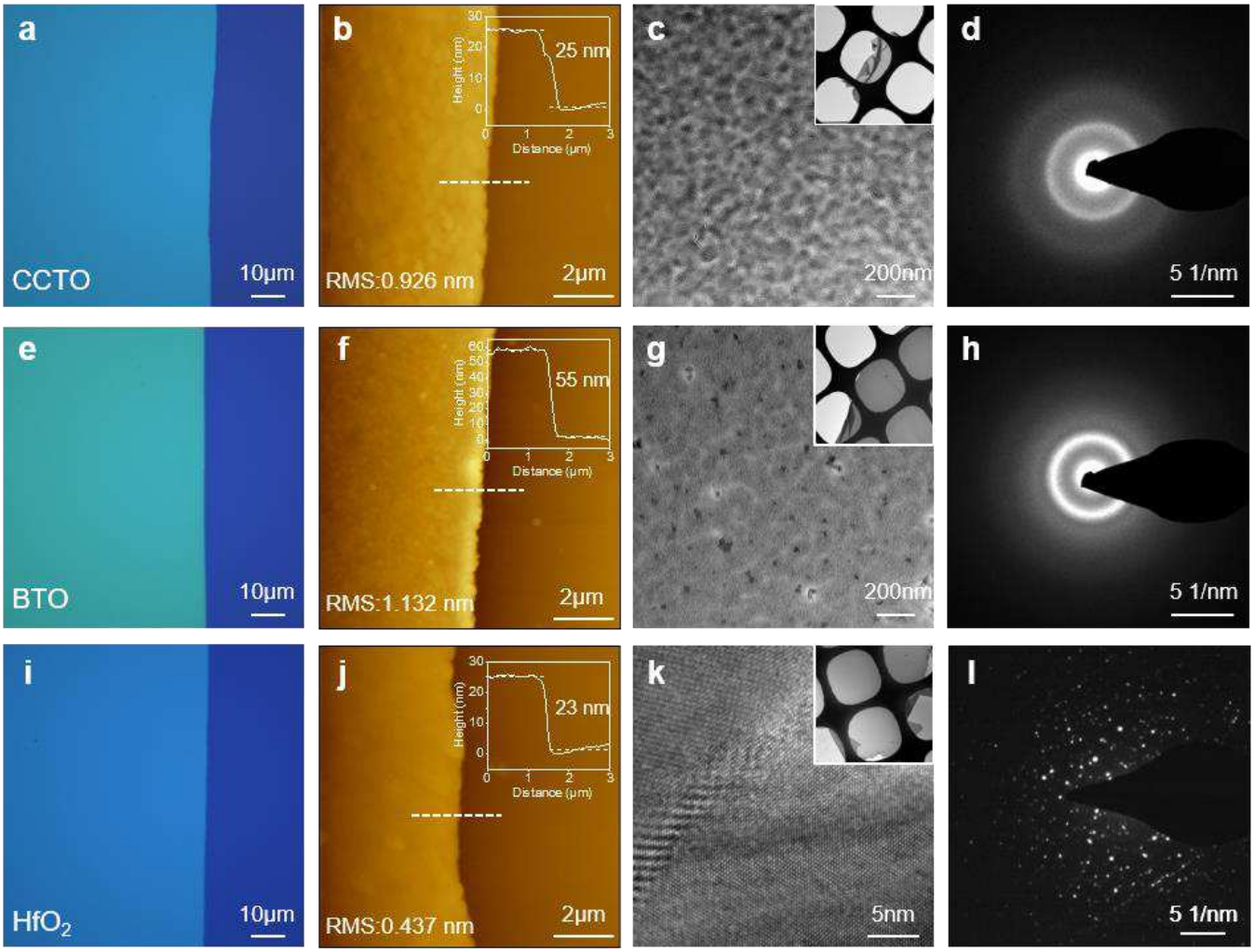


Fig. 2 | Structural and morphological characterizations of the dielectric films. a-d, Characterizations of the sputtered CCTO film. The optical image (**a**), atomic force microscope (AFM) image with the root-mean-square roughness (RMS) of 0.926 nm and the thickness of 25 nm (**b**), transmission electron microscope (TEM) image (**c**), and the corresponding selected area electron diffraction (SAED) pattern (**d**) displaying diffuse halos characteristic of an amorphous structure. **e-h**, Characterizations of the sputtered BTO film. The optical image (**e**), AFM image (RMS 1.132 nm, thickness 55 nm) (**f**), TEM image (**g**), and SAED pattern (**h**) also showing diffuse halos indicative of an amorphous phase. **i-l**, Characterizations of the ALD-deposited HfO_2 film. The optical image (**i**), AFM image (RMS 0.437 nm, thickness 23 nm) (**j**), TEM image (**k**), and SAED pattern (**l**) exhibiting distinct diffraction spots that confirm a polycrystalline structure.

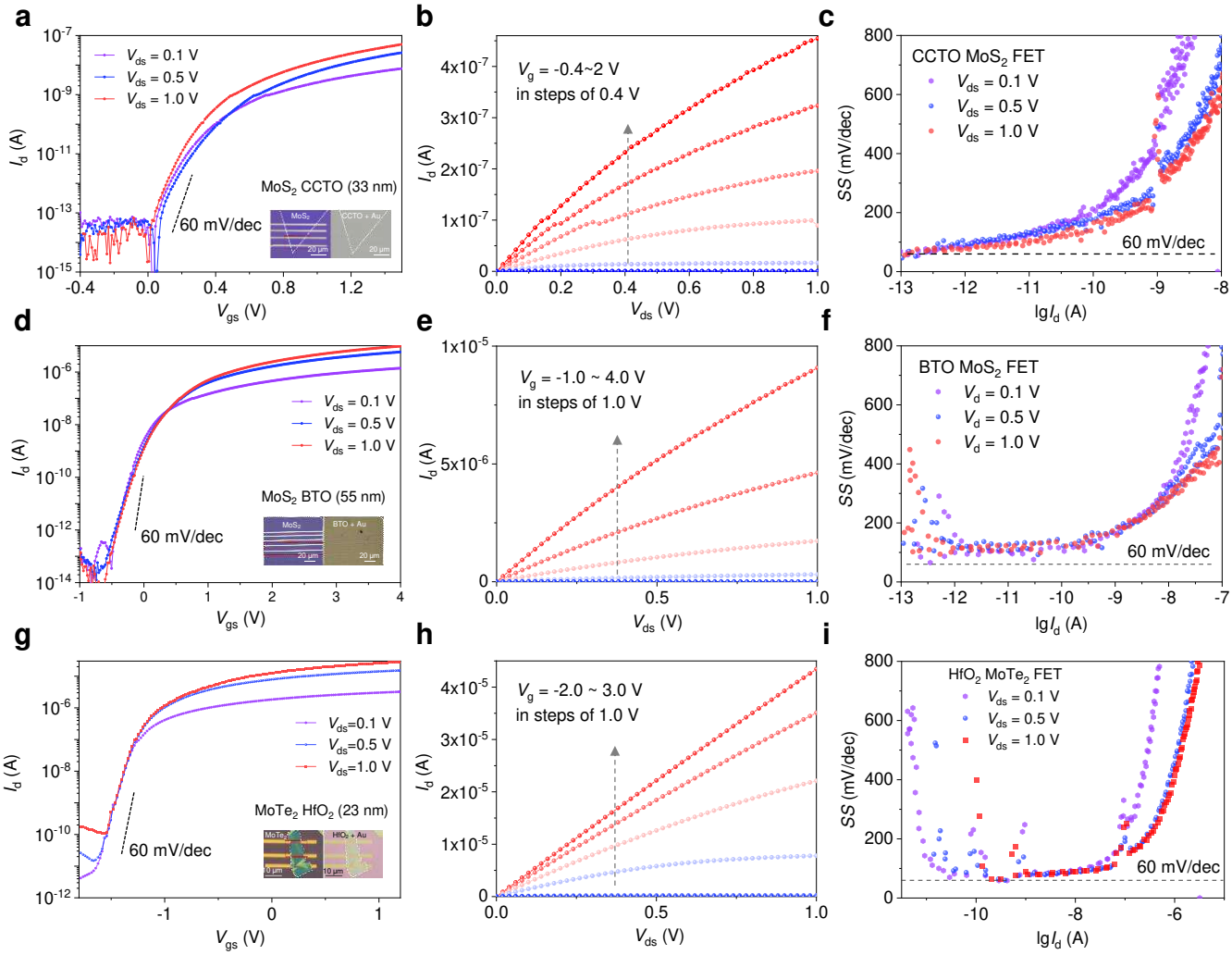


Fig. 3 | Electrical performance of the top-gate transistors. a-c, Electrical characteristics of the MoS2/CCTO transistor (channel width W_{ch} = 15.8 μm, channel length L_{ch} = 8.9 μm). The transfer characteristics (V_{gs}-I_d) (**a**), output characteristics (V_{ds}-I_d) (**b**), and the subthreshold swing (*SS*) as a function of the drain current (**c**) showing a minimum *SS* of approximately 60 mV/dec (*SS* over four orders of magnitude ($SS_{4\text{-dec}}$) ~ 76 mV/dec). **d-f,** Electrical characteristics of the MoS2/BTO transistor (W_{ch} = 127.8 μm, L_{ch} = 8.7 μm). The transfer characteristics (V_{gs}-I_d) (**d**), output characteristics (V_{ds}-I_d) (**e**), and the *SS* as a function of the drain current (**f**) showing a minimum *SS* of approximately 100 mV/dec ($SS_{4\text{-dec}}$ ~ 123 mV/dec). **g-i,** Electrical characteristics of the MoTe2/HfO2 transistor (W_{ch} = 6.8 μm, L_{ch} = 5.8 μm). The transfer characteristics (V_{gs}-I_d) (**g**), output characteristics (V_{ds}-I_d) (**h**), and the *SS* as a function of drain current (**i**) showing a minimum *SS* near 70 mV/dec ($SS_{4\text{-dec}}$ ~ 95 mV/dec). Insets: optical micrographs of the corresponding devices before and after top-gate films transfer. The white boxes depict the 2D semiconductors and red boxes indicate the measured channel regions.

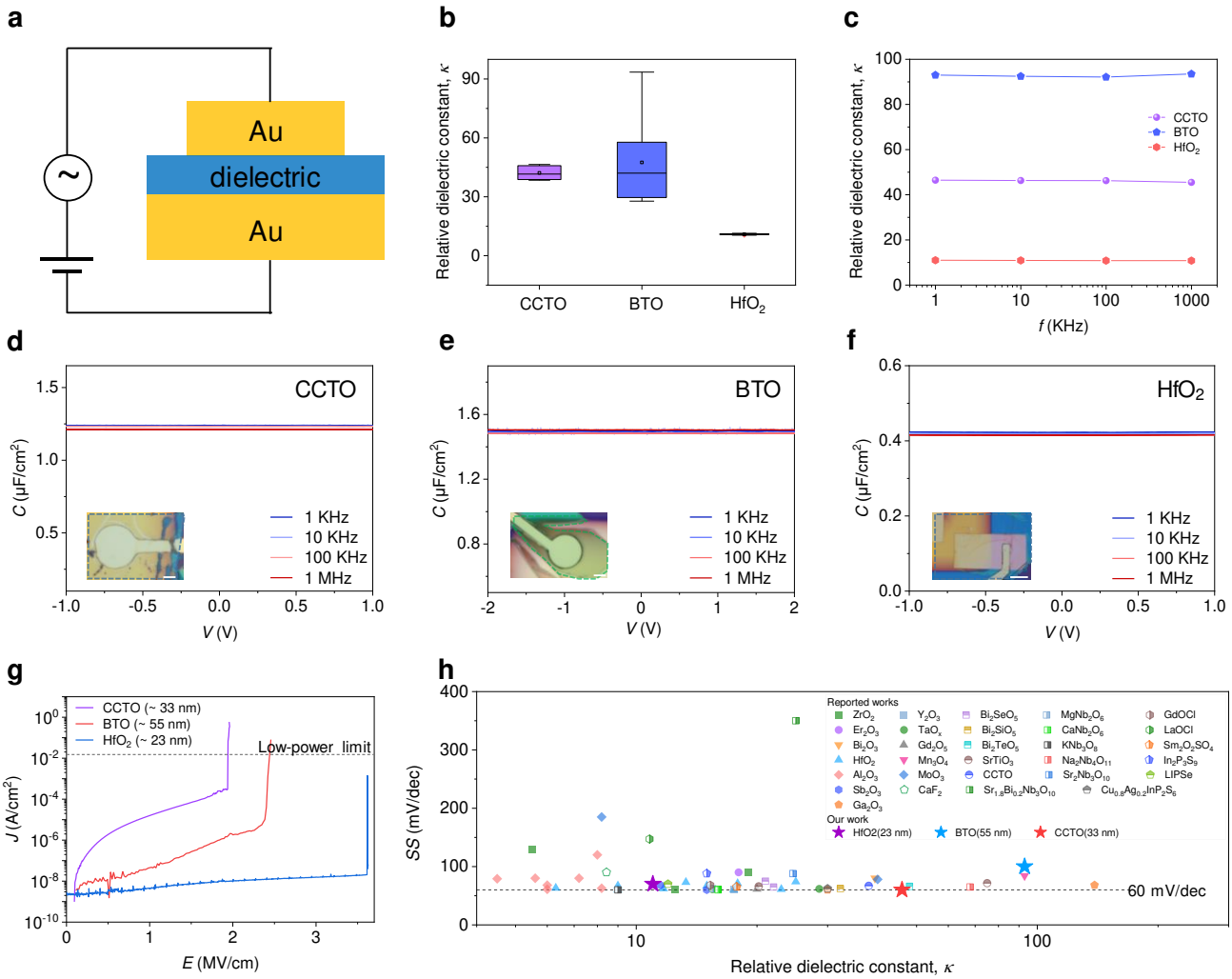


Fig. 4 | Dielectric properties of the transferred top-gate films. a, Schematic of the metal-insulator-metal (MIM) capacitor structure used for capacitance-voltage (*C-V*) measurements. **b,** Statistical results of the relative dielectric constant (κ) for three types of materials inlcuding CCTO (~33 nm), BTO (~55 nm), and HfO_2 (~23 nm). **c,** Frequency-dependent relative dielectric constants for the representative dielectric films. **d-f,** *C-V* characteristics at various frequencies for capacitors with CCTO (~33 nm) (**d**), BTO (~55 nm) (**e**), and HfO_2 (~23 nm) (**f**). The corresponding capacitor devices are shown in the inset images. Scale bars: 10 μm (d, e); 50 μm (f). **g,** The leakage current density as a function of the breakdown field strength for the capacitors. **h,** Benchmarking of the relative dielectric constants (κ) and the subthreshold swings (*SS*) for 2D semiconductor transistors in this work compared to the reported values of devices employing high-κ gate dielectrics. The $MoTe_2$ transistor incorporating transferred ALD-HfO_2 ($\kappa \approx 11$) achieves a minimum *SS* of ~70 mV/dec, on par with state-of-the-art HfO_2-based devices. The sputtered films, CCTO ($\kappa \approx 46$) and BTO ($\kappa \approx 93$), preserve high dielectric constants while enabling MoS_2 transistors with subthreshold swings (*SS*) of approximately 60 mV/dec and 100 mV/dec, respectively.

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