SUPPLEMENTARY INFORMANTION

Amorphous High-κ Dielectrics for Top-Gate Integration in 2D Semiconductor Transistors

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Table S1. Representative studies on high-κ dielectric top-gate transistors

Fabrication strategy	**ALD**			**Oxidation**						**Thermal evaporation**		**MBE**	**PLD**	**Wet-chemistry**
	ALD + seeding or buffer layers		ALD + transfer	Oxidizing semiconductors			Oxidizing metals							
Reference	Xinran Wang, et al.[1]	Tianyou Zhai, et al.[2]	Yuan Liu, et al.[3]	Hailin Peng, et al.[4]	Sungjoo Lee, et al.[5]	Peng Zhou, et al.[6]	Xiangfeng Duan, et al.[7]	Zengfeng Di, et al.[8]	Zheng Liu, et al.[9]	Kosuke Nagashio, et al.[10]	Tianyou Zhai, et al.[11]	Tibor Grasser, et al.[12]	Sean Li, et al.[13]	Junjie Guo, et al.[14]
Dielectric materials	HfO_2 (PTCDA)	HfO_2 (Sb_2O_3)	Al_2O_3	Bi_2SeO_5	HfO_2	MoO_3	Y_2O_3	c-Al_2O_3	Ga_2O_3	Er_2O_3	Sb_2O_3	CaF_2	$SrTiO_3$	CCTO
κ	~9	~17.5	~6	22	23	~8.2	17.5	~6	30	18	11.5	8.43	~75	~38
Thickness /EOT (nm)	3 nm /1.3 nm	3 nm /0.67 nm	10 nm /6.5 nm	2.7 nm /0.48 nm	10 nm /1.7 nm	1.34 nm /0.64 nm	18.8 nm /4.2 nm	2 nm /1.3 nm	2.7 nm /0.4 nm	5.3 nm /1.1 nm	10 nm /3.3 nm	2 nm /0.9 nm	16 nm /0.83 nm	15 nm /1.54 nm
Channel materials	MoS_2 1 layer	MoS_2 1 layer	MoS_2 1 layer	Bi_2O_2Se /	MoS_2 5 nm	MoS_2 1 layer	MoS_2 few layers	MoS_2 3 layers	MoS_2 3 layers	MoS_2 1 layer	MoS_2 /	MoS_2 2 layers	MoS_2 1 layer	MoS_2 2.4 nm
SS_{min} (mV/dec)	60	~60	68	65	61	~200	60	61	60	90	68	~90	71.5	67

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Fabrication strategy	**Exfoliation**		**CVD**							**PVD**	**CVT**	**Sputtering (+transfer)**	
Reference	Tianyou Zhai, et al.[15]	Xiaosheng Fang, et al.[16]	Cheng-Yan Xu , et al.[17]	Yu Zhou , et al.[18]	Jun He , et al.[19]	Shengxue Yang, et al.[20]	Wei Liu, et al.[21]	Wei Liu, et al.[22]	Xidong Duan, et al.[23]	Nengjie Huo , et al.[24]	Yang Chai, et al.[25]	**Our work**	
Dielectric materials	$KBe_2BO_3F_2$	$Sr_2Nb_3O_{10}$	$MgNb_2O_6$	$CaNb_2O_6$	Gd_2O_5	GdOCl	$Sm_2O_2SO_4$	Mn_3O_4	Sb_2O_3	MoO_3	$Cu_{0.8}Ag_{0.2}InP_2S_6$	**CCTO**	**BTO**
κ	63 (bulk)	24.6	15.5	16	~20	15.3	17.8	~93	15	40	~30	**46**	**93**
Thickness /EOT (nm)	–	185 nm /29 nm	4 nm /1 nm	15 nm /3.66 nm	8.5 nm /1.66 nm	14.5 nm /3.7 nm	14.6 nm /3.2 nm	22.9 nm /0.96 nm	6 nm /1.5 nm	9.31 nm /0.9 nm	65 nm /8.45 nm	**33 nm /2.8 nm**	**55 nm /2.3 nm**
Channel materials	MoS_2 /	MoS_2 6 nm	MoS_2 1 layer	MoS_2 few layers	MoS_2 few layers	MoS_2 /	MoS_2 3.1 nm	MoS_2 few layers	WSe_2 2 layers	MoS_2 few layers	MoS_2 few layers	**MoS_2 1 layer**	**MoS_2 1 layer**
SS_{min} (mV/dec)	60	88	62	61	61.5	67.9	65.2	84	60	78	62	**60**	**100**

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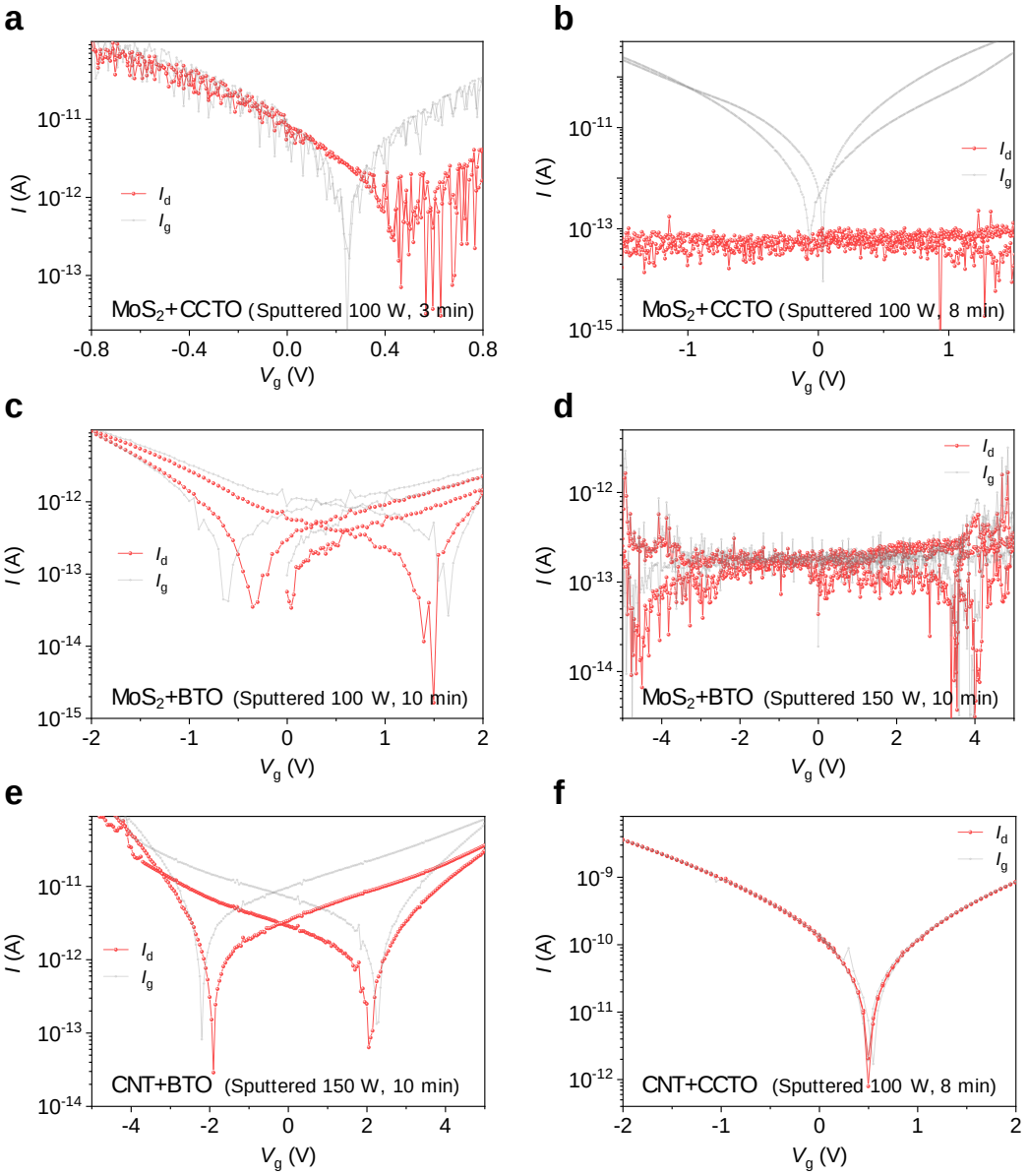
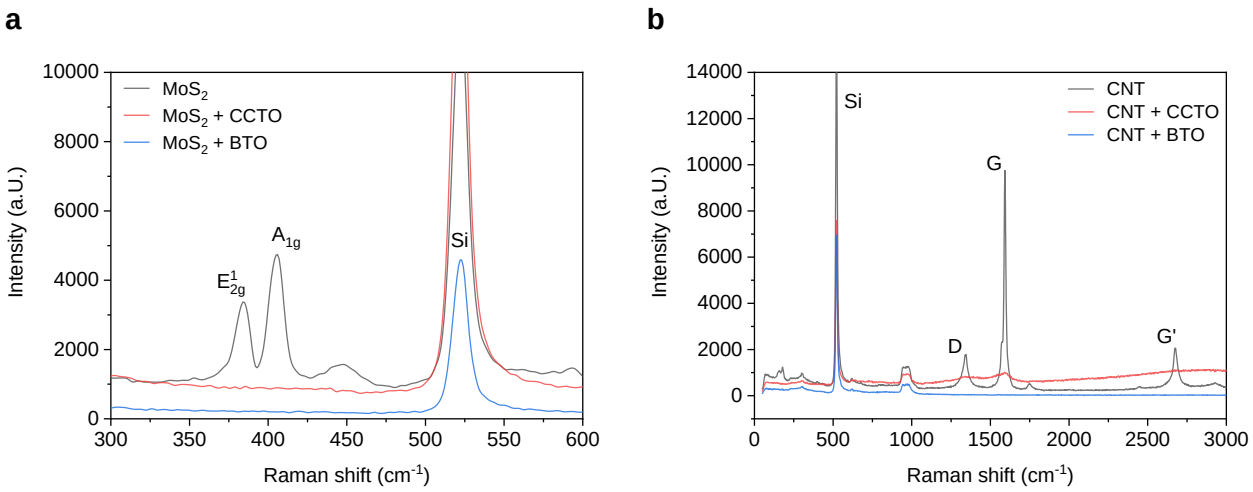
Table S2. Comparison of the advantages and disadvantages of methods for preparing gate dielectrics

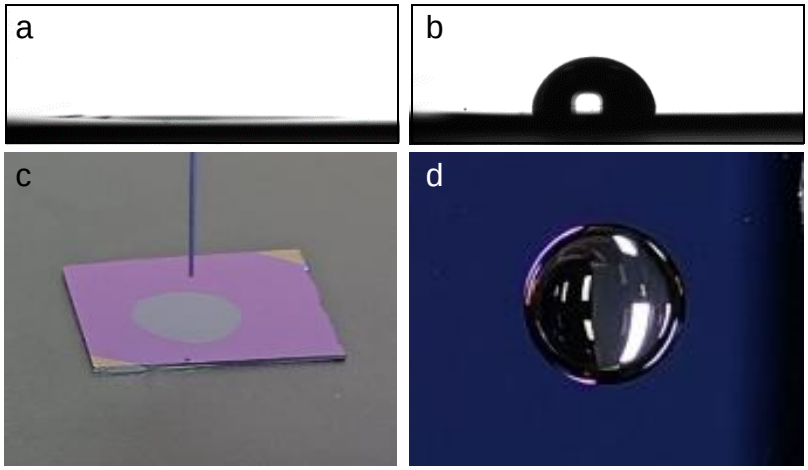
	Magnetron sputtering	Atomic layer deposition (ald)	Chemical vapor deposition (cvd)	Molecular beam epitaxy (mbe)	Thermal evaporation	Oxidation
Principle	Physical sputtering, plasma bombards a target, ejecting atoms towards the substrate.	Sequential surface chemical reactions, precursor pulses alternate in a self-limiting growth manner.	Gas-phase reaction, gaseous precursors undergo chemical reactions on a heated substrate surface.	Physical evaporation, beams of atoms or molecules are directed onto the substrate.	Thermal evaporation, material is heated and vaporized; atoms travel in a line-of-sight path.	The channel or metal materials are oxidized to its corresponding natural oxides.
Film uniformity	Moderate	Excellent	Good	Very high	Poor	Good
Deposition rate	Relatively fast	Extremely slow	Moderate	Very slow	Moderate	Fast
Process temperature	Low	Low	High	High	Low	High
Step coverage	Moderate	Excellent	Good	Moderate	Poor	Moderate
Cost	Moderate	High	Moderate	Highest	Low	Low
Advantages	Wide material choice, Excellent scalability, Easily industrialized, etc.	Atomic-level thickness control, etc.	High crystal quality, etc.	Highest crystal quality, In-situ monitoring, etc.	Simple equipment, etc.	High-quality oxide layer, etc.
Disadvantages	Plasma damage to 2d semiconductors	Expensive precursors	Stringent growth temperature	Poor scalability	Poor densification	Suitable for few materials



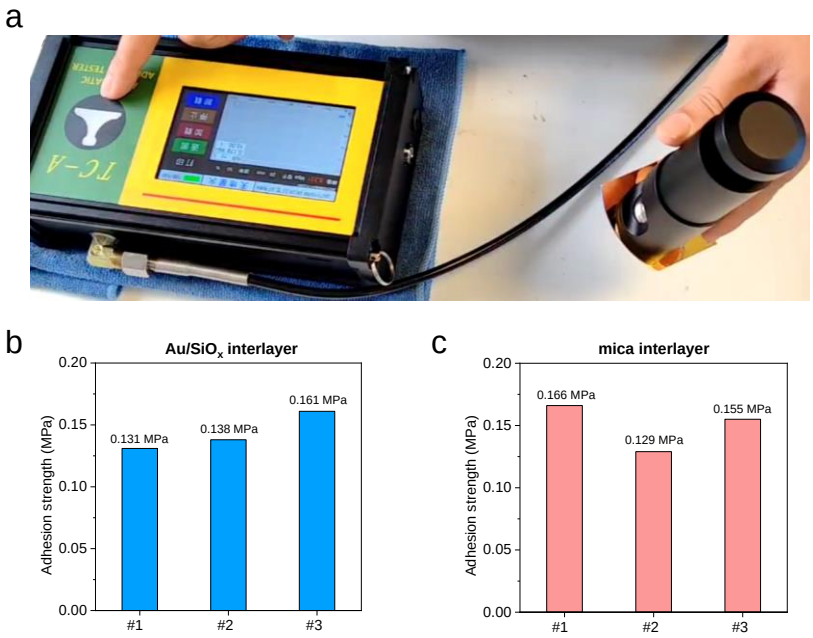
Supplementary Fig. 1 | Electrical characteristics of transistors after direct sputtering of dielectrics. **a,b,** Transfer characteristics of MoS_2 transistors after direct sputtering of CCTO at 100 W for 3 minutes (**a**) and 8 minutes (**b**). **c,d,** Transfer characteristics of MoS_2 transistors after direct sputtering of BTO at 100 W (**c**) and 150 W (**d**) for 10 minutes. **e,f,** Transfer characteristics of CNT transistors after direct sputtering of BTO (**e**) and CCTO (**f**). All devices exhibit severely degraded current levels and nonfunctional transistor behavior, confirming the damaging effect of direct sputter deposition on two-dimensional channel materials.



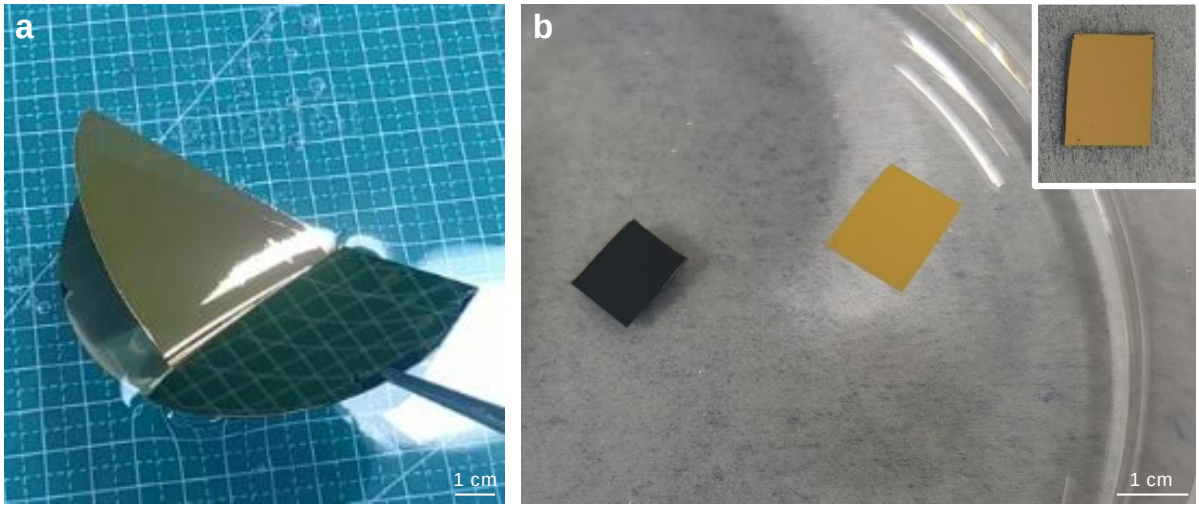
Supplementary Fig. 2 | Raman spectroscopic analysis of channel materials before and after direct dielectric sputtering. a, Raman spectra of MoS_2 before and after sputtering. **b,** Raman spectra of CNTs before and after sputtering. The characteristic Raman peaks of MoS_2 and CNTs disappeared after sputtering, regardless of whether CCTO or BTO was sputtered, indicating that magnetron sputtering damaged the MoS_2 and CNTs channels.



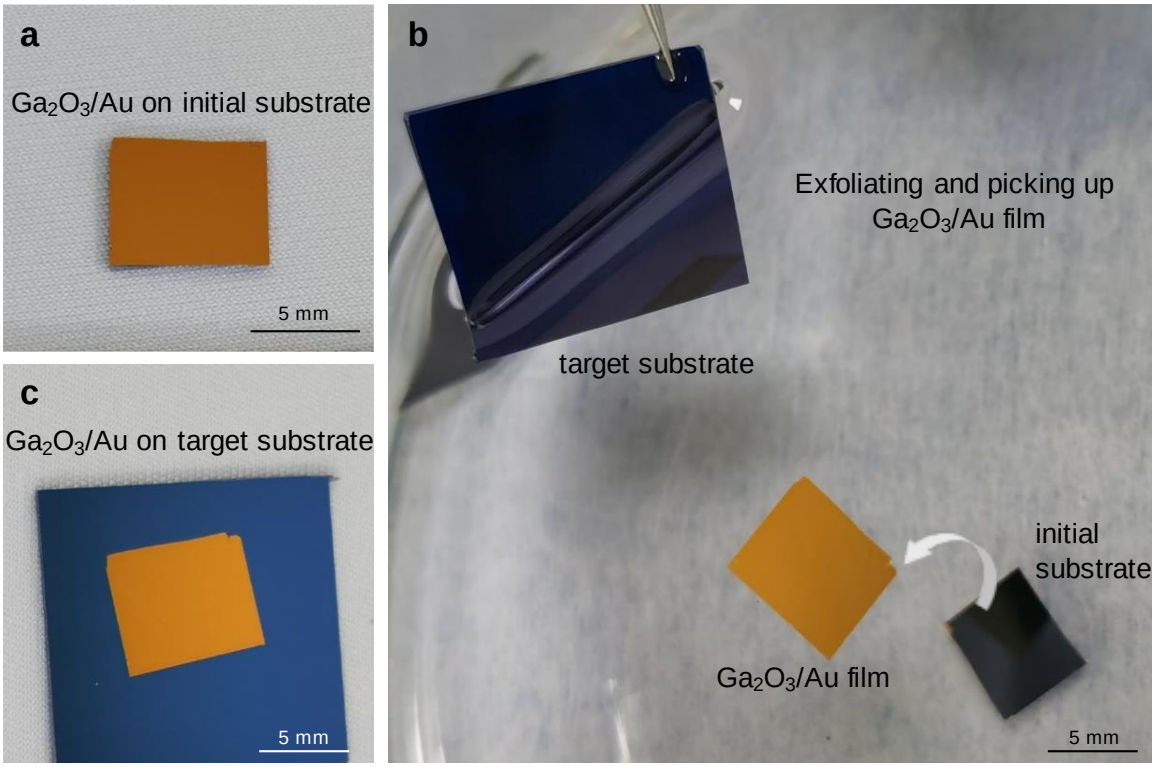
Supplementary Fig. 3 | Contact-angle comparison of freshly deposited SiO_x and a commercial SiO_2/Si substrate. a,c, cross-sectional (**a**) and top-view (**c**) images of a water droplet on the freshly deposited SiO_x surface in air. **b,d,** cross-sectional (**b**) and top-view (**d**) images of a water droplet on the commercial SiO_2/Si substrate in air.



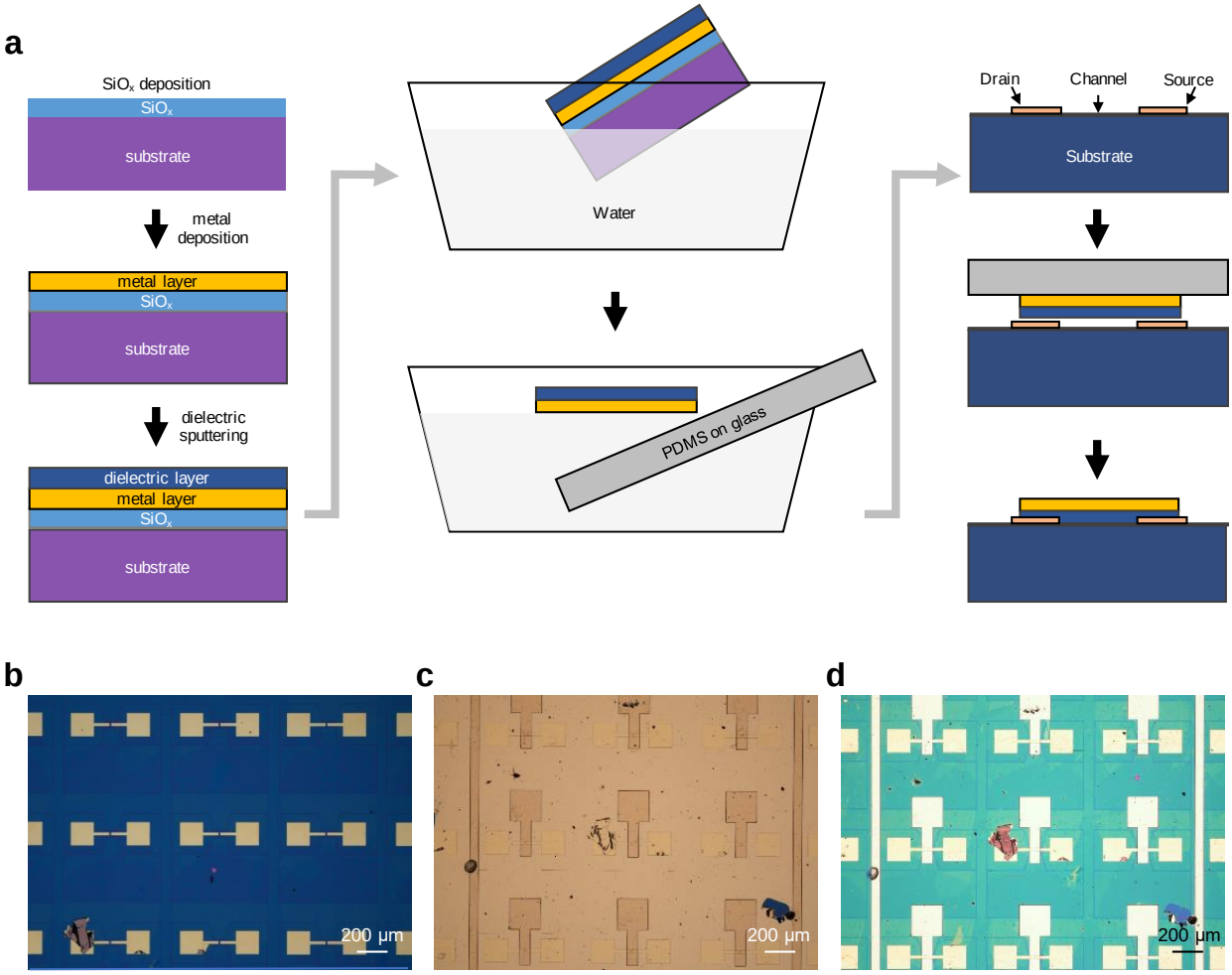
Supplementary Fig. 4 | Adhesion strength measurement. a, Photograph of the setup for the pull-out adhesion strength test. **b,** Measured adhesion strengths of three Au film samples; the mean value is 0.143 MPa. **c,** Measured adhesion strengths of three mica samples; the mean value is 0.150 MPa.



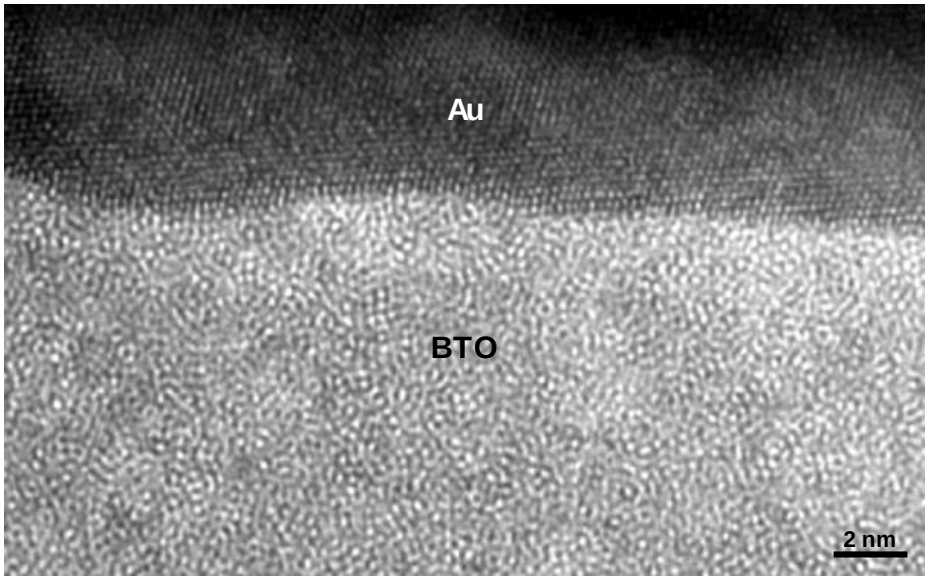
Supplementary Fig. 5 | Exfoliation of the Au film. a, Photograph of the exfoliation process for a wafer-scale Au film. **b,** Photograph of the free-floating Au film on water after exfoliation. Inset: the initial Au film on the SiO_x/Si substrate prior to exfoliation.



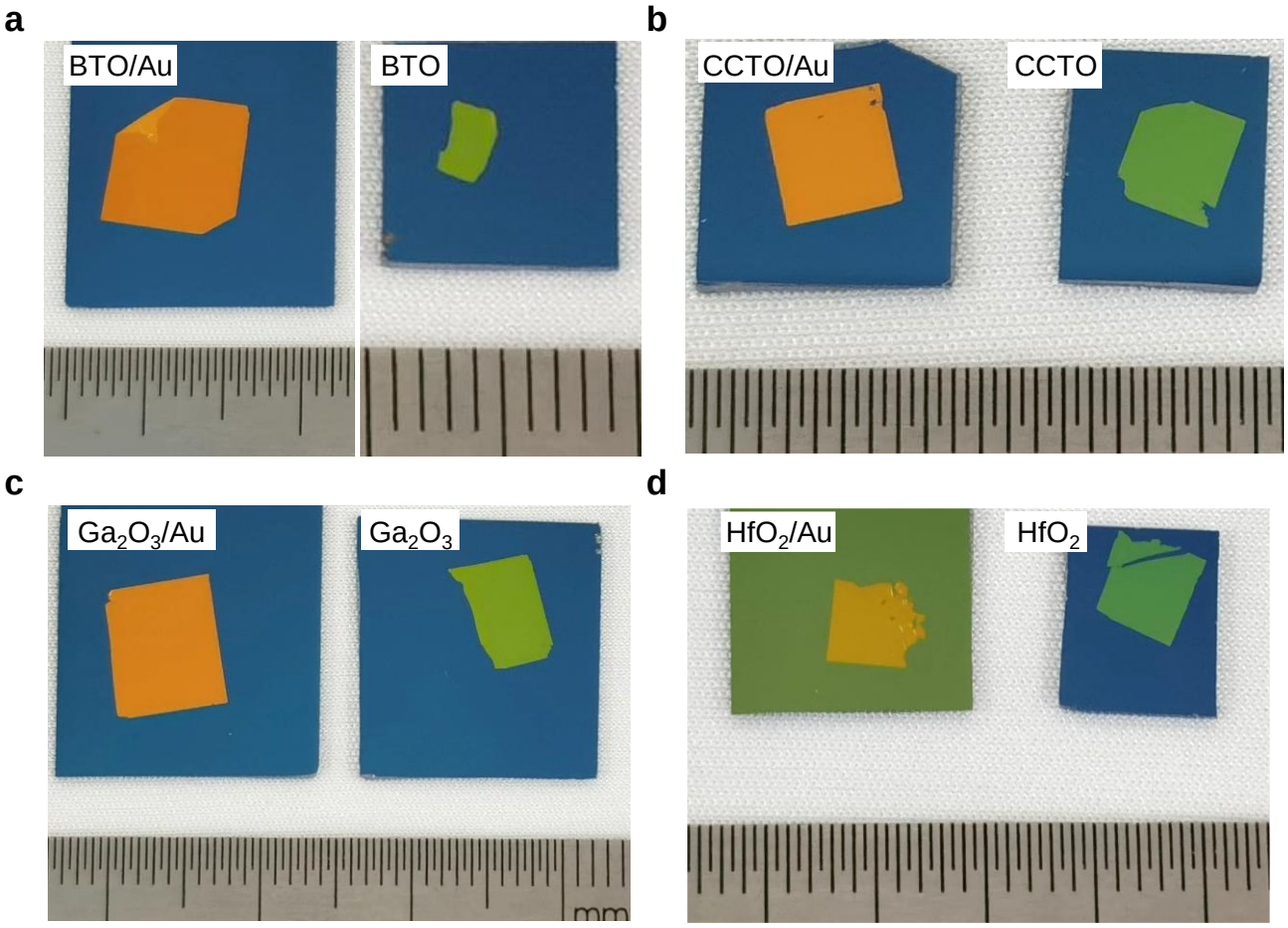
Supplementary Fig. 6 | Exfoliation and transfer of a Ga_2O_3/Au film. a, Photograph of the Ga_2O_3/Au film deposited on the initial substrate. **b,** Image showing the retrieval process of the exfoliated film from the water surface. **c,** Photograph of the Ga_2O_3/Au film on the target substrate.



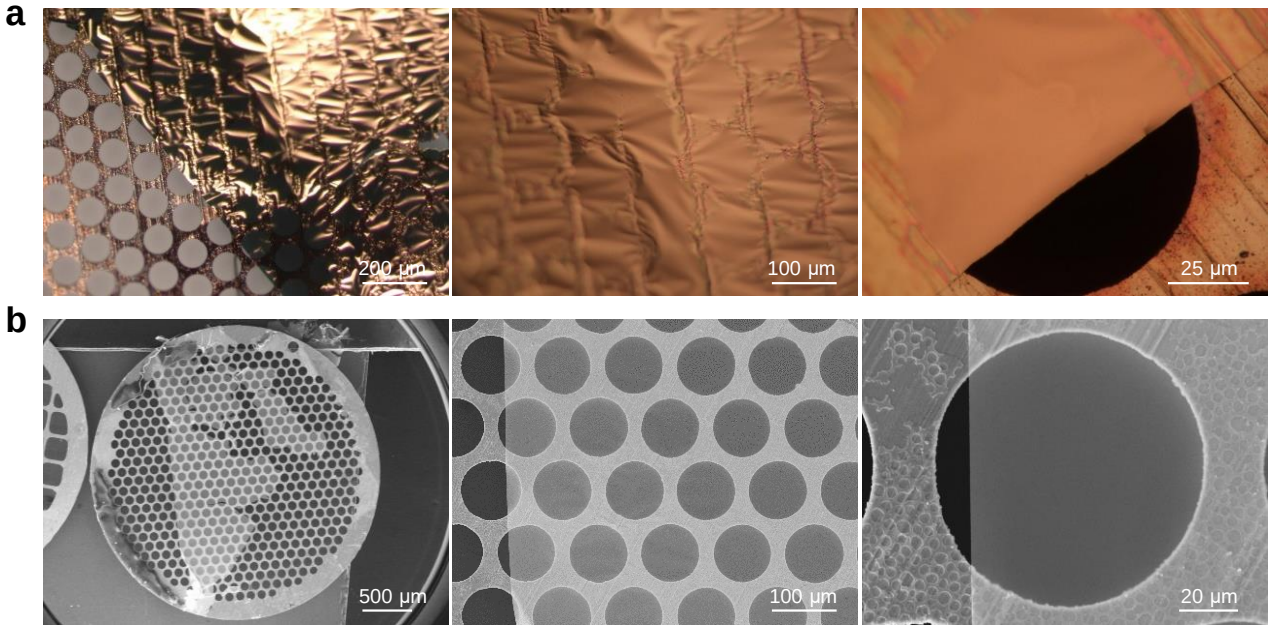
Supplementary Fig. 7 | Fabrication process of the top-gate transistors. a, Schematic illustrating the complete fabrication process of the top-gate transistors, including the deposition, exfoliation, and transfer of the gate stack film, as well as the construction of the source, drain, and channel. **b,** Optical micrograph of a MoS_2 field-effect transistor (FET) array showing bottom contacts and channels. **c,** MoS_2 FET array after patterning of the top-gate film, prepared for etching. **d,** Completed top-gate MoS_2 FET array.



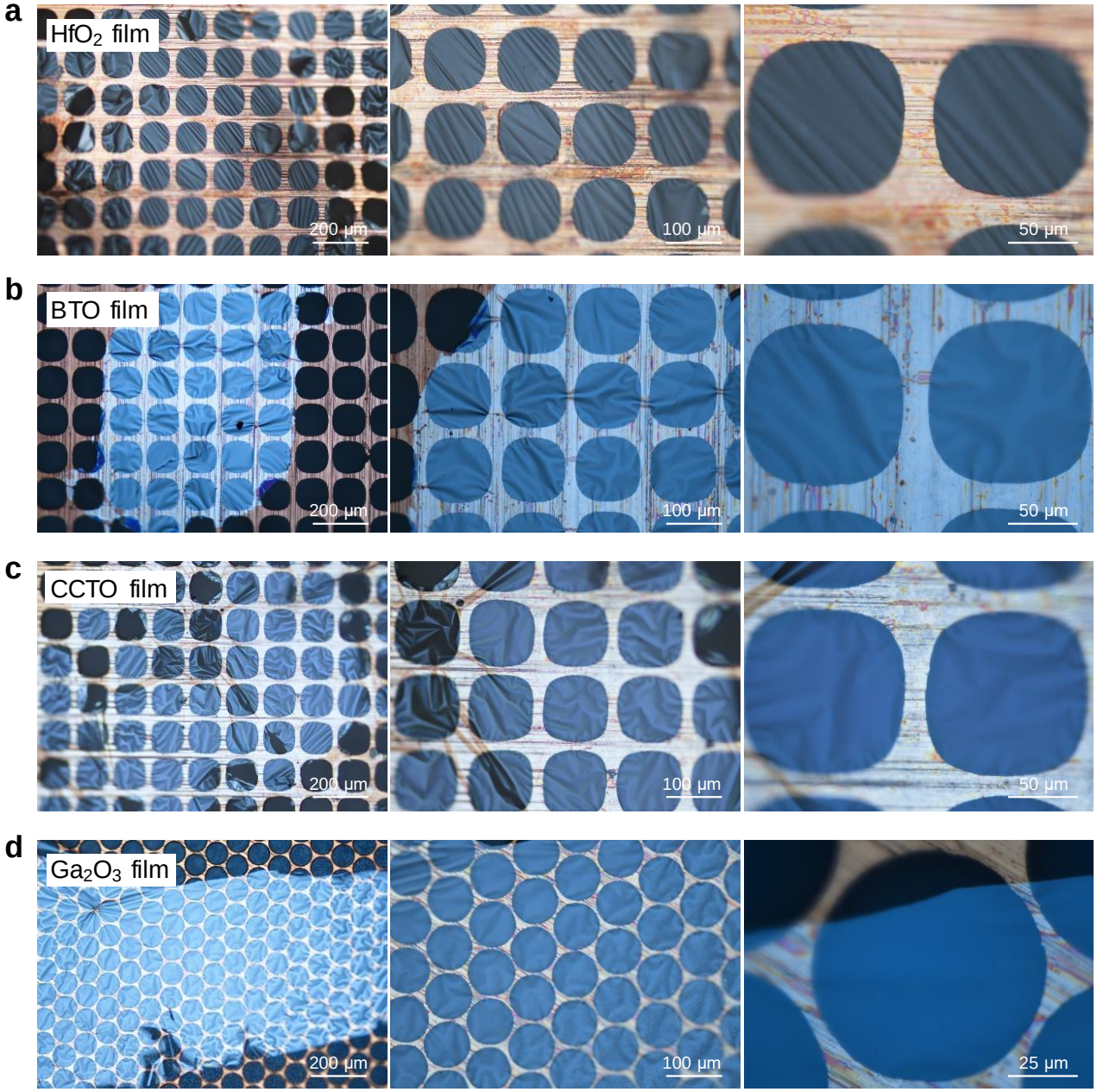
Supplementary Fig. 8 | High-magnification cross-sectional transmission electron microscope (TEM) image of BTO/Au film. The underlying BTO layer is fully amorphous, whereas the top Au layer exhibits clear crystallinity.



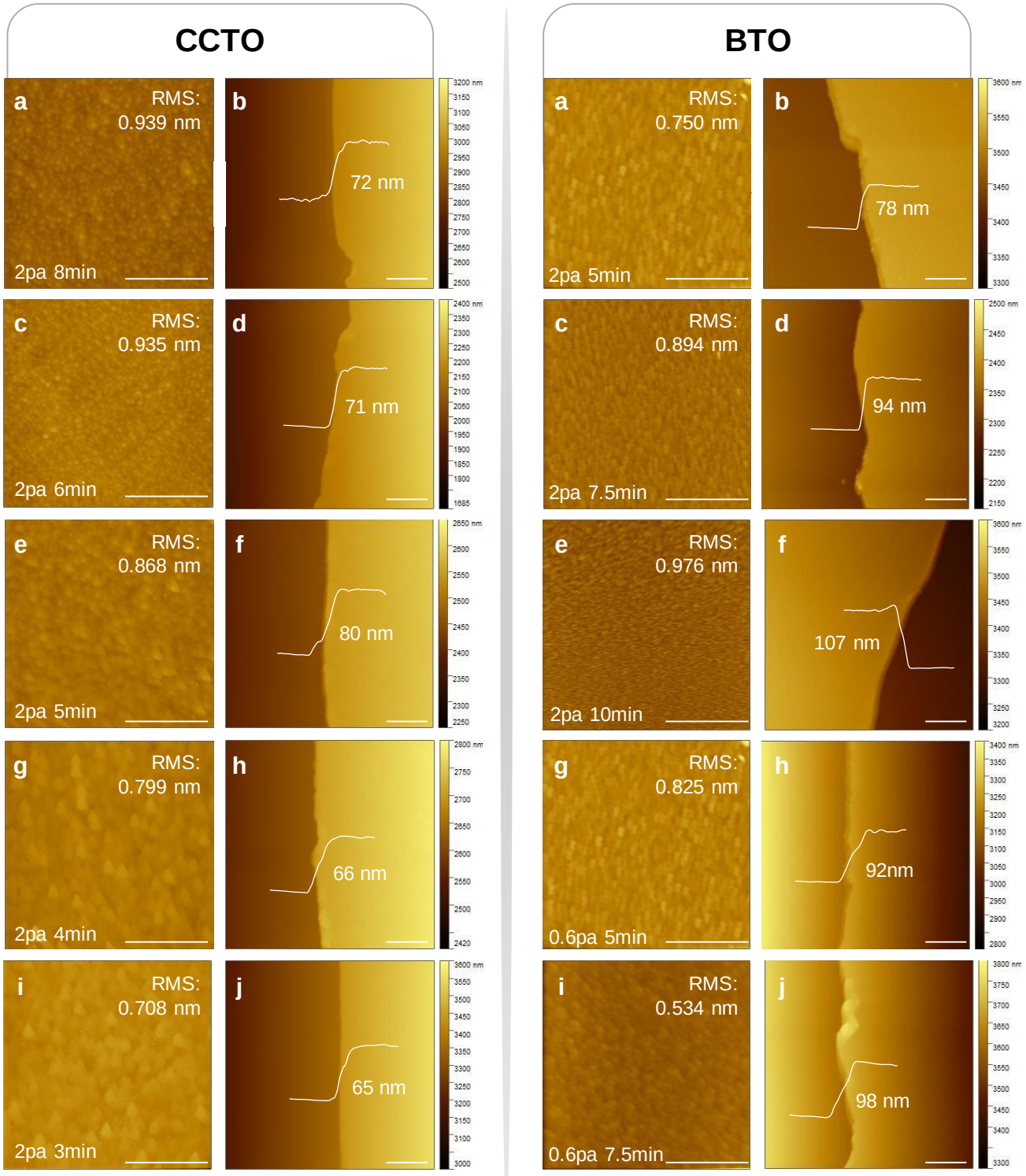
Supplementary Fig. 9 | Photographs of various transferred dielectric films with and without the Au capping layer. $BaTiO_3$ (BTO) films (**a**); $CaCu_3Ti_4O_{12}$ (CCTO) films (**b**); Ga_2O_3 films (**c**); HfO_2 films (**d**). For films shown without Au, the metal layer was removed by wet etching. The minimum scale of rulers is 1 mm.



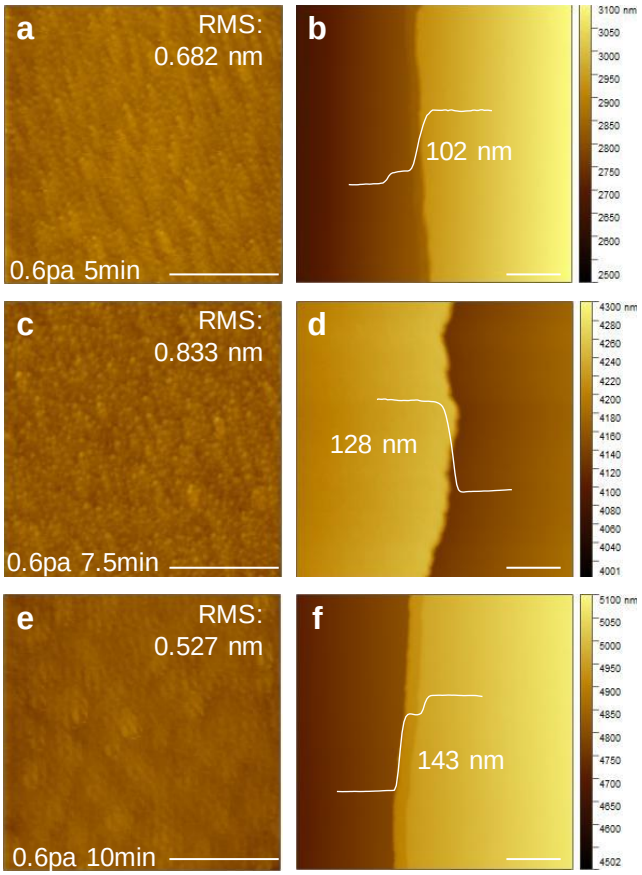
Supplementary Fig. 10 | Images of the transferred Au film on the Cu mesh. a, Optical images of the transferred Au film. **b,** Scanning electron microscope (SEM) images of the transferred Au film.



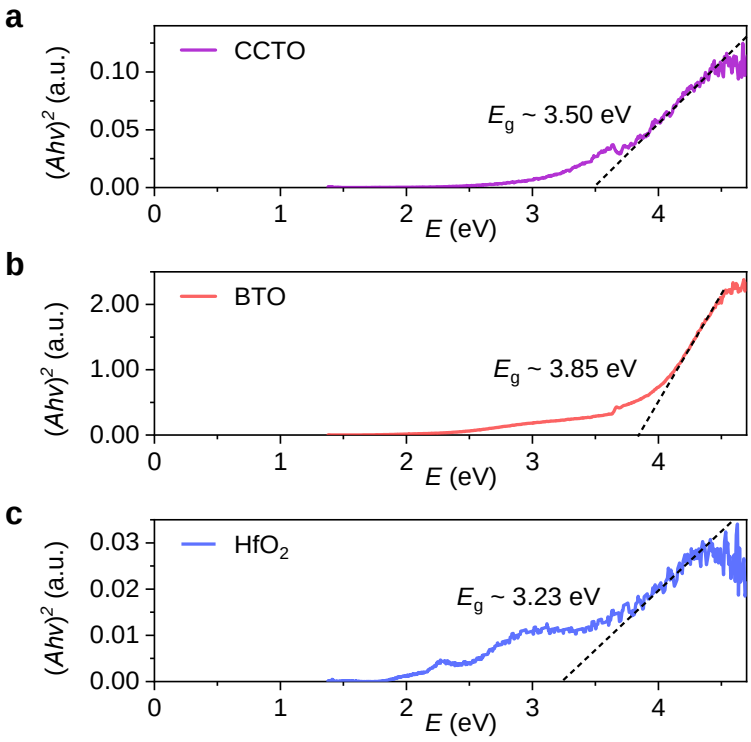
Supplementary Fig. 11 | Optical images of dielectric films transferred onto Cu meshes: HfO_2 film (**a**); BTO film (**b**); CCTO film (**c**); Ga_2O_3 film (**d**).



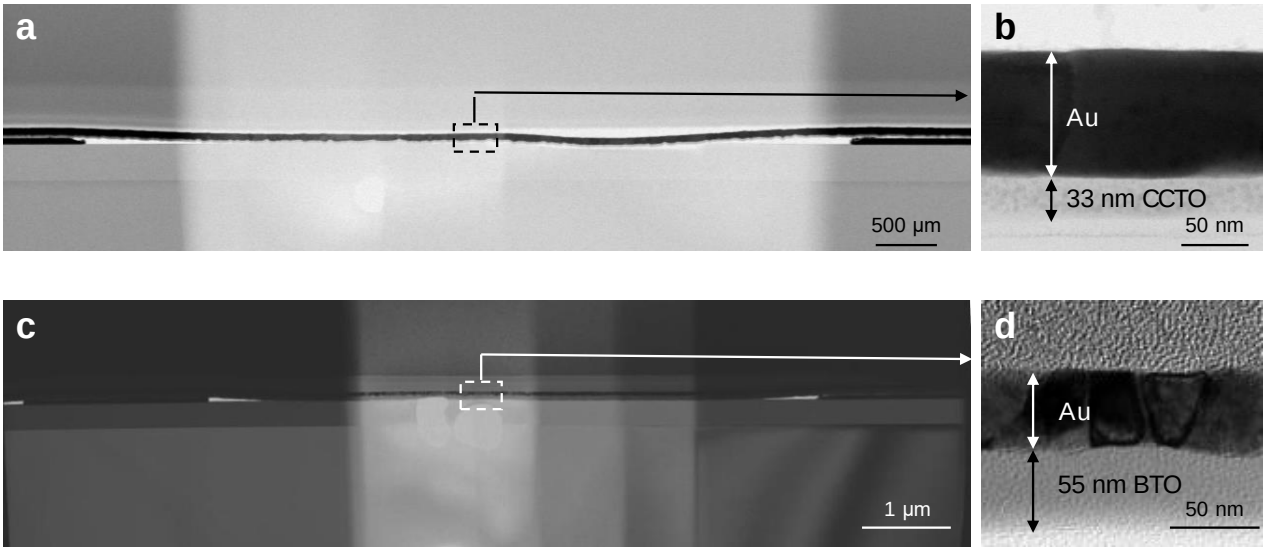
Supplementary Fig. 12 | Atomic force microscope (AFM) images of the sputtered dielectric/Au films (left: CCTO/Au films; right: BTO/Au films). For each set, films were deposited under varying sputtering pressures and durations, as indicated in the corresponding images. All thickness values denote the total stack height (dielectric + Au). The dielectric layer thickness was determined by subtracting the Au thickness (50 nm for CCTO, 60 nm for BTO). In all cases, the root-mean-square (RMS) surface roughness remains below 1 nm. Scale bars: 2 μm.



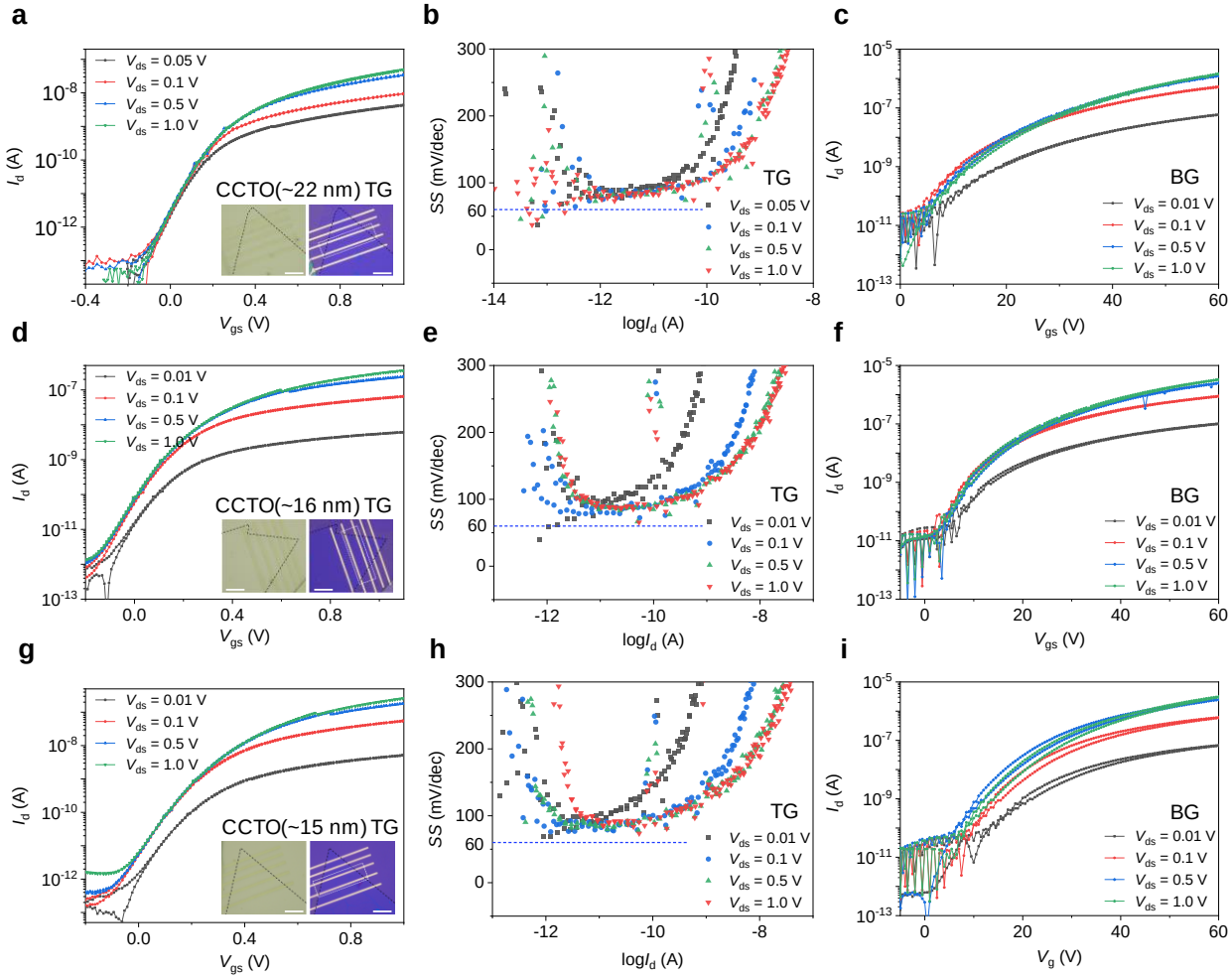
Supplementary Fig. 13 | AFM images of sputtered Ga_2O_3/Au films with varying deposition durations. The sputtering conditions, RMS roughness, and total stack thickness (Ga_2O_3 + 60-nm-thick Au layer) are indicated on each panel. Film thickness shows a generally linear dependence on sputtering time, with smooth surfaces exhibiting RMS roughness below 1 nm. Scale bars: 2 μm.



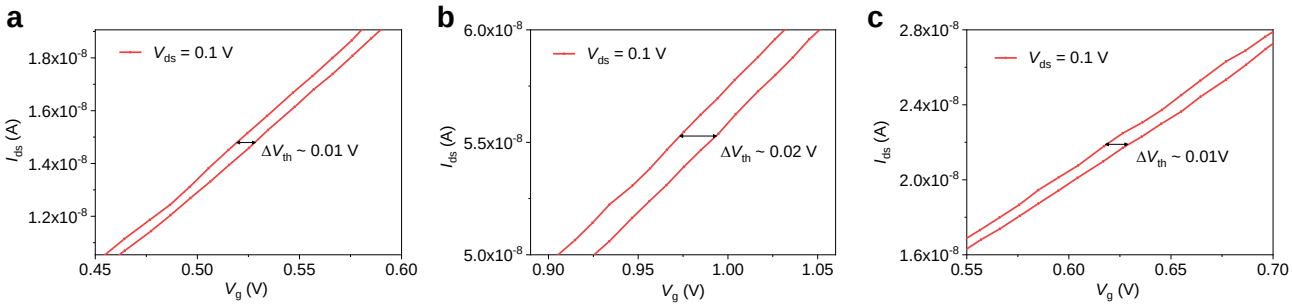
Supplementary Fig. 14 | Tauc plots of $(Ah\nu)^2$ versus photon energy ($h\nu$) for the CCTO (a), BTO (b), and HfO_2 (c) films. A is the absorbance (A = -ln T). The direct optical bandgaps are determined by extrapolating the linear regions of the Tauc plots (dashed lines), yielding values of 3.50 eV for CCTO, 3.85 eV for BTO, and 3.23 eV for HfO_2.



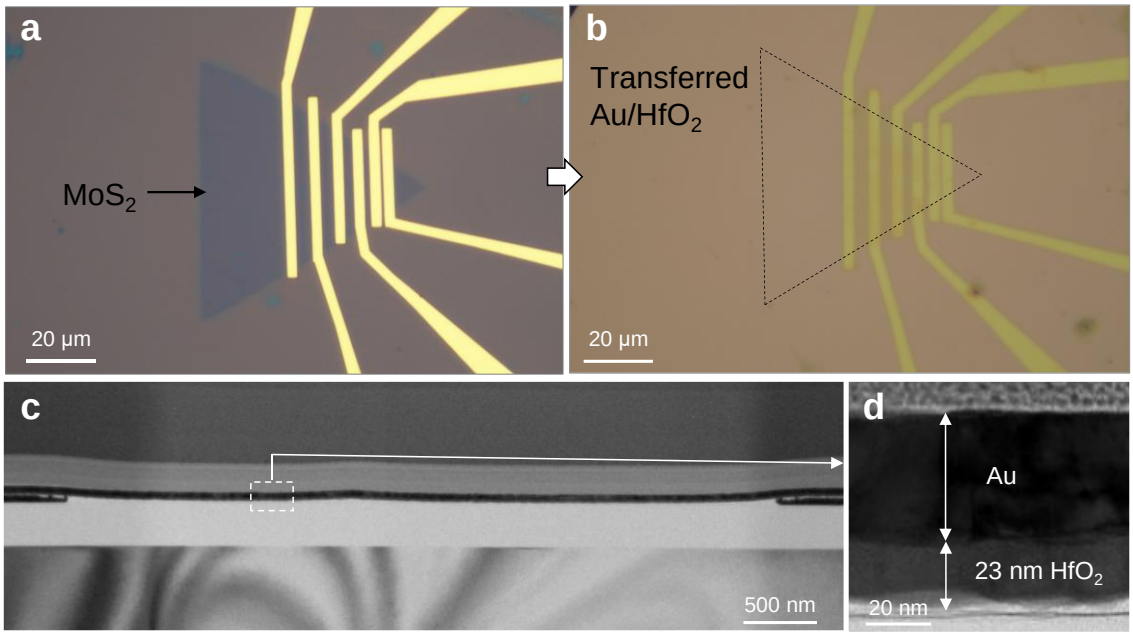
Supplementary Fig. 15 | Cross-sectional TEM images of top-gate transistors. a, Cross-sectional TEM image of a MoS_2 transistor with a transferred CCTO top-gate dielectric. **b,** Magnified view of the region outlined in white in a, showing the CCTO dielectric layer with a thickness of approximately 33 nm. **c,** Cross-sectional TEM image of a MoS_2 transistor with a transferred BTO top-gate dielectric. **d,** Magnified view of the region outlined in white in c, showing the BTO dielectric layer with a thickness of approximately 55 nm.



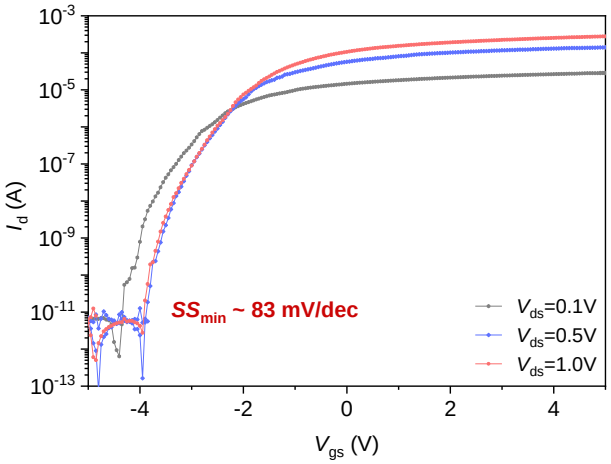
Supplementary Fig. 16 | Transfer characteristics of MoS_2 transistors with CCTO top-gate dielectrics of different thicknesses. a-c, Device with a 22-nm-thick CCTO dielectric: top-gate transfer characteristics (V_{gs}-I_d) (**a**); corresponding top-gate subthreshold swing (*SS*) versus I_d (**b**); back-gate transfer characteristics of the same device (**c**). **d-f,** Device with a 16-nm-thick CCTO dielectric: top-gate transfer characteristics (**d**); top-gate *SS* versus I_d (**e**); back-gate transfer characteristics (**f**). **g-i,** Device with a 15-nm-thick CCTO dielectric: top-gate transfer characteristics (**g**); top-gate *SS* versus I_d (**h**); back-gate transfer characteristics (**i**). Insets: optical micrographs of the corresponding devices before and after top-gate transfer and the white dashed boxes indicate the tested channels. For all devices, the top-gate operation achieves a minimum *SS* near 80 mV/dec, compared to the back-gate *SS* of approximately 5 V/dec (300 nm SiO_2 dielectric), highlighting the advanced performance of the sputtered top-gate stack. Scale bars in insets: 20 μm.



Supplementary Fig. 17 | Hysteresis in the transfer characteristics of MoS_2/CCTO top-gate transistors. Hysteresis windows measured at V_{ds} = 0.1 V for devices with CCTO dielectric thicknesses of 22 nm (**a**), 16 nm (**b**), and 15 nm (**c**).



Supplementary Fig. 18 | Optical and TEM images of a MoS_2/HfO_2 top-gate transistor. a, Optical micrograph of the MoS_2 transistor before top-gate integration. **b,** Optical micrograph of the same device after the transfer of the Au/HfO_2 top-gate stack. **c,** Cross-sectional TEM image of the completed transistor. **d,** Magnified view of the region outlined in white in **c**, showing the HfO_2 dielectric layer with a thickness of approximately 23 nm.



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138 **Supplementary Fig. 19 | Transfer characteristics of the MoS_2/HfO_2 top-gate transistor.**

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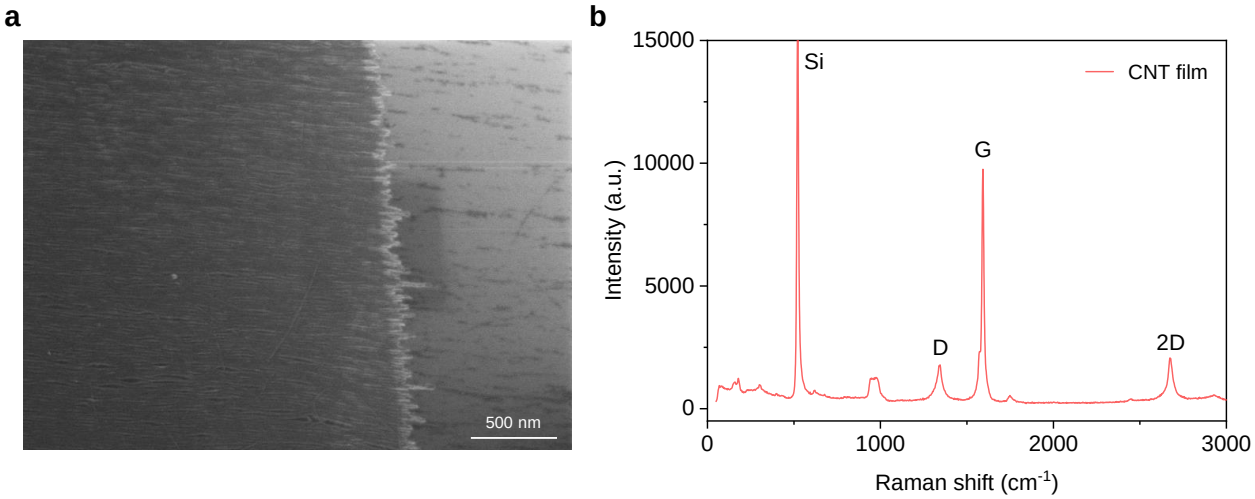

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142 **Supplementary Fig. 20 | Characterizations of oriented carbon nanotubes (CNTs). a,** SEM image of the

143 oriented CNTs. **b,** Raman spectrum of the oriented CNTs.

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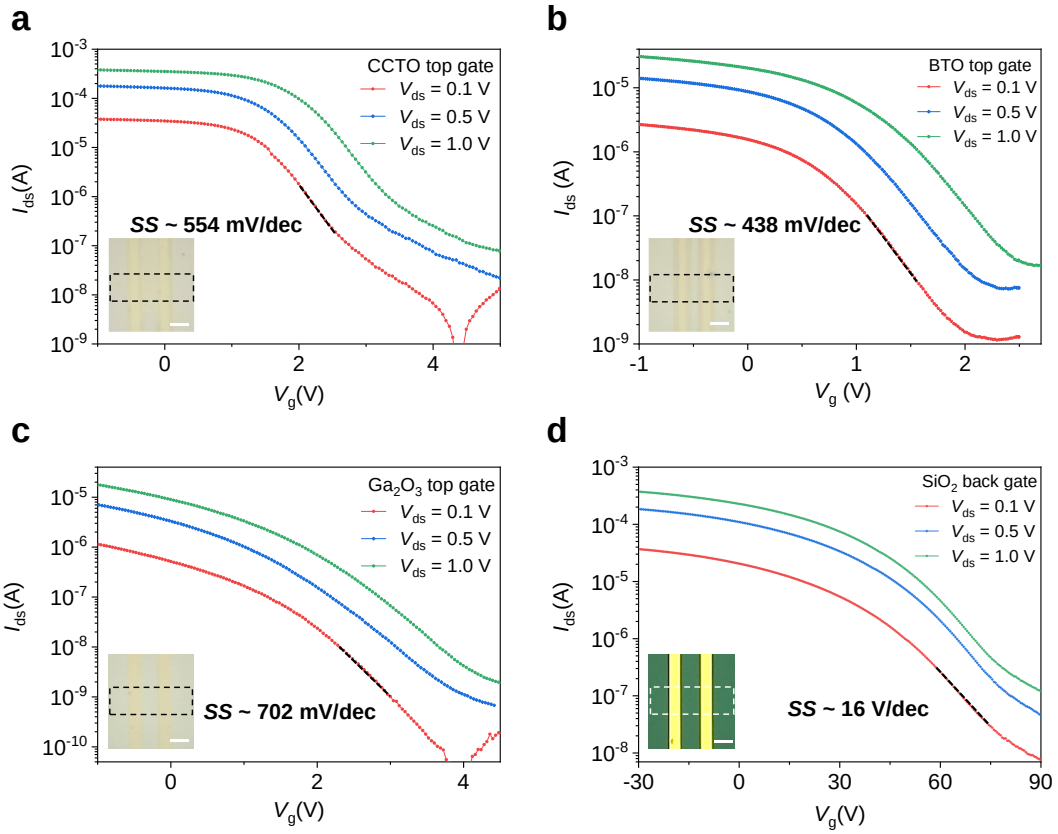
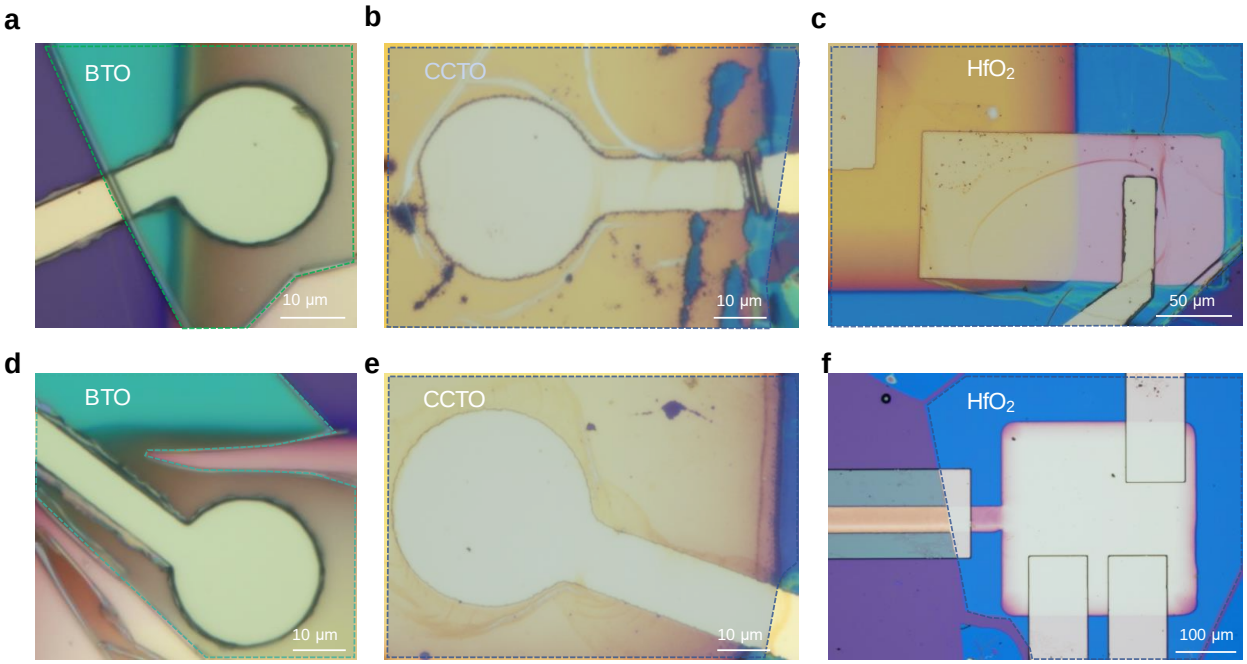


Supplementary Fig. 21 | Transfer characteristics of the oriented CNT transistors. a–c, Top-gate transfer characteristics of the oriented CNT transistors with CCTO (sputtering conditions: 2 Pa, 8 min) (**a**), BTO (0.6 Pa, 5 min) (**b**), and Ga_2O_3 (0.6 Pa, 5 min) (**c**) as the gate dielectric, respectively. **d,** Back-gate transfer characteristics of an oriented CNT transistor with 300 nm SiO_2 as the gate dielectric. Insets show optical micrographs of the corresponding devices, with dashed boxes indicating the channel regions. Scale bars in insets: 10 μm. The subthreshold swings of the top-gate transistors are at least 20 times lower than those of the conventional SiO_2 back-gate device.



Supplementary Fig. 22 | Optical images of the fabricated BTO/CCTO/HfO_2 capacitors. a,d, Capacitors with a 55-nm-thick BTO dielectric layer. **b,e,** Capacitors with a 33-nm-thick CCTO dielectric layer. **c,f,** Capacitors with a 23-nm-thick HfO_2 dielectric layer. The shaded areas indicate the regions of the dielectric films.

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