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# Energy-Efficient Hybrid Approximate Radix-8 Multiplication Architecture for Adaptive Acoustic Feedback Suppression in Wearable Hearing Aids

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## ABSTRACT

Wearable hearing aids require low-power and low-latency signal processing to provide clear speech perception in acoustically challenging environments. But the acoustic feedback between the loudspeaker and microphone also affects speech intelligibility and device performance significantly. This paper proposes an energy-efficient adaptive feedback suppression architecture based on a hybrid approximate Radix-8 multiplication framework to reduce computational complexity while maintaining high speech enhancement quality. The input speech is first digitized by an approximate successive approximation register analog-to-digital converter to acquire the signal with energy efficiency. The digitized signal is then processed using a Parks-McClellan optimized adaptive feedback suppression filter, where multiplication-intensive finite impulse response filtering is accelerated through a hybrid approximate Radix-8 multiplier. The proposed multiplier is optimized Radix-8 Booth encoding and decoding scheme, an approximate truncated round multiplier and an approximate 5:3 compressor for reducing partial-product generation complexity, hardware resources, power consumption and critical-path delay. A Xilinx Kintex-7 XC7K325T FPGA is used for the implementation of the proposed architecture for hardware validation. The experimental results are: Perceptual Evaluation of Speech Quality (PESQ)of 3.46 dB, Signal-to-Noise ratio (SNR) improvement of 20.5 dB, Processing delay of 43.05 ns, and power consumption of 119.8 mW. The proposed architecture also consumes less power than ScaleTRIM, DA-AFIR-leadx-hybam-AC, DAAFA, and ARCWM by 36.85%, 42.94%, 23.07%, and 33.21%, respectively.

**Keywords:** Wearable hearing aids, Adaptive Feedback Suppression, Optimized Radix-8 Booth Encoder and Decoder, Approximate Truncated Round Multiplier, Speech quality.

## 1 INTRODUCTION

Sound is a vital communication tool, allowing humans to share information and interact with the world around them. It is possible to detect whether this sound is from a human or another object, by processing an existing audio signal. Speech signals are different in nature for different individuals and have important characteristics that are related to human communication [1][2]. Words from sound signals can also be used to control or direct various devices. Hence, the importance of processing and utilization of an audio signal. People with hearing loss may struggle to grasp the actual message of speech in their daily routines [3]. The problem is addressed by the development of a wearable hearing aid device, which is frequently used to compensate for hearing loss by adjusting the dynamic range. Even when hearing aids work well, however, many people experience the noise from the hearing aid interfering with the speech input to the ear. Specifically, there are only 23% of people with hearing impairment (HI) who use hearing aid devices [4][5].

Acoustic feedback cancellation is used in many applications, such as hearing aids, active noise reduction systems and public address systems, and adaptive filtering methods are well known and commonly used. An adaptive filter is used in hearing aid systems to compensate for the feedback path between the microphone and loudspeaker [6][7]. The acoustic feedback interference is then cancelled out and effective acoustic feedback cancellation is accomplished subtractively by subtracting the estimated acoustic feedback component from the microphone signal. The hearing aid microphone and speaker operating too close to each other cause this problem. In hearing aids, the amplified signal is returned to the microphone on a path known as the Feedback path [8,9]. Too much gain causes the system to become unstable and causes the user to become uncomfortable as it produces howling in the ear, while the acoustic feedback prevents the maximum gain possible. In reality, however, the adaptive filter estimate will generally be biased because of the correlation between the input signal and the signal from the loudspeaker in the closed-loop acoustical system [10].

The estimation of the acoustic feedback path is typically based on common methods such as least mean squares (LMS) or normalized LMS (NLMS), which are simple yet efficient. Unfortunately, these algorithms cause the convergence rate of an AFC system to suffer when applied to the scenario of spectrally coloured incoming signals [11][12][13]. The LMS and NLMS adaptive filters are effective for acoustic feedback cancellation, but are difficult to implement in wearable devices because they require a large amount of calculation and energy. The process of adaptation is continuous and involves the repeated execution of arithmetic

operations that lead to a delay of power consumption and increase the processing delay [14]15]. To address these issues, a novel HARMONIC AFS is proposed. The primary key contributions are,

- ❖ The primary objective of this paper is to propose a novel HARMONIC-AFS for low-power and real-time speech enhancement in wearable hearing aid applications.
- ❖ SAR-ADC is used to efficiently digitize the input speech signal with minimized power consumption and conversion latency to enable energy-efficient signal acquisition.
- ❖ The proposed method uses a Parks-McClellan optimized AFS filter is used to effectively estimate and suppress acoustic feedback while preserving the desired speech components.
- ❖ HARMONIC multiplier is designed by integrating ORBED, ATRM and an approximate 5:3 compressor to perform the multiplication operations in the AFS filter with minimized hardware complexity, power consumption and propagation delay.
- ❖ Experimental results demonstrate that the proposed method provides low power and low hardware cost for the real-time wearable hearing-aid applications with enhanced speech augmentation performance.

The rest of this paper is organized as follows: Section 2 provides a review of the literature, and Section 3 presents the proposed methodology. The experimental data are discussed in Section 4, and the conclusions and suggestions for further research are given in Section 5.

## 2 LITERATURE REVIEW

In 2025, Tadigadapa, P. and Jagadamba, P., [16] designed a 16-bit multiplier design where only the carry generated by the first 16 Most Significant Bits of the output is taken into consideration. The image compression application using DCT was tested with the designed multiplier architecture with reduced power consumption and space requirement as compared to existing multiplier architectures, and the results of the simulation were quantified. For the same PSNR of 22.19 dB, the approximation multiplier design in the suggested work achieves 67.62% power saving.

In 2026, Farahmand, E et al., [17] suggested scaleTRIM, a scalable approximate multiplier design that mimics the multiplication operation using linearization, or fitting linear functions. Diagonal slicing was applied to the input operands, reducing them to a reduced bit-width representation using their leading-one positions, and a novel error-reduction technique is provided in the proposed design, which is based on a lookup table (LUT). The suggested design

is the best as compared to the existing designs. Specifically, it exhibits about 15.2% MRED (Mean Relative Error Distance) and about 22.8% PDP (Power Delay Product) reduction.

In 2024, Vafaei, J. and Akbari, O., [18] introduced an adaptive FIR filter design which employs an approximation adder and an approximate multiplier of hybridizing (Radix-8 Booth and TRAM) structure to reduce the noise of the sensor node (DA-AFIR-leadx-hybam-AC). The HPRMul consisted of two reduced precision (RP) multipliers and a simple voter to choose the output. When compared to the standard Triple Modular Redundancy (TMR) based multipliers, the efficiency of the proposed HPR-Mul is evaluated in comparison with it for 15-nm FinFET technology, and the result shows that it consumes up to 70% and 69% power and area, respectively.

In 2023, Immareddy, S et al., [19] presented an adaptive FIR filter design that reduces the noise in the sensor node by using an approximation adder and a hybridizing (Radix-8 Booth and TRAM) approximate multiplier (DA-AFIR-leadx-hybam-AC). The synthesized design was carried out in an FPGA using the tool Xilinx ISE 14.5, and the designed approach was simulated in a Verilog file. Compared to the current designs, the designed filter achieves a delay reduction of 43.58%, 11.3%, and 33.07% and a power reduction of 33.6%, 22.75%, and 29.69%.

In 2024, James, B.P et al., [20] developed an efficient distributed arithmetic adaptive FIR filter (DAAFA) structure with radix-4 and radix-8 processing. The design uses an adaptive FIR filter, with a low complexity single multiply and add (MAC) unit to implement it in fixed point. The experimental results show that the architecture reduces the area by almost 92.03% in terms of Slices and enhances the processing speed by about 90.7% over the conventional architecture.

In 2025, Madhushankara, M et al., [21] suggested a modified recursive least squares (M-RLS) algorithm was used to improve the speech quality of electrolarynx-based communication by effectively suppressing the excitation noise. The PDP of the hardware implementation is only 15.41 pJ, runs at 1 GHz and consumes 16.9 mW. These attributes are suitable for power-limited speech enhancement applications. In addition, the proposed approach was successfully implemented using rapid prototyping on a DE10 FPGA board and testable at 253.8 MHz.

In 2024, Sadeghi, A et al.,[22] presented two low-complexity approximate 4:2 compressors, namely an 8-transistor and a 14-transistor design, and integrated them into an approximate multiplier architecture for image processing applications. When compared to the precise multiplier, the designed multiplier has 50% area saving, 93% power-delay-product reduction, higher accuracy and 38% PDP improvement.

In 2024, Thannoon, H. and Hashim, I., [23] introduced an adaptive filter architecture for ECG signal denoising applications using retimed delay (RD). The strategy was built on a systolic design, which minimizes the amount of processing components, such as adders and multipliers, in each iterative process in order to lower the critical path time. The power consumption of the RDLMS, RDRLS and RDAP filters was reduced by approximately 40.5%, 28.6% and 5.9%, respectively.

In 2022, Perri, S et al., [24] designed an approximate multiplier for ASIC and FPGA applications that is energy-efficient and platform-independent. The designed approach performs the bit-significance-based encoding logic and computes the approximation product by using precise sub-multiplications in an innovative way instead of using the standard static or dynamic bit-truncation method. Experimental results indicate that up to 80% energy savings over the precise multipliers, and up to 82% reduced energy consumption in edge detectors and 2D digital filters, give energy efficiency of about 2 times higher than the current state of the art approximation multipliers.

In 2026, Rizos, I et al., [25] presented an Approximate Reduced Complexity Wallace Multiplier (ARCWM) for less energy-consuming parallel multiplication applications. The proposed approach uses approximate Full Adders instead of exact Full Adders in the partial product reduction stage to improve the conventional Reduced Complexity Wallace Multiplier (RCWM). The experimental results show up to 65% area reduction and 70% power saving with the same delay as conventional RCWM, which is suitable for error-tolerant applications like neural accelerators and signal processing systems.

According to the literature review, the existing approximate multiplier and adaptive feedback suppression techniques still face several limitations. The existing methods have high hardware resource consumption, high propagation delay, and high-power consumption, making them unsuitable for resource-constrained real-time applications. Moreover, the challenge of achieving an effective balance between speech enhancement quality and hardware efficiency is still a challenging problem, especially for wearable hearing-aid applications. To tackle these challenges, a novel HARMONIC-AFS is proposed to achieve high-quality speech enhancement with minimized hardware complexity, low power consumption and high-speed operation.

## 3 PROPOSED HARMONIC AFS METHOD

In this section, a novel Hybrid Approximate Radix-8 Multiplier-Based Adaptive Feedback Suppression (HARMONIC-AFS) system is proposed for high-quality speech enhancement. The proposed Harmonic AFS system for energy-efficient adaptive feedback suppression in wearable devices is illustrated in Figure 1. The input speech signal is initially digitized by an enhanced successive approximation register (SAR) analog-to-digital converter (ADC), which only processes significant bits to conserve overall energy consumption. The digital signal is then applied to the Adaptive Feedback Suppression (AFS) where the feedback component is estimated and removed using the finite impulse response filter (FIR). All multiplication operations in the filter are performed using the HARMONIC multiplier to minimize the power and hardware complexity. The Parks-McClellan algorithm updates the filter coefficients to estimate and suppress the acoustic feedback component. Finally, the processed signal is then adjusted to obtain the desired output speech, and the speech quality is finally evaluated using the perceptual evaluation of speech quality metric.

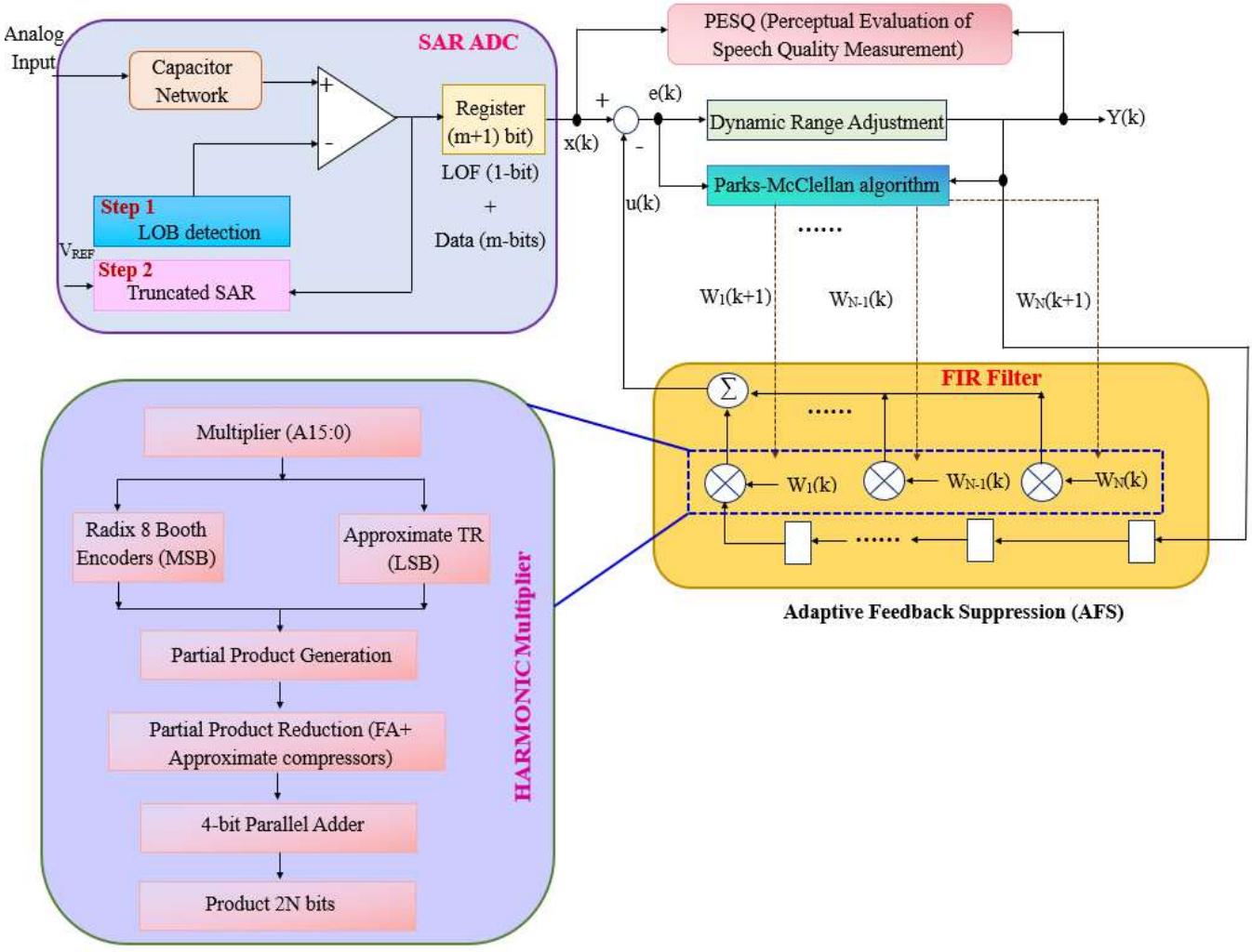



**Figure 1: Architecture of the Proposed Harmonic AFS System**

### 3.1 Approximate SAR-ADC

The analog form of the input speech signal received by the microphone cannot be processed directly by the adaptive feedback suppression unit. The analog voice signal is converted to digital form for further processing using a successive approximation register analog-to-digital converter (SAR ADC). SAR-ADC is used because of its low power consumption, moderate to high resolution, and simple hardware implementation, making it very suitable for use in wearable and battery-powered speech processing applications. Most SAR ADCs operate by a charge redistribution mechanism with a binary search algorithm to determine the digital output. The conversion starts by comparing the sampled input voltage ($V_{IN}$)with one-half of the reference voltage ($V_{REF}$) to determine the most significant bit (MSB). Based on the result of the comparison, the MSB is set to either a logic '1' or a logic '0'. The remaining bits are then computed one at a time by comparing the input voltage with successive reference levels until the LSB is determined. In this operation, the capacitor array within the SAR ADC is repeatedly switched to produce the desired reference voltages and to produce the final digital output.

The conventional SAR ADC has the advantage of accurate conversion, but the capacitors corresponding to the higher-order bits are much larger than the capacitors corresponding to the lower-order bits, so that the energy consumption is very high during the determination of the higher-order bits. As a result, a power dissipation increase during the conversion process happens when switching these large capacitors repeatedly. Most samples in speech processing applications have relatively small amplitudes, so that many of the higher-order bits are zero. As a result, a significant amount of switching energy is unnecessarily expended in processing these insignificant bits, thereby reducing the overall energy efficiency of the converter. To exploit this characteristic of speech signals, an approximate SAR ADC is employed in the proposed method. The converter identifies the significant part of the sampled data and only converts the effective bits rather than converting all the bits of the input signal. The approximate conversion process is achieved by two consecutive stages: leading one-bit detection and truncated successive approximation conversion.

#### 3.1.1 Analog Leading One Bit Detection

The approximate SAR-ADC first stage function is Analog Leading-One-Bit (ALOB) detection, which is used to determine the position of the first significant bit of the sampled input signal. It first checks if the leading-one-bit position is greater than a bit position m before it begins the conversion process from the most significant bit. This operation takes only one comparison

cycle, and also the unnecessary switching activities of higher order bits are reduced. Instead of using the reference voltage of the most significant bit, the sampled input voltage ($V_{IN}$) is compared with an $m^{th}$ bit position reference voltage. The energy used in this comparison is significantly less than the capacitor used for the $m^{th}$ bit is significantly smaller than the capacitor used for the most significant bit. If the value of the sampled input voltage is higher than the value of the reference voltage at position m, then the converter sets the leading one bit above the $m^{th}$ bit position. Otherwise, the most significant bit is assumed to be in the lower-order bit positions. The result of the comparison gives a one-bit Analog Leading-One Flag (ALOF), which represents the region that has the significant data bits.

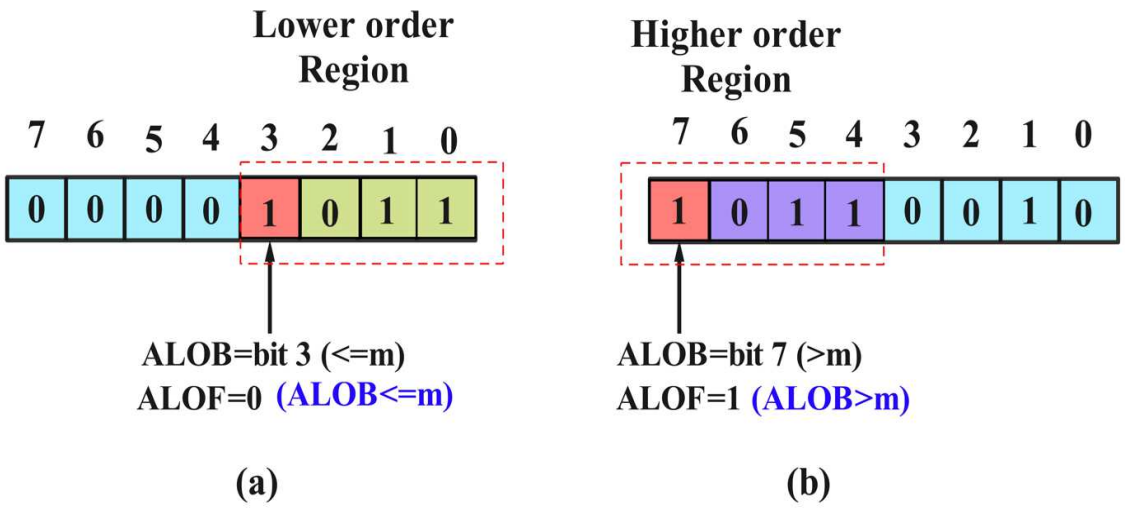



**Figure 2: Illustration of ALOB for (a) lower-order region (b) higher-order region**

Figure 2 illustrates the operation of the leading one-bit detection mechanism in the SAR-ADC. In Figure 2 (a), the first significant bit is located in the lower-order region ($ALOB \leq m$) and the ALOF is set to 0. In Figure 2(b), the first significant bit lies in the higher-order region ($ALOB > m$) which results in the generation of an ALOF value of 1. The generated ALOF is subsequently utilized by the truncated SAR conversion stage to identify the significant bit region and determine the starting point of the conversion process.

### 3.1.2 Truncated SAR

The truncated SAR stage only converts the significant bits that are detected by the leading one-bit detection circuit, and the insignificant bits are ignored. After determining the position of the ALOB, the generated ALOF is utilized to determine the starting point of the successive approximation process. Truncated SAR truncates the conversion after the m most significant

bits, and the number of comparison cycles is greatly reduced. The successive approximation method begins with the most significant bit and only calculates the m higher-order bits if the most significant bit is greater than the bit position m. Otherwise, the conversion starts at the $m^{th}$ bit position and continues for m cycles. Thus, only the effective bits that actually affect the speech signal are processed, and the remaining bits are discarded. The approximation comes from the fact that the insignificant bits, which contribute less to the final digital approximation are truncated. Truncation-induced loss of information has minimal influence on perceived speech quality because speech signals are of low amplitude and error-tolerant in nature. As a result, the truncated SAR conversion has significantly lowered the energy consumption, switched activity and hardware complexity while still retained an adequate conversion accuracy for adaptive speech signal processing applications. The digital signals generated by the approximate SAR ADC are subsequently given to the adaptive feedback suppression unit to calculate and remove the acoustic feedback from the microphone signal.

### 3.2 Adaptive Feedback Suppression Using Finite Impulse Response Filter

The adaptive finite impulse response (FIR) filter estimates and suppresses the acoustic feedback part of the microphone signal with the Adaptive Feedback Suppression unit. The filter changes its filter coefficients continuously in order to minimize the difference between the estimated feedback signal and the desired signal. The error signal e(k) is given by Equation (1).

$$e(k) = d(k) - u(k) \qquad (1)$$

Where d(k) represents the microphone input signal, and u(k) denotes the estimated feedback signal generated by the adaptive FIR filter. The objective of the adaptive filter is to minimize the mean square value of the error signal to improve the accuracy of feedback estimation.

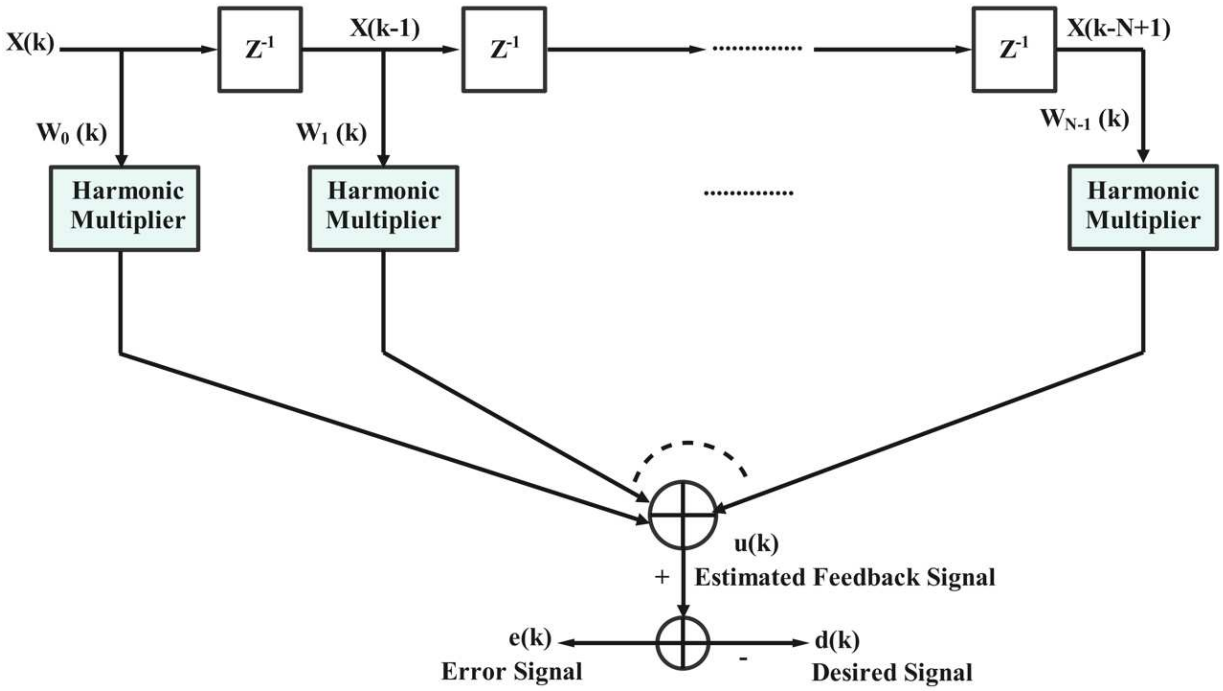



**Figure 3: Adaptive Finite Impulse Response Filter Architecture using HARMONIC Multiplier for Acoustic Feedback Suppression**

The architecture of the adaptive FIR filter used for the HARMONIC-AFS system is shown in Figure 3. The HARMONIC multiplier generates an estimated feedback signal $u(k)$ by multiplying the delayed input signal by the filter coefficients. The estimated feedback signal is then subtracted from the $d(k)$ to produce $e(k)$ for use in the adaptive feedback suppression and coefficient updating. Then, the corresponding cost function $\zeta$ is defined in Equation (2).

$$\zeta = \left(e^2(k)\right) \qquad (2)$$

where the expectation operator is denoted by E[.]. The estimate of the acoustic feedback signal is given in equation (3) and is calculated from the output of the adaptive FIR filter.

$$u(k) = \sum_{i=0}^{N-1} W_i(k)x(k-i) \qquad (3)$$

The adaptive filter coefficients are denoted as $W_i\ (k)$ and the delayed input speech samples are denoted as $x\ (k-i)$. A coefficient vector and a vector of the input sample are provided in Equation (4).

$$W(k) = [W_o(k), W_1(k), \ldots\ldots, W_{N-1}(k)]^T \qquad (4)$$

$$X(k) = [x(k), x(k-1), \ldots\ldots\ldots, x(k-N+1)] \qquad (5)$$

The adaptive filter updates its coefficients iteratively based on the computed error signal, so that the best speech quality is provided while the best estimate of the acoustic feedback path is obtained. In the proposed approach, the coefficient adaptation is implemented by the Parks - McClellan algorithm, which allows efficient optimization of the coefficients with lower computational complexity.

### 3.2.1 Parks-McClellan Based Coefficient Update Algorithm

The Parks-McClellan algorithm is used to generate and optimize the coefficients of the adaptive FIR filter used for acoustic feedback suppression. The adaptive feedback suppression unit's performance is mainly dependent on the accuracy of the filter coefficients, since inaccurate coefficients lead to low-quality feedback estimation, acoustic feedback, and impaired speech quality. The Parks-McClellan algorithm, developed by James McClellan and Thomas Parks, is one of the most popular approaches to optimal FIR filter design. The Remez exchange theorem is used to develop the algorithm, and it is based on the Chebyshev approximation principle which chooses the frequency response that has the smallest largest deviation from the desired frequency response. The algorithm gives an Equi ripple response in both pass-band and stop-band regions, which gives better frequency selectivity and lower approximation error than the traditional filter design approaches. The parameters that control the design of the FIR filter are the order N, the passband edge frequency $f_p$, stopband edge frequency $f_s$, passband ripple $\delta_p$, and stopband ripple $\delta_s$. The filter order for a given set of filter requirements is determined by Equation (6).

$$N = \frac{-20\ log_{10}\left(\sqrt{\delta_p \delta_s}\ - 13\right)}{2.32|\theta_p - \theta_s|} \qquad (6)$$

Where $\theta_p$ is the passband-edge digital frequency and $\theta_s$ is the stop-band-edge digital frequency. Figure 4 illustrates the flow chart of the Parks-McClellan-based coefficient optimization process.

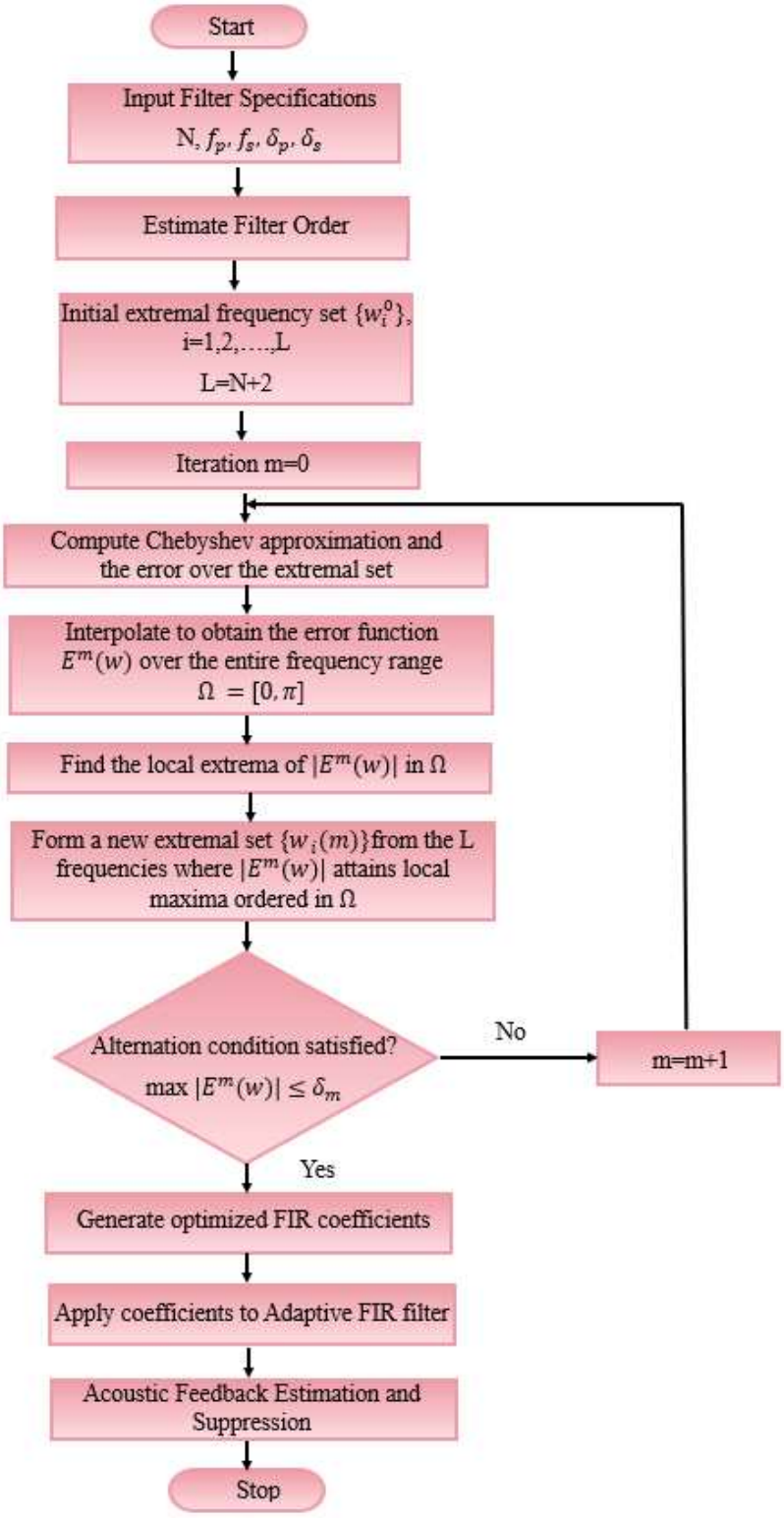



**Figure 4: Flow chart of the Parks-McClellan-based coefficient optimization process**

The coefficient of the adaptive FIR filter for acoustic feedback suppression is generated and optimized by the Parks-McClellan algorithm. An optimised coefficient set is generated after convergence and stored for implementation in an adaptive FIR filter. The adaptive feedback

suppression unit uses the new coefficients to form an estimated model of the acoustic feedback path and suppress the unwanted feedback signal in the microphone input.

### 3.3 HARMONIC Multiplier

The HARMONIC multiplier is employed in the adaptive feedback suppression system to perform the multiplication operations between the input speech samples and the adaptive FIR filter coefficients. The multiplier is widely employed throughout the feedback estimation procedure, and thus plays a significant role in the power consumption, hardware complexity and computational delay of the adaptive FIR filter. The Hybrid Approximate Radix-8 Booth Multiplier with Optimized Novel Inexact Compression (HARMONIC) multiplier is an approximate multiplier that aims at minimizing the hardware complexity and energy consumption of multiplication-intensive signal processing applications. The HARMONIC multiplier combines an Optimized Radix-8 Booth Encoder and Decoder (ORBED), an Approximate Truncated-Round Multiplier (ATRM), and approximate 5:3 compressors to minimize the number of partial products generated, while preserving the accuracy of the computation within acceptable limits. The product of the multiplier A and the multiplicand B is shown in Equation (7).

$$M = A\ X\ B = \sum_{c=1}^{2D} m_c\, 2^{-c} \qquad (7)$$

Where M is the result of the multiplication and D is the word length of the operand. The multiplier and multiplicand operands are given in Equations (8) and (9).

$$A = \sum_{E=1}^{D} a_E 2^{-E} \qquad (8)$$

$$B = \sum_{F=1}^{D} b_F 2^{-F} \qquad (9)$$

where $a_E$ are the individual bits of the multiplier and $b_F$ are the individual bits of the multiplicand.

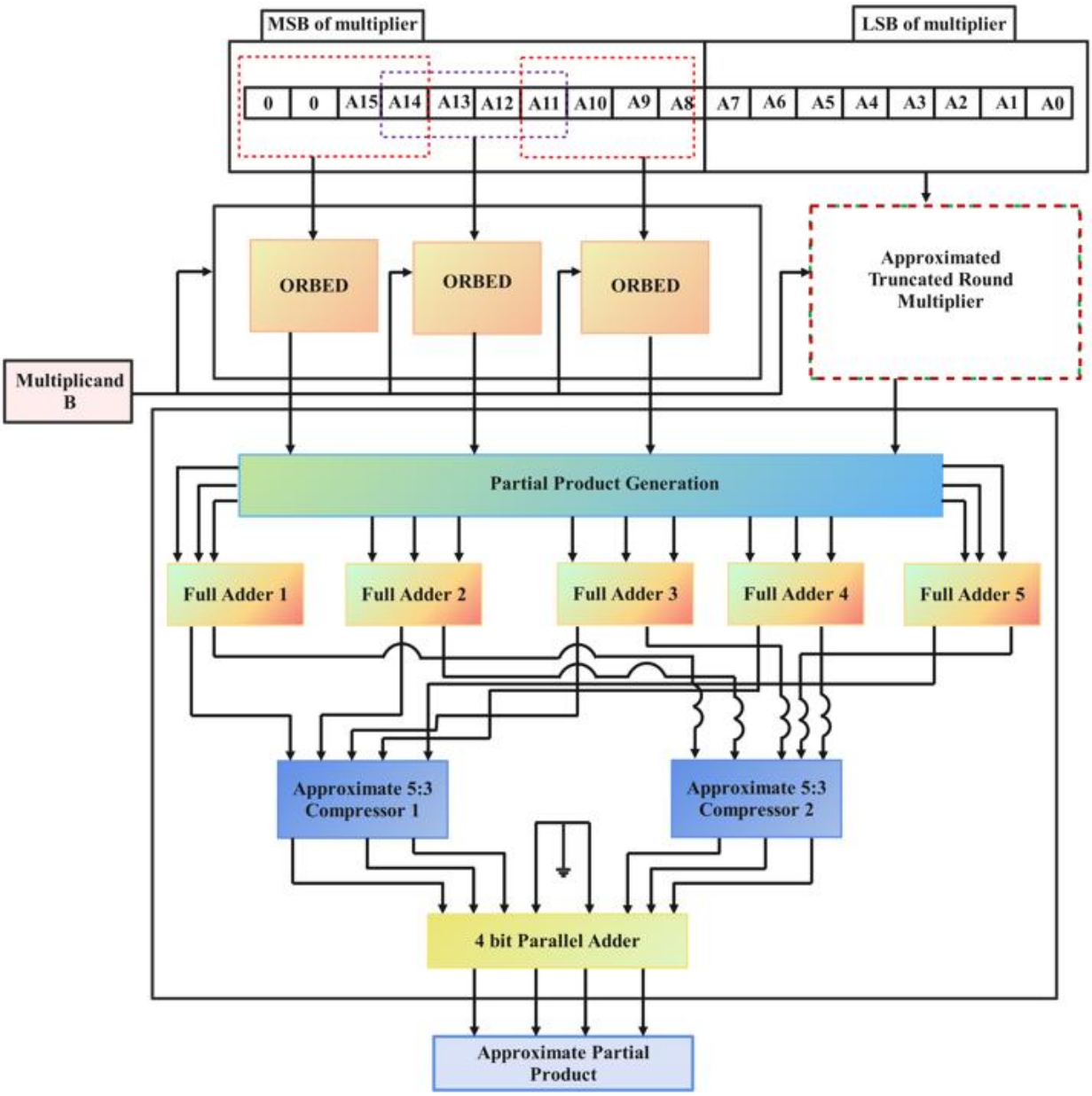



**Figure 5: Architecture of the 16-bit HARMONIC Multiplier**

The architecture of the 16-bit HARMONIC multiplier is shown in Figure 5. The multiplier is split into two computational parts depending on the value of the bits. The ORBED unit processes the most significant bits (MSBs) of the multiplier and multiplicand, while the ATRM unit processes the least significant bits (LSBs) of the multiplier and multiplicand. The ORBED uses the Booth recoding technique to minimise the number of partial products produced and preserve high multiplication accuracy in the higher order bits. By contrast, the ATRM unit emulates the lower order calculations by truncating and rounding, which reduces switching activity, hardware usage and power consumption. In a partial product generation stage, the partial products of the two units are combined, followed by compression in approximate 5:3

compressors and full adders, and finally accumulation in a parallel adder to obtain an approximate multiplication result.

### 3.3.1 Optimized Radix-8 Booth Encoder and Decoder (ORBED)

The Optimized Radix-8 Booth Encoder and Decoder (ORBED) is introduced in the HARMONIC multiplier to process the most significant bits (MSBs) of the multiplier and multiplicand efficiently. In ORBED, optimized Radix-8 Booth recoding is used to reduce the number of partial products generated, without compromising the accuracy of multiplication in the higher-order bit region. This reduction decreases the energy efficiency and computational speed of the adaptive FIR filter in terms of hardware complexity, switching activity and propagation delay. The gate-level architecture of the proposed ORBED used in the HARMONIC multiplier is shown in Figure 6. Figure 6(a) shows the ORBED encoder, which takes the multiplier bits $Y_{2i+1}$, $Y_{2i}$, and $Y_{2i-1}$ and provides the control signals $Zero_i$, $neg_i$, $ot_i$, and $cor_i$ for efficient Booth recoding. They are control signals which are used to specify the multiplication operation and, at the same time reduce the amount of unnecessary switching activity in the generation of partial products. The corresponding ORBED decoder is shown in Figure 6(b), which uses the encoded control signals along with the multiplicand bits to produce the required partial products. The decoder has an efficient implementation of the $0X$, $\pm 1X$, and $\pm 2X$ multiplication operations, which minimize hardware, switching activity and propagation delay. Table 1 shows the truth table of the ORBED with various combinations of inputs.

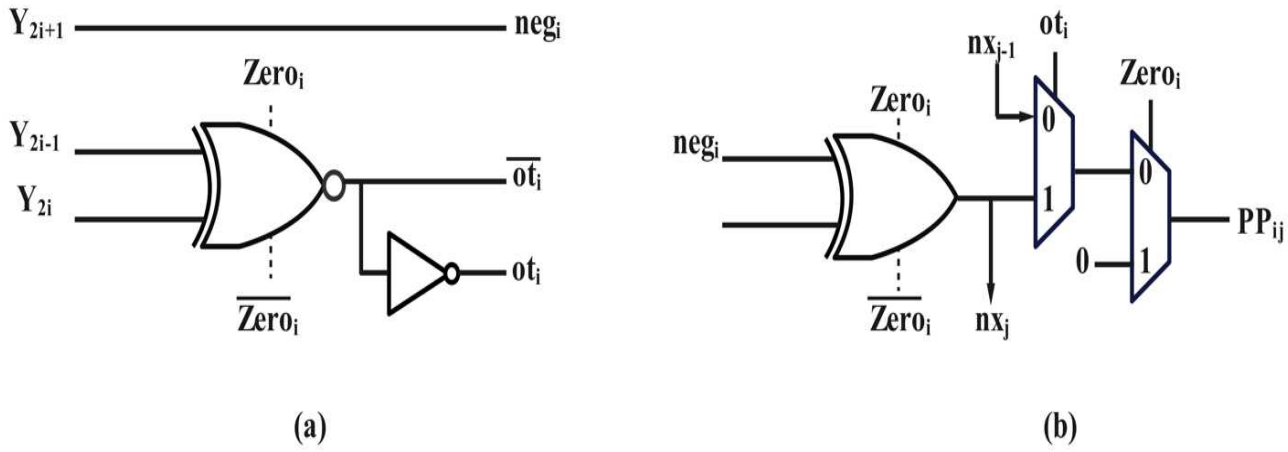



**Figure 6: Gate-Level architecture of the ORBED (a) Encoder (b) Decoder**

**Table 1: Truth table of the ORBED**

| Input Pattern | | | Operation on X | $Zero_i$ | $neg_i$ | $ot_i$ | $cor_i$ |
|---|---|---|---|---|---|---|---|
| $Y_{2i+1}$ | $Y_{2i}$ | $Y_{2i-1}$ | | | | | |
| 0 | 0 | 0 | 0X | 1 | 0 | d | 0 |
| 0 | 0 | 1 | +1X | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | -1X | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | +2X | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | -2X | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | -1X | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | -1X | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0X | 1 | 1 | d | 0 |

The ORBED encoder takes three consecutive bits of the multiplier and produces three bits of the output code, namely $neg_i$, $ot_i$, and $zero_i$. A signal $zero_i$ is provided at the pre-encoding stage for detecting the 0X multiplication condition at an early stage. The encoder circuit enables gating logic, which helps to eliminate unnecessary switching activities when the 0X condition is detected, thus reducing both dynamic and leakage power consumption. Otherwise, the encoder operates normally and generates the corresponding Booth encoded signals. The generated control signals for the encoded control signals are represented in Equations (10) and (11).

$$neg_i = Y_{2i+1} \qquad (10)$$

$$ot_i = Y_{2i-1} \oplus Y_{2i} \qquad (11)$$

where $neg_i$ indicates the sign of the partial product and $ot_i$ indicates the multiplication factor that is created by Booth recoding. For simplicity of the correction circuitry, the correction signal is provided by Equation (12).

$$Cor_i = Y_{2i+1}.\overline{Zero_i} \qquad (12)$$

where $Cor_i$ is active only when the correction of the encoded partial product is needed. The encoder can be in two modes of operation. If the three multiplier bits are not all equal, then the $zero_i = 0$. With this condition, the encoder does normal booth recoding, and produces the encoded control signals needed for the generation of partial products. If all three multiplier bits are the same, then $zero_i = 1$. The encoder maintains the unused logic transitions disabled by using the gating mechanism, thus reducing switching activity and lowering both the static and dynamic power consumption. The signals generated by the ORBED encoder are then input to

the decoder to form the partial products. The multiplicand bit $x_j$, together with the encoded ss ($neg_i, ot_i, zero_i$)are fed to the decoder, which produces the Booth partial products. The decoder will output either +X, -X, +2X, -2X or 0X as per the operation encoded, depending on the other hardware components being used for decoding. Table 2 illustrates the partial product generation of the ORBED decoder.

**Table 2: Partial Product Generation of the ORBED Decoder**

| Case | $Zero_i$ | $ot_i$ | $cor_i$ | $PP_{ij}$ |
|---|---|---|---|---|
| 0X | 1 | d | 0 | 0 |
| $\pm 1X$ | 0 | 1 | $neg_i$ | $neg_i \oplus X_j$ |
| $\pm 2X$ | 0 | 0 | $neg_i$ | $neg_i \oplus X_{j-1}$ |

The partial products corresponding to $\pm X$and $\pm 2X$ are given in Equations (13) and (14).

$$PP_{\pm 1X} = neg_i \oplus x_j = nx_j \qquad (13)$$

$$PP_{\pm 2X} = neg_i \oplus x_{j-1} = nx_{j-1} \qquad (14)$$

The final partial product is provided in Equation (15).

$$PP_{ij} = Zero_i.0 + \overline{Zero_i}.(ot_i.nx_j + \overline{ot_i}.nx_{j-1}) \qquad (15)$$

Where $PP_{ij}$ represents the generated partial product for a booth. Similar to the encoder, the decoder also adopts a gating mechanism controlled by the $zero_i$ signal. In the 0X condition, the decoder directly sets the related partial product to zero and also disables the partial products that do not contribute to the sum. The decoder carries out the normal partial product generation for all other Booth patterns based on the encoded control signals. The ORBED minimizes the number of partial products generated before they are given to the compression stage. This reduction reduces the complexity of the subsequent approximate compressors and parallel adder, and thereby reduces hardware usage, power consumption and critical path delay.

### 3.3.2 Approximate Truncated Round Multiplier (ATRM)

The HARMONIC multiplier uses the Approximate Truncated-Round Multiplier (ATRM) for the LSBs of the multiplier and multiplicand. The lower-order bits of a multiplication contribute relatively less to the final multiplication result than the higher-order bits of the multiplication, and approximation can be used in this region with a relatively small reduction in computational accuracy. The ATRM not only decreases the complexity of hardware but also decreases the

switching activity, propagation delay, and power consumption for maintaining the multiplication accuracy needed for adaptive acoustic feedback suppression. The 8-bit least significant bits (LSBs) of the multiplier and multiplicand are first passed through an approximate fixed unit to provide simplified representations of the operands for low-complexity multiplication. The approximate values are then sent to the Digital Leading-One Detector (DLOD), which determines the position of the most significant active bit. The detected leading one position is used as a reference for the following truncation and alignment operation, which is to reduce the amount of unnecessary arithmetic computation.

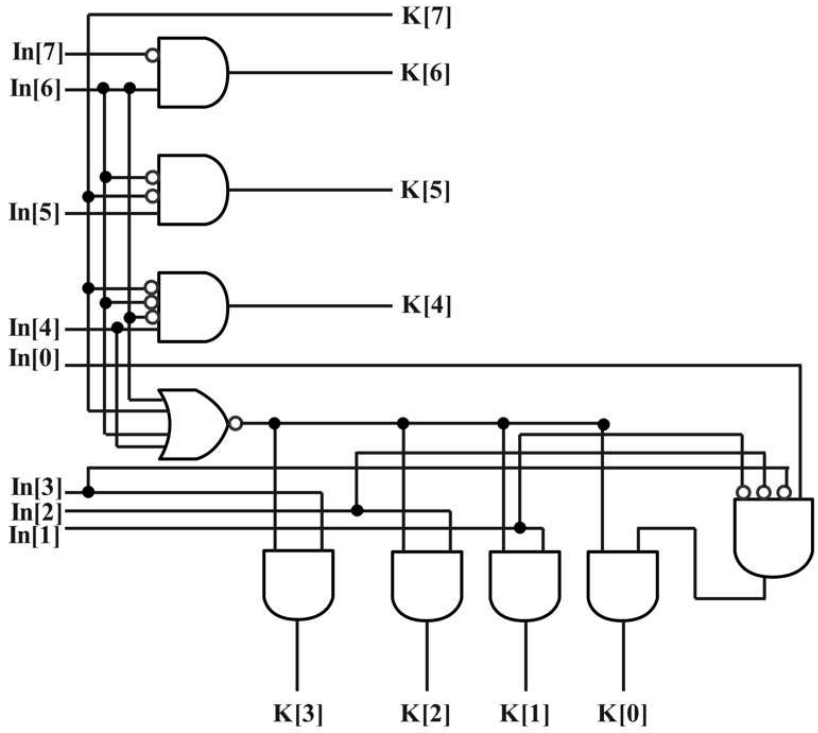



**Figure 7: Architecture of the DLOD**

The architecture of the Digital Leading-One Detector used in the ATRM is shown in Figure 7. The approximate 8-bit operand produced by the approximate fixed unit is fed into the detector. A combination of logic gates examines the input bits from the most significant position toward the least significant position and generates the output signals K [7] to K [0]. The output for the top logic '1' is activated, and the other outputs are not. This one-hot encoding output points to the position of the most significant bit, which the truncation unit subsequently uses to remove the insignificant lower-order bits and make the multiplication easier. The proposed detector simplifies the hardware complexity and switching activity in comparison with conventional leading one detection circuits, as only the location of the leading one is required. The Primary

Solitary Detector (PSD) function is the position of the leading one detected by the DLOD, as shown in Equation (16).

$$PSD = \left[\wedge_{n=g+1}^{z-2} \ \overline{|AB|(n)} \ \hat{} \ AB(g)\right] \qquad (16)$$

In this case, AB is used to represent the approximate absolute value of the operands, g is the bit position, and z is the word length of the operand. The specified leading-one position is the most significant bit (MSB) of the approximate operand, and also represents the reference point for the following truncation process. The output of the DLOD unit is then passed to the truncation unit that retains only the significant lower-order bits necessary for the multiplication operation and discards the insignificant bits. The truncation unit effectively reduces the switching activity, hardware cost and propagation delay of the multiplier without significantly compromising multiplication accuracy, since the computations performed on these low-significant bits are omitted. The truncation operation is given in Equation (17).

$$TU(g) = V_{g=0}^{z-2}\big(PSD(g) \wedge AB(g+n-k)\big), g < t \qquad (17)$$

Where TU(g) represents the truncated output for the bit position selected, and t represents the truncation threshold. The truncation unit outputs are then sent to the Arithmetic Unit Block (AUB), where approximation operations and the rounding operations are performed to compensate for the loss of lower-order bits. The AUB is embedded in the arithmetic process, which provides no need for extra circuits for approximation corrections, further simplifying the circuit and saving power consumption. The intermediate results from the AUB are then passed to the Shift Unit (SU), where the generated approximate partial products are shifted in the leading-one position determined by the DLOD. The approximate partial products are positioned correctly before they are added together in proper alignment. Finally, the outputs from the aligned outputs are fed into the Sign and Zero Detector Unit (SZDU). The SZDU resets the sign of the multiplication result when multiplication is performed on signed operations, and the output is a zero value when either operand is a zero value. The estimated partial products produced by the ATRM are then passed to the partial product generation stage of the HARMONIC multiplier for final accumulation.

### 3.3.3 Approximate 5:3 compressors

Approximate 5:3 compressors are integrated in the HARMONIC multiplier to efficiently suppress the partial products generated by the ORBED and ATRM modules. It uses the approximate 5:3 compressors to simplify the compression process and adopts the AND–OR

based grouping strategy, which is designed to minimize the logic depth, switching activity, hardware utilization and power dissipation while keeping the multiplication accuracy within a reasonable range. First, the five partial-product inputs obtained during the partial-product generation stage are provided in Equation (18).

$$Sum = \sum\{A_0\,A_1, A_0 + A_1, A_2A_3, A_2 + A_3, A_4\} \qquad (18)$$

where $K_0$, $K_1$, $K_2$, $K_3$, and $K_4$ represents the five-input partial-product bits, which are applied to the compressor. To make the hardware implementation easier, the partial-product terms generated are regrouped as shown in Equation (19) by using AND and OR.

$$Sum = \sum\{(A_0A_1)(A_2 + A_3), (A_2A_3)(A_0 + A_1)(A_0A) + (A_2 + A_3), (A_2A_3)(A_0 + A_1)\} \qquad (19)$$

The chances of the occurrence of several terms in Equation (19) are very small. So these terms can be neglected without causing a significant error in the multiplication process. The approximate compressor output is given in Equation (20).

$$Sum_{CAPP} = \sum\{A_0\,A_1 + A_2 + A_3, A_0 + A_1, A_2A_3 + A_4\} \qquad (20)$$

where $Sum_{CAPP}$ is the approximate compressed output produced by the compressor. Table 3 shows the approximate 5:3 compressor truth table.

**Table 3: Truth table of the Approximate 5:3 compressor**

| A4 | A3 | A2 | A1 | A0 | M3 | M2 | M1 | Sum | $Sum_{CApp}$ | $Err_i$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 2 | 2 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2 | 2 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 2 | 2 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3 | 2 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 2 | 2 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 2 | 2 | 0 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 3 | 2 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 2 | 2 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 3 | 3 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 3 | 3 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 | 3 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 2 | 2 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2 | 2 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 3 | 2 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 2 | 3 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 3 | 2 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 3 | 3 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 4 | 3 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 2 | 3 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 3 | 2 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 3 | 3 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 4 | 3 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 3 | 2 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 4 | 3 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 4 | 3 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 5 | 3 | 2 |

The outputs produced by the approximate 5:3 compressor are then combined into the partial-product reduction network of the HARMONIC multiplier. The partial products generated by the ORBED and ATRM modules are first created in the partial-product generation stage. The intermediate sum and carry signals are processed by a network of full adders, which combine these partial products while simultaneously compressing the intermediate sum and carry signals to the approximate 5:3 compressors. This initial reduction reduces the information that needs to be compressed in the partial-product bits and makes it easier to accumulate later. The approximate 5:3 compressors then further compress the reduced partial products by using multiple bits from the input to produce fewer bits from the output, and with a much smaller number of components. The compressed outputs from the two compressor blocks are fed into a 4-bit parallel adder, which accumulates the reduced partial products to give the approximate partial product for the HARMONIC multiplier.

## 4 RESULT AND DISCUSSION

In this section, the performance of the proposed HARMONIC-AFS method is evaluated through performance analysis and comparative analysis. The proposed method is tested using the NOIZEUS speech data set in various noisy conditions and verified in real-time FPGA hardware implementation. The proposed technique is applied to the Xilinx XC7K325T FPGA development board using Xilinx Vivado Design Suite. Moreover, the performance of the proposed method is evaluated based on the speech enhancement metrics and the hardware performance parameters, and compared with the existing methods to prove the efficiency of the proposed method.

### 4.1 Dataset description

The proposed method was tested with the NOIZEUS speech dataset, which is one of the existing benchmark databases for speech enhancement and noise suppression research. The database is composed of 30 phonetically balanced IEEE sentences produced by six speakers (three females and three males). The speech recordings are analyzed with 16-bit resolution at 8kHz sampling rate and contain several real-world noise conditions. The variety of speakers, noise types and SNR levels allows a reliable benchmark for the effectiveness of the proposed method for realistic acoustic environments.

### 4.2 Hardware Implementation

The experimental setup of hardware implementation for the proposed method using the Xilinx Kintex-7 FPGA development board is shown in Figure 8. The input speech signal from the NOIZEUS speech dataset is initially fed to the host computer and then processed in the Xilinx Vivado environment. The speech samples are then uploaded to the FPGA board via the USB programming interface, and the HARMONIC-AFS architecture performs the acoustic feedback suppression. The improved speech waveform is created and displayed in the Vivado processing window on the host machine. Finally, the processed speech is played back by the audio speaker with the attached mechanism, effectively demonstrating the feasibility of the proposed method in real-time hardware systems.

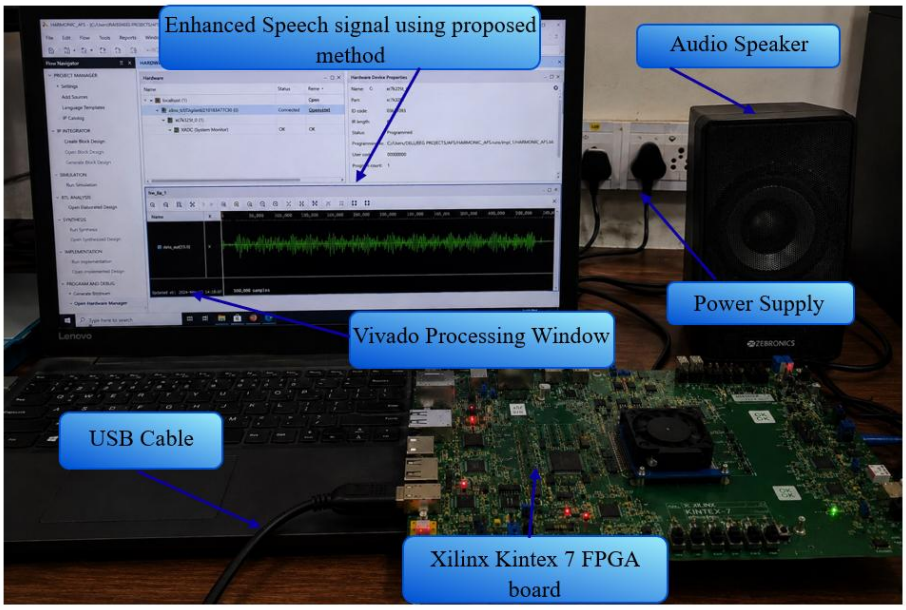



**Figure 8: Experimental hardware implementation setup of the proposed method**

### 4.3 Performance metrics

**Area:** Area is the number of FPGA hardware resources needed for hardware implementation. Look-Up Tables (LUTs) are simple components in FPGAs that represent combinational logic where output values are pre-computed for various inputs. The number of LUTs required determines the complexity of the hardware and affects resource usage and system performance.

**Power:** Power is the average energy expended during the operation of a circuit. The dynamic power, caused by the switching of the transistors, and the static power, caused by leakage currents, are both significant and should be taken into account when considering power consumption and heat dissipation of digital systems.

**Delay:** Delay is the time interval between the change of the input signal and the time at which the change is happen at the output of the circuit. It indicates the switching time of logic gates and the propagation delay of the interconnection, which is a measure of the overall operating speed of the circuit.

**PESQ:** The Perceptual Evaluation of Speech Quality (PESQ) is an objective measure for assessing perceived speech quality of processed speech. A higher PESQ value indicates greater speech quality and intelligibility.

**SNR:** The Signal-to-Noise Ratio (SNR) is an objective measure of the ratio of the speech signal to noise in the environment.

**MSE:** The Mean Square Error (MSE) is the average squared difference between the improved speech signal and the reference speech signal.

$$MSE = \frac{1}{N}\sum_{n=1}^{N}[x(n) - \hat{x}\,(n)]^2 \qquad (21)$$

Where N denotes the total number of speech samples, x(n) is the clean speech signal, and $\hat{x}(n)$ is the improved speech signal.

### 4.4 Performance analysis

In this section, the performance of the proposed method is evaluated with respect to time domain waveform, power spectrum, magnitude responses, and quantitative speech enhancement metrics in various SNR conditions. The results obtained are analyzed using PESQ, SNR improvement and MSE to show the effectiveness of the proposed method in acoustic feedback suppression and speech quality improvement.

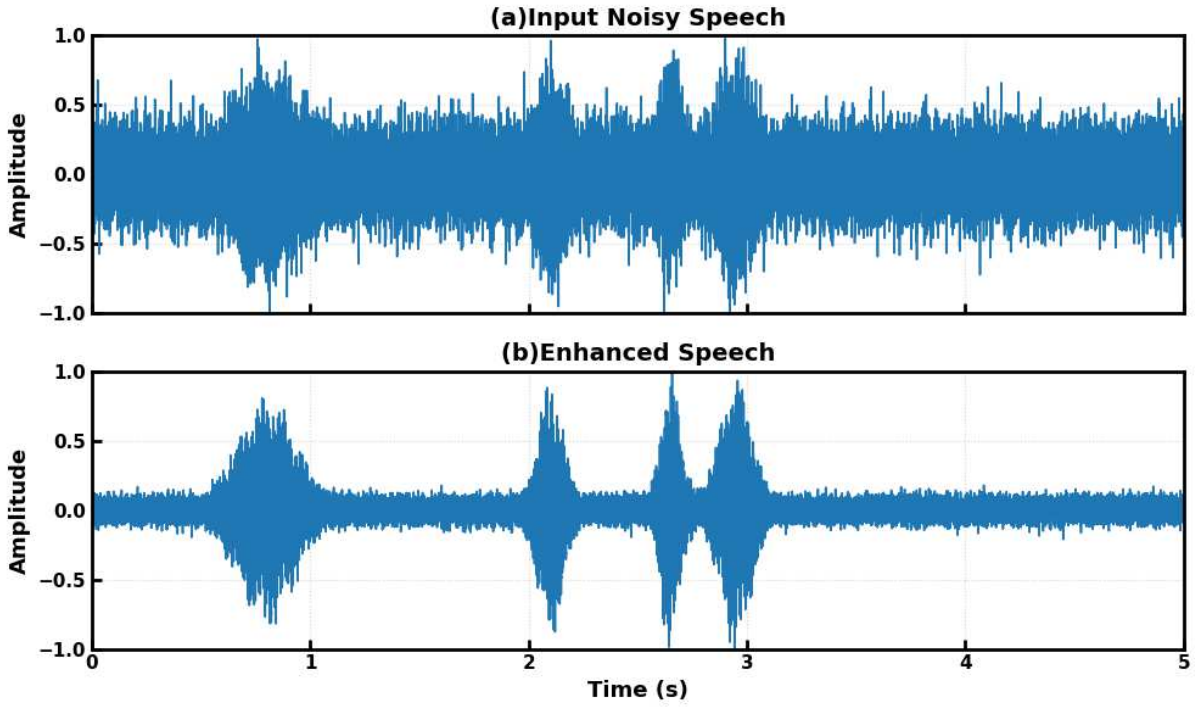



**Figure 8: Time domain waveform comparison of (a) input noisy speech signal and (b) enhanced speech signal obtained using the proposed method**

The time domain waveforms of the input speech signal used and the enhanced speech signal by the proposed method are presented in Figure 8. The amplitude of the input speech is not regular throughout the speech, and heavily dominated by the background noise and acoustical feedback components, as shown in the Figure 8(a). Figure 8(b) illustrates that the proposed

method is able to successfully remove the unwanted noise while retaining the dominant speech components. The improved waveform exhibits a clearer temporal structure and reduced background noise, highlighting the effectiveness of the proposed technique in enhancing speech quality.

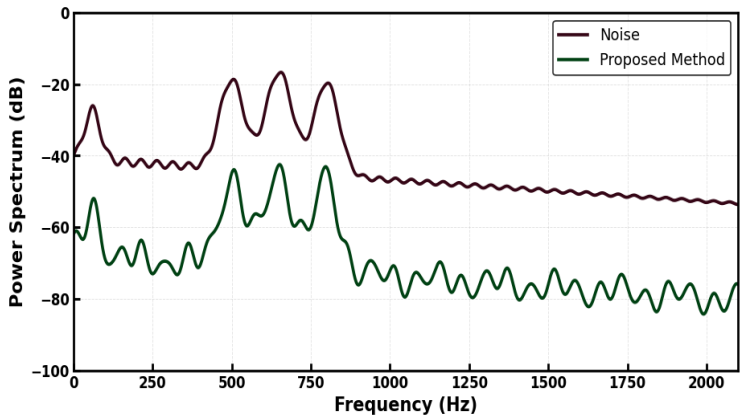



**Figure 9: Power spectrum comparison of the noisy input signal and the output of the proposed method**

Figure 9 shows the power spectrum of the noisy input signal and the speech signal processed by the proposed method. The spectrogram of the enhanced output shows a significant decrease in the power spectral density of the acoustic feedback elements in the operating frequency band, while the spectral characteristics of the desired speech signal remain the same. These observations validate the proposed technique for acoustic feedback suppression and enhancement of the speech signal spectral quality with minimal distortion caused by processing the signal.

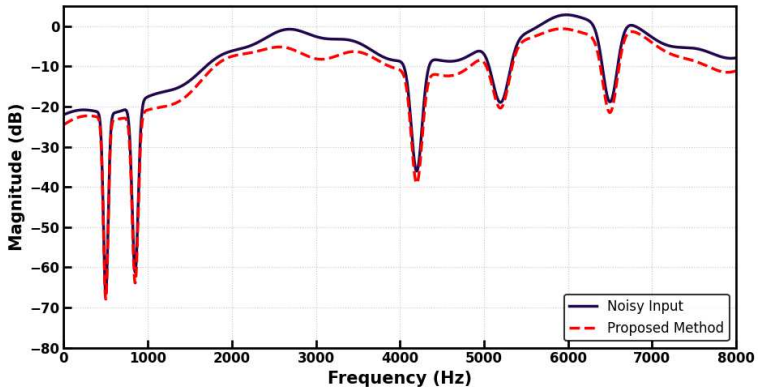



**Figure 10: Magnitude response comparison of the noisy input signal and the signal processed using the proposed method**

The magnitude response comparison between the noisy input signal and the signal processed using the proposed method over the operating frequency range is shown in Figure 10. The processed output has a wider and more stable frequency band with less magnitude change than the input signal, which is noisy. The observed results demonstrate the effectiveness of the proposed method to suppress the unwanted frequency components caused by acoustic feedback, while preserving the important frequency components of the desired speech signal. The better magnitude response further verifies the proposed method to achieve stable adaptive feedback suppression and improved signal quality.

**Table 4: Performance evaluation of the proposed method under different input SNR levels**

| Input SNR (dB) | PESQ | SNR Improvement (dB) | MSE |
|---|---|---|---|
| 0 | 2.41 | 10.8 | 0.021 |
| 5 | 2.76 | 14.2 | 0.016 |
| 10 | 3.14 | 17.6 | 0.011 |
| 15 | 3.46 | 20.3 | 0.008 |

Table 4 shows the performance evaluation of the proposed method at various input SNR levels. An increase in the input SNR from 0 dB to 15 dB results in a corresponding increase in PESQ score from 2.41 to 3.46, which shows an improvement in the perceptual speech quality. The SNR is improved from 10.9 dB to 20.3 dB, which shows that the acoustic feedback and background noises are suppressed more effectively. The MSE value decreases from 0.021 to 0.008, which shows that the reconstructed speech signal is increasingly closer to the reference speech. The results show that the proposed method is effective for different input SNR conditions.

### 4.5 Comparative analysis

This section compares the proposed method with the existing designs in terms of speech enhancement performance, hardware efficiency, timing characteristics, error metrics, and FPGA implementation. To demonstrate the effectiveness of the proposed method, the comparative analysis is performed based on PESQ, SNR improvement, MSE, area, power consumption, propagation delay, operating frequency, and hardware resource utilization.

**Table 5: Comparative Speech Enhancement Performance of the Proposed Method with Existing Techniques**

| Techniques | PESQ | SNR Improvement (dB) | MSE |
|---|---|---|---|
| ScaleTRIM | 3.08 | 16.8 | 0.015 |
| DA-AFIR-leadx-hybam-AC | 2.15 | 18.65 | 0.021 |
| DAAFA | 2.47 | 15.72 | 0.011 |
| ARCWM | 2.01 | 17.21 | 0.019 |
| **Proposed** | **3.46** | **20.5** | **0.008** |

Table 5 shows the speech enhancement performance of the proposed HARMONIC-AFS method with the existing methods. The proposed method obtains the maximum PESQ score of 3.46, which is a superior perceptual speech quality. It also delivers an SNR gain of 20.50 dB and the lowest MSE of 0.008, which shows that the improved speech signal is very close to the clean reference signal with minimum distortion. The results show that the proposed method has better performance of speech enhancement than the existing methods.

**Table 6: Hardware performance comparison of the proposed designs with the existing designs**

| Author | Technique | Area (LUT) | Power (mW) | Delay (ns) |
|---|---|---|---|---|
| Farahmand, E et al., [17] | ScaleTRIM | 3265 | 189.71 | 75.41 |
| Immareddy, S et al., [19] | DA-AFIR-leadx-hybam-AC | 7890 | 209.97 | 89.36 |
| James, B.P et al., [20] | DAAFA | 2298 | 155.74 | 98.32 |
| Rizos, I et al., [25] | ARCWM | 3211 | 179.36 | 67.36 |
| **Proposed** | **HARMONIC-AFS** | **1220** | **119.8** | **43.05** |

Table 6 shows the hardware performance comparison of the proposed HARMONIC-AFS method with existing methods in terms of area, power consumption and delay. The proposed method achieves the lowest area of 1220 LUT and 119.8 mW of power consumption. Moreover, the proposed design achieves a lowest delay of 43.05 ns when compared with the existing

designs. The proposed method achieves a power consumption of 36.85%,42.94%,23.07% and 33.21% when compared to existing designs such as ScaleTRIM [17], DA-AFIR-leadx-hybam-AC [19], DAAFA [20] and ARCWM [25], respectively. The results demonstrate that the proposed method is effective in reducing the area, power consumption, and processing delay, thereby improving the hardware efficiency and making it well-suited to wearable hearing-aid applications in real time.

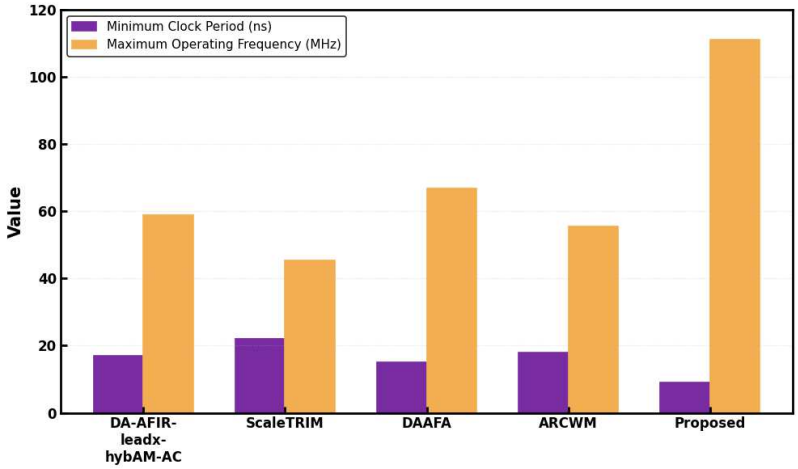



**Figure 11: Comparison of the minimum clock period and maximum operating frequency between the proposed design and existing designs**

The performance of the proposed architecture is compared with the existing architectures in terms of minimum clock period and maximum operating frequency, as shown in Figure 11. Among the compared methods, the proposed HARMONIC-AFS architecture has the smallest minimum clock period of 9 ns and the highest operating frequency of 111.1 MHz. The results showed the better timing performance of the proposed design, and it is suitable for an efficient real-time hardware implementation.

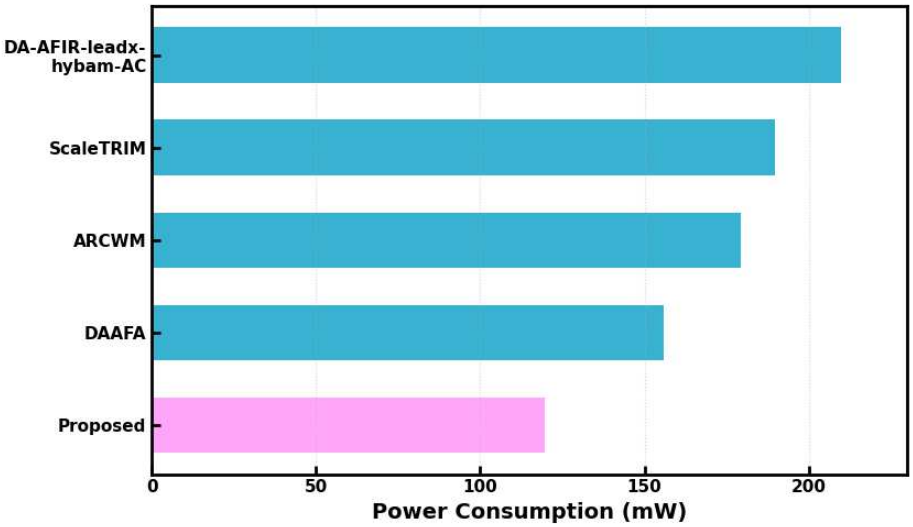



**Figure 12: Quantitative comparison of the power consumption of the proposed method Vs existing designs**

Figure 12 shows the quantitative comparison of the power consumption of the proposed method with the existing designs. The proposed HARMONIC-AFS method provides reduced power consumption compared to the existing designs, thus allowing an energy-efficient hardware implementation. The optimised hardware architecture and adaptive feedback suppression strategy are considered to be the main causes of the decrease in power consumption.

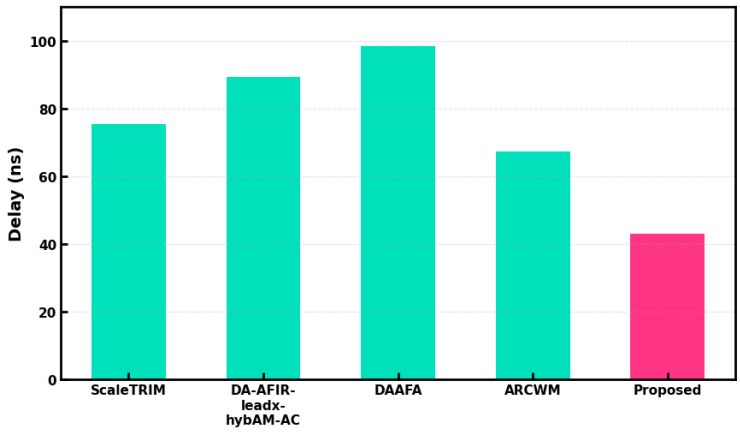



**Figure 13: Quantitative comparison of the propagation delay of the proposed method with existing methods**

The quantitative comparison of the propagation delay of the proposed method and existing methods is shown in Figure 13. The proposed method is observed to give the minimum propagation delay among the compared methods, which is a good indication of high processing speed and good hardware operation. The lower propagation delay proves the appropriateness

of the design for a real-time adaptive feedback suppression for the wearable hearing-aid application.

**Table 7: Comparative error analysis of the proposed method with the existing designs**

| Techniques | ER (%) | ED | MED | NMED ($\mathbf{x10^{-3}}$) | MRED ($\mathbf{x10^{-3}}$) |
|---|---|---|---|---|---|
| DA-AFIR-leadx-hybAM-AC | 3.20 | 13 | 0.024 | 0.187 | 0.237 |
| DAAFA | 2.86 | 10 | 0.020 | 0.139 | 0.197 |
| ARCWM | 3.89 | 15 | 0.018 | 0.175 | 0.176 |
| HPR-Mul | 2.49 | 8 | 0.015 | 0.143 | 0.221 |
| **Proposed** | **1.68** | **5** | **0.011** | **0.103** | **0.125** |

Table 7 compares the proposed design with the existing designs in terms of error measures such as Error Rate (ER), Error Distance (ED), Mean Relative Error Distance (MRED), Mean Error Distance (MED), and Normalized Mean Error Distance (NMED).The proposed method achieves the lowest ER of 1.68%, ED of 5, MED of 0.011, NMED of $0.103 \times 10^{-3}$, and MRED of $0.125 \times 10^{-3}$ among the compared techniques. The comparison of the reduced error metrics shows that the proposed method ensures high computational accuracy with an efficient operation of the hardware.

**Table 8: Hardware Implementation comparison of the proposed method with the existing method**

| Parameters | ScaleTRIM | DA-AFIR-leadx-HybAM-AC[] | DAAFA | ARCWM | Proposed |
|---|---|---|---|---|---|
| FPGA Chip | Xilinx Kintex 7 | Xilinx Kintex 7 | Xilinx Kintex 7 | Xilinx Kintex 7 | Xilinx Kintex 7 |
| Device | XC7K325T | XC7K325T | XC7K325T | XC7K325T | XC7K325T |
| Number of slices LUTs | 3265 | 7432 | 2298 | 3124 | 1220 |

| Number of slice registers | 19 | 15 | 17 | 12 | 9 |
|---|---|---|---|---|---|
| Maximum operating Frequency (MHz) | 105.32 | 71.4 | 95.4 | 87.2 | 111.10 |

The comparison of the actual hardware implementation of the proposed designs with the existing designs is shown in Table 8. All the techniques were re-implemented on the Xilinx Kintex 7 XC7K325T FPGA Platform for fair comparison. The proposed design consumes only 1220 slice LUTs, while ScaleTRIM, DA-AFIR-leadx-hybAM-AC, DAAFA and ARCWM use 3265, 7432, 2298, and 3124 LUTs, respectively. In the same manner, the proposed architecture requires only 9 slice registers, whereas the existing ones require 19, 15, 17 and 12 slice registers, which shows better utilization of hardware resources. In addition, the proposed method has the highest maximum operating frequency of 111.10 MHz, which is better than ScaleTRIM (105.32 MHz), DAAFA (95.40 MHz), ARCWM (87.20 MHz), and DA-AFIR-leadx-hybAM-AC (71.40 MHz). The results show that the proposed method offers an efficient trade-off between the reduction in hardware resource consumption and the increase in operating frequency which is suitable for real-time wearable hearing-aid applications.

## 5 CONCLUSIONS

In this research, a novel HARMONIC-AFS (Hybrid Approximate Radix-8 Multiplier-Based Adaptive Feedback Suppression) is proposed for low-power and high-quality speech enhancement in wearable hearing-aid applications. The proposed method combines an Approximate SAR-ADC to digitize the speech signal and a Parks-McClellan optimised AFS filter to eliminate acoustic feedback. The HARMONIC multiplier is proposed, which integrates ORBED, ATRM and approximate 5:3 compressors to minimize the hardware complexity in the AFS unit while maintaining high speech enhancement quality. Experimental results are simulated and implemented on the Kintex 7 XC7K325T FPGA Platform and evaluated using the NOIZEUS speech dataset. The experimental results validate the effectiveness of the proposed method in achieving a high PESQ score of 3.46, an SNR gain of 20.5 dB, and a minimum MSE of 0.008, while suppressing acoustic feedback effectively and achieving high speech quality. The proposed design needs only 1220 LUTs, 119.8 mW of power, a propagation delay of 43.05 ns and a maximum frequency of 111.1 MHz, which shows the best hardware efficiency than the existing techniques. To achieve high computational accuracy, the proposed

method was analyzed with existing designs and achieved the lowest ER of 1.68%, NMED of $0.103 \times 10^{-3}$, and MRED of $0.125 \times 10^{-3}$. The proposed method achieves a power consumption of 36.85%,42.94%,23.07% and 33.21% when compared to existing designs such as ScaleTRIM, DA-AFIR-leadx-hybam-AC, DAAFA and ARCWM, respectively. For future research, the proposed method will be extended to multi-channel speech enhancement for robust acoustic feedback suppression in complex real-world acoustic environments. Moreover, the proposed approach will be realized in an ASIC with advanced CMOS technology to further minimize area, power consumption and latency of the next generation of low-power wearable hearing-aid systems.

**References**


1. Matharine, L. and Noria, F., 2025. Smart wearable devices for speech and hearing support: Integrating AI, signal processing, and human-centred design. *Journal of Intelligent Assistive Communication Technologies*, pp.25-32.
2. Anwar, U., Arslan, T., Hussain, A. and Lomax, P., 2022. Next generation cognition-aware hearing aid devices with microwave sensors: Opportunities and challenges. *IEEE Access*, *10*, pp.82214-82235.
3. Ne, C.K.H., Muzaffar, J., Amlani, A. and Bance, M., 2021. Hearables, in-ear sensing devices for bio-signal acquisition: a narrative review. *Expert Review of Medical Devices*, *18*(sup1), pp.95-128.
4. Han, U.G., Lee, J.Y., Kim, G.Y., Jo, M., Lee, J., Bang, K.H., Cho, Y.S., Hong, S.H. and Moon, I.J., 2022. Real-world effectiveness of wearable augmented reality device for patients with hearing loss: prospective study. *JMIR mHealth and uHealth*, *10*(3), p.e33476.
5. Pavlidou, A. and Lo, B., 2021, July. Artificial ear-a wearable device for the hearing impaired. In *2021 IEEE 17th International Conference on Wearable and Implantable Body Sensor Networks (BSN)* (pp. 1-4). IEEE.
6. Eren, Y., Güvenç, B.Ç. and Mengüç, E.C., 2024. Cost-effective acoustic feedback cancellers for digital hearing aids. *IEEE/ACM Transactions on Audio, Speech, and Language Processing*, *32*, pp.2367-2377.
7. Yin, Y. and Chen, F., 2023. Acoustic feedback cancellation algorithm for hearing aids based on a weighted error adaptive filter. *Electronics*, *12*(7), p.1528.

8. Eren, Y., Güvenç, B.Ç. and Mengüç, E.C., 2024. Cost-effective acoustic feedback cancellers for digital hearing aids. *IEEE/ACM Transactions on Audio, Speech, and Language Processing*, *32*, pp.2367-2377.
9. Park, J., Kwak, J.Y., Trueb, J., Kim, J.U., Jo, Y.J., Cho, S., Kang, S., Li, S., Yang, X., Huang, Y. and Johnson, A.M., 2026. Wearable system for feedback-enhanced control over vocal intensity across a range of ambient noise levels. *Device*.
10. Sokolova, A., Rallapalli, V., Yellamsetty, A., Hunt, M., Aksanli, B., Harris, F. and Garudadri, H., 2023, October. Validation of frequency warping (freping) as a new tool for feedback control in hearing aids. In *2023 57th Asilomar conference on signals, systems, and computers* (pp. 1410-1414). IEEE.
11. Homana, I., Muresan, I., Topa, M. and Contan, C., 2011. FPGA implementation of LMS and NLMS adaptive filters for acoustic echo cancellation. *Acta Technica Napocensis*, *52*(4), p.13.
12. Karakaya, E. and Aytar, O., 2026. FPGA Implementation of NLMS and VSLMS Algorithms for Underwater Acoustics Applications. IEEE Access, 14, pp.53860-53872.
13. Rodrigo, W.S.C., Buddhika, R.P., Nirmal, W.C., Ranasinghe, A.C. and Mallawathanthri, S.L., 2025, December. Stored-Reference LMS Filtering on FPGA for Low-Latency Acoustic Feedback Cancellation in Live Audio Systems. In *2025 International Conference on Advances in Technology and Computing (ICATC)* (pp. 1-6). IEEE.
14. Nagar, M.S., Mathuriya, A., Patel, S.H. and Engineer, P.J., 2024. High-speed energy-efficient fixed-point signed multipliers for FPGA-based DSP applications. *IEEE Embedded Systems Letters*, *16*(4), pp.417-420.
15. Chikyal, N., Bhar, C., Kar, A. and Christensen, M.G., 2025. Sparsity Apprised Logarithmic Hyperbolic Tan Adaptive Filters for Nonlinear System Identification and Acoustic Feedback Cancellation. *IEEE Open Journal of Signal Processing*.
16. Tadigadapa, P. and Jagadamba, P., 2025. Design of Power-Efficient Approximate Multiplier. *Procedia Computer Science*, *260*, pp.784-795.
17. Farahmand, E., Askarizadeh, M.J., Mahani, A., Ghavami, B., Ghasemzadeh, H., Hanif, M.A. and Shafique, M., 2026. scaletrim: Scalable truncation-based integer approximate multiplier with linearization and compensation. *IEEE Access*, *14*, pp.51108-51125.
18. Vafaei, J. and Akbari, O., 2024. Hpr-mul: An area and energy-efficient high-precision redundancy multiplier by approximate computing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *32*(11), pp.2012-2022.

19. Immareddy, S., Sundaramoorthy, A. and Alagarsamy, A., 2023. Adaptive FIR filter design with approximate adder and hybridized multiplier for efficient noise eradication in sensor nodes. *ECS Journal of Solid State Science and Technology*, *12*(9), p.097002.
20. James, B.P., Leung, M.F., Vaithiyanathan, D. and Mariammal, K., 2024. Optimal realization of distributed arithmetic-based MAC adaptive FIR filter architecture incorporating radix-4 and radix-8 computation. *Electronics*, *13*(17), p.3551.
21. Madhushankara, M., Mathew, R., Muralikrishna, H., Shenoy, S., Darshan, B.S. and Rao, R.L., 2025. Speech Enhancement for Electrolarynx Devices Using M-RLS: Intelligibility Improvement and Low-Power Hardware Feasibility. *IEEE Access*.
22. Sadeghi, A., Rasheedi, R., Partin-Vaisband, I. and Pal, D., 2024. Energy efficient compact approximate multiplier for error-resilient applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *71*(12), pp.4989-4993.
23. Thannoon, H. and Hashim, I., 2024. FPGA implementation of efficient adaptive filter incorporating systolic architecture. *Engineering and Technology Journal*, *42*(2), pp.261-275.
24. Perri, S., Spagnolo, F., Frustaci, F. and Corsonello, P., 2022. Designing energy-efficient approximate multipliers. *Journal of Low Power Electronics and Applications*, *12*(4), p.49.
25. Rizos, I., Papatheodorou, G. and Efthymiou, A., 2025. Designing approximate reduced complexity Wallace multipliers. *Electronics*, *14*(2), p.333.