

# Mitigation of Common Mode Voltage in Multilevel Inverters for Linear and Non-linear Resistive Loads

Ankesh S

MAMATHA N

Visvesvaraya Technological University

MANJULA B K

JEYKISHAN KUMAR

VENUGOPAL B T

[venugopalbt.rvitm@rvtm.edu.in](mailto:venugopalbt.rvitm@rvtm.edu.in)

Visvesvaraya Technological University

---

## Research Article

**Keywords:** Common mode voltage, leakage current, multilevel inverter, Silicon carbide (SiC), Linear-Non Linear Loads

**Posted Date:** October 15th, 2026

**DOI:** <https://doi.org/10.21203/rs.3.rs-10458146/v1>

**License:**   This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

**Additional Declarations:** No competing interests reported.

---

# Mitigation of Common Mode Voltage in Multilevel Inverters for Linear and Non-linear Resistive Loads

Ankesh S<sup>1\*</sup>, Mamatha N<sup>2</sup>, Manjula B K<sup>3</sup>, Jeykishan Kumar K<sup>4</sup> and  
Venugopal B T<sup>5</sup>

<sup>1,3,4</sup>CPRI, Bengaluru, <sup>2</sup>PESCE,  
Mandya, <sup>5</sup>RVITM, Bengaluru  
venugopalbt.rvitm@rvei.edu.in

**Abstract.** Multilevel inverters (MLIs) are popular due to their ability to provide voltage quality and reduce harmonics. However, common mode voltage (CMV) can undermine these advantages by affecting systems and electromagnetic compatibility. CMV can lead to electrical noise, Electromagnetic Interference (EMI), and potential damage to connected devices. To address this issue, a novel circuit is proposed in this paper aimed at effectively mitigating CMV in multilevel inverters when driving both linear and non-linear resistive loads. The modified circuit is designed to minimize CMV with experimental validation, and the results are graphically presented. The study encompasses a comprehensive analysis of CMV reduction and the effectiveness of the circuit modification in achieving significantly reduced CMV, contributing to improved system performance and reliability. The experimentation offers valuable insights in the field of power electronics, providing a practical solution for CMV reduction in multilevel inverter applications.

**Keywords:** Common mode voltage, leakage current, multilevel inverter, Silicon carbide (SiC), Linear-Non Linear Loads.

## 1 Introduction

An inverter is an essential electronic device used to convert direct current (DC) electricity into alternating current (AC). It plays a crucial role in various applications, from powering household appliances to driving industrial machinery and enabling renewable energy integration [1]. Inverters are particularly vital in contexts where the available power source, such as batteries or solar panels, generates DC electricity. To make this energy usable for most appliances and equipment that run on AC power, the inverter employs a series of electronic components and control algorithms.

The basic principle of an inverter involves converting the fixed voltage and polarity of DC power into a variable voltage and alternating polarity, resembling the sinusoidal waveform of standard AC power. This transformation enables the smooth operation of devices like refrigerators, computers, and air conditioners that require AC power. The basic block diagram of an Inverter is given in the Fig.1.

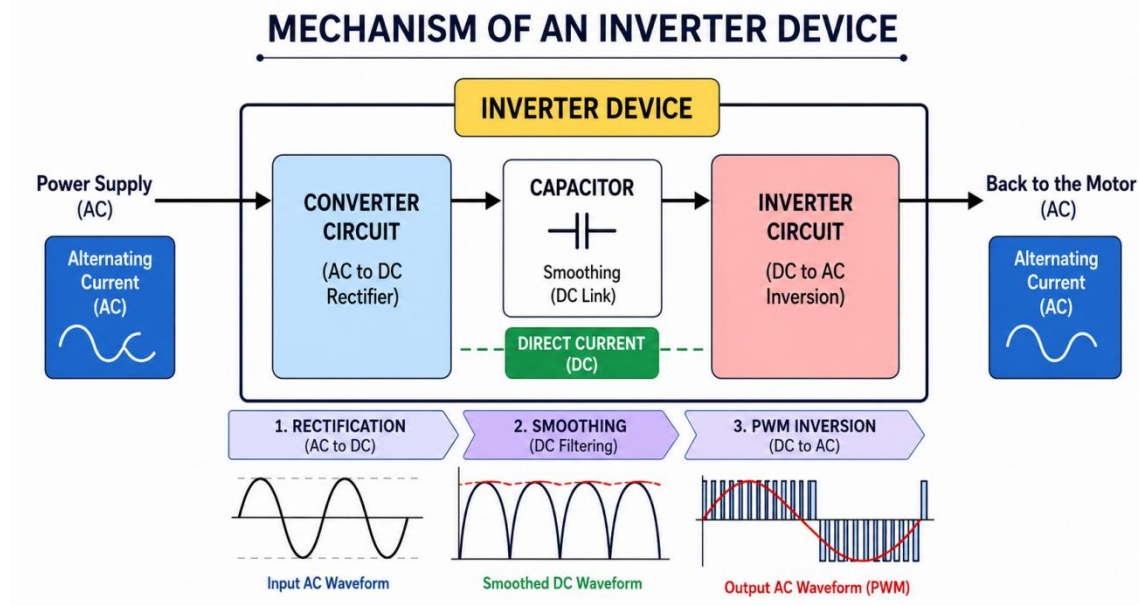


**Fig 1.** Basic functional block diagram of an inverter

Inverters come in various types, such as single-phase and three-phase inverters for residential and commercial applications, as well as specialized designs for specific uses like motor drives and grid-tied solar systems. They are characterized by their efficiency, output waveform quality, and features like voltage regulation, frequency control, and protection mechanisms. The proliferation of renewable energy sources, such as solar and wind power, has elevated the importance of inverters in modern energy systems, facilitating the integration of clean energy into conventional power grids [2] and enhancing overall energy efficiency.

A MLI is a specialized power electronic device designed to generate high-quality AC waveforms with multiple voltage levels, offering advantages over traditional two-level inverters. MLIs are extensively used in various applications, including industrial motor drives, renewable energy systems, and high-voltage direct current (HVDC) transmission. Unlike conventional two-level inverters, which produce output waveforms with a limited number of voltage levels (typically  $+V_{dc}$  and  $-V_{dc}$ ), MLIs provide more voltage levels by employing a series of power semiconductor switches and capacitors.

This arrangement allows the MLI to synthesize complex output voltage waveforms that closely resemble sinusoidal AC waveforms, thereby reducing harmonic distortion and improving power quality. MLIs offer benefits such as lower Total Harmonic Distortion (THD), reduced voltage stress on components, and improved efficiency compared to their two-level counterparts. They are particularly well-suited for high-power applications, where the use of higher voltage levels can lead to lower current and reduced losses [3]. There are various topologies of multi-level inverters, including the diode-clamped (neutral-point clamped) inverter, the flying capacitor inverter, and the cascaded H-bridge inverter. Each topology has its own advantages and limitations, and the choice depends on factors such as desired output quality, voltage levels, and cost considerations.

The primary distinction between two level and multilevel inverters lies in the number of voltage levels they generate. Two-level inverters produce two different voltage levels, while multilevel inverters produce multiple voltage levels. Two-level

inverters are used in low-voltage applications and are simple and cost-effective, while multilevel. This is crucial for sensitive electronic devices, industrial equipment, and utility grids, as it prevents potential damage and operational inefficiencies caused by distorted voltage waveforms. MLIs allow for higher-voltage operation without requiring extremely high-voltage switching components. Leading to increased energy efficiency and better system reliability. MLIs are well suited for renewable energy systems like solar and wind power. These systems generate DC power that needs to be converted to AC for grid integration. MLIs can efficiently manage and convert this DC power while ensuring minimal harmonic distortion, facilitating the seamless integration of clean energy into the electrical grid. MLIs play a crucial role in high-voltage direct current (HVDC) transmission, where the need for efficient power conversion, voltage regulation, and harmonic reduction is paramount.

MLIs have emerged as essential components in modern power conversion systems due to their ability to address several critical challenges associated with conventional two-level inverters. One of the primary reasons for the need for multi-level inverters is the improvement in output waveform quality. Conventional inverters produce output waveforms with a limited number of voltage levels, leading to higher levels of harmonic distortion. MLIs, on the other hand, offer the capability to synthesize output waveforms with multiple voltage levels, resulting in reduced harmonic content and improved power quality. This is crucial for applications sensitive to voltage distortion, such as motor drives, where smooth voltage waveforms lead to reduced motor heating and noise [4]. Another significant advantage is their ability to operate at higher voltage levels without requiring excessively high-voltage-rated components. By distributing the voltage across multiple levels, MLIs can achieve the desired output voltage without subjecting individual components to extremely high stress. This characteristic is particularly beneficial in high-power applications, where lower current [5] and reduced losses contribute to enhanced overall efficiency.

## 2 Common Mode Voltage in Multilevel Inverter

Common mode voltage in an inverter refers to an undesired voltage level that appears between the output terminal and the ground reference. It occurs when both the high and low sides of the inverter's output switches experience simultaneous voltage fluctuations relative to the ground [6]. Common-mode voltage can lead to electromagnetic interference, equipment malfunctions, and safety hazards. Minimizing or eliminating common mode voltage is essential to ensuring proper operation, reliability, and compliance with electromagnetic compatibility standards in various applications, including motor drives, power electronics, and renewable energy systems.

Motor bearing currents are enhanced as a result of the high-frequency common-mode (CM) voltage produced by converters, which is a major factor in the deterioration and failure of bearings [7]. Due to the repetitive switching of bearing currents, the high frequency bearing currents raise the temperature of the oil film (lubrication) of the bearing [8]. The metal may melt at such a high temperature, resulting in damage like small pits, a rough surface, and grooves. Fig.2 illustrates some bearing degradation from electric corrosion brought on by bearing currents. In addition to bearing failure, these mechanical defects cause motor shaft vibrations and noise, which shorten the motors' useful lives.

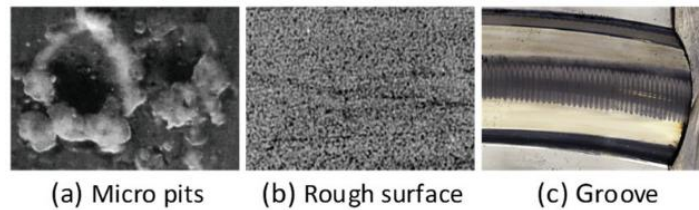


Fig 2. Various types of bearing damages caused by bearing currents

The common mode voltage in an inverter arises due to the asymmetrical switching of its power semiconductor devices. In an inverter, the power switches, such as insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs), alternate between on and off states to generate the desired output voltage waveform. However, due to manufacturing tolerances, parasitic components, and differences in switching speeds, the switching transitions are not perfectly synchronized. Silicon carbide (SiC) [9] switches are increasingly favored in inverters due to their superior characteristics. SiC devices [10], such as SiC MOSFETs or SiC Schottky diodes, offer lower conduction losses and faster switching speeds compared to traditional silicon-based components. This leads to higher inverter efficiency, reduced heat generation, and enhanced power density. SiC[10] switches can operate at higher temperatures, allowing for compact and robust designs. Moreover, their reduced switching losses result in less energy waste, making them ideal for renewable energy applications like solar and wind inverters.

This simultaneous fluctuation creates a voltage potential between the output and the ground reference, leading to the common mode voltage. Common mode voltage can induce electromagnetic interference, impact nearby electronic systems and causing unintended signal distortions or malfunctions [11]. It can also stress insulation materials and compromise the safety of the system, potentially leading to an insulation breakdown or electrical shocks. Therefore, managing and reducing common mode voltage is crucial to ensure reliable operation, mitigate electromagnetic interference, and maintain the safety and performance of inverter-based systems [12].

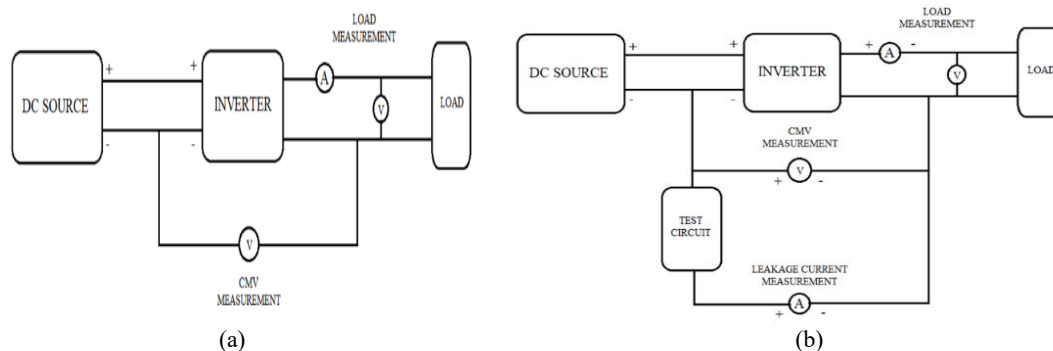
The necessity of reducing common mode voltage (CMV) in an inverter is rooted in its profound impact on the performance, longevity, and safety of electrical systems across various domains. Elevated breakdowns and CMV can lead to premature degradation and failure of equipment. In motors and drives, high CMV stresses insulation materials, potentially causing breakdowns and leading to costly downtime and repairs [13]. CMV-induced bearing currents in motors can also result in mechanical wear, reducing their operational lifespan. CMV is a significant source of electromagnetic interference (EMI). CMV reduction enhances system efficiency. Excessive CMV results in additional power losses, reducing the overall efficiency of the inverter and connected systems. By mitigating CMV-related losses, energy consumption is optimized, leading to cost savings and reduced environmental impact.

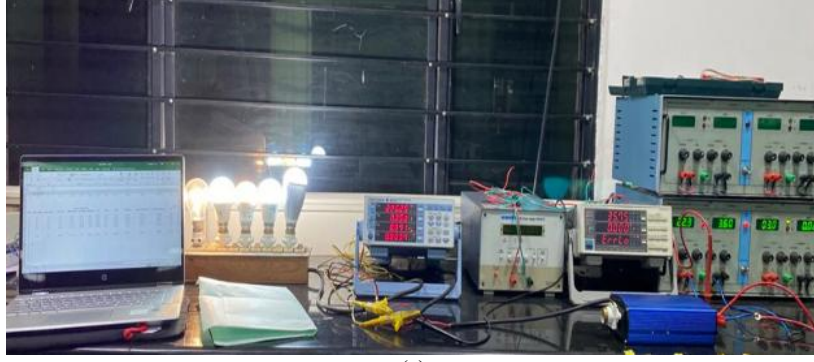
Types of common mode voltage reduction technique

- Differential Signaling:** One of the most effective methods to reduce common-mode voltage is to use differential signaling. In this technique, the signal is transmitted as the difference between two voltages rather than as a single voltage [14]. This makes the circuit less susceptible to common-mode interference because any interference affects both signals equally, and the differential receiver can reject it.
- Balanced Circuits:** In balanced circuits, signals are transmitted on a pair of conductors with equal impedance [15]. This helps reject common-mode interference, as any common-mode voltage will be equally coupled onto both conductors and can be cancelled out.
- Common-Mode Chokes:** Common-mode chokes or baluns (balanced-to-unbalanced transformers) [2] are passive components that can be added to cables or circuits to suppress common-mode signals. They work by providing a high impedance to common-mode signals, effectively blocking them.
- Active Common-Mode Rejection:** Some differential amplifiers and instrumentation amplifiers have active common-mode rejection features [16]. These circuits actively amplify the differential signal while rejecting common-mode signals.
- Differential Amplification:** Using operational amplifiers or instrumentation amplifiers in differential mode [17] can amplify the difference between two input signals while ignoring common-mode components.
- Common-Mode Feedback:** In some applications, common-mode feedback circuits can be used to actively cancel common-mode signals, particularly in instrumentation and precision measurement systems [18].

### 3 Experimentation

A model of two-level MLI is fabricated in the laboratory for resistive load is shown in fig 3. that explains an electrical system with a DC source, an inverter, a load, and a CMV measurement. The DC source provides a constant voltage of 24V to the inverter. The inverter converts the DC voltage to an AC voltage, which is then supplied to the load. The load is the device that consumes the electrical power from the system. The CMV measuring technique is shown in fig 3.b. The CMV measurement measures the voltage difference between the neutral point of the load and the common ground or the DC mid-point. The CMV measurement is important because it can indicate the presence of leakage currents in the system [8]. Leakage currents can flow through parasitic capacitances and inductances in the system. The hardware experimental set up for the same is shown in the figure 3.c.





(c)

**Fig 3.** (a) Block diagram representing the measurement of CMV  
(b) Block diagram representing the connection of modified circuit  
(c) Experimental setup

By adopting the residual current detection circuit from IEC standard, a novel impedance control circuit is derived and proposed in this study to understand and reduce the common mode voltage effects.

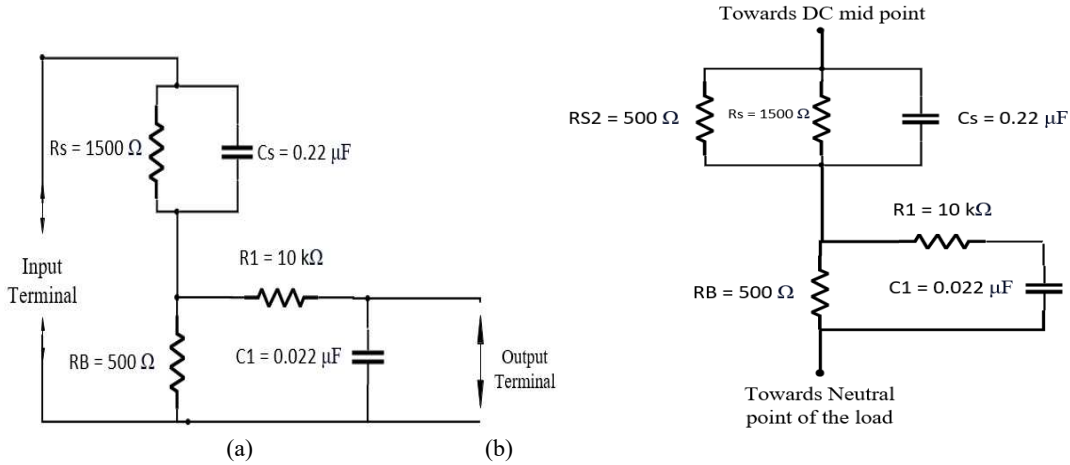


**Fig 4.** (a) Reference circuit from IEC 60990 (b) Modified circuit

This circuit helps to improve the reduction of leakage current in the inverter circuit which also helps to reduce the common mode voltage. The standard circuit configuration is considered as the reference circuit. The components used in reference circuits are as shown in fig 4.a. whose frequency ranges from 15Hz up to 1 MHz. By using these components in the circuit, the leakage current can be measured.

The reference circuit has been modified with respect to change in the total impedance. The modified circuit components and their specifications are shown in fig. 4.b.

By using these components in the circuit, the common mode voltage and the leakage current can be reduced. This circuit is similar to voltage divider circuit. When the DC voltage source is applied, current flows through the two resistors and capacitors. The capacitors charge and discharge, smoothing out the voltage ripple. The load sees a more stable AC voltage at the RB resistor. This can reduce the leakage current due to impedance and reduces the common mode voltage.

In order to reduce the CMV the modified circuit is connected as shown in fig 4.b.

The block diagram shown in fig 4.b. an electrical system with a DC source, an inverter, a load, and a leakage current measurement circuit. The DC source provides a constant voltage to the inverter. The inverter converts the DC voltage to an AC voltage, which is then supplied to the load. The load is the device that consumes the electrical power from the system. The leakage current measurement circuit measures the current flowing through the leakage path. The leakage path is a path that allows current to flow even when the load is not turned on. Leakage currents can flow through parasitic capacitances and inductances in the system, and can cause problems such as noise, interference, and even safety hazards.

Hence the modified circuit shown in Fig 5.b, will be connected in between DC negative and the neutral point of the load to reduce the leakage current, therefore reducing the common mode voltage. The simulation and experimental results show CMV developed at DC negative and the neutral point of the load

is Fig 9 and 10.

## 4 Experimental Results

When the resistive load is supplied from three-level PWM inverter, CMV varies from  $+V_{dc}/2$  to  $-V_{dc}/2$  with step of  $V_{dc}/3$ . The leakage current is measured between DC negative and the neutral point of the load. The leakage currents peak is also reduced to one fourth when resistive load is driven by the three-level inverter with the modified circuit.

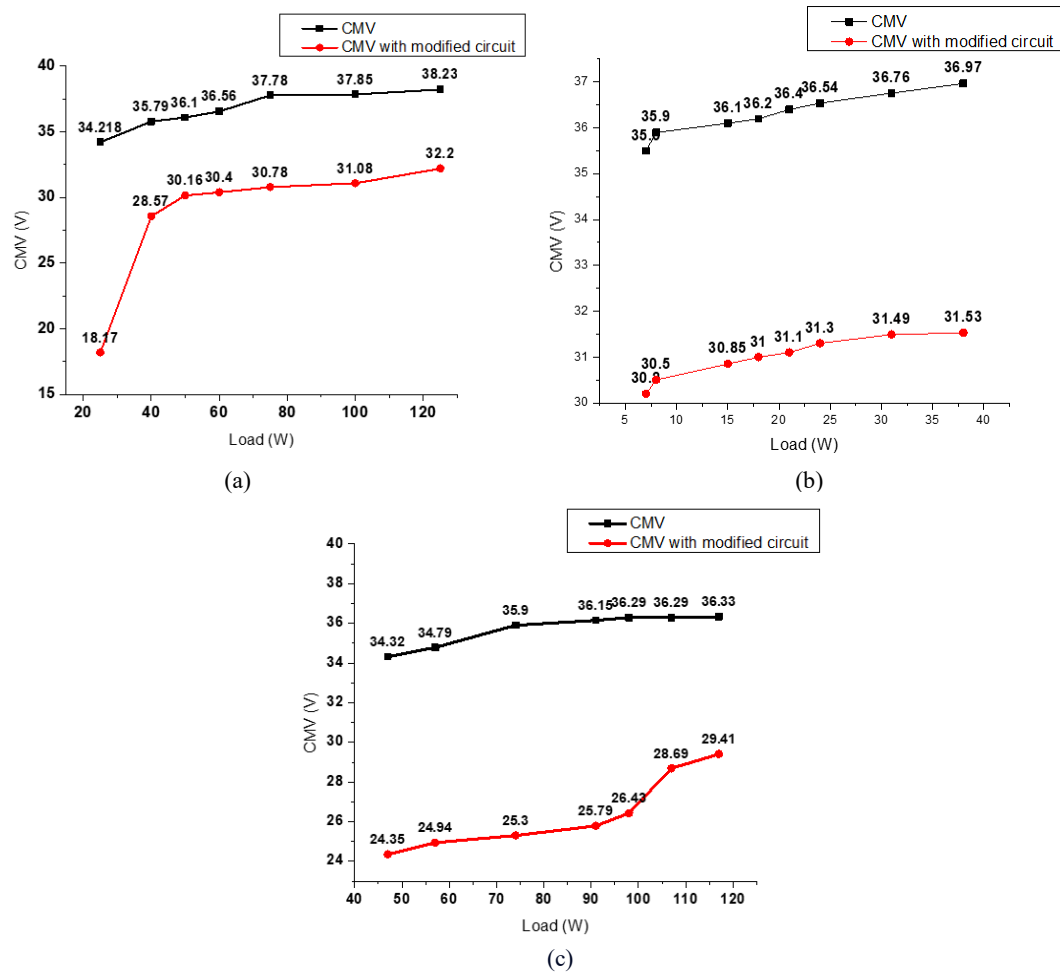
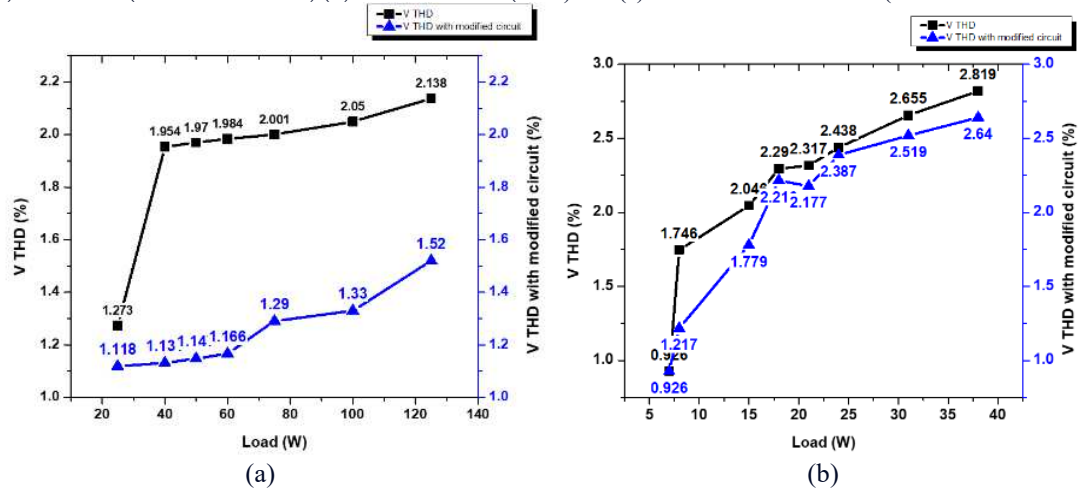


Fig 5. Result of CMV with and without modified circuit for

(a) linear load (incandescent bulb) (b) non-linear load (LED) and (c) linear + non-linear load (incandescent + LED)



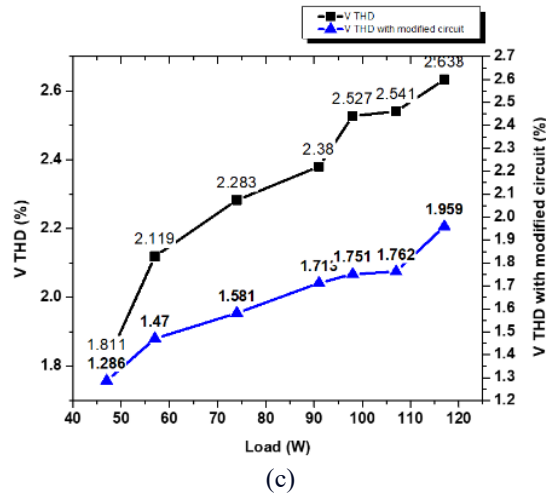


**Fig 6.** Result of Voltage THD with and without modified circuit for

(a) linear load (incandescent bulb) (b) non-linear load (LED) and (c) linear + non-linear load (incandescent + LED)

With the usage of the modified circuit fig 6 shows the result of the experiment that the common mode voltage has been reduced up to certain values for different loads and fig 7 shows that the voltage THD is also reduced for different load conditions. This leads to reduction in switching losses and improved efficiency.

## 5 Conclusion

The CMV generated by the conventional PWM inverter has been found to be major cause. In this paper, it is shown through experimental results that if the modified circuit is implemented it reduces the CMV up to 4.35%. Multilevel inverter reduces the  $dv/dt$  as well as leakage current which are responsible for damage in the load. The voltage THD of inverter are considerably improved. The proposed technique to reduce the CMV. Experimental results using modified circuit shows the superiority and feasibility of multilevel inverter. Usage of silicon carbide switches can also advantageous due to their higher thermal conductivity. These concepts can be applied to medium voltage as well as low voltage drives to increase the life of load and improves the reliability of it. In future this circuit can be further developed by reducing the impedance and balance the circuit to eliminate the leakage current.

## Acknowledgement

This research was supported by the Energy Efficiency and Renewable Energy Division (ERED), Central Power Research Institute (CPRI), Bengaluru, and the University of Visveswaraya College of Engineering (UVCE), Bengaluru. I thank my guide from CPRI and my Professor at the Electrical Department, UVCE for providing insight and expertise that greatly assisted the research.

## Reference

1. K. Suresh and E. Parimalasundar, "A Modified Multi Level Inverter With Inverted SPWM Control," in IEEE Canadian Journal of Electrical and Computer Engineering, vol. 45, no. 2, pp. 99-104, Spring 2022, doi: 10.1109/ICJECE.2022.3150367.
2. A. Srivastava and J. Seshadrinath, "A New Nine-Level Highly Efficient Boost Inverter for Transformerless Grid-Connected PV Application," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 3, pp. 2730-2741, June 2023, doi: 10.1109/JESTPE.2022.3210512.
3. X. Huang et al., "Comprehensive Analysis and Improvement Methods of Noise Immunity of Desat Protection for High Voltage SiC MOSFETs With High  $DV/DT$ ," in IEEE Open Journal of Power Electronics, vol. 3, pp. 36-50, 2022, doi: 10.1109/OJPEL.2021.3134498.
4. D. Han, F. Z. Peng and S. Dwari, "Advanced PWM Techniques for Multi-Level Inverters With a Multi-Level Active CM Noise Filter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 6, pp. 6865-6879, Dec. 2022, doi: 10.1109/JESTPE.2021.3128274.
5. L. Qiu, T. Meng, B. Yao, Z. Du and X. Yuan, "A High-Speed Low-Noise Comparator With Auxiliary-Inverter-Based Common Mode-Self-Regulation for Low-Supply-Voltage SAR ADCs," in

- IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 1, pp. 152-156, Jan. 2023, doi: 10.1109/TVLSI.2022.3224237.
6. R. Zhao, X. Jiang, C. Wang, Y. Wang, H. Xu and Q. Yan, "A Novel Zero-Sequence-Voltage-Balanced SVPWM With the Analyses of Common-Mode Voltage and Differential-Mode Current," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 2, pp. 2483-2496, April 2022, doi: 10.1109/JESTPE.2021.3120624.
  7. M. N and R. H. R., "Comparative Analysis of Modulation Techniques for Elimination of CMV in Multilevel Inverters," 2022 Fourth International Conference on Emerging Research in Electronics, Computer Science and Technology (ICERECT), Mandya, India, 2022, pp. 1-11, doi: 10.1109/ICERECT56837.2022.10060103.
  8. D. Zhang and X. She, "Hybrid Multilevel Converter With Silicon and Silicon Carbide Devices: Impact to Aviation Industry and Beyond," in IEEE Transactions on Power Electronics, vol. 38, no. 6, pp. 6806-6810, June 2023, doi: 10.1109/TPEL.2023.3253716.
  9. D. Yang, K. Yang and F. Gao, "Topology Optimization Analysis of Leakage Current Suppression in Three-Level Four-Leg Photovoltaic Grid-Connected Inverter," in IEEE Access, vol. 11, pp. 50145-50156, 2023, doi: 10.1109/ACCESS.2023.3277971.
  10. Z. Wu et al., "Dynamic dv/dt Control Strategy of SiC MOSFET for Switching Loss Reduction in the Operational Power Range," in IEEE Transactions on Power Electronics, vol. 37, no. 6, pp. 6237-6241, June 2022, doi: 10.1109/TPEL.2021.3137825.
  11. Current, M. (1995). International workshop illustrates progress in determination of 2-d dopant profiles. MRS Bulletin, 20(6), 58-58. <https://doi.org/10.1557/s0883769400037003>
  12. J. F. Ardashir, M. Ghassemi, B. Rozmeh, F. Blaabjerg and S. Peyghami, "A Five-Level Transformer-Less Grid-Tied Inverter Structure With Capacitive Voltage Divider Concept With Leakage Current Elimination," in IEEE Transactions on Industry Applications, vol. 59, no. 5, pp. 6025-6036, Sept.-Oct. 2023, doi: 10.1109/TIA.2023.3275928.
  13. T. Oshima, Y. Nakamura and T. Yamawaki, "Fast CMOS Analog Multiplier and Divider With Continuous-Time Inverter-Based Flash Digitizer," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 3, pp. 934-938, March 2022, doi: 10.1109/TCSII.2021.3134415.
  14. F. Zhang, Y. Zheng, X. Zhang, X. Yang and W. Chen, "Analysis and Flexible DV/DT Control of an Active Clamping Topology for Series-Connected SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 38, no. 4, pp. 4840-4855, April 2023, doi: 10.1109/TPEL.2022.3233725.
  15. Y. Yang, M. Huang, S. Du, R. P. Martins and Y. Lu, "A Level Shifter With Almost Full Immunity to Positive dv/dt for Buck Converters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 11, pp. 4595-4604, Nov. 2023, doi: 10.1109/TCSI.2023.3307869.
  16. Z. Zhang, M. Wang, C. Liu, Y. Si, Y. Liu and Q. Lei, "High-dv/dt-Immune Fine-Controlled Parameter-Adaptive Synchronous Gate Driving for GaN-Based Secondary Rectifier in EV Onboard Charger," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 3, pp. 3302-3323, June 2022, doi: 10.1109/JESTPE.2020.3034036.
  17. Y. -R. Lee, J. Yoo, I. Hwang and S. -K. Sul, "Analysis of Position Estimation Error in Signal-Injection Sensorless Control Induced by Inverter dv/dt-Based Current Measurement Noise," in IEEE Transactions on Power Electronics, vol. 38, no. 1, pp. 839-851, Jan. 2023, doi: 10.1109/TPEL.2022.3202170.
  18. M. Meraj, S. Rahman, A. Iqbal and N. Al Emadi, "Novel Level Shifted PWM Technique for Unequal and Equal Power Sharing in Quasi Z-Source Cascaded Multilevel Inverter for PV Systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 1, pp. 937-948, Feb. 2021, doi: 10.1109/JESTPE.













