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Research Article

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Low-Cost ADS-B Out Architecture with Certification-Oriented Design and Integrated RF Monitoring

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Abstract

Certified 1090 MHz Extended Squitter (1090ES) ADS-B Out transponders remain cost-prohibitive for experimental and small unmanned aircraft system (UAS) platforms, while existing low-cost software-defined radio (SDR) alternatives lack the deterministic timing, fault management, and structural software properties required for avionics certification. This paper proposes *OpenADSB-Out*, a low-cost, non-SDR ADS-B Out architecture based exclusively on commercial off-the-shelf (COTS) components, designed from the outset with structural properties compatible with RTCA DO-260B, DO-178C, DO-254, and DO-160G. The architecture employs an ADF4351 PLL/VCO for deterministic 1090 MHz carrier generation, a hardware timer-driven RF switch for Binary Pulse Position Modulation (BPPM) encoding with sub-50 ns symbol jitter, and an AD8318 logarithmic detector for per-frame RF power monitoring. A hierarchical Built-In Test (BIT) framework comprising eight Power-On checks and ten Continuous monitors implements fail-silent transmission behaviour. The ADS-B Encoding Engine is validated as a portable C library cross-checked against the independent *pyModeS* decoder over 122,104 encoding operations: zero CRC-24 errors across 10,000 frames, maximum CPR position error of 3.80 m (threshold 30 m), exact altitude encoding, and zero failures in a 100,000-call stress test. A structured open-items analysis shows that only two architectural additions are required to reach a formal DO-260B compliance programme; all remaining gaps are evidential artefacts requiring no design changes.

Keywords: ADS-B Out, 1090ES, avionics certification, DO-260B, built-in test, low-cost avionics

1. Introduction

Automatic Dependent Surveillance–Broadcast (ADS-B) is the primary cooperative surveillance technology of modern air traffic management, standardised for the 1090 MHz Extended Squitter (1090ES) datalink in RTCA DO-260B [1] and DO-260C [2]. Mandatory ADS-B Out equipage was concluded in the United States by January 2020 and is progressively enforced in European airspace under Commission Implementing Regulation (EU) 2017/386 [3].

The integration of UAS into controlled airspace has amplified demand for lightweight, low-cost surveillance solutions. Size, weight, power, and cost (SWaP-C) constraints are fundamentally at odds with the complexity of certified avionics transponders, whose acquisition cost can exceed several thousand euros [4]. Existing low-cost approaches partition into three classes: (i) certified transponders (TSO/ETSO-C166b), which satisfy all compliance requirements but at prohibitive cost; (ii) SDR-based experimental transmitters [5], which achieve low hardware cost at the expense of determinism and certification compatibility; and (iii) open-source receivers (*dump1090*, *pyModeS* [6, 7]), which address only the reception problem.

A critical gap therefore exists: no publicly available, open-architecture ADS-B Out system has been designed according to certification-oriented principles from the outset using COTS components. This paper addresses that gap with *OpenADSB-Out*, whose contributions are:

1. A non-SDR, deterministic ADS-B Out architecture based exclusively on COTS components, with a compliance mapping to DO-260B, DO-178C, DO-254, and DO-160G.
2. Integration of a real-time RF power monitoring subsystem into a low-cost avionics-like design.
3. A hierarchical BIT framework with fail-silent transmission as the fault response.
4. A methodology for bridging experimental prototypes and certifiable systems through explicit requirement traceability and fault containment.

The objective is not to present a certified product, but to demonstrate that the structural properties required for future certification can be embedded from the outset in a cost-constrained open architecture.

2. Background and Related Work

2.1. ADS-B Out and the Mode S Extended Squitter Standard

ADS-B is defined within the Mode S secondary surveillance radar framework of ICAO Annex 10 [8]. The Extended Squitter (DF17) is a 112-bit spontaneous downlink message carrying ADS-B state vector data without ground interrogation [7]. RTCA DO-260B [1] specifies message rates, navigation accuracy categories (NACp, NACv), source integrity levels (SIL), and RF output power classes. The core DF17 message set includes airborne position (Type Codes 9–18, using Compact Position Reporting encoding), airborne velocity (Type Code 19), aircraft identification (Type Codes 1–4), and operational status (Type Code 31) [7]. Each frame carries a 24-bit CRC parity field computed with the Mode S generator polynomial.

2.2. Low-Cost and SDR-Based ADS-B Transmitters

Doronin and Shmelova [5] demonstrated ADS-B frame generation with HackRF One and GNU Radio Companion. While hardware cost is minimal, sample delivery jitter over USB (tens to hundreds of microseconds) is incompatible with the Mode S symbol period of 1 µs and the DO-260B pulse width tolerance of ± 0.05 µs [1]. No fault monitoring or transmission inhibition logic is described. Baddeley et al. [4] confirmed that acquisition costs of certified transponders for sub-5 kg UAS are driven more by certification overhead than by hardware, motivating an architecture that separates structural certification compatibility from immediate regulatory compliance.

2.3. Certification-Oriented COTS Avionics

DO-254 [9] and DO-178C [10] govern hardware and software design assurance for airborne systems. Hierarchical BIT—comprising a Power-On BIT (PBIT) at startup and Continuous BIT (CBIT) during operation—is an established mitigation for COTS integration [11, 12]. Logarithmic power detectors such as the AD8318 (1 MHz–8 GHz, 70 dB dynamic range, 10 ns response [13]) are standard in transmitter subsystems but have not been reported in low-cost ADS-B Out designs. Hilderman and Baghai [14] reported that programmes investing in upfront DO-178C architecture alignment reduced verification effort by 30–40% compared to retrospective compliance approaches.

Table 1 positions *OpenADSB-Out* relative to existing implementation classes across four discriminating attributes.

Table 1: Comparative positioning of ADS-B Out implementation approaches. ✓ = present; – = absent.

Implementation	**Non-SDR**	**RF monitor**	**BIT**	**Cert.-oriented**
Certified (TSO/ETSO)	✓	✓	✓	✓
SDR-based [5]	–	–	–	–
Open-source receiver	–	–	–	–
OpenADSB-Out	✓	✓	✓	✓

3. System Architecture

3.1. Functional Decomposition

The system decomposes into six subsystems arranged in a data-flow chain from navigation source to radiated signal, with a cross-cutting health monitoring path.

Fig. 1 shows the top-level signal flow from navigation source to radiated signal. The dashed feedback path represents the RF monitoring return to the MCU health supervisor; the Transmission Gate is a logical inhibit controlled exclusively by the BIT Supervisor.

(1) GNSS Navigation Subsystem. Provides geodetic position, velocity, geometric altitude, and a 1 pulse-per-second (PPS) timing reference, along with the NACp, NACv, and SIL integrity indicators required by DO-260B [1].

(2) Microcontroller Unit (MCU). Single computational hub responsible for ADS-B frame encoding, PPM timing generation via hardware timers, subsystem health supervision, and BIT execution. No operating system is interposed; all timing-critical functions are driven directly by MCU hardware peripherals.

(3) RF Synthesis Subsystem. Generates the 1090 MHz carrier using an ADF4351 PLL/VCO [15], configured via SPI at startup. Lock status is continuously monitored via the LD (Lock Detect) pin.

(4) RF Modulation and Power Stage. Encodes the pre-computed ADS-B bit stream onto the 1090 MHz carrier using BPPM through a fast RF switch controlled by an MCU timer output compare unit. A power amplifier brings output to 20–33 dBm; a SAW filter suppresses harmonics.

(5) RF Monitoring Subsystem. An AD8318 logarithmic detector [13] samples forward power via a directional coupler after the filter stage. Its DC output is digitised by an MCU ADC channel and processed by the BIT

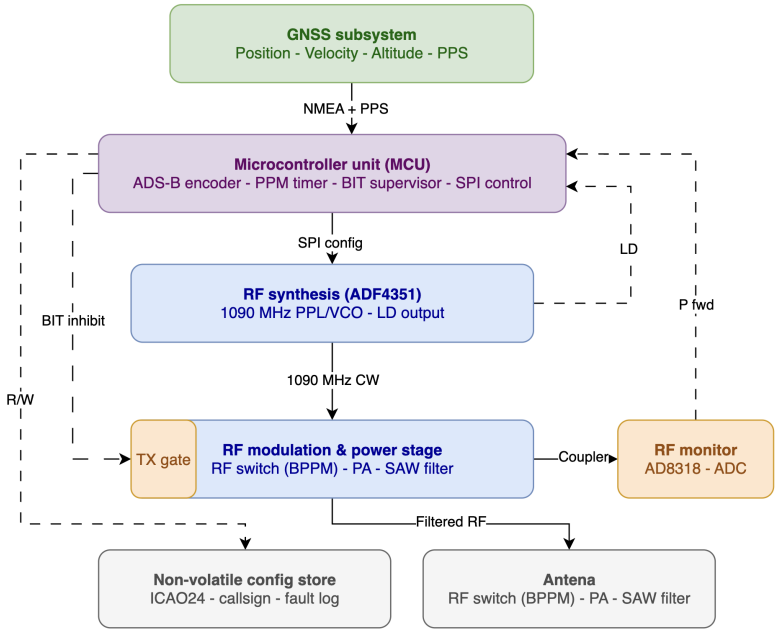


Figure 1: Top-level block diagram of *OpenADSB-Out*. Solid arrows: data and control flow. Dashed arrow: AD8318 RF monitoring feedback to BIT Supervisor. The Transmission Gate opens only when all P3 conditions are satisfied simultaneously.

supervisor to detect PA failures, antenna disconnection, and excessive power deviation.

(6) Non-Volatile Configuration Store. Retains the ICAO 24-bit address, callsign, and configuration in CRC-protected dual-copy SPI EEPROM. Fault events are also logged here.

3.2. Design Principles

Five design principles, each traceable to a requirement of DO-260B [1], DO-178C [10], or DO-254 [9], govern the architecture.

P1 — Non-SDR Deterministic RF. PLL-based carrier generation and timer-driven RF switching achieve symbol-level timing determinism without any general-purpose OS in the timing path. The ADF4351 PLL guarantees frequency stability and lock detection independently of firmware execution; the BPPM waveform is generated entirely by DMA-driven timer compare registers with no CPU involvement during transmission. This directly addresses DO-260B Section 2.2 symbol timing requirements (± 50 ns jitter budget [1]).

P2 — Single-MCU Centralised Supervision. A single MCU is the sole computational authority for frame generation and system supervision, implementing the fault containment philosophy of DO-178C Section 4 [10] without the inter-processor synchronisation complexity of a distributed architecture.

P3 — Conditional Transmission Gate. Transmission is enabled only when all of the following hold simultaneously: GNSS fix valid with NACp ≥ 9; PLL lock confirmed; forward RF power within $[P_{\min}, P_{\max}]$; no active critical fault; configuration CRC valid. Any violation causes immediate, persistent inhibition of the RF switch, implementing fail-silent behaviour consistent with DO-178C Section 6.4 [10].

P4 — Integrated Real-Time RF Health Monitoring. The AD8318 path provides per-frame, independent verification that each transmission occurred at the expected power level, implementing the output monitoring function recommended for DAL-C software under DO-178C [10] and DO-254 Section 4 [9].

P5 — Layered Software Architecture with Traceability. Three horizontal layers (HAL / Drivers / Application) with strict downward dependencies and explicit requirement traceability support DO-178C objectives for structural coverage analysis (MC/DC) and requirement traceability [10].

3.3. Hardware Component Summary

Table 2 summarises the selected components.

Table 2: Hardware component summary.

Subsystem	**Device**	**Primary role**
MCU	STM32H563 [16]	Encoding, BIT, RF control
GNSS	u-blox MAX-M10S [17]	Position, velocity, PPS
RF synthesis	ADF4351 [15]	1090 MHz carrier
RF switch	PE4259 [18] / HMC547	BPPM modulation
Power amplifier	RF2126 / RFMD	20–33 dBm output
SAW filter	B3731 (TDK)	Harmonic suppression
RF monitor	AD8318 [13]	Forward power detection
Config memory	M95M02 (SPI EEPROM)	ICAO24, callsign, fault log

MCU selection. The STM32H563 (Arm Cortex-M33, 250 MHz, 375 DMIPS [16]) provides 16 hardware timers with 4 ns resolution—well below the ± 50 ns

DO-260B jitter budget [1]—a 12-bit ADC with 75 ns conversion time, and a Memory Protection Unit for fault containment partitioning. Operating temperature coverage (−40 to +85 °C, junction +130 °C) is consistent with DO-160G Category B2 [19].

GNSS selection. The u-blox MAX-M10S provides PPS timing accuracy of 30 ns RMS (60 ns at 99th percentile [17]), sufficient to discipline the MCU timer epoch for DO-260B message scheduling. NACp is derived directly from the HAcc field of the UBX-NAV-PVT message; the BIT supervisor inhibits transmission when NACp drops below 9.

RF synthesis and modulation. The ADF4351 operates with its internal VCO at 2180 MHz and output divider set to divide-by-2, yielding 1090 MHz. Phase noise is approximately −112 dBc/Hz at 10 kHz offset [15], satisfying the implicit DO-260B spectral mask constraint. A 25 MHz TCXO (±1 ppm) ensures frequency accuracy within the ±1 MHz DO-260B requirement [1] across the full temperature range. BPPM modulation is realised by a discrete SPST RF switch (PE4259 [18] or HMC547, switching time <20 ns), driven by DMA-armed timer compare registers; no CPU instruction is in the timing path during transmission.

RF monitoring. The AD8318 output voltage V_{out} relates to input power P_{in} (dBm) as [13]:

$$V_{\text{out}} = V_{\text{slope}} \cdot (P_{0\text{dBm}} - P_{\text{in}}) \tag{1}$$

where $V_{\text{slope}} \approx 22\,\text{mV/dB}$ and $P_{0\text{dBm}} \approx +17\,\text{dBm}$ at 1090 MHz. The MCU ADC samples at 250 ns after each pulse rising edge, giving total monitoring latency under 100 ns. Three fault conditions are detected: antenna disconnection (forward power below $P_{\min}$), PA failure (power outside $[P_{\min}, P_{\max}]$), and RF path open circuit.

Fig. 2 illustrates the complete RF signal chain with nominal power levels at each stage for DO-260B Power Class A (+20 dBm at the antenna connector).

4. Firmware and Software Architecture

The firmware is structured in three horizontal layers aligned with DO-178C Section 5 architectural design objectives [10].

HAL (Hardware Abstraction Layer): wraps all MCU peripheral register access behind hardware-independent API groups, built on the STM32Cube HAL driver library [20] (`hal_timer`, `hal_spi`, `hal_adc`, `hal_uart`, `hal_nvm`).

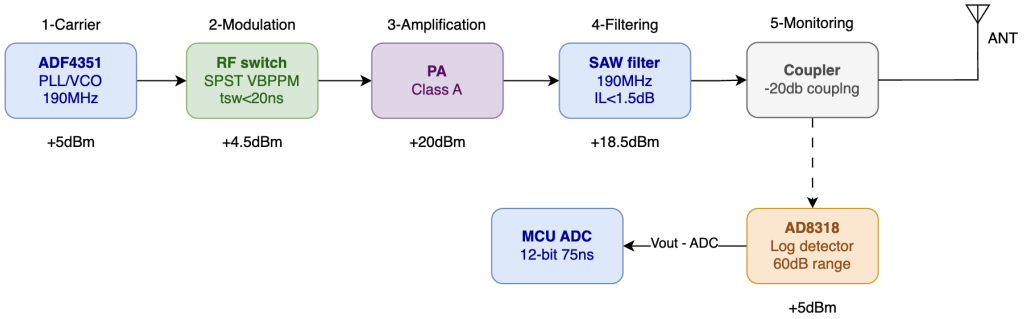


Figure 2: RF signal chain from ADF4351 output to antenna. Nominal power levels correspond to DO-260B Power Class A. The directional coupler ($-20\,\mathrm{dB}$) feeds the AD8318 monitor; the valid power window $[P_{\min}, P_{\max}]$ is stored in NVM and enforced by the BIT Supervisor on every frame.

Drivers: device-level protocol implementations for ADF4351 [15] (fractional-N register computation and SPI programming), GNSS [17] (UBX-NAV-PVT/VELNED parsing over DMA-buffered UART), and NVM (dual-copy CRC-16 read/write).

Application: three independent modules with no lateral coupling—ADS-B Encoding Engine, Navigation Processor, and Health Monitor (BIT Supervisor). All inter-module state passes through a single `system_state_t` structure in an MPU-protected RAM region writable only by the BIT Supervisor.

The firmware executes as a bare-metal, non-preemptive main loop with no RTOS, providing deterministic resource consumption consistent with DO-178C guidance [10, 21]. Timing-critical BPPM generation and ADC sampling execute entirely in hardware once armed; the CPU is not in the timing path during transmission.

The layered structure is shown in Fig. 3, with inter-layer dependencies strictly downward and no lateral coupling between Application modules.

4.1. ADS-B Encoding Engine

The engine generates the four DF17 message types required by DO-260B [1]. CPR encoding follows the algorithm of Sun et al. [7] implemented in fixed-point arithmetic:

$$\mathrm{lat_cpr} = \left\lfloor 2^{17} \cdot \mathrm{mod}\left(\frac{\phi}{\Delta\phi_z}, 1\right) \right\rfloor \tag{2}$$

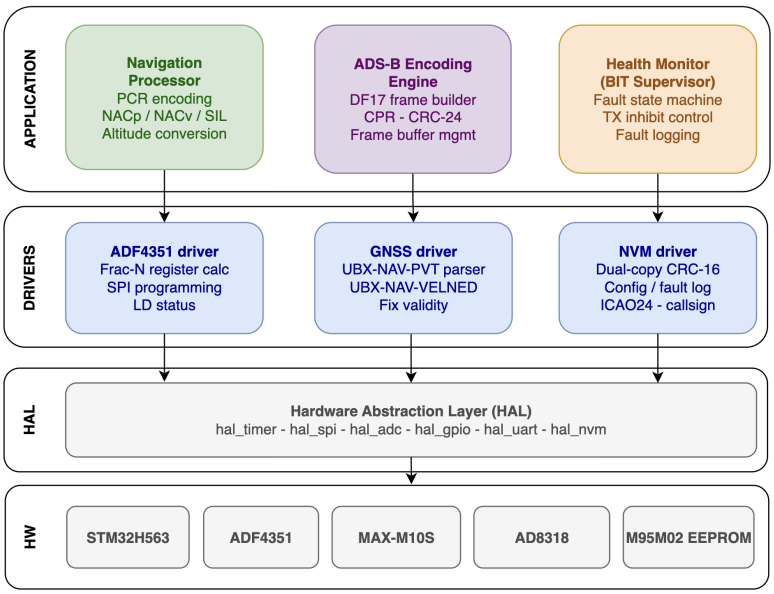


Figure 3: Layered firmware architecture. All hardware access is through the HAL; no Application module calls another directly. The `system_state_t` shared structure (grey) is writable only by the BIT Supervisor, enforced by the MCU MPU.

where ϕ is WGS-84 latitude and $\Delta\phi_z$ is the zone width for the even ($z = 0$) or odd ($z = 1$) format [7]. CRC-24 is computed with the Mode S generator polynomial:

$$G(x) = x^{24} + x^{23} + x^{10} + x^3 + 1 \tag{3}$$

using a 256-entry lookup table stored in Flash (11 lookups per 88-bit message, under 1 µs at 250 MHz). Four statically pre-allocated 14-byte frame buffers—one per message type—are updated atomically on each GNSS epoch, eliminating dynamic memory allocation consistent with DO-178C guidance for safety-critical software [10].

Table 3 presents a representative subset of the requirement traceability matrix, mapping DO-260B requirements to software requirements and verification tests.

5. Built-In Test and Fault Management

The BIT framework ensures the system never transmits when it cannot guarantee the correctness, completeness, and RF integrity of the output signal. Its hierarchical structure follows the pattern described in [11, 12, 22].

Table 3: Representative requirement traceability matrix for the ADS-B Encoding Engine. SWR = Software Requirement.

System req.	SWR	Verification criterion	Test ref.
DO-260B §3.1.2.3	SWR-ENC-01: DF = 17 for all DF17 frames	Bits 1–5 = 10001_2	TC-ENC-01
DO-260B §3.1.7.2	SWR-ENC-03: CRC with polynomial $G(x)$	*pyModeS* CRC residual = 0	TC-ENC-03
DO-260B §3.1.2.9	SWR-ENC-05: CPR globally unambiguous	Position error $\leq$30 m (NACp 9)	TC-ENC-05
DO-260B §3.1.2.6	SWR-ENC-06: ICAO 8824 character set	All callsign chars from permitted set	TC-ENC-06

5.1. Power-On BIT

The PBIT executes eight checks in strict order before any transmission is permitted (Table 4). Any failure halts the sequence, logs the fault, and transitions the system to INHIBITED.

Step 6 (RF path continuity) is the most architecturally novel element: the RF switch is enabled for 120 µs while the ADF4351 is locked and the PA is biased, and the AD8318 output is sampled to confirm a near-50 Ω load [13]. An open-circuit antenna produces excessive VSWR detected as a forward power reading outside the valid window.

5.2. Continuous BIT

CBIT executes per-epoch (1 Hz, driven by GNSS PPS) and per-frame. The ten checks include: PLL lock status (LD GPIO), GNSS fix validity, navigation accuracy (HAcc $<$ 30 m), UTC validity, supply voltage, MCU junction temperature ($<$110 °C), NVM CRC, RF forward power (AD8318 ADC sample at each pulse midpoint), frame CRC-24 re-verification before DMA arm, and transmission epoch monitoring.

Critical faults (PLL unlock, invalid position, RF power anomaly, memory CRC failure) cause immediate, persistent transmission inhibit with fault log entry. Non-critical faults set a degraded flag and auto-clear after three

Table 4: Power-On BIT check sequence.

Step	Check	Pass criterion	Class
1	RAM (March-C [23])	Zero bit-flip errors	Critical
2	Flash CRC-32 [10]	CRC matches golden value	Critical
3	NVM dual-copy CRC	Both copies valid	Critical
4	ICAO address	$\neq$ 0x000000 / 0xFFFFFF	Critical
5	PLL lock [15]	LD asserted within 10 ms	Critical
6	RF path continuity [13]	AD8318 output in valid range	Critical
7	GNSS first fix [17]	Fix valid; NACp $\geq$ 9	Critical
8	Supply voltage	$V \in [3.0, 3.6]$ V	Non-critical

consecutive clean epochs. The fail-silent response prevents injection of erroneous frames into the shared 1090 MHz channel [24], consistent with fault containment principles for avionics communication functions [25].

6. Certification-Oriented Design Methodology

Table 5 maps the principal DO-260B transmitter requirements to *OpenADSB-Out* design elements.

The firmware addresses all DO-178C DAL-D objectives and several DAL-C structural properties proactively: (i) *static memory allocation*—all buffers allocated at link time, stack depth bounded and measurable at compile time [10]; (ii) *MISRA-C:2012 conformance* [26]—explicit initialisation, mandatory `default` in all `switch` statements, restricted pointer arithmetic, explicit integer casts; (iii) *layered architecture* with MPU partitioning enforcing module independence [10].

For the relevant failure condition—transmission of erroneous position data—ARP4761 functional hazard assessment [27] typically yields a *Major* severity class (DAL-C under DO-178C). The RF monitoring path implements the independent output monitoring recommended for DAL-C hardware under DO-254 Section 4 [9].

Table 5: DO-260B transmitter requirement compliance mapping [1].

Clause	Requirement	Implementation
§2.2.1	Freq. 1090 ± 1 MHz	ADF4351 + ± 1 ppm TCXO; worst-case <1.09 kHz
§2.2.2	Power Class A $\geq$ $+18.5$ dBm	PA + SAW path $\geq$ $+18.5$ dBm
§2.2.4	Symbol period 1.0 ± 0.05 µs	250 MHz timer; jitter <20 ns
§3.1.7.2	CRC-24 Mode S polynomial	Table-driven CRC (SWR-ENC-03)
§2.1.3	TX inhibit on invalid nav data	Conditional gate; BIT Supervisor
§2.2.3.4	Position rate ≥ 2 Hz	SW timer on GNSS epoch (SWR-ENC-04)

Table 6 catalogues remaining open items, distinguishing architectural changes (Type A) from evidential artefacts only (Type E).

Only two items require architectural additions—both additive (barometric sensor; FDE-capable GNSS module). All remaining gaps are evidential, confirming that the architecture is substantively correct for certification and that the remaining work is production of required evidence rather than redesign, consistent with the findings of Hilderman and Baghai [14].

7. Validation and Results

Validation is confined to the *adsblib* encoding library— the portable C implementation of the ADS-B Encoding Engine compiled for x86-64 from the same source that targets the STM32H563. A Python test harness exercises the library via `ctypes`; outputs are independently verified by *pyModeS* [6] (v2.10, Python 3.11.5, NumPy 1.26) as a cross-oracle.

7.1. Test 1 — CRC-24 Correctness

10,000 identification frames with random ICAO addresses and callsigns were generated and verified by `pyModeS.util.crc()`. **Result: 100.00% pass** (zero CRC residuals), confirming bit-exact agreement with the reference implementation [6] (SWR-ENC-03).

Table 6: Open items toward TSO-C166b/ETSO-C166b qualification. A = architectural change required; E = evidential artefact only.

Open item	**Type**	**Standard**
Barometric altitude input	A	DO-260B §2.1.1.2
SIL upgrade to level 2 (FDE GNSS)	A	DO-260B §2.2.4
Formal SW requirements specification	E	DO-178C §5
SW verification cases and procedures	E	DO-178C §6
Structural coverage analysis (MC/DC)	E	DO-178C §6.4
SW/HW accomplishment summaries	E	DO-178C/254
DO-160G environmental test report	E	DO-160G
RF spectral mask measurement	E	DO-260B §2.2.3

7.2. Test 2 — Callsign Encoding

Four representative callsigns (`ECABC`, `IBE1234`, `RYR52AB`, `VLG1001`) were encoded and decoded. **Result: 4/4 pass**, confirming correct ICAO 8824 character mapping as required by DO-260B [1] (SWR-ENC-06).

7.3. Test 3 — CPR Position Encoding

10,000 random positions (latitude $\in [-80°, +80°]$, longitude $\in [-180°, +180°]$, altitude $\in [0, 40{,}000]$ ft) were encoded as even/odd frame pairs and decoded by *pyModeS* [6]. Haversine distance between input and decoded coordinates is the error metric.

Result: 100% compliance. The maximum error of 3.80 m is 87.5% below the 30 m NACp 9 threshold and consistent with the theoretical CPR quantisation bound of $\approx$4.8 m near the equator [7].

7.4. Test 4 — Altitude Encoding

100 altitudes at 500 ft spacing over $[0, 49{,}500]$ ft were encoded and decoded. **Result: mean/max altitude error 0.0 ft** across all samples, confirming bit-exact Gillham altitude encoding (DO-260B §3.1.2.7 [1]).

Table 7: CPR position encoding error statistics ($N = 10{,}000$ random positions).

Metric	**Value**	**Threshold**
Mean absolute error	2.015 m	—
Maximum absolute error	3.798 m	< 30 m
95th-percentile error	3.149 m	—
Compliance ≤ 30 m	**100.0%**	$\geq 99\%$

7.5. Test 5 — Velocity Encoding

2,000 random velocity vectors (ground speed 50–600 kt, track 0°–360°, vertical rate ±3,000 ft/min) were encoded and decoded. Compliance thresholds follow the LSB resolution of the DO-260B encoding [1].

Table 8: Velocity encoding error statistics ($N = 2{,}000$).

Field	**Mean err.**	**Max err.**	**Compliance**	**Threshold**
Ground speed	0.476 kt	1.0 kt	**100%**	≤ 2 kt
Track angle	0.063°	0.575°	**100%**	$\leq 2°$
Vertical rate	15.9 ft/min	32.0 ft/min	**100%**	≤ 64 ft/min

Result: 100% compliance on all three fields; no errors exceeding one LSB were observed, consistent with the encoding resolution defined in DO-260B [1] and Sun et al. [7].

7.6. Test 6 — Stress Test

100,000 encoding calls uniformly distributed among the three message types with fully random parameters. **Result: zero encoder failures, zero CRC failures, zero decode failures** (100.0% success rate).

The combined validation population across all six tests is $N_{\text{total}} = 122{,}104$ encoding operations. All produced correctly structured, CRC-valid DF17 frames independently decodable by *pyModeS* [6]. The cross-oracle methodology provides verification independence equivalent to DO-178C requirements for independent verification activities [10].

8. Discussion

OpenADSB-Out occupies a design space unoccupied in the literature: a low-cost open-architecture ADS-B Out transmitter whose engineering pro-

cess is structurally aligned with avionics certification standards from initial design. The incremental cost relative to a minimal SDR transmitter is modest: the ADF4351 PLL synthesiser [15] adds approximately $8–12 per unit, the AD8318 RF monitoring path [13] adds $6–9, and the layered firmware structure and traceability overhead adds approximately 20–30% to initial firmware development effort [14]. In exchange, these additions eliminate the two Type-A items in Table 6 that would otherwise require architectural redesign.

The principal limitation of the current work is the absence of a physical prototype: claims regarding symbol-level timing determinism, RF power class compliance [1], and PA spectral purity are based on component specifications and architectural analysis rather than measurement data. The u-blox MAX-M10S [17] also does not provide Fault Detection and Exclusion (FDE), constraining the architecture to SIL = 1 rather than the SIL = 2 recommended by DO-260B [1] for surveillance-dependent airspace operation.

Future work comprises four phases in priority order: (1) hardware prototype assembly and RF validation (BPPM timing vs DO-260B ±50 ns budget [1]; spectral mask at 1090 MHz; functional reception via *dump1090*); (2) BIT coverage measurement through fault injection and live GNSS integration [17]; (3) DO-160G [19] pre-compliance temperature cycling and EMI testing; (4) GNSS upgrade to an FDE-capable receiver and barometric altitude integration to close the two Type-A open items and establish the hardware configuration for a formal DO-260B compliance test programme [1].

9. Conclusions

This paper has presented *OpenADSB-Out*, a low-cost, non-SDR ADS-B Out architecture demonstrating that COTS-based transmitter systems can be designed with structural certification compatibility from the outset.

Five principal contributions have been made. First, a non-SDR, deterministic RF generation chain using an ADF4351 [15] PLL/VCO and hardware timer-driven RF switch achieves DO-260B [1] symbol timing compatibility without any general-purpose OS in the timing path. Second, an AD8318 [13] RF power monitoring path provides per-frame independent transmission health verification—not previously reported in low-cost ADS-B transmitter designs [5, 4]. Third, a hierarchical BIT framework [11, 12] with eight PBIT checks and ten CBIT monitors implements fail-silent transmission as the response to all critical faults [25]. Fourth, explicit compliance

mappings to DO-260B [1], DO-178C [10], DO-254 [9], and DO-160G [19], combined with MISRA-C:2012 conformance [26] and a structured open-items catalogue (Table 6), demonstrate that only two architectural additions are required for a formal compliance test programme; all remaining gaps are evidential. Fifth, cross-oracle validation [6] of the ADS-B Encoding Engine over 122,104 encoding operations produced zero CRC errors, exact altitude encoding, maximum CPR position error of 3.80 m [7], and zero stress-test failures.

The work provides a concrete open architectural reference for researchers developing low-cost avionics, UAS surveillance equipage [4, 28], and experimental platforms that aspire to a future certification path [14].

Declaration of Competing Interests

The author declares no known competing financial interests or personal relationships that could have influenced the work reported in this paper.

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Conflicts of interest

The authors declare that they have no conflicts of interest.

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